1Mbit(1Mx1bit) Fast Page Mode, 1K Refresh, 20Pin ZIP, 5V Design
Part No. HMD1M1Z1

DESCRIPTION

The HMD1M1Z1 is an 1M x 1 bits Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells
within the same row. Power supply voltage (+5V), access time (-5, -6), power consumption(Normal or Low power), and package type (ZIP) are optional features of this Module. The HMD1M1Z1 have CAS-before-RAS refresh, RAS-only refresh and Hidden refresh capabilities.

The HMD1M1Z1 is optimized for application to the systems, which are required high density and large capacity such as main memory for main frames and mini computers, personal computer and high performance microprocessor systems.

The HMD1M1Z1 provides common data and outputs.

Features

- Fast Page Mode operation
- CAS-before-RAS refresh capability
- RAS-only and Hidden refresh capability
- Fast parallel test mode capability
- TTL(5V) compatible inputs and outputs
- Early write or output enable controlled write
- Available in 20pin ZIP packages
- Single +5V±10% power supply
- 1,024 Refresh Cycles/16ms
- Performance Range

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
HMD1M1Z1-5	50	15	90	35
HMD1M1Z1-6	60	15	110	40

PIN DESCRIPTION

PIN	FUNCTION	PIN	FUNCTION
A0 – A8	Address Inputs	/WE	Read/Write Enable
DQ0 – DQ3	Data Input/Output	Vcc	Power (+5V)
/RAS	Row Address Strobe	Vss	Ground
/CAS	Column Address Strobe	NC	No Connection

PIN ASSIGNMENT

PIN	SYMBOL
1	NC
2	/CAS
3	DOUT
4	V_{SS}
5	DIN
6	/WE
7	/RAS
8	NC
9	NC
10	A9NC
11	A0
12	A1
13	A2
14	A3
15	V_{CC}
16	A4
17	A5
18	A6
19	A7
20	A8

ABSOLUTE MAXIMUM RATINGS*

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature under Bias	**0 ~ 70**	C
TSTG	Storage Temperature (Plastic)	**-55 ~ 150**	C
VIN/VOUT	Voltage on any Pin Relative to Vss	**-1.0 ~ 7.0**	V
VCC	Power Supply Voltage	**-1.0 ~ 7.0**	V
IOUT	Short Circuit Output Current	**50**	mA
PD	Power Dissipation	**600**	mW

*****NOTE: 1. Stress greater than above absolute Maximum Ratings? May cause permanent damage to the device.

RECOMMENDED DC OPERATING CONDITIONS (T_A = 0 ~ 70C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	Vcc+1	V
Input Low Voltage	V_{IL}	-1.0	-	0.8	V

*****NOTE: All voltages referenced to Vcc

DC AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER		MIN	MAX	UNIT
V_{OH}	Output High Level Voltage (**I**OUT = -5mA)		2.4		V
V_{OL}	Output Low Level Voltage (**I**OUT = 4.2mA)		0	0.4	V
I_{CC1}	Operating Current	-5		85	mA
	(/RAS,/CAS,Address Cycling : **t**RC = **t**RC min)	-6		75	
I_{CC2}	Standby Current (/RAS,/CAS = V_{IH})		-	2	mA
I_{CC3}	/RAS Only Refresh Current	-5		85	mA
	(/RAS Cycling, /CAS = V_{IH},: **t**RC = **t**RC min)	-6		75	
I_{CC4}	Fast Page Mode Current	-5		65	mA
	(/RAS =V_{IL}, /CAS, Address Cycling : tPC = tPC min)	-6		55	mA
I_{CC5}	Standby Current (/RAS,/CAS >= Vcc –0.2V)			1	mA
I_{CC6}	/CAS before /RAS Refresh Current (**t**RC = **t**RC min)	-5		85	mA
		-6		75	
I_{CCS}	Self Refresh Current (/RAS=/UCAS=/LCAS=V_{IL}, /WE=/OE=A0~A9= Vcc –0.2V or 0.2V, DQ0~DQ31= Vcc –0.2V, 0.2V or Open)		-	-	uA
$I_{I(L)}$	Input Leakage Current (Any Input (0V<=V_{IN}<= V_{IN} + 0.5V, All Other Pins Not Under Test = 0V)		-5	5	uA
$I_{O(L)}$	Output Leakage Current(DOUT is Disabled, 0V<=V_{OUT}<= Vcc)		-5	5	uA

Note: 1. Icc depends on output load condition when the device is selected.

Icc (max) is specified at the output open condition.

2. Address can be changed once or less while /RAS = $V_{IL.}$

3. Address can be changed once or less while /CAS = V_{IH}

CAPACITANCE (T_A=25°C, Vcc = 5V+/- 10%, f = 1Mhz)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS	NOTE
Input Capacitance (A0-A9)	C_{I1}	-	5	pF	1
Input Capacitance (/WE,/RAS, /CAS0-/CAS3,/OE)	C_{I2}	-	7	pF	1,2
Input/Output Capacitance (DQ0-31)	C_{DQ1}	-	7	pF	1,2

Note: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. /CAS = VIH to disable DOUT.

AC CHARACTERISTICS (0°C ≤ T_A ≤ 70°C , Vcc = 5V±10%, V_{IH}/V_{IL} = 2.4/0.8V, V_{OH}/V_{OL} =2.4/0.4V, See notes 1,2)

SYMBOL	PARAMETER	-5		-6		UNIT	NOTE
		MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	90		110		ns	
t_{RWC}	Read-modify-writer cycle time	110		130		ns	
t_{RAC}	Access Time from /RAS		50		60	ns	3,4,10
t_{CAC}	Access Time from /CAS		15		15	ns	3,4,5
t_{aa}	Access Time from Column Address		25		30	ns	3,10
t_{OFF}	Output Buffer Turn-off Time	0	12	0	12	ns	6
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	2
t_{RP}	/RAS Precharge Time	30		40		ns	
t_{RAS}	/RAS Pulse Width	50	10K	60	10K	ns	
t_{RSH}	/RAS Hold Time	15		15		ns	
t_{CSH}	/CAS Hold Time	50		60		ns	
t_{CAS}	/CAS Pulse Width	15	10K	15	10K	ns	
t_{RCD}	/RAS to /CAS Delay Time	20	35	20	45	ns	4
t_{RAD}	/RAS to Column Address Delay Time	15	25	15	30	ns	10
t_{CRP}	/CAS to /RAS Precharge Time	5		5		ns	
t_{ASR}	Row Address Setup Time	0		0		ns	
t_{RAH}	Row Address Hold Time	10		10		ns	
t_{ASC}	Column Address Setup Time	0		0		ns	11
t_{CAH}	Column Address Hold Time	10		10		ns	11
t_{RAL}	Column Address to /RAS Lead Time	25		30		ns	
t_{RCS}	Read Command Setup Time	0		0		ns	

t_{RCH}	Read Command Hold Time to /CAS	0		0		ns	8
t_{RRH}	Read Command Hold Time to /RAS	0		0		ns	8
t_{WCH}	Write Command Hold Time	10		10		ns	
t_{WP}	Write Command Pulse Width	10		10		ns	
t_{RWL}	Write Command to /RAS Lead Time	15		15		ns	
t_{CWL}	Write Command to /CAS Lead Time	13		15		ns	
t_{DS}	Data-in Setup Time	0		0		ns	9
t_{DH}	Data-in Hold Time	10		10		ns	9
t_{REF}	Refresh Period (1024 Cycle)		16		16	ms	
t_{wcs}	Write Command Setup Time	0		0		ms	7
t_{CWD}	/CAS to /WE delay time	15		15		ms	7,13
t_{RWD}	/RAS to /WE delay time	50		60		ns	7
t_{AWD}	Column Address to /WE delay time	25		30		ns	7
t_{CPWD}	/CAS precharge to /WE delay time	30		35		ns	7
t_{CSR}	/CAS Setup Time (/CAS-before-/RAS Refresh Cycle)	10		10		ns	15
t_{CHR}	/CAS Hold Time (/CAS-before-/RAS Refresh Cycle)	10		10		ns	16
t_{RPC}	/RAS Precharge to /CAS Hold Time	5		5		ns	
t_{CPA}	Access Time from /CAS Precharge		30		35	ns	3
t_{PC}	Fast Page Mode Cycle Time	35		40		ns	
t_{CP}	Fast Page Mode /RAS Precharge Time	10		10		ns	12
t_{RASP}	Fast Page Mode /CAS Pulse Time	50	200K	60	200K	ns	
t_{RHCP}	/RAS Hold Time time from /CAS Precharge	30		35		ns	
t_{RASS}	/RAS Pulse Width(CBR self refresh)	100		100		us	
t_{PRS}	/RAS Precharge Time(CBR self refresh)	90		110		ns	
t_{CHS}	/CAS Hold Time(CBR self refresh)	-50		-50		ns	

Note: 1. An initial pause of 200us is required after power-up followed by any 8 /RAS-only refresh or /CAS-before-/RAS refresh cycles

before proper device operation is achieved.

2. Input voltage levels are V_{IH} / V_{IL}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between . V_{IH} and V_{IL} are assumed to be 5ns for all inputs.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Operation with the $\mathbf{t}_{RCD}$ (max) limit insures that $\mathbf{t}_{RAC}$ (max) can be met, $\mathbf{t}_{RCD}$ (max) is specified as a reference point only, if $\mathbf{t}_{RCD}$ is greater than the specified $\mathbf{t}_{RCD}$(max) limit, then access time is controlled exclusively by $\mathbf{t}_{CAC}$.
5. Assumes that $\mathbf{t}_{RCD}$ <= $\mathbf{t}_{RCD}$ (max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} / V_{OL} .

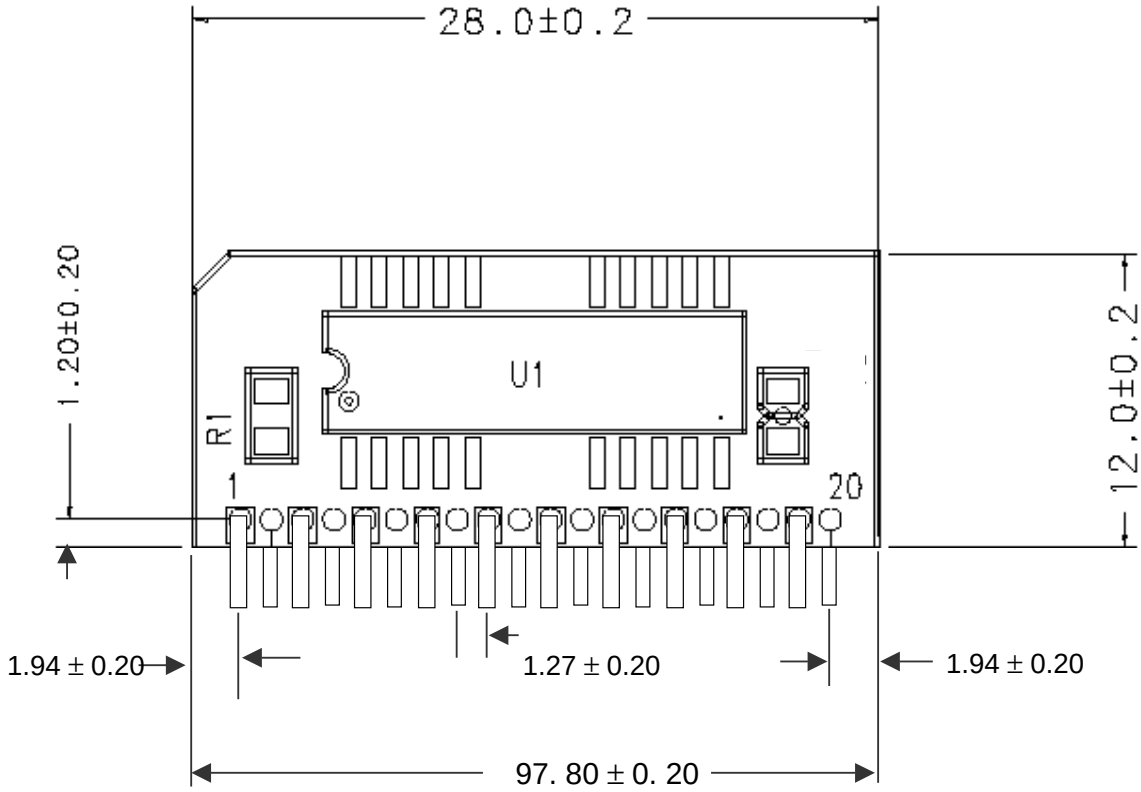
7. $T_{WCS,}$ $T_{RWD,}$ $T_{CWD,}$ T_{CPWD} are non restrictive operating parameter. They are included in the data sheet as electrical characteristics

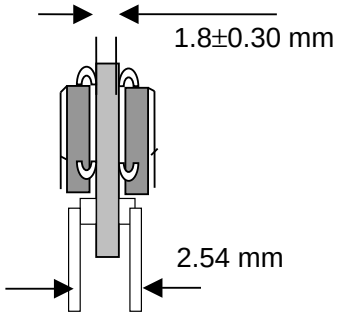
only. If $\mathbf{t}_{wcs}$ >= $\mathbf{t}_{wcs}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout

the entire cycle. If $\mathbf{t}_{CWD}$ >= $\mathbf{t}_{CWD}$ (min), $\mathbf{t}_{RWD}$ >= $\mathbf{t}_{RWD}$ (min), T_{CPWD}>= T_{CPWD}(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.

8. Either **t**RCH or **t**RRH must be satisfied for a read cycles.
9. These parameters are referenced to /CAS falling edge in early write cycles and to /WE falling edge in /OE controlled write cycle and read-modify-write cycles.
10. Operation with the $\mathbf{t}_{RAD}$ (max) limit insures that $\mathbf{t}_{RAC}$ (max) can be met, $\mathbf{t}_{RAD}$ (max) is specified as a reference point only, if $\mathbf{t}_{RAD}$ is greater than the specified $\mathbf{t}_{RAD}$ (max) limit, then access time is controlled exclusively by $\mathbf{t}_{AA}$.
11. $\mathbf{t}_{ASC,}$ $\mathbf{t}_{CAH}$ are are referenced to the earlier /CAS falling edge.
12. $\mathbf{t}_{CP}$ is specified from the later /CAS rising edge in the previous cycle to the earlier /CAS falling edge in the next cycle.
13. $\mathbf{t}_{CWD}$ is referenced to the later /CAS falling edge at word read-modify-write cycle.
14. $\mathbf{t}_{CWL}$ is specified from /WE falling edge to the earlier /CAS rising edge .
15. $\mathbf{t}_{CSR}$ is referenced to the earlier /CAS falling edge before /RAS transition low.
16. $\mathbf{t}_{CHR}$ is referenced to the later /CAS rising edge after /RAS transition low.

PACKAGING INFORMATION





ORDERING INFORMATION

Part Number	Density	Org.	Package	Component Number	Vcc	MODE	SPEED
HMD1M1Z1-5	1Mbit	1M x 1Bit	20 Pin-ZIP	1EA	5V	FP	50ns
HMD1M1Z1-6	1Mbit	1M x 1Bit	20 Pin-ZIP	1EA	5V	FP	60ns

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