

DESCRIPTION

The LTC[®] 1451/LTC1453, respectively, are 5V and 3V 12-bit, rail-to-rail output D/A converters. The LTC1451 draws 2mW and the LTC1453 draws 0.75mW. Both of these parts are monotonic over the industrial temperature range, with differential nonlinearity guaranteed to be less than 0.5LSB. The LTC1451 and LTC1453 are complete with a rail-to-rail output buffer amplifier and reference in an SO-8 package that occupies just 0.1 inch², including a bypass capacitor. The low power supply current and small size makes these circuits ideal for portable battery-powered applications. In addition, these circuits are also used for digital calibration, industrial process control and ATE. The LTC1451/LTC1453 demonstration board allows the user to evaluate the LTC1451 and LTC1453 12-bit rail-to-rail D/A converters. In addition, the LTC1451/LTC1453 demonstration board is intended to demonstrate layout and bypassing techniques required to obtain optimum performance from these parts. The demonstration board is designed to be easy to use and requires only one 7V to 15V supply. Since these DACs have a 3-pin serial interface (SPI and QSPI compatible), the demonstration board includes parallel-to-serial conversion circuitry. The user can set any 12-bit code by means of dip switches, or connect a

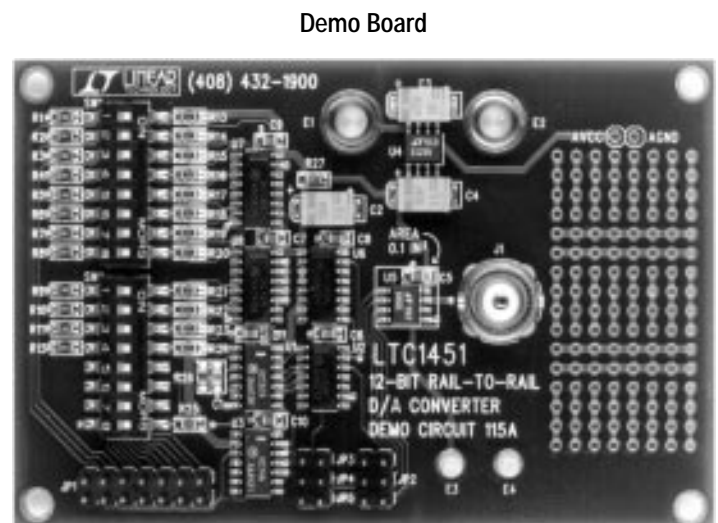
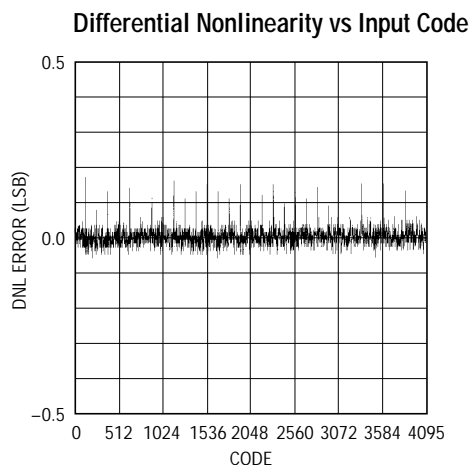
GPIO parallel bus to drive the LTC1451/LTC1453. The user can also drive the LTC1451/LTC1453 CLK, D_{IN} and CS/LD inputs directly through connections to the appropriate terminals. The outputs of the parallel-to-serial conversion circuitry are brought out to these same terminals for monitoring or driving other serial parts. The rail-to-rail voltage output of the LTC1451/LTC1453 is available on a BNC connector and the onboard reference of the LTC1451/LTC1453 is brought out to a terminal. This manual shows how to use this demonstration board and includes a timing diagram for driving the part with a 12-bit bus. Additionally, a schematic, parts list, drawings and dimensions of all the PC board layers are included. An explanation of the layout strategy is also provided. **Gerber files for this circuit board are available. Call the LTC factory.**

Some key features of this demonstration board include:

- 0.5LSB Max Differential Nonlinearity (0.2LSB typ)
- Rail-to-Rail Output Capability
- Convenient 12-Bit Parallel-to-Serial Converter
- Separate Prototype Area

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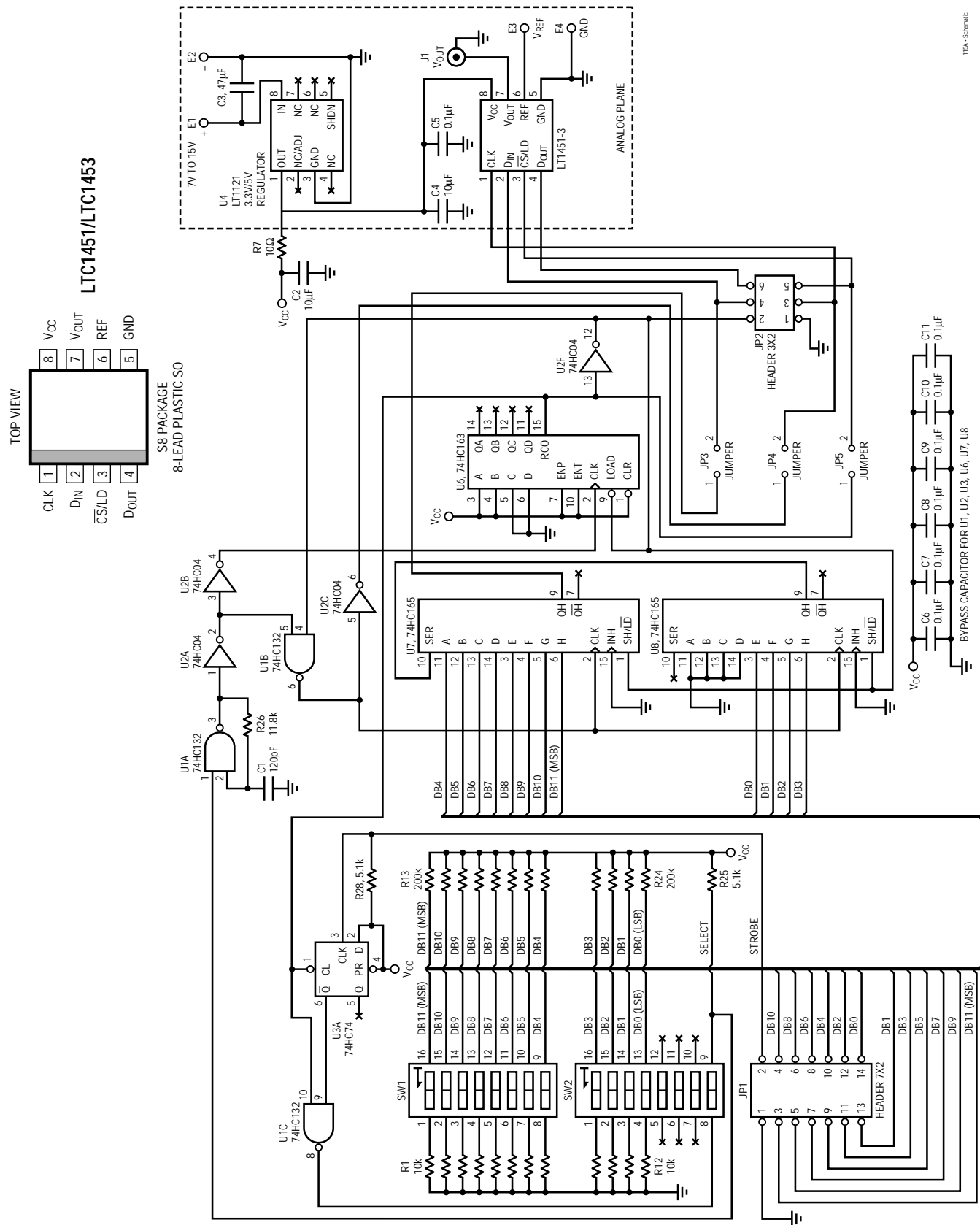
TYPICAL PERFORMANCE CHARACTERISTICS AND BOARD PHOTO



DEMO MANUAL DC115

12-BIT RAIL-TO-RAIL CONVERTER

PACKAGE AND SCHEMATIC DIAGRAMS



Demo Board Schematic

DEMO MANUAL DC115

12-BIT RAIL-TO-RAIL CONVERTER

PARTS LIST

| REFERENCE DESIGNATOR | QUANTITY | PART NUMBER | DESCRIPTION | VENDOR | TELEPHONE |
|----------------------|----------|-------------------|--|----------|----------------|
| C1 | 1 | 08055A121KATM | 120pF 50V NPO Chip Capacitor | AVX | (803) 946-0362 |
| C2, C4 | 2 | TPSD106M035R0100 | 10 μ F 35V 20% Tantalum Capacitor | AVX | (803) 946-0238 |
| C3 | 1 | TAJD476K016R | 47 μ F 16V 10% Tantalum Capacitor | AVX | (803) 946-0238 |
| C5 to C11 | 7 | 08055G104ZAT3S | 0.1 μ F 50V 20% Y5V Chip Capacitor | AVX | (803) 946-0362 |
| E1, E2 | 2 | 575-4 | Banana Jack | Keystone | (718) 956-8900 |
| E3, E4 | 2 | 1502-02 | Turret Terminal | Keystone | (718) 956-8900 |
| JP1 | 1 | 3201S-7-G1 | 0.100 7X2 Header | Com Con | (818) 301-4200 |
| JP2 (JP3, JP4, JP5) | 2 | 3201S-3-G1 | 0.100 3X2 Header | Com Con | (818) 301-4200 |
| J1 | 1 | 112404 | Vert PC-MNT Connector | Connex | (805) 378-6464 |
| R1 to R12 | 12 | CR21-103J-T 0805 | 10k 1/8W 5% Chip Resistor | AVX | (803) 946-0524 |
| R13 to R24 | 12 | CR21-204J-T 0805 | 200k 1/8W 5% Chip Resistor | AVX | (803) 946-0524 |
| R25, R28 | 2 | CR21-512J-T 0805 | 5.1k 1/8W 5% Chip Resistor | AVX | (803) 946-0524 |
| R26 | 1 | CR21-1182F-T 0805 | 11.8k 1/8W 1% Chip Resistor | AVX | (803) 946-0524 |
| R27 | 1 | CR21-100J-T 0805 | 10 Ω 1/8W 5% Chip Resistor | AVX | (803) 946-0524 |
| SW1,SW2 | 2 | DM08 (MORS) | SMD Switch | APEM | (781) 246-1007 |
| U1 | 1 | 74HC132AD | Quad 2-Input Nand Gate IC | Motorola | (602) 244-3576 |
| U2 | 1 | 74HC04AD | Hex Inverter IC | Motorola | (602) 244-3576 |
| U3 | 1 | 74HC74AD | Dual D Flip/Flop Set IC | Motorola | (602) 244-3576 |
| U4 (for 5V) | 1 | LT1121IS8-3.3/5 | Micropower Regulator ICs | LTC | (408) 432-1900 |
| U5 (for 5V) | 1 | LTC1451IS8 | Use with 5V LTC1451IS8 IC | LTC | (408) 432-1900 |
| U4 (for 3.3V) | 1 | LT1121IS8-5 | Micropower Regulator ICs | LTC | (408) 432-1900 |
| U5 (for 3.3V) | 1 | LTC1453IS8 | Use with 3.3V LTC1453IS8 | LTC | (408) 432-1900 |
| U6 | 1 | 74HC163AD | Presettable Counter IC | Motorola | (602) 244-3576 |
| U7, U8 | 2 | 74HC165D | 8-Bit Parallel Input IC | Motorola | (602) 244-3576 |
| | 4 | 4-40 | 1/2" Nylon Stand-Off Screw | Any | |
| | 4 | 4-40 | 1/4" Screw | Any | |
| | 3 | CCIJ230-G | Shunt | Com Con | (818) 301-4200 |

OPERATION

OPERATING THE BOARD

Powering the Board

To use the demonstration board, apply 7V to 15V at 10mA to banana jack E1 and 0V (GND) to banana jack E2. An internal regulator is included: an LT1121-5 provides a 5V supply for the LTC1451 board and an LT1121-3.3 provides a 3.3V supply for the LTC1453 board.

Operation Using the Onboard Dip Switches to Set Input Code

The two banks of dip-switches, SW1 and SW2, can be used to set the appropriate 12-bit input code for the LTC1451/LTC1453. The onboard parallel-to-serial conversion circuitry will generate the appropriate serial stream of data (CLK, D_{IN} and $\overline{CS/LD}$) for the LTC1451/LTC1453. The CLK, D_{IN} and $\overline{CS/LD}$ signals are present on JP2-3, JP2-4 and JP2-5, respectively. The $\overline{CS/LD}$ signal is inverted by U2F, creating an LD signal for the user. The LD signal is present on JP2-2. The LTC1451/LTC1453 D_{OUT} is also brought out to Pin 6 of JP2 along with GND on Pin 1. This pin provides a convenient GND terminal when measuring or driving these signals. The LTC1451/LTC1453 onboard reference is available on terminal E3. The LTC1451 has a 2.048V reference and the LTC1453 has a 1.22V reference.

Switch 1 on SW1 selects the logic state of the MSB (DB11) and switch 4 on SW2 selects the logic state of the LSB (DB0), as shown on the schematic. Switch 8 on SW2 selects the logic state of the SELECT signal. This signal activates the parallel-to-serial circuitry. Push the appropriate switch to the OFF position to set a bit high or to the ON position to set a bit low. Setting the SELECT switch to the OFF position places the parallel-to-serial circuitry in continuous mode. This mode continuously generates a serial stream of whatever is set on the data bits (switches 1–8 on SW1 and switches 1–4 on SW2). As soon as any

of these bits are changed, the serial stream, and hence the output of the LTC1451/LTC1453, changes appropriately. Move the SELECT switch to the ON position to stop the parallel-to-serial circuitry. Any changes on the data-bit switches will be ignored until the SELECT switch is returned to the OFF position.

Operation Using an External 12-Bit Parallel Bus

The inputs to the parallel-to-serial converter are also available on the pins of jumper JP1. Pin 3 is the MSB and Pin 14 is the LSB. The external data source is loaded by 200k pull-up resistors to V_{CC} and by 10k pull-down resistors through the switches, SW1 and SW2, to GND. These must be overdriven when an external 12-bit parallel data word is applied to JP1. The parallel-to-serial circuitry is activated by a falling-edge-triggered STROBE signal on Pin 2 of JP1. This STROBE pin is loaded by a 5.1k pull-up resistor to V_{CC} . Be sure to set the SELECT switch to the ON position for noncontinuous mode. If SELECT is still active, changing any bit on JP1 creates an instant change to the continuous serial data stream applied to the LTC1451/LTC1453. As soon as the 12-bit data word is loaded into the LTC1451/LTC1453, the parallel-to-serial circuitry can be activated once by a falling edge on STROBE (see the timing diagram in Figure 1).

Driving the CLK, D_{IN} and $\overline{CS/LD}$ Pins Directly

Through JP2, the LTC1451/LTC1453's SPI-compatible serial interface can receive data directly from an external serial data source. Disconnect jumpers JP3, JP4 and JP5 and use JP2 to drive the digital inputs. On JP2, Pin 3 is CLK, Pin 4 is D_{IN} and Pin 5 is $\overline{CS/LD}$. The LTC1451/LTC1453's daisy-chain serial data output, D_{OUT} , is also available on Pin 6 of JP2. This is the digital output from the onboard 12-bit shift register of the LTC1451/LTC1453. See timing diagram from LTC1451/LTC1452/LTC1453 data sheet for timing details.

OPERATION

LAYOUT

A well-designed printed circuit board layout incorporating the LTC1451/LTC1453 uses separate analog and digital ground planes. Because the LTC1451/LTC1453 has only one GND pin, it is acceptable to use only one ground plane on a PCB layout. However, if there is considerable digital circuitry on the board, such as on the LTC1451/LTC1453 demonstration board, it is advisable to have separate ground planes.

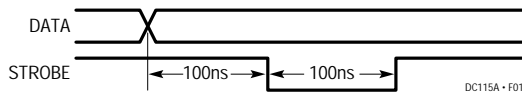


Figure 1. Timing Diagram For STROBE Signal

The demonstration board layout (section titled “PCB Layout and Film”) shows the best way to configure and connect the ground planes and the appropriate supply bypassing.

Table 1. Functional Description of User Configurable Jumpers

| JUMPER | JUMPER NAME | JUMPER CONNECTION |
|--------|------------------------|--|
| JP3 | D _{IN} Enable | Open to Drive D _{IN} Pin Externally |
| JP4 | CLK Enable | Open to Drive CLK Pin Externally |
| JP5 | CS/LD Enable | Open to Drive CS/LD Pin Externally |

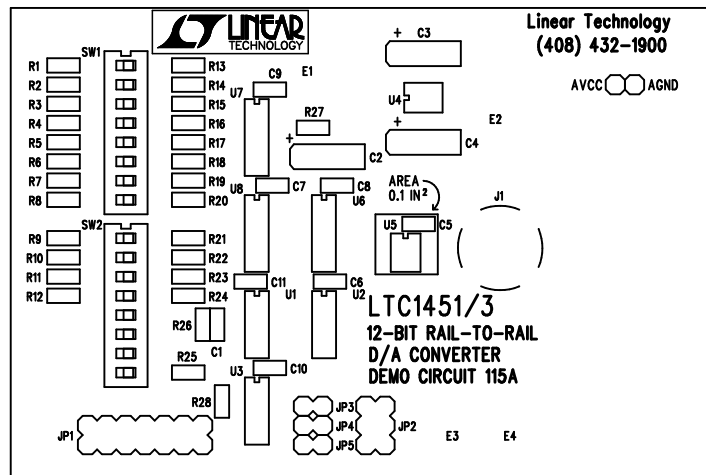
Table 2. Input and Output Pin Functional Description

| INPUT/OUTPUT PIN | FUNCTION |
|------------------|---|
| E1 | Supply Voltage: 7V to 15V at 10mA |
| E2 | Supply Ground |
| E3 | LTC1451/LTC1453 Reference Output |
| E4 | Analog Ground Terminal |
| J1 | LTC1451/LTC1453 Rail-to-Rail Voltage Output |
| JP1-1 | Digital Ground |
| JP1-2 | STROBE Input |
| JP1-3 | DB11 |
| JP1-4 | DB10 |
| JP1-5 | DB9 |
| JP1-6 | DB8 |
| JP1-7 | DB7 |
| JP1-8 | DB6 |
| JP1-9 | DB5 |
| JP1-10 | DB4 |
| JP1-11 | DB3 |
| JP1-12 | DB2 |
| JP1-13 | DB1 |
| JP1-14 | DB0 |
| JP2-1 | Digital Ground |
| JP2-2 | LD Output |
| JP2-3 | CLK Input/Output |
| JP2-4 | D _{IN} Input/Output |
| JP2-5 | CS/LD Input/Output |
| JP2-6 | LTC1451/LTC1453 D _{OUT} Output |

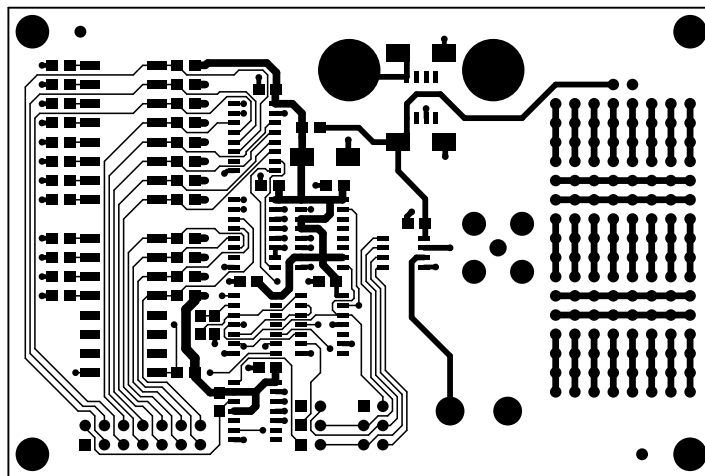
DEMO MANUAL DC115

12-BIT RAIL-TO-RAIL CONVERTER

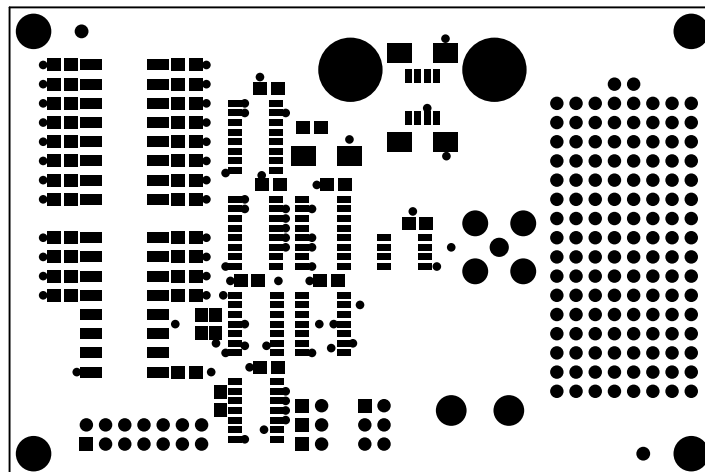
PCB LAYOUT AND FILM



Component Side Silkscreen



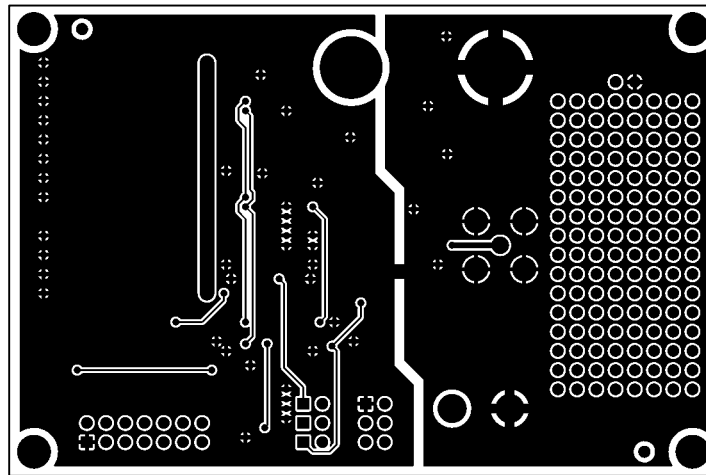
Component Side



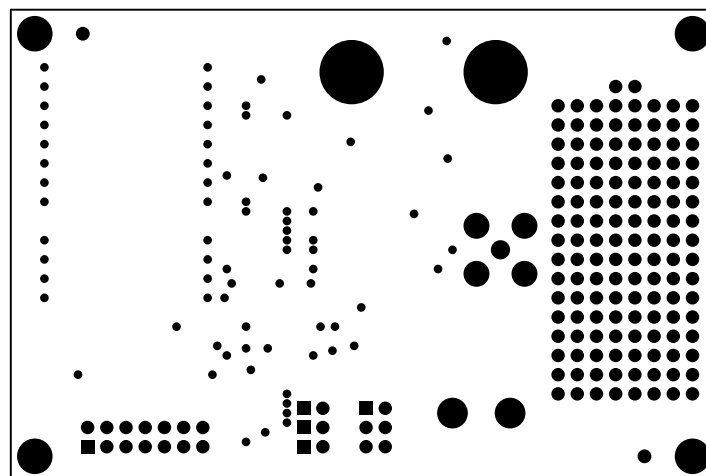
Component Side Mask

DEMO MANUAL DC115

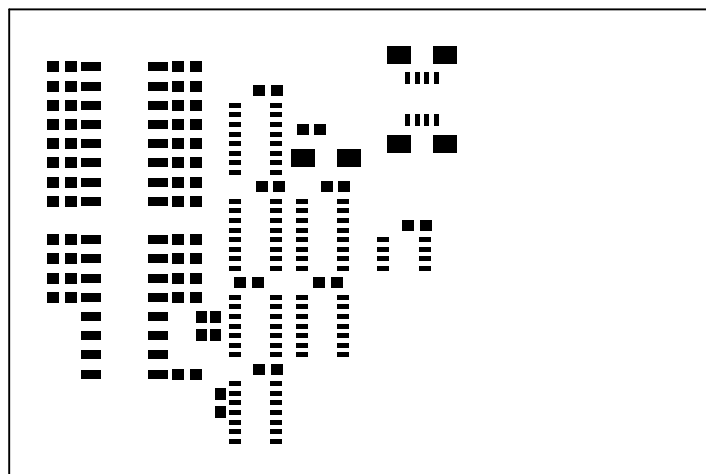
12-BIT RAIL-TO-RAIL CONVERTER



Solder Side



Solder Side Mask

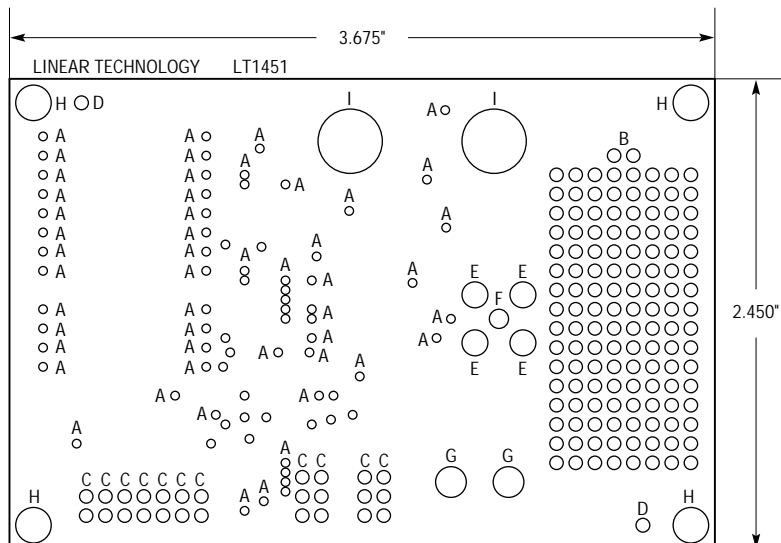


Pastemask Top

DEMO MANUAL DC115

12-BIT RAIL-TO-RAIL CONVERTER

PC FAB DRAWING



| SYMBOL | DIAMETER (INCH) | NUMBER OF HOLES | PLATED |
|--------|-----------------|-----------------|--------|
| A | 0.020 | 75 | YES |
| B | 0.035 | 130 | YES |
| C | 0.040 | 26 | YES |
| D | 0.072 | 2 | NO |
| E | 0.062 | 4 | YES |
| F | 0.052 | 1 | YES |
| G | 0.094 | 2 | YES |
| H | 0.125 | 4 | YES |
| I | 0.205 | 2 | YES |

NOTES: UNLESS OTHERWISE SPECIFIED

- MATERIAL: FR4 OR EQUIVALENT EPOXY, 2 OZ. COPPER CLAD. THICKNESS 0.061 ± 0.006 TOTAL OF 2 LAYERS.
- FINISH: ALL PLATED HOLES 0.001 MIN / 0.0015 MAX COPPER PLATE ELECTRODEPOSITED TIN-LEAD COMPOSITION. BEFORE RELOW, SOLDER MASK OVER BARE COPPER (SMOBC).
- SOLDER MASK: BOTH SIDES USING GREEN PC-401 OR EQUIVALENT
- SILKSCREEN: USING WHITE NON-CONDUCTIVE EPOXY INK.
- ALL DIMENSIONS ARE IN INCHES.



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