# VC709 Evaluation Board for the Virtex-7 FPGA

## *User Guide*

**UG887 (v1.6) March 11, 2019**

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# Revision History

The following table shows the revision history for this document.

| Date | Version | Revision |
|---|---|---|
| 02/04/2013 | 1.0 | Initial Xilinx release. |
| 06/04/2013 | 1.1 | Changed XC7VX690T-2FFG1761CES to XC7VX690T-2FFG1761C throughout the document. Changed SiT9122 to SiT9102. The data rate in Linear BPI Flash Memory changed from 40 MHz to 80 MHz. Added items 28 and 29 to the board photograph in Figure 1-2. FPGA EMCC clock information was added to Table 1-7, Table 1-8, Figure 1-13, and FPGA EMCC Clock. In Table 1-18, the DS1 description for RED changed. Replaced Figure 1-22 *Configuration Mode and Upper Linear Flash Address Switch*. Enhanced section Switches. Updated part ordering information in FMC_VADJ Voltage. Updated Figure 1-29 *VC709 Board Configuration Circuit*. Replaced Appendix C, *Master UCF Listing* with Xilinx Design Constraints. Updated References. |
| 01/07/2014 | 1.2 | Revised the content of Table 1-16. Revised Table 1-20 to correct connection of FMC1_HPC_LA29_N to FPGA pin T30 (Was W30). Revised all links and references in Appendix G, Additional Resources and revised links to web pages and documents throughout document to conform to latest linking style convention. Added caution note about power connections to J18 on the VC709 board on Appendix D. |
| 03/11/2014 | 1.2.1 | Tech Pubs edit. Technical content not affected. |

| Date | Version | Revision |
|---|---|---|
| 04/30/2014 | 1.3 | Revised the data rate for the small outline dual-inline memory modules (SODIMMs) in VC709 Board Features and Dual DDR3 Memory SODIMMs. |
| 12/04/2014 | 1.4 | Added MT28GU01GAAA1EGC-0SIT part number for the BPI parallel NOR flash memory component to Table 1-1, Linear BPI Flash Memory, and References. Added a note to Table 1-1. Updated User SMA Clock (USER_SMA_CLOCK_P and USER_SMA_CLOCK_N), Jitter-Attenuated Clock, I2C Bus, and Power Management. Updated part number in Figure 1-4. Updated Figure 1-11 to correct net names. Added I/O standard information to Table 1-4, Table 1-5, Table 1-6, Table 1-8, Table 1-14, Table 1-19, and Table 1-20. Added PCIe® edge connector information after Table 1-12. Updated description for XADC_GPIO_3, 2, 1, 0 in Table 1-25. Updated Table A-3 and added Figure A-3. Updated References. |
| 09/02/2015 | 1.4.1 | Made typographical edits. |
| 03/18/2016 | 1.5 | Updated Figure 1-16. Added thickness information in Appendix E, Board Specifications. |
| 08/12/2016 | 1.5.1 | Made a typographical edit. |
| 03/11/2019 | 1.6 | Added the latest version of ESD Directive in Electrostatic Discharge Caution. Updated the description of Dual DDR3 Memory SODIMMs. In Appendix C, Xilinx Design Constraints changed the title of the appendix, updated the description, and removed the VC709 Board XDC Listing. Updated Appendix F, Regulatory and Compliance Information. Updated Appendix G, Additional Resources. |

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Chapter 1

# VC709 Evaluation Board Features

## Overview

The VC709 evaluation board for the Virtex®-7 FPGA provides a hardware environment for developing and evaluating designs targeting the Virtex-7 XC7VX690T-2FFG1761C FPGA. The VC709 board provides features common to many embedded processing systems, including dual DDR3 small outline dual-inline memory module (SODIMM) memories, an 8-lane PCI Express® interface, general purpose I/O, and a UART interface. Other features can be added by using mezzanine cards attached to the VITA-57 FPGA mezzanine connector (FMC) provided on the board. A high pin count (HPC) FMC is provided. See VC709 Board Features for a complete list of features. The details for each feature are described in Feature Descriptions.

### Additional Information

See Appendix G, Additional Resources for references to documents, files, and resources relevant to the VC709 board.

### VC709 Board Features

- Virtex-7 XC7VX690T-2FFG1761C FPGA
- 2X 4 GB 1600MTs DDR3 memory SODIMMs
- 128 MB linear byte-wide peripheral interface (BPI) flash memory
- USB JTAG through Digilent module
- Clock generation
  - Fixed 200 MHz LVDS oscillator
  - Fixed 233.33 MHz LVDS oscillator
  - $I^2C$ programmable LVDS oscillator
  - SMA connectors
  - SMA connectors for GTH transceiver clocking
- GTH transceivers
  - FMC HPC connector (ten transceivers)
  - SMA connectors (one pair for MGT_REFCLK)
  - PCI Express (eight lanes)
  - 4 X Small form-factor pluggable plus (SFP+) connectors
- PCI Express endpoint connectivity
  - Gen1 8-lane (x8)
  - Gen2 8-lane (x8)

    - Gen3 8-lane (x8)
- 4 X SFP+ connectors
- USB-to-UART bridge
- $I^2C$ bus
    - $I^2C$ MUX
    - $I^2C$ EEPROM (1 KB)
    - USER $I^2C$ programmable LVDS oscillator
    - 2 X DDR3 SODIMM socket
    - FMC HPC connector
    - 4 X SFP+ connector
    - $I^2C$ programmable jitter-attenuating precision clock multiplier
- Status LEDs
    - 12VDC power on
    - TI controlled power good
    - Linear power good
    - FPGA INIT
    - FPGA DONE
- User I/O
    - User LEDs (eight GPIO)
    - User pushbuttons (five directional)
    - CPU reset pushbutton
    - User DIP switch (8-pole GPIO)
- Switches
    - Power on/off slide switch
    - FPGA_PROG_B pushbutton
    - Configuration mode DIP switch
- VITA 57.1 FMC HPC connector
- Power management
    - PMBus voltage and current monitoring through TI power controllers
- XADC header
- Configuration options
    - Linear BPI flash memory
    - USB JTAG (Digilent) configuration port

The VC709 board block diagram is shown in Figure 1-1.

## Electrostatic Discharge Caution

***Caution!*** ESD can damage electronic components when they are improperly handled, and can result in total or intermittent failures. Always follow ESD-prevention procedures when removing and replacing components.

To prevent ESD damage:

- Use an ESD wrist or ankle strap and ensure that it makes skin contact. Connect the equipment end of the strap to an unpainted metal surface on the chassis.
- Avoid touching the adapter against your clothing. The wrist strap protects components from ESD on the body only.
- Handle the adapter by its bracket or edges only. Avoid touching the printed circuit board or the connectors.
- Put the adapter down only on an antistatic surface such as the bag supplied in your kit.
- If you are returning the adapter to Xilinx Product Support, place it back in its antistatic bag immediately.

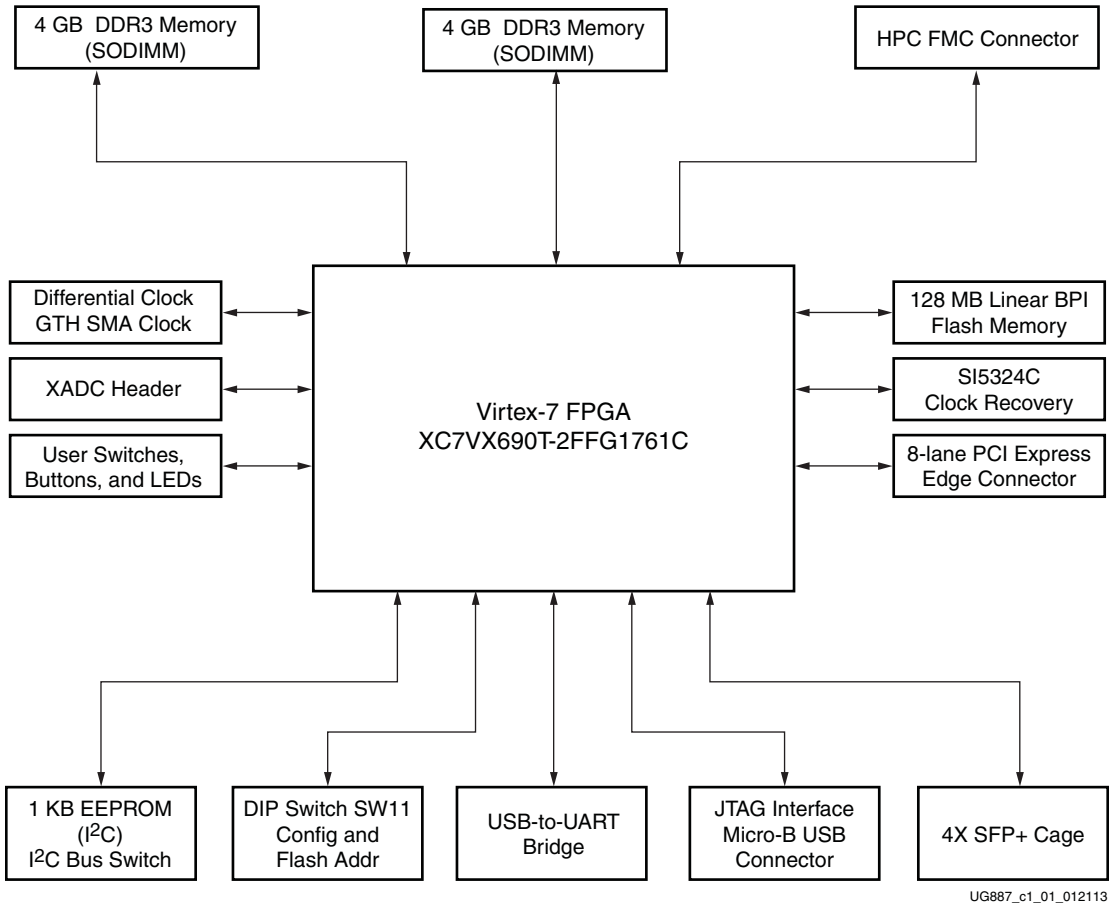


*Figure 1-1:* **VC709 Board Block Diagram**

# Feature Descriptions

Figure 1-2 shows the VC709 board. Each numbered feature that is referenced in Figure 1-2 is described in Table 1-1 and following sections.

***Note:*** The image in Figure 1-2 is for reference only and might not reflect the current revision of the board.

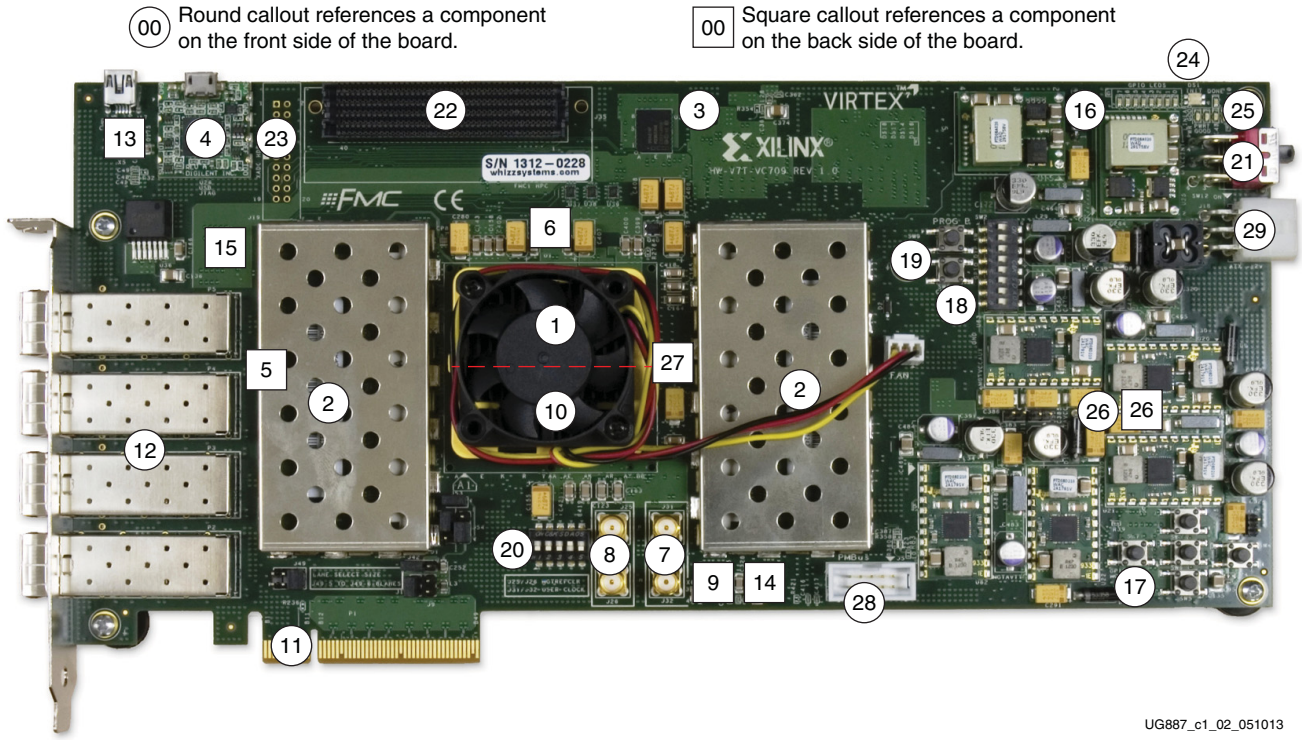


*Figure 1-2:* **VC709 Board Component Locations**

*Table 1-1:* **VC709 Board Component Descriptions**

| Callout | Reference Designator | Component Description | Notes | Schematic 0381499 Page Number |
|---|---|---|---|---|
| 1 | U1 | Virtex-7 FPGAXC7VX690T-2FFG1761C with cooling fan | XC7VX690T-2FFG1761C | |
| 2 | J1, J3 | Two DDR3 SODIMM memories (4 GB each) | Micron MT8KTF51264HZ-1G9E1 | 10, 14 |
| 3 | U3 | BPI parallel NOR flash memory (1 Gb) | Micron PC28F00AG18FE/ MT28GU01GAAA1EGC-0SIT | 24 |
| 4 | U26 | USB JTAG interface (micro-B USB connector) | Digilent USB JTAG module | 5 |
| 5 | U51 | System clock, 200 MHz, LVDS (back side of board) | SiTime SIT9102-243N25E200.0000 | 3 |
| 6 | U34 | $I^2C$ programmable user clock LVDS, 156.250 MHz default frequency (back side of board) | Silicon Labs SI570BAB0000544DG ($I^2C$ 0x5D) | 3 |
| 7 | J31, J32 | User SMA clock | Rosenberger 32K10K-400L5 | 3 |

*Table 1-1:* **VC709 Board Component Descriptions *(Cont'd)***

| Callout | Reference Designator | Component Description | Notes | Schematic 0381499 Page Number |
|---|---|---|---|---|
| 8 | J25, J26 | GTH transceiver SMA reference clock | Rosenberger 32K10K-400L5 | 30 |
| 9 | U24 | Jitter-attenuated clock (back side of board) | Silicon Labs SI5324C-C-GM | 4 |
| 10 | U1 | GTH transceiver Quad 111–Quad 119 | Embedded within FPGA U1 | 30, 36–38 |
| 11 | P1 | PCI Express connector | 8-lane card edge connector | 35 |
| 12 | P2–P5 | 4 X SFP/SFP+ module connector ($I^2C$ 0x50) | Molex 74441-0010 | 31–35 |
| 13 | U44, J17 | USB-to-UART bridge with mini-B USB connector | Silicon Labs CP2103GM | 6 |
| 14 | U52 | $I^2C$ bus switch ($I^2C$ 0x74) (back side of board) | TI PCA9548ARGER | 29 |
| 15 | U14 | $I^2C$ bus switch ($I^2C$ 0x75) (back side of board) | TI PCA9546ARGVR | 29 |
| 16 | DS2–DS9 | User LEDs, Green | Lumex SML-LX0603GW | 25 |
| 17 | SW3–SW7 | User pushbuttons, active-High | E-Switch TL3301EP100QG | 25 |
| 18 | SW2 | User DIP switch, active-High | 8-pole C and K SDA08H1SBD | 25 |
| 19 | SW8, SW9 | CPU RESET, FPGA PROG pushbuttons | E-Switch TL3301EP100QG | 25, 7 |
| 20 | SW11 | Configuration mode/upper linear flash address DIP switch | 5-pole C and K SDA05H1IBD | 7 |
| 21 | SW12 | Power on/off slide switch | C and K 1201M2S3AQE2 | 46 |
| 22 | J35 | FMC HPC connector | Samtec ASP_134486_01 | 18–21 |
| 23 | J19 | Xilinx XADC header | 2 x 10 0.1-inch male header | 27 |
| 24 | DS1 | INIT LED, dual color Red/Green | Avago HSMF-C155 | 38 |
| 25 | DS10, DS14, DS16–DS18 | Power ON and Power GOOD LEDs | Lumex SML-LX0603GW | 38 |
| 26 | Various | Power management system (front and back side of board) | TI UCD9248PFC in conjunction with various regulators | 45–56 |
| 27 | U13 | Memory clock, 233.33 MHz, LVDS (back side of board) | SiTime SIT9122AC-2D3-25E233.333333 | 3 |
| 28 | J35 | 2 x 5 shrouded PMBus connector | Assman HW10G-0202 | 46 |
| 29 | J18 | 12V power input 2 x 3 connector | Molex 39-30-1060 | 46 |

**Notes:**

1. Jumper header locations are identified in Appendix A, Default Switch and Jumper Settings.

# Virtex-7 XC7VX690T-2FFG1761C FPGA

[Figure 1-2, callout 1]

The VC709 board is populated with the *Virtex-7 XC7VX690T-2FFG1761C FPGA*.

For further information on Virtex-7 FPGAs, see *7 Series FPGAs Overview* (DS180) [Ref 1].

## FPGA Configuration

The VC709 board supports two of the five 7 series FPGA configuration modes:

- Master BPI using the onboard linear BPI flash memory
- JTAG using a type-A to micro-B USB cable for connecting the host PC to the VC709 board configuration port

Each configuration interface corresponds to one or more configuration modes and bus widths as listed in Table 1-2. The mode switches M2, M1, and M0 are on SW11 positions 3, 4, and 5 respectively as shown in Figure 1-3.

***Note:*** To determine the FPGA type resident on the VC709 board, see the Virtex-7 VC709 Evaluation Kit Master Answer Record (AR 51901).

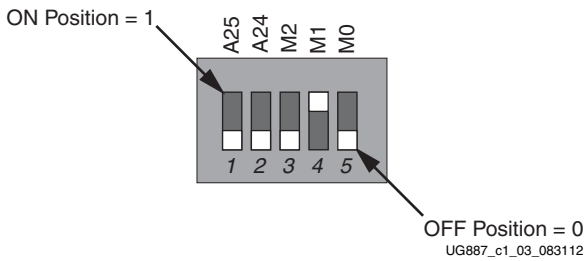


*Figure 1-3:* **SW11 Default Settings**

The default mode setting is M[2:0] = `010`, which selects Master BPI at board power-on. See Configuration Options for detailed information about the mode switch SW11.

*Table 1-2:* **VC709 Board FPGA Configuration Modes**

| Configuration Mode | SW13 DIP Switch Settings (M[2:0]) | Bus Width | CCLK Direction |
|---|---|---|---|
| Master BPI | `010` | x8, x16 | Output |
| JTAG | `101` | x1 | Not applicable |

For full details on configuring the FPGA, see *7 Series FPGAs Configuration User Guide* (UG470) [Ref 3].

## I/O Voltage Rails

There are 17 I/O banks available on the Virtex-7 device. Fourteen I/O banks are available on the VC709 board, and banks 12, 16, and 18 are not used. The voltages applied to the FPGA I/O banks used by the VC709 board are listed in Table 1-3.

*Table 1-3:* **I/O Voltage Rails**

| FPGA (U1) Bank | Power Supply Rail Net Name | Voltage |
|---|---|---|
| Bank 0 | VCC1V8_FPGA | 1.8V |
| Bank 12 | NOT USED | 1.8V |
| Bank 13 | VCC1V8_FPGA | 1.8V |
| Bank 14 | VCC1V8_FPGA | 1.8V |
| Bank 15 | VCC1V8_FPGA | 1.8V |
| Bank 16 | NOT USED | 1.8V |
| Bank 17 | VCC1V8_FPGA | 1.8V |
| Bank 18 | NOT USED | 1.8V |
| Bank 19 | VCC1V8_FPGA | 1.8V |
| Bank 31 | VCC1V5_FPGA | 1.5V |
| Bank 32 | VCC1V5_FPGA | 1.5V |
| Bank 33 | VCC1V5_FPGA | 1.5V |
| Bank 34 | VCC1V8_FPGA | 1.8V |
| Bank 35 | VADJ_FPGA | 1.8V |
| Bank 36 | FMC1_VIO_B_M2C | Variable |
| Bank 37 | VCC1V5_FPGA | 1.5V |
| Bank 38 | VCC1V5_FPGA | 1.5V |
| Bank 39 | VCC1V5_FPGA | 1.5V |

## Dual DDR3 Memory SODIMMs

[Figure 1-2, callout 2]

The memory modules at J1 and J3 are 4 GB DDR3 small outline dual-inline memory modules (SODIMMs), providing volatile synchronous dynamic random access memory (SDRAM) for storing user code and data.

- Part number: MT8KTF51264HZ-1G9E1 (Micron Technology)
- Supply voltage: 1.5V
- Configuration: 4GB (512 Mb x 64)
- Datapath width: 64 bits
- Data rate: Up to 1600 MT/s

The VC709 XC7VX690T FPGA memory interface performance is documented in the *Virtex-7 T and XT FPGAs Data Sheet: DC and AC Switching Characteristics* (DS183) [Ref 2].

Each DDR3 interface is implemented across three I/O banks: 37, 38, and 39 for J1 and 31, 32 and 33 for J3. Each bank is a 1.5V high-performance bank having a dedicated DCI VRP/N resistor connection. An external 0.75V reference $V_{TTREF}$ is provided for data interface banks 37, 39, 31, and 33. Any interface connected to these banks that requires a reference voltage must use this FPGA voltage reference. The connections between the DDR3 memory SODIMM sockets and the FPGA are listed in Table 1-4 and Table 1-5.

*Table 1-4:* **DDR3 SODIMM Socket J1 Connections to the FPGA**

| XCVX690T (U1) Pin | Net Name | I/O Standard | DDR3 SODIMM Memory J1 | |
|---|---|---|---|---|
| | | | Pin Number | Pin Number |
| A20 | DDR3_A_A0 | SSTL15 | 98 | A0 |
| B19 | DDR3_A_A1 | SSTL15 | 97 | A1 |
| C20 | DDR3_A_A2 | SSTL15 | 96 | A2 |
| A19 | DDR3_A_A3 | SSTL15 | 95 | A3 |
| A17 | DDR3_A_A4 | SSTL15 | 92 | A4 |
| A16 | DDR3_A_A5 | SSTL15 | 91 | A5 |
| D20 | DDR3_A_A6 | SSTL15 | 90 | A6 |
| C18 | DDR3_A_A7 | SSTL15 | 86 | A7 |
| D17 | DDR3_A_A8 | SSTL15 | 89 | A8 |
| C19 | DDR3_A_A9 | SSTL15 | 85 | A9 |
| B21 | DDR3_A_A10 | SSTL15 | 107 | A10/AP |
| B17 | DDR3_A_A11 | SSTL15 | 84 | A11 |
| A15 | DDR3_A_A12 | SSTL15 | 83 | A12_BC_N |
| A21 | DDR3_A_A13 | SSTL15 | 119 | A13 |
| F17 | DDR3_A_A14 | SSTL15 | 80 | A14 |
| E17 | DDR3_A_A15 | SSTL15 | 78 | A15 |
| D21 | DDR3_A_BA0 | SSTL15 | 109 | BA0 |

*Table 1-4:* **DDR3 SODIMM Socket J1 Connections to the FPGA *(Cont'd)***

| XCVX690T (U1) Pin | Net Name | I/O Standard | DDR3 SODIMM Memory J1 | |
|---|---|---|---|---|
| | | | Pin Number | Pin Number |
| C21 | DDR3_A_BA1 | SSTL15 | 108 | BA1 |
| D18 | DDR3_A_BA2 | SSTL15 | 79 | BA2 |
| N14 | DDR3_A_D0 | SSTL15 | 5 | DQ0 |
| N13 | DDR3_A_D1 | SSTL15 | 7 | DQ1 |
| L14 | DDR3_A_D2 | SSTL15 | 15 | DQ2 |
| M14 | DDR3_A_D3 | SSTL15 | 17 | DQ3 |
| M12 | DDR3_A_D4 | SSTL15 | 4 | DQ4 |
| N15 | DDR3_A_D5 | SSTL15 | 6 | DQ5 |
| M11 | DDR3_A_D6 | SSTL15 | 16 | DQ6 |
| L12 | DDR3_A_D7 | SSTL15 | 18 | DQ7 |
| K14 | DDR3_A_D8 | SSTL15 | 21 | DQ8 |
| K13 | DDR3_A_D9 | SSTL15 | 23 | DQ9 |
| H13 | DDR3_A_D10 | SSTL15 | 33 | DQ10 |
| J13 | DDR3_A_D11 | SSTL15 | 35 | DQ11 |
| L16 | DDR3_A_D12 | SSTL15 | 22 | DQ12 |
| L15 | DDR3_A_D13 | SSTL15 | 24 | DQ13 |
| H14 | DDR3_A_D14 | SSTL15 | 34 | DQ14 |
| J15 | DDR3_A_D15 | SSTL15 | 36 | DQ15 |
| E15 | DDR3_A_D16 | SSTL15 | 39 | DQ16 |
| E13 | DDR3_A_D17 | SSTL15 | 41 | DQ17 |
| F15 | DDR3_A_D18 | SSTL15 | 51 | DQ18 |
| E14 | DDR3_A_D19 | SSTL15 | 53 | DQ19 |
| G13 | DDR3_A_D20 | SSTL15 | 40 | DQ20 |
| G12 | DDR3_A_D21 | SSTL15 | 42 | DQ21 |
| F14 | DDR3_A_D22 | SSTL15 | 50 | DQ22 |
| G14 | DDR3_A_D23 | SSTL15 | 52 | DQ23 |
| B14 | DDR3_A_D24 | SSTL15 | 57 | DQ24 |
| C13 | DDR3_A_D25 | SSTL15 | 59 | DQ25 |
| B16 | DDR3_A_D26 | SSTL15 | 67 | DQ26 |
| D15 | DDR3_A_D27 | SSTL15 | 69 | DQ27 |
| D13 | DDR3_A_D28 | SSTL15 | 56 | DQ28 |
| E12 | DDR3_A_D29 | SSTL15 | 58 | DQ29 |

Table 1-4: **DDR3 SODIMM Socket J1 Connections to the FPGA *(Cont'd)***

| XCVX690T (U1) Pin | Net Name | I/O Standard | DDR3 SODIMM Memory J1 | |
|---|---|---|---|---|
| | | | Pin Number | Pin Number |
| C16 | DDR3_A_D30 | SSTL15 | 68 | DQ30 |
| D16 | DDR3_A_D31 | SSTL15 | 70 | DQ31 |
| A24 | DDR3_A_D32 | SSTL15 | 129 | DQ32 |
| B23 | DDR3_A_D33 | SSTL15 | 131 | DQ33 |
| B27 | DDR3_A_D34 | SSTL15 | 141 | DQ34 |
| B26 | DDR3_A_D35 | SSTL15 | 143 | DQ35 |
| A22 | DDR3_A_D36 | SSTL15 | 130 | DQ36 |
| B22 | DDR3_A_D37 | SSTL15 | 132 | DQ37 |
| A25 | DDR3_A_D38 | SSTL15 | 140 | DQ38 |
| C24 | DDR3_A_D39 | SSTL15 | 142 | DQ39 |
| E24 | DDR3_A_D40 | SSTL15 | 147 | DQ40 |
| D23 | DDR3_A_D41 | SSTL15 | 149 | DQ41 |
| D26 | DDR3_A_D42 | SSTL15 | 157 | DQ42 |
| C25 | DDR3_A_D43 | SSTL15 | 159 | DQ43 |
| E23 | DDR3_A_D44 | SSTL15 | 146 | DQ44 |
| D22 | DDR3_A_D45 | SSTL15 | 148 | DQ45 |
| F22 | DDR3_A_D46 | SSTL15 | 158 | DQ46 |
| E22 | DDR3_A_D47 | SSTL15 | 160 | DQ47 |
| A30 | DDR3_A_D48 | SSTL15 | 163 | DQ48 |
| D27 | DDR3_A_D49 | SSTL15 | 165 | DQ49 |
| A29 | DDR3_A_D50 | SSTL15 | 175 | DQ50 |
| C28 | DDR3_A_D51 | SSTL15 | 177 | DQ51 |
| D28 | DDR3_A_D52 | SSTL15 | 164 | DQ52 |
| B31 | DDR3_A_D53 | SSTL15 | 166 | DQ53 |
| A31 | DDR3_A_D54 | SSTL15 | 174 | DQ54 |
| A32 | DDR3_A_D55 | SSTL15 | 176 | DQ55 |
| E30 | DDR3_A_D56 | SSTL15 | 181 | DQ56 |
| F29 | DDR3_A_D57 | SSTL15 | 183 | DQ57 |
| F30 | DDR3_A_D58 | SSTL15 | 191 | DQ58 |
| F27 | DDR3_A_D59 | SSTL15 | 193 | DQ59 |
| C30 | DDR3_A_D60 | SSTL15 | 180 | DQ60 |
| E29 | DDR3_A_D61 | SSTL15 | 182 | DQ61 |

*Table 1-4:* **DDR3 SODIMM Socket J1 Connections to the FPGA *(Cont'd)***

| XCVX690T (U1) Pin | Net Name | I/O Standard | DDR3 SODIMM Memory J1 | |
|---|---|---|---|---|
| | | | Pin Number | Pin Number |
| F26 | DDR3_A_D62 | SSTL15 | 192 | DQ62 |
| D30 | DDR3_A_D63 | SSTL15 | 194 | DQ63 |
| M13 | DDR3_A_DM0 | SSTL15 | 11 | DM0 |
| K15 | DDR3_A_DM1 | SSTL15 | 28 | DM1 |
| F12 | DDR3_A_DM2 | SSTL15 | 46 | DM2 |
| A14 | DDR3_A_DM3 | SSTL15 | 63 | DM3 |
| C23 | DDR3_A_DM4 | SSTL15 | 136 | DM4 |
| D25 | DDR3_A_DM5 | SSTL15 | 153 | DM5 |
| C31 | DDR3_A_DM6 | SSTL15 | 170 | DM6 |
| F31 | DDR3_A_DM7 | SSTL15 | 187 | DM7 |
| M16 | DDR3_A_DQS0_N | DIFF_SSTL15 | 10 | DQS0_N |
| N16 | DDR3_A_DQS0_P | DIFF_SSTL15 | 12 | DQS0_P |
| J12 | DDR3_A_DQS1_N | DIFF_SSTL15 | 27 | DQS1_N |
| K12 | DDR3_A_DQS1_P | DIFF_SSTL15 | 29 | DQS1_P |
| G16 | DDR3_A_DQS2_N | DIFF_SSTL15 | 45 | DQS2_N |
| H16 | DDR3_A_DQS2_P | DIFF_SSTL15 | 47 | DQS2_P |
| C14 | DDR3_A_DQS3_N | DIFF_SSTL15 | 62 | DQS3_N |
| C15 | DDR3_A_DQS3_P | DIFF_SSTL15 | 64 | DQS3_P |
| A27 | DDR3_A_DQS4_N | DIFF_SSTL15 | 135 | DQS4_N |
| A26 | DDR3_A_DQS4_P | DIFF_SSTL15 | 137 | DQS4_P |
| E25 | DDR3_A_DQS5_N | DIFF_SSTL15 | 152 | DQS5_N |
| F25 | DDR3_A_DQS5_P | DIFF_SSTL15 | 154 | DQS5_P |
| B29 | DDR3_A_DQS6_N | DIFF_SSTL15 | 169 | DQS6_N |
| B28 | DDR3_A_DQS6_P | DIFF_SSTL15 | 171 | DQS6_P |
| E28 | DDR3_A_DQS7_N | DIFF_SSTL15 | 186 | DQS7_N |
| E27 | DDR3_A_DQS7_P | DIFF_SSTL15 | 188 | DQS7_P |
| E18 | DDR3_A_CLK0_N | DIFF_SSTL15 | 103 | CK0_N |
| E19 | DDR3_A_CLK0_P | DIFF_SSTL15 | 101 | CK0_P |
| F19 | DDR3_A_CLK1_N | DIFF_SSTL15 | 104 | CK1_N |
| G19 | DDR3_A_CLK1_P | DIFF_SSTL15 | 102 | CK1_P |
| K19 | DDR3_A_CKE0 | SSTL15 | 73 | CKE0 |
| J18 | DDR3_A_CKE1 | SSTL15 | 74 | CKE1 |

*Table 1-4:* **DDR3 SODIMM Socket J1 Connections to the FPGA *(Cont'd)***

| XCVX690T (U1) Pin | Net Name | I/O Standard | DDR3 SODIMM Memory J1 | |
|---|---|---|---|---|
| | | | Pin Number | Pin Number |
| E20 | DDR3_A_RAS_B | SSTL15 | 110 | RAS_B |
| F20 | DDR3_A_WE_B | SSTL15 | 113 | WE_B |
| K17 | DDR3_A_CAS_B | SSTL15 | 115 | CAS_B |
| H20 | DDR3_A_ODT0 | SSTL15 | 116 | ODT0 |
| H18 | DDR3_A_ODT1 | SSTL15 | 120 | ODT1 |
| J17 | DDR3_A_S0_B | SSTL15 | 114 | S0_B |
| J20 | DDR3_A_S1_B | SSTL15 | 121 | S1_B |
| P18 | DDR3_A_RESET_B | SSTL15 | 30 | RESET_B |
| G17 | DDR3_A_TEMP_EVENT_B | SSTL15 | 198 | EVENT_B |

*Table 1-5:* **DDR3 SODIMM Socket J3 Connections to the FPGA**

| XCVX690T (U1) Pin | Net Name | I/O Standard | DDR3 SODIMM Memory J3 | |
|---|---|---|---|---|
| | | | Pin Number | Pin Name |
| AN19 | DDR3_B_A0 | SSTL15 | 98 | A0 |
| AR19 | DDR3_B_A1 | SSTL15 | 97 | A1 |
| AP20 | DDR3_B_A2 | SSTL15 | 96 | A2 |
| AP17 | DDR3_B_A3 | SSTL15 | 95 | A3 |
| AP18 | DDR3_B_A4 | SSTL15 | 92 | A4 |
| AJ18 | DDR3_B_A5 | SSTL15 | 91 | A5 |
| AN16 | DDR3_B_A6 | SSTL15 | 90 | A6 |
| AM16 | DDR3_B_A7 | SSTL15 | 86 | A7 |
| AK18 | DDR3_B_A8 | SSTL15 | 89 | A8 |
| AK19 | DDR3_B_A9 | SSTL15 | 85 | A9 |
| AM17 | DDR3_B_A10 | SSTL15 | 107 | A10/AP |
| AM18 | DDR3_B_A11 | SSTL15 | 84 | A11 |
| AL17 | DDR3_B_A12 | SSTL15 | 83 | A12_BC_N |
| AK17 | DDR3_B_A13 | SSTL15 | 119 | A13 |
| AM19 | DDR3_B_A14 | SSTL15 | 80 | A14 |
| AL19 | DDR3_B_A15 | SSTL15 | 78 | A15 |
| AR17 | DDR3_B_BA0 | SSTL15 | 109 | BA0 |
| AR18 | DDR3_B_BA1 | SSTL15 | 108 | BA1 |
| AN18 | DDR3_B_BA2 | SSTL15 | 79 | BA2 |

*Table 1-5:* **DDR3 SODIMM Socket J3 Connections to the FPGA *(Cont'd)***

| XCVX690T (U1) Pin | Net Name | I/O Standard | DDR3 SODIMM Memory J3 | |
|---|---|---|---|---|
| | | | Pin Number | Pin Name |
| AN24 | DDR3_B_D0 | SSTL15 | 5 | DQ0 |
| AM24 | DDR3_B_D1 | SSTL15 | 7 | DQ1 |
| AR22 | DDR3_B_D2 | SSTL15 | 15 | DQ2 |
| AR23 | DDR3_B_D3 | SSTL15 | 17 | DQ3 |
| AN23 | DDR3_B_D4 | SSTL15 | 4 | DQ4 |
| AM23 | DDR3_B_D5 | SSTL15 | 6 | DQ5 |
| AN21 | DDR3_B_D6 | SSTL15 | 16 | DQ6 |
| AP21 | DDR3_B_D7 | SSTL15 | 18 | DQ7 |
| AK23 | DDR3_B_D8 | SSTL15 | 21 | DQ8 |
| AJ23 | DDR3_B_D9 | SSTL15 | 23 | DQ9 |
| AL21 | DDR3_B_D10 | SSTL15 | 33 | DQ10 |
| AM21 | DDR3_B_D11 | SSTL15 | 35 | DQ11 |
| AJ21 | DDR3_B_D12 | SSTL15 | 22 | DQ12 |
| AJ20 | DDR3_B_D13 | SSTL15 | 24 | DQ13 |
| AK20 | DDR3_B_D14 | SSTL15 | 34 | DQ14 |
| AL20 | DDR3_B_D15 | SSTL15 | 36 | DQ15 |
| AW22 | DDR3_B_D16 | SSTL15 | 39 | DQ16 |
| AW23 | DDR3_B_D17 | SSTL15 | 41 | DQ17 |
| AW21 | DDR3_B_D18 | SSTL15 | 51 | DQ18 |
| AV21 | DDR3_B_D19 | SSTL15 | 53 | DQ19 |
| AU23 | DDR3_B_D20 | SSTL15 | 40 | DQ20 |
| AV23 | DDR3_B_D21 | SSTL15 | 42 | DQ21 |
| AR24 | DDR3_B_D22 | SSTL15 | 50 | DQ22 |
| AT24 | DDR3_B_D23 | SSTL15 | 52 | DQ23 |
| BB24 | DDR3_B_D24 | SSTL15 | 57 | DQ24 |
| BA24 | DDR3_B_D25 | SSTL15 | 59 | DQ25 |
| AY23 | DDR3_B_D26 | SSTL15 | 67 | DQ26 |
| AY24 | DDR3_B_D27 | SSTL15 | 69 | DQ27 |
| AY25 | DDR3_B_D28 | SSTL15 | 56 | DQ28 |
| BA25 | DDR3_B_D29 | SSTL15 | 58 | DQ29 |
| BB21 | DDR3_B_D30 | SSTL15 | 68 | DQ30 |
| BA21 | DDR3_B_D31 | SSTL15 | 70 | DQ31 |

*Table 1-5:* **DDR3 SODIMM Socket J3 Connections to the FPGA *(Cont'd)***

| XCVX690T (U1) Pin | Net Name | I/O Standard | DDR3 SODIMM Memory J3 | |
|---|---|---|---|---|
| | | | Pin Number | Pin Name |
| AY14 | DDR3_B_D32 | SSTL15 | 129 | DQ32 |
| AW15 | DDR3_B_D33 | SSTL15 | 131 | DQ33 |
| BB14 | DDR3_B_D34 | SSTL15 | 141 | DQ34 |
| BB13 | DDR3_B_D35 | SSTL15 | 143 | DQ35 |
| AW12 | DDR3_B_D36 | SSTL15 | 130 | DQ36 |
| AY13 | DDR3_B_D37 | SSTL15 | 132 | DQ37 |
| AY12 | DDR3_B_D38 | SSTL15 | 140 | DQ38 |
| BA12 | DDR3_B_D39 | SSTL15 | 142 | DQ39 |
| AU12 | DDR3_B_D40 | SSTL15 | 147 | DQ40 |
| AU13 | DDR3_B_D41 | SSTL15 | 149 | DQ41 |
| AT12 | DDR3_B_D42 | SSTL15 | 157 | DQ42 |
| AU14 | DDR3_B_D43 | SSTL15 | 159 | DQ43 |
| AV13 | DDR3_B_D44 | SSTL15 | 146 | DQ44 |
| AW13 | DDR3_B_D45 | SSTL15 | 148 | DQ45 |
| AT15 | DDR3_B_D46 | SSTL15 | 158 | DQ46 |
| AR15 | DDR3_B_D47 | SSTL15 | 160 | DQ47 |
| AL15 | DDR3_B_D48 | SSTL15 | 163 | DQ48 |
| AJ15 | DDR3_B_D49 | SSTL15 | 165 | DQ49 |
| AK14 | DDR3_B_D50 | SSTL15 | 175 | DQ50 |
| AJ12 | DDR3_B_D51 | SSTL15 | 177 | DQ51 |
| AJ16 | DDR3_B_D52 | SSTL15 | 164 | DQ52 |
| AL16 | DDR3_B_D53 | SSTL15 | 166 | DQ53 |
| AJ13 | DDR3_B_D54 | SSTL15 | 174 | DQ54 |
| AK13 | DDR3_B_D55 | SSTL15 | 176 | DQ55 |
| AR14 | DDR3_B_D56 | SSTL15 | 181 | DQ56 |
| AT14 | DDR3_B_D57 | SSTL15 | 183 | DQ57 |
| AM12 | DDR3_B_D58 | SSTL15 | 191 | DQ58 |
| AP11 | DDR3_B_D59 | SSTL15 | 193 | DQ59 |
| AM13 | DDR3_B_D60 | SSTL15 | 180 | DQ60 |
| AN13 | DDR3_B_D61 | SSTL15 | 182 | DQ61 |
| AM11 | DDR3_B_D62 | SSTL15 | 192 | DQ62 |
| AN11 | DDR3_B_D63 | SSTL15 | 194 | DQ63 |

*Table 1-5:* **DDR3 SODIMM Socket J3 Connections to the FPGA *(Cont'd)***

| XCVX690T (U1) Pin | Net Name | I/O Standard | DDR3 SODIMM Memory J3 | |
|---|---|---|---|---|
| | | | Pin Number | Pin Name |
| AT22 | DDR3_B_DM0 | SSTL15 | 11 | DM0 |
| AL22 | DDR3_B_DM1 | SSTL15 | 28 | DM1 |
| AU24 | DDR3_B_DM2 | SSTL15 | 46 | DM2 |
| BB23 | DDR3_B_DM3 | SSTL15 | 63 | DM3 |
| BB12 | DDR3_B_DM4 | SSTL15 | 136 | DM4 |
| AV15 | DDR3_B_DM5 | SSTL15 | 153 | DM5 |
| AK12 | DDR3_B_DM6 | SSTL15 | 170 | DM6 |
| AP13 | DDR3_B_DM7 | SSTL15 | 187 | DM7 |
| AP22 | DDR3_B_DQS0_N | DIFF_SSTL15 | 10 | DQS0_N |
| AP23 | DDR3_B_DQS0_P | DIFF_SSTL15 | 12 | DQS0_P |
| AK22 | DDR3_B_DQS1_N | DIFF_SSTL15 | 27 | DQS1_N |
| AJ22 | DDR3_B_DQS1_P | DIFF_SSTL15 | 29 | DQS1_P |
| AU21 | DDR3_B_DQS2_N | DIFF_SSTL15 | 45 | DQS2_N |
| AT21 | DDR3_B_DQS2_P | DIFF_SSTL15 | 47 | DQS2_P |
| BB22 | DDR3_B_DQS3_N | DIFF_SSTL15 | 62 | DQS3_N |
| BA22 | DDR3_B_DQS3_P | DIFF_SSTL15 | 64 | DQS3_P |
| BA14 | DDR3_B_DQS4_N | DIFF_SSTL15 | 135 | DQS4_N |
| BA15 | DDR3_B_DQS4_P | DIFF_SSTL15 | 137 | DQS4_P |
| AR12 | DDR3_B_DQS5_N | DIFF_SSTL15 | 152 | DQS5_N |
| AP12 | DDR3_B_DQS5_P | DIFF_SSTL15 | 154 | DQS5_P |
| AL14 | DDR3_B_DQS6_N | DIFF_SSTL15 | 169 | DQS6_N |
| AK15 | DDR3_B_DQS6_P | DIFF_SSTL15 | 171 | DQS6_P |
| AN14 | DDR3_B_DQS7_N | DIFF_SSTL15 | 186 | DQS7_N |
| AN15 | DDR3_B_DQS7_P | DIFF_SSTL15 | 188 | DQS7_P |
| AU17 | DDR3_B_CLK0_N | DIFF_SSTL15 | 101 | CK0_P |
| AT17 | DDR3_B_CLK0_P | DIFF_SSTL15 | 103 | CK0_N |
| AV18 | DDR3_B_CLK1_N | DIFF_SSTL15 | 102 | CK1_P |
| AU18 | DDR3_B_CLK1_P | DIFF_SSTL15 | 104 | CK1_N |
| AW17 | DDR3_B_CKE0 | SSTL15 | 73 | CKE0 |
| AW18 | DDR3_B_CKE1 | SSTL15 | 74 | CKE1 |
| AV19 | DDR3_B_RAS_B | SSTL15 | 110 | RAS_B |
| AU19 | DDR3_B_WE_B | SSTL15 | 113 | WE_B |

*Table 1-5:* **DDR3 SODIMM Socket J3 Connections to the FPGA *(Cont'd)***

| XCVX690T (U1) Pin | Net Name | I/O Standard | DDR3 SODIMM Memory J3 | |
|---|---|---|---|---|
| | | | Pin Number | Pin Name |
| AT20 | DDR3_B_CAS_B | SSTL15 | 115 | CAS_B |
| AT16 | DDR3_B_ODT0 | SSTL15 | 116 | ODT0 |
| AW16 | DDR3_B_ODT1 | SSTL15 | 120 | ODT1 |
| AV16 | DDR3_B_S0_B | SSTL15 | 114 | S0_B |
| AT19 | DDR3_B_S1_B | SSTL15 | 121 | S1_B |
| BB19 | DDR3_B_RESET_B | SSTL15 | 30 | RESET_B |
| AU16 | DDR3_B_TEMP_EVENT_B | SSTL15 | 198 | EVENT_B |

The VC709 DDR3 SODIMM interfaces adhere to the constraints guidelines documented in the DDR3 Design Guidelines section of *7 Series FPGAs Memory Interface Solutions User Guide* (UG586) [Ref 4]. The VC709 DDR3 SODIMM interfaces are 40Ω impedance implementations. Other memory interface details are also available in *7 Series FPGAs Memory Interface Solutions User Guide* (UG586) [Ref 4] and *7 Series FPGAs Memory Resources User Guide* (UG473) [Ref 5].

## Linear BPI Flash Memory

[Figure 1-2, callout 3]

The linear BPI flash memory located at U3 provides 128 MB of nonvolatile storage that can be used for configuration or software storage. The data, address, and control signals are connected to the FPGA. The BPI flash memory device is packaged in a 64-pin BGA.

- Part number: PC28F00AG18FE/MT28GU01GAAA1EGC-0SIT

  ***Note:*** MT28GU01GAAA1EGC-0SIT is a new Micron part, and either part might be installed on the VC709 board.
- Supply voltage: 1.8V
- Datapath width: 16 bits (26 address lines and 7 control signals)
- Data rate: Up to 80 MHz

The linear BPI flash memory can synchronously configure the FPGA in Master BPI mode at the 80 MHz data rate supported by the flash memory by using a configuration bitstream generated with BitGen options for synchronous configuration. The fastest configuration method uses the external 80 MHz oscillator connected to the FPGA EMCCLK pin.

Multiple bitstreams can be stored in the linear BPI flash. The two most significant address bits (A25, A24) of the flash memory are connected to DIP switch SW11 positions 1 and 2 respectively, and to the RS1 and RS0 pins of the FPGA. By placing valid XC7VX690T bitstreams at four different offset addresses in the flash memory, 1 of the 4 bitstreams can be selected to configure the FPGA by appropriately setting the DIP switch SW11. The connections between the BPI flash memory and the FPGA are listed in Table 1-6.

*Table 1-6:* **BPI Flash Memory Connections to the FPGA**

| FPGA (U1) Pin | Net Name | I/O Standard | BPI Flash Memory (U3) | |
|---|---|---|---|---|
| | | | Pin Number | Pin Name |
| AJ28 | FLASH_A0 | LVCMOS18 | A1 | A1 |
| AH28 | FLASH_A1 | LVCMOS18 | B1 | A2 |
| AG31 | FLASH_A2 | LVCMOS18 | C1 | A3 |
| AF30 | FLASH_A3 | LVCMOS18 | D1 | A4 |
| AK29 | FLASH_A4 | LVCMOS18 | D2 | A5 |
| AK28 | FLASH_A5 | LVCMOS18 | A2 | A6 |
| AG29 | FLASH_A6 | LVCMOS18 | C2 | A7 |
| AK30 | FLASH_A7 | LVCMOS18 | A3 | A8 |
| AJ30 | FLASH_A8 | LVCMOS18 | B3 | A9 |
| AH30 | FLASH_A9 | LVCMOS18 | C3 | A10 |
| AH29 | FLASH_A10 | LVCMOS18 | D3 | A11 |
| AL30 | FLASH_A11 | LVCMOS18 | C4 | A12 |
| AL29 | FLASH_A12 | LVCMOS18 | A5 | A13 |
| AN33 | FLASH_A13 | LVCMOS18 | B5 | A14 |
| AM33 | FLASH_A14 | LVCMOS18 | C5 | A15 |
| AM32 | FLASH_A15 | LVCMOS18 | D7 | A16 |
| AV41 | FLASH_A16 | LVCMOS18 | D8 | A17 |
| AU41 | FLASH_A17 | LVCMOS18 | A7 | A18 |
| BA42 | FLASH_A18 | LVCMOS18 | B7 | A19 |
| AU42 | FLASH_A19 | LVCMOS18 | C7 | A20 |
| AT41 | FLASH_A20 | LVCMOS18 | C8 | A21 |
| BA40 | FLASH_A21 | LVCMOS18 | A8 | A22 |
| BA39 | FLASH_A22 | LVCMOS18 | G1 | A23 |
| BB39 | FLASH_A23 | LVCMOS18 | H8 | A24 |
| AW42 | FLASH_A24 | LVCMOS18 | B6 | A25 |
| AW41 | FLASH_A25 | LVCMOS18 | B8 | A26 |
| NA | NC | NA | H1 | A27 |
| AM36 | FLASH_D0 | LVCMOS18 | F2 | DQ0 |

*Table 1-6:* **BPI Flash Memory Connections to the FPGA *(Cont'd)***

| FPGA (U1) Pin | Net Name | I/O Standard | BPI Flash Memory (U3) | |
|---|---|---|---|---|
| | | | Pin Number | Pin Name |
| AN36 | FLASH_D1 | LVCMOS18 | E2 | DQ1 |
| AJ36 | FLASH_D2 | LVCMOS18 | G3 | DQ2 |
| AJ37 | FLASH_D3 | LVCMOS18 | E4 | DQ3 |
| AK37 | FLASH_D4 | LVCMOS18 | E5 | DQ4 |
| AL37 | FLASH_D5 | LVCMOS18 | G5 | DQ5 |
| AN35 | FLASH_D6 | LVCMOS18 | G6 | DQ6 |
| AP35 | FLASH_D7 | LVCMOS18 | H7 | DQ7 |
| AM37 | FLASH_D8 | LVCMOS18 | E1 | DQ8 |
| AG33 | FLASH_D9 | LVCMOS18 | E3 | DQ9 |
| AH33 | FLASH_D10 | LVCMOS18 | F3 | DQ10 |
| AK35 | FLASH_D11 | LVCMOS18 | F4 | DQ11 |
| AL35 | FLASH_D12 | LVCMOS18 | F5 | DQ12 |
| AJ31 | FLASH_D13 | LVCMOS18 | H5 | DQ13 |
| AH34 | FLASH_D14 | LVCMOS18 | G7 | DQ14 |
| AJ35 | FLASH_D15 | LVCMOS18 | E7 | DQ15 |
| AM34 | FLASH_WAIT | LVCMOS18 | F7 | WAIT |
| BB41 | FPGA_FWE_B | LVCMOS18 | G8 | WE_B |
| BA41 | FLASH_OE_B | LVCMOS18 | F8 | OE_B |
| N10 | FPGA_CCLK | LVCMOS18 | E6 | CLK |
| AL36 | FLASH_CE_B | LVCMOS18 | B4 | CE_B |
| AY37 | FLASH_ADV_B | LVCMOS18 | F6 | ADV_B |
| AG11 | FPGA_INIT_B | LVCMOS18 | D4 | RST_B |

Additional FPGA bitstreams can be stored and used for configuration by setting the Warm Boot Start Address (WBSTAR) register contained in 7 series FPGAs. More information is available in the reconfiguration and multiboot section in *7 Series FPGAs Configuration User Guide* (UG470) [Ref 3].

The configuration section of *7 Series FPGAs Configuration User Guide* (UG470) [Ref 3] provides details on the Master BPI configuration mode.

Figure 1-4 shows the linear BPI flash memory on the VC709 board. For more details, see the Micron Technology, Inc MT28GU01GAAA1EGC data sheet[Ref 13].

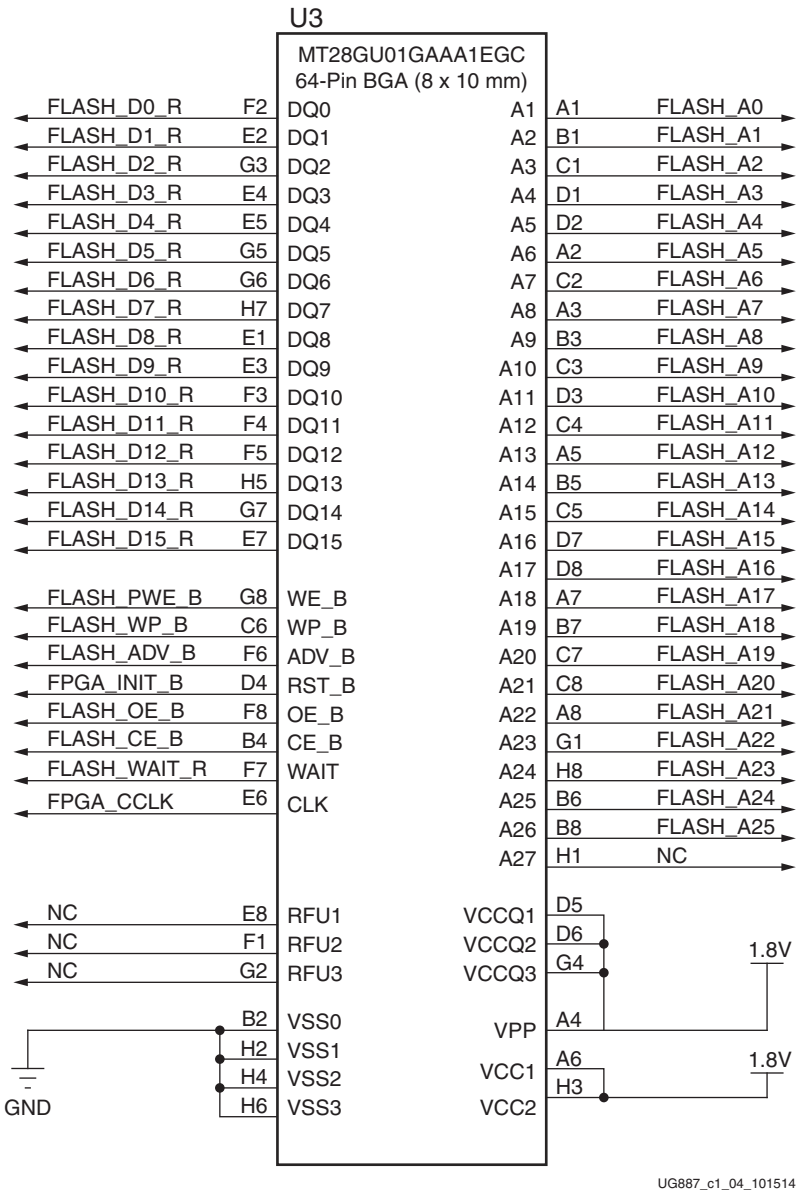


*Figure 1-4:* **128 MB Linear Flash Memory (U3)**

## USB JTAG

[Figure 1-2, callout 4]

JTAG configuration is provided solely through a Digilent onboard USB-to-JTAG configuration logic module (U26) where a host computer accesses the VC709 board JTAG chain through a type-A (host side) to micro-B (VC709 board side) USB cable.

The JTAG chain of the VC709 board is illustrated in Figure 1-5. JTAG configuration is allowed at any time regardless of FPGA mode pin settings. JTAG initiated configuration takes priority over the configuration method selected through the FPGA mode pin settings at SW11.

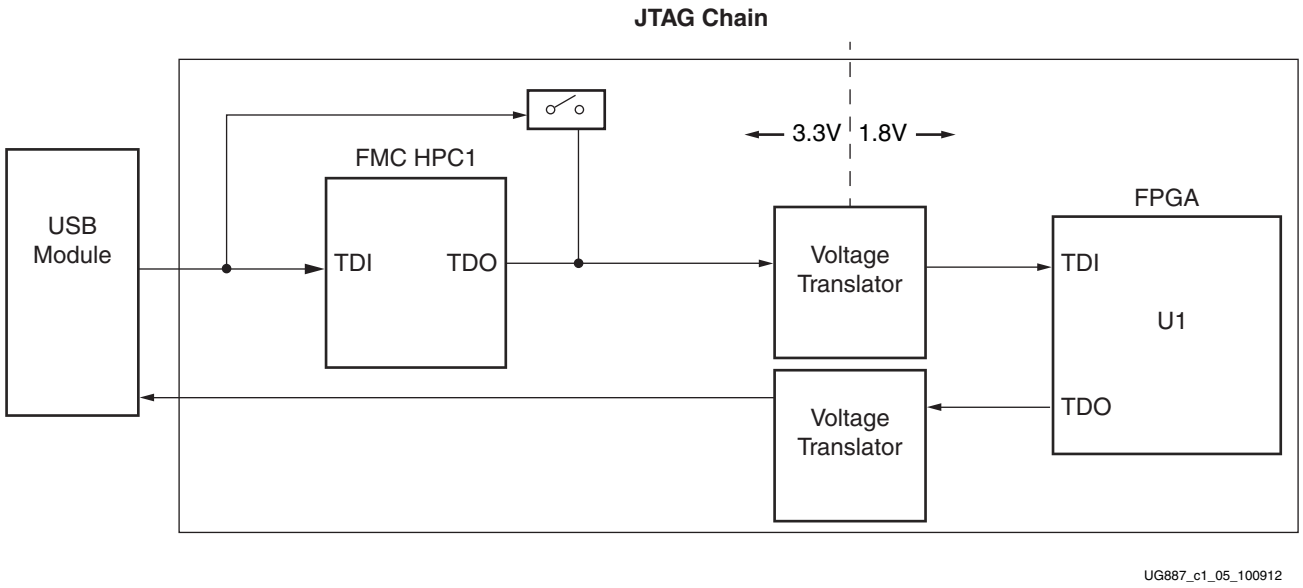


*Figure 1-5:* **JTAG Chain Block Diagram**

When an FMC mezzanine card is attached to the VC709 HPC connector J35, it is automatically added to the JTAG chain through electronically controlled single-pole single-throw (SPST) switch U27. The SPST switch is in a normally closed state and transitions to an open state when an FMC mezzanine card is attached. Switch U27 adds an attached FMC mezzanine card to the FPGAs JTAG chain as determined by the FMC_HPC_PRSNT_M2C_B signal. The attached FMC card must implement a TDI-to-TDO connection through a device or bypass jumper for the JTAG chain to be completed to the FPGA U1.

The JTAG connectivity on the VC709 board allows a host computer to download bitstreams to the FPGA using the Xilinx tools. In addition, the JTAG connector allows debug tools or a software debugger to access the FPGA. The Xilinx tools can also indirectly program the linear BPI flash memory. To accomplish this, the Xilinx tools configure the FPGA with a temporary design to access and program the BPI memory device.

The JTAG circuit details are shown in Figure 1-6.

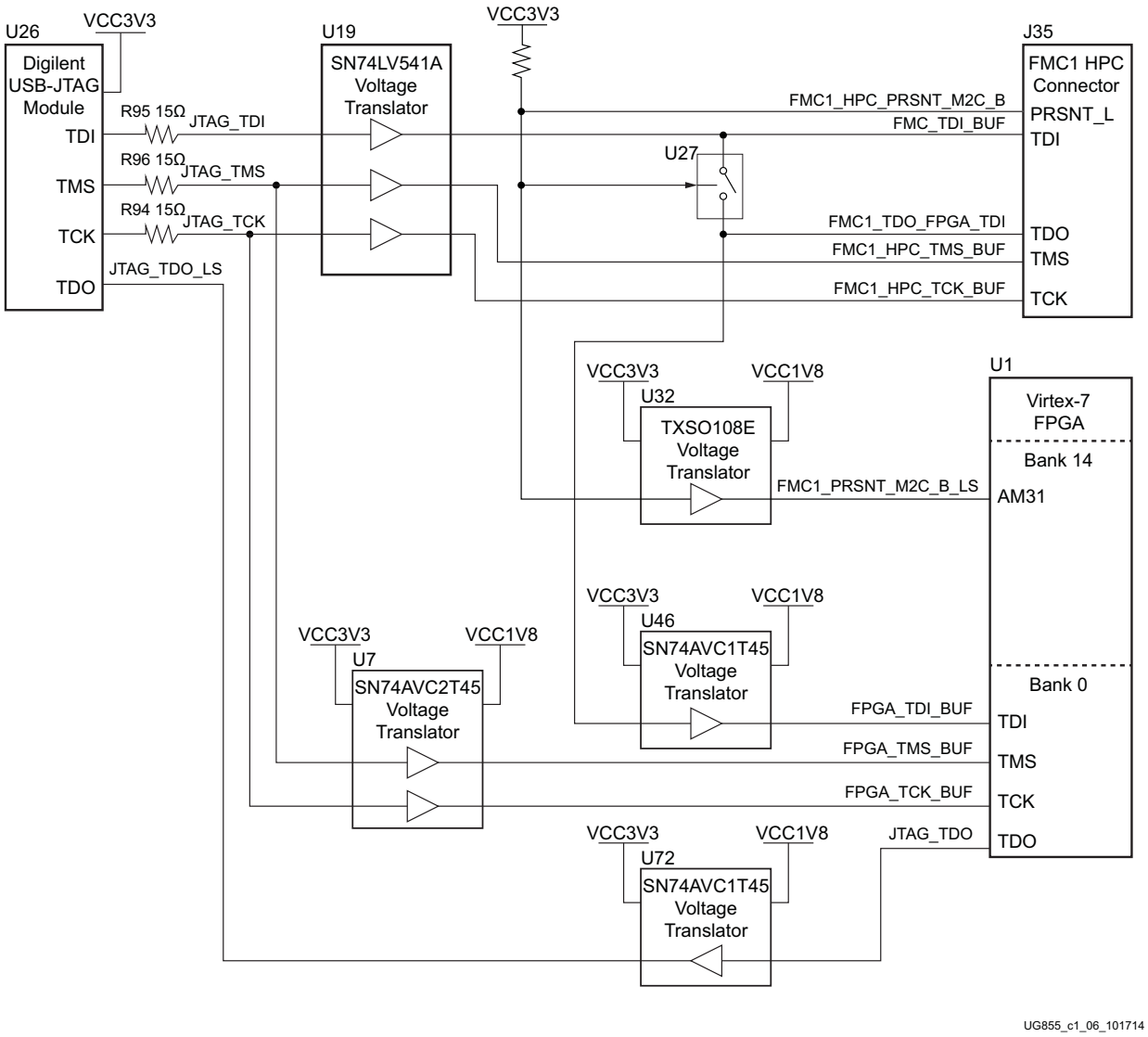


*Figure 1-6:* **JTAG Circuit**

## Clock Generation

The VC709 board provides six clock sources for the FPGA. Table 1-7 lists the source devices for each clock.

*Table 1-7:* **VC709 Board Clock Sources**

| Clock Name | Clock Source | Description |
|---|---|---|
| System clock | U51 | SiT9102 2.5V LVDS 200 MHz fixed frequency oscillator (Si Time)<br>See System Clock (SYSCLK_P and SYSCLK_N). |
| User clock | U34 | Si570 3.3V LVDS $I^2C$ Programmable Oscillator, ($I^2C$ address `0x5D`), 156.250 MHz default (Silicon Labs).<br>See Programmable User Clock (USER_CLOCK_P and USER_CLOCK_N). |
| User SMA clock (differential pair) | J31 | USER_SMA_CLOCK_P (net name)<br>See User SMA Clock (USER_SMA_CLOCK_P and USER_SMA_CLOCK_N). |
| | J32 | USER_SMA_CLOCK_N (net name)<br>See User SMA Clock (USER_SMA_CLOCK_P and USER_SMA_CLOCK_N). |
| GTH SMA REF clock (differential pair) | J25 | SMA_MGT_REFCLK_C_P (net name)<br>See GTH SMA Clock (SMA_MGT_REFCLK_P and SMA_MGT_REFCLK_N). |
| | J26 | SMA_MGT_REFCLK_C_N (net name)<br>See GTH SMA Clock (SMA_MGT_REFCLK_P and SMA_MGT_REFCLK_N). |
| Jitter-attenuated clock | U24 | Si5324C LVDS precision clock multiplier/jitter attenuator (Silicon Labs)<br>See Jitter-Attenuated Clock. |
| Memory clock | U13 | SiT9122 2.5V LVDS 233.33 MHz fixed frequency oscillator (Si Time).<br>See Memory Clock (SYSCLK_233_P and SYSCLK_233_N). |
| FPGA EMCC clock | U40 | SiT8103 LVCMOS single-ended, 80 MHz, fixed-frequency oscillator (Si Time). See FPGA EMCC Clock. |

Table 1-8 lists the pin-to-pin connections from each clock source to the FPGA.

*Table 1-8:* **Clock Connections, Source to FPGA**

| Clock Source Pin | Net Name | I/O Standard | XCVX690T (U1) Pin |
|---|---|---|---|
| U51.5 | SYSCLK_N | DIFF_SSTL15 | G18 |
| U51.4 | SYSCLK_P | DIFF_SSTL15 | H19 |
| U34.5 | USER_CLOCK_N | LVDS | AL34 |
| U34.4 | USER_CLOCK_P | LVDS | AK34 |
| J26.1 | SMA_MGT_REFCLK_N | NA | AK7 |
| J25.1 | SMA_MGT_REFCLK_P | NA | AK8 |
| J32.1 | USER_SMA_CLOCK_N | LVDS | AK32 |
| J31.1 | USER_SMA_CLOCK_P | LVDS | AJ32 |
| U24.29 | Si5324_OUT_N | LVDS | AH7 |
| U24.28 | Si5324_OUT_P | LVDS | AH8 |
| U13.5 | SYSCLK_233_N | DIFF_SSTL15 | AY17 |
| U13.4 | SYSCLK_233_P | DIFF_SSTL15 | AY18 |
| U40.3 | FPGA_EMCCLK | LVCMOS18 | AP37 |

## System Clock (SYSCLK_P and SYSCLK_N)

[Figure 1-2, callout 5]

The VC709 board has an LVDS 200 MHz oscillator (U51) soldered onto the back side of the board and wired to an FPGA MRCC clock input on bank 38. This 200 MHz signal pair is named SYSCLK_P and SYSCLK_N, which are connected to FPGA U1 pins H19 and G18 respectively.

- Oscillator: Si Time SiT9102AI-243N25E200.00000 (200 MHz)
- PPM frequency jitter: 50 ppm
- Differential output

The LVDS termination resistor R2, located within the FPGA via matrix on the bottom of the board, is not populated. One possible I/O standard for the FPGA design clock input is:

```
NET "sysclk_p"  LOC = "H19" | IOSTANDARD = DIFF_SSTL15_DCI | #Bank 38
MRCC input
NET "sysclk_n"  LOC = "G18" | IOSTANDARD = DIFF_SSTL15_DCI | #Diff.
Rterm R2 DNP
```

For more details, see the Si Time SiT9102 data sheet. The system clock circuit is shown in Figure 1-7.

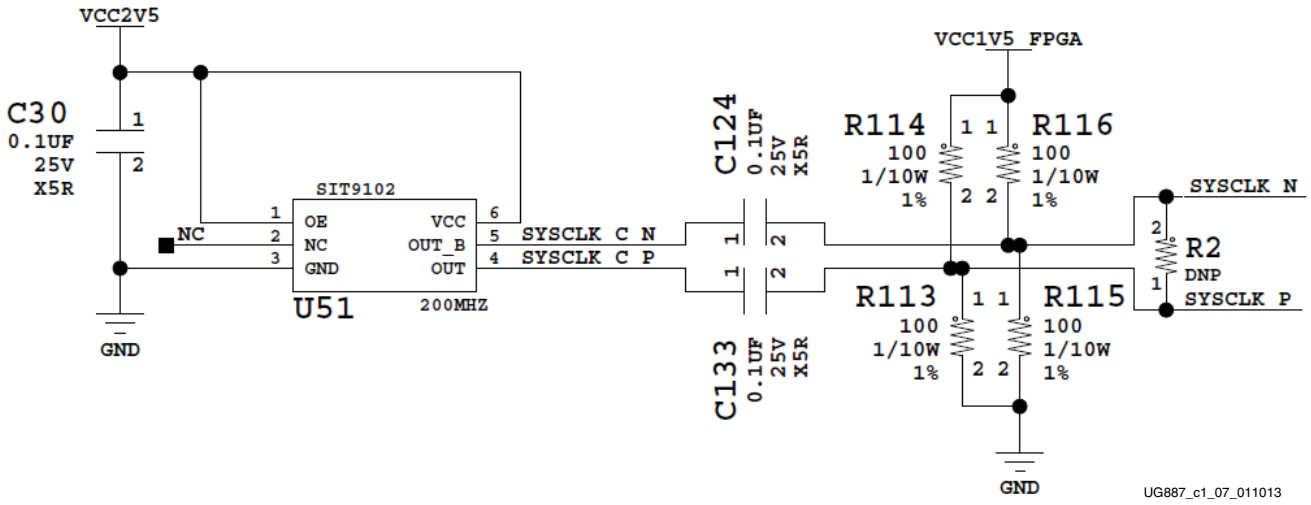


*Figure 1-7:* **System Clock Source**

## Programmable User Clock (USER_CLOCK_P and USER_CLOCK_N)

[Figure 1-2, callout 6]

The VC709 board has a programmable low-jitter 3.3V differential oscillator (U34) connected to the FPGA MRCC inputs of bank 14. This USER_CLOCK_P and USER_CLOCK_N clock signal pair are connected to FPGA U1 pins AK34 and AL34 respectively. On power-up, the user clock defaults to an output frequency of 156.250 MHz. User applications can change the output frequency within the range of 10 MHz to 810 MHz through an $I^2C$ interface. Power cycling the VC709 board reverts the user clock to its default frequency of 156.250 MHz.

- Programmable oscillator: Silicon Labs Si570BAB0000544DG (10 MHz – 810 MHz)
- PPM frequency jitter: 50 ppm
- Differential output
- $I^2C$ address `0x5D`

For more details, see the Silicon Labs Si570 data sheet. The user clock circuit is shown in Figure 1-8.

***Note:*** In Figure 1-8, USER_CLOCK_N and USER_CLOCK_P are differential clock signals.

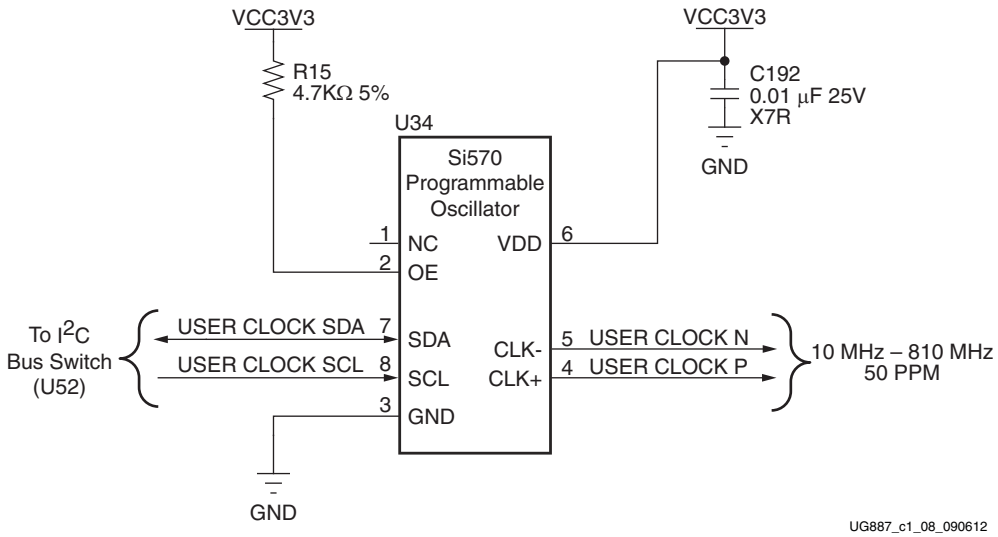


*Figure 1-8:* **User Clock Source**

## User SMA Clock (USER_SMA_CLOCK_P and USER_SMA_CLOCK_N)

[Figure 1-2, callout 7]

An external high-precision clock signal can be provided to the FPGA bank 14 by connecting differential clock signals through the onboard 50Ω SMA connectors J31 (P) and J32 (N). The differential clock signal names are USER_SMA_CLOCK_P and USER_SMA_CLOCK_N, which are connected to FPGA U1 pins AJ32 and AK32 respectively. These clock connections are connected directly to the FPGA U1 pins (no series capacitors and no external parallel termination resistor).The user-provided 1.8V differential clock circuit is shown in Figure 1-9.

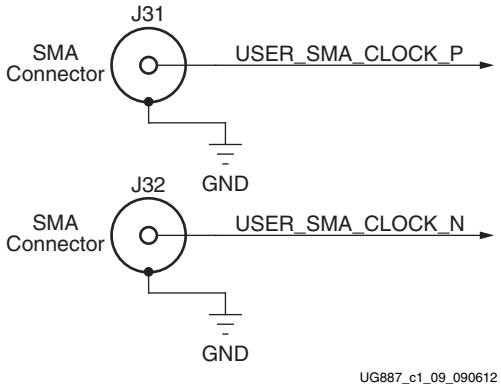


*Figure 1-9:* **User SMA Clock Source**

## GTH SMA Clock (SMA_MGT_REFCLK_P and SMA_MGT_REFCLK_N)

[Figure 1-2, callout 8]

The VC709 board includes a pair of SMA connectors for a GTH clock wired to GTH Quad bank 113. This differential clock has signal names SMA_MGT_REFCLK_P and SMA_REFCLK_N, which are connected to FPGA U1 pins AK8 and AK7 respectively. Figure 1-10 shows this AC-coupled clock circuit.

- External user-provided GTH reference clock on SMA input connectors
- 1.8V differential input

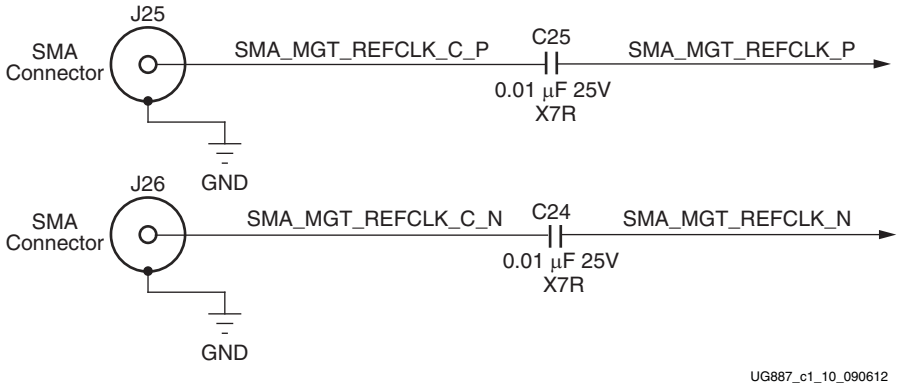


*Figure 1-10:* **GTH SMA Clock Source**

## Jitter-Attenuated Clock

[Figure 1-2, callout 9]

The VC709 board includes a Silicon Labs Si5324 jitter attenuator U24 on the back side of the board. FPGA user logic can implement a clock recovery circuit and then output this clock to a differential I/O pair on I/O bank 13 (REC_CLOCK_C_P, FPGA U1 pin AW32 and REC_CLOCK_C_N, FPGA U1 pin AW33) for jitter attenuation. The jitter-attenuated clock (Si5324_OUT_C_P, Si5324_OUT_C_N) is then routed as a reference clock to GTH Quad 113 inputs MGTREFCLK0P (FPGA U1 pin AH8) and MGTREFCLK0N (FPGA U1 pin AH7). The Si5324 U24 jitter attenuator has two LVCMOS18 connections to the XCVX690T FPGA U1.

The Silicon Labs Si5324 U24 pin 1 reset net SI5324_RST must be driven High to enable the device. U24 pin 3 net SI5324_INT_ALM is level-shifted to 1.8V by U47 and is connected to U1 bank 13 pin AU34. U24 pin 1 net SI5324_RST is level-shifted to 1.8V by U39 and is connected to U1 bank 13 pin AT36. An active-Low input performs an external hardware reset of device. This resets all internal logic to a known state and forces the device registers to their default value. The clock outputs are disabled during reset. The part must be programmed after a reset or power-on to get a clock output. The reset pin 1 has a weak internal pull-up.

The primary purpose of this clock is to support CPRI/OBSAI applications that perform clock recovery from a user-supplied SFP/SFP+ module and use the jitter-attenuated recovered clock to drive the reference clock inputs of a GTH transceiver. The jitter-attenuated clock circuit is shown in Figure 1-11.

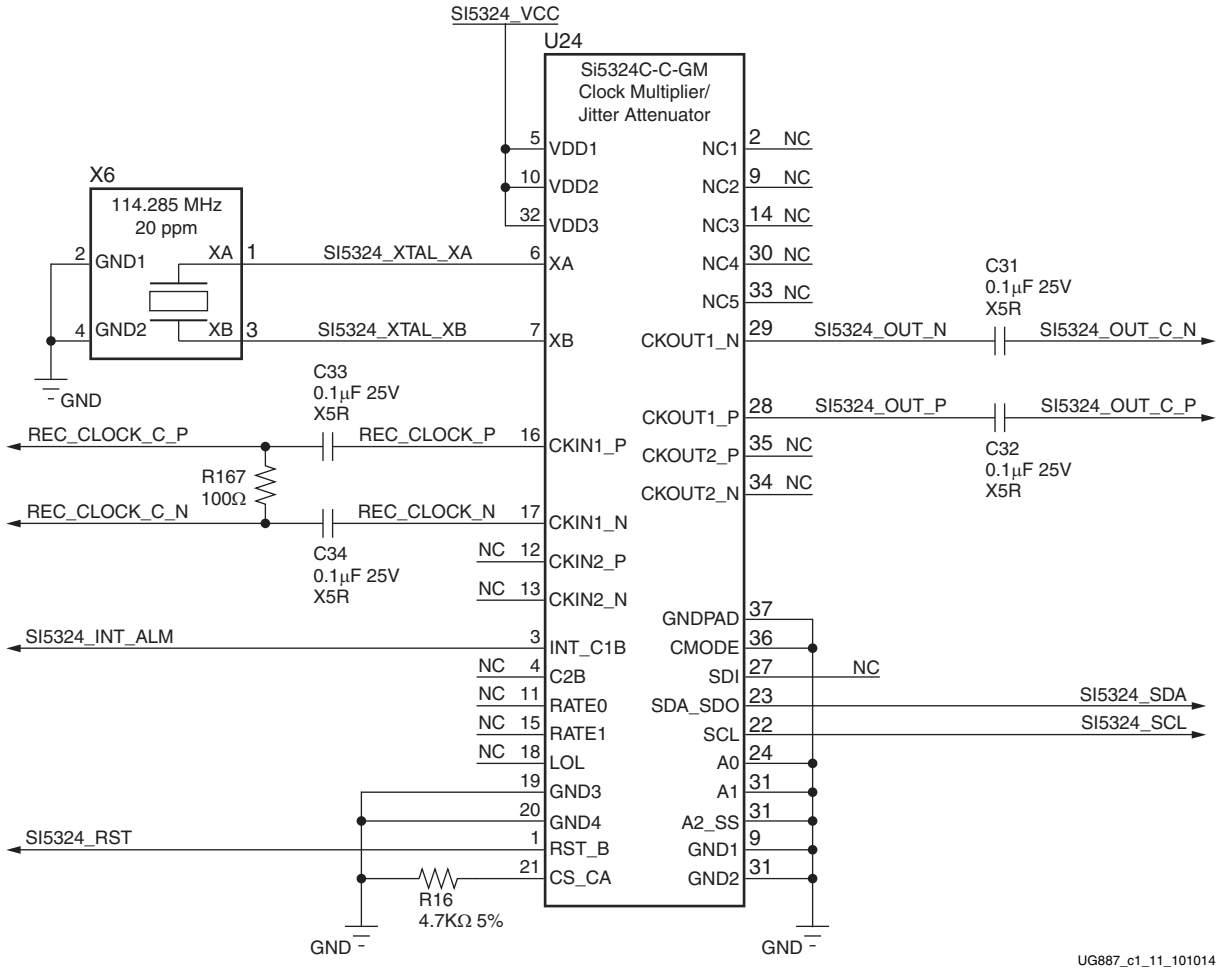


*Figure 1-11:* **Jitter-Attenuated Clock**

1. See the Silicon Labs Si5324 data sheet for more information on this device.

## Memory Clock (SYSCLK_233_P and SYSCLK_233_N)

[Figure 1-2, callout 27]

The VC709 board has a LVDS 233.3333 MHz oscillator (U13) soldered onto the back side of the board and wired to an FPGA MRCC clock input on bank 32. This 233.3333 MHz signal pair is named SYSCLK_233_P and SYSCLK_233_N. The P and N signals are connected to FPGA U1 pins AY18 and AY17 respectively.

- Oscillator: Si Time SIT9122AC-2D3-25E233.333333 (233.3333 MHz)
- PPM frequency jitter: 50 ppm
- Differential output

The LVDS termination resistor R43 is located within the FPGA via matrix on the bottom of the board, and is not populated.

One possible I/O standard for the FPGA design clock input is:

```
NET "sysclk_233_p"  LOC = "AY18" | IOSTANDARD = DIFF_SSTL15_DCI | #Bank
32 MRCC input
NET "sysclk_233_n"  LOC = "AY17" | IOSTANDARD = DIFF_SSTL15_DCI | #Diff.
Rterm R43 DNP
```

2. For more details, see the Si Time SiT9122 data sheet. The system clock circuit is shown in Figure 1-12.

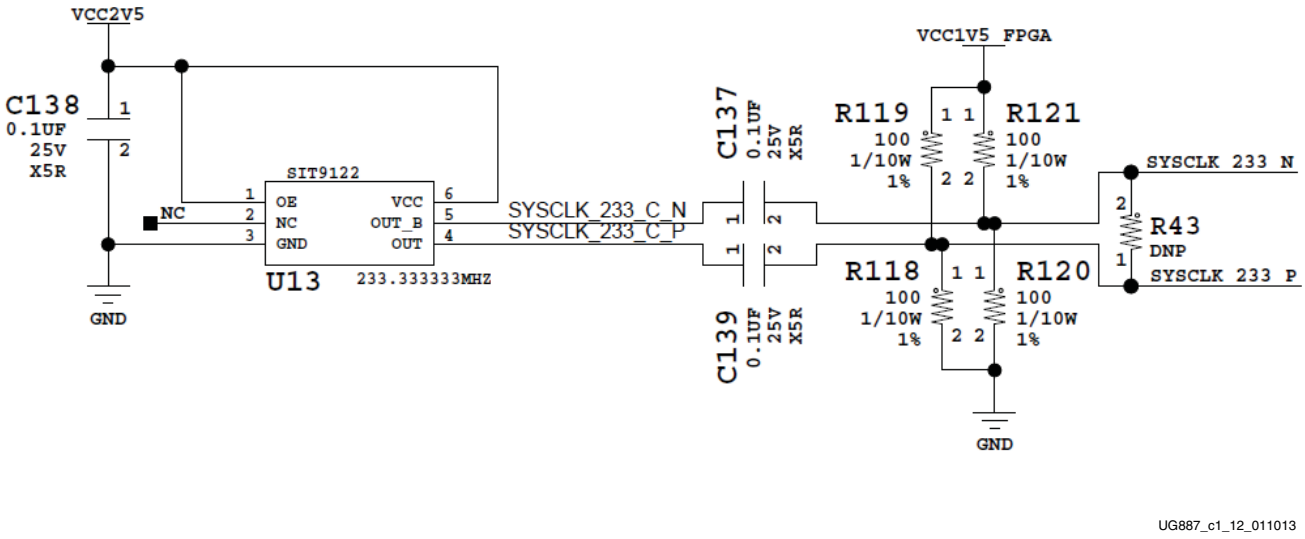


*Figure 1-12:* **Memory Clock Source**

## FPGA EMCC Clock

***Note:*** There is no Figure 1-2 callout for this clock. It is located on the top side of the board near the upper left edge of SODIMM socket J3.

The VC709 board has a LVCMOS 80 MHz oscillator (U40) soldered onto the board and wired to the FPGA EMCCLK clock input pin AP37 on bank 14. This 80 MHz single-ended signal is named FPGA_EMCCLK.

- Oscillator: Si Time SIT8103AC-23-18E-80.0000Y
- PPM frequency jitter: 50 ppm
- Single-ended 1.8V LVCMOS output

The FPGA EMCC external configuration clock circuit is shown in Figure 1-13.

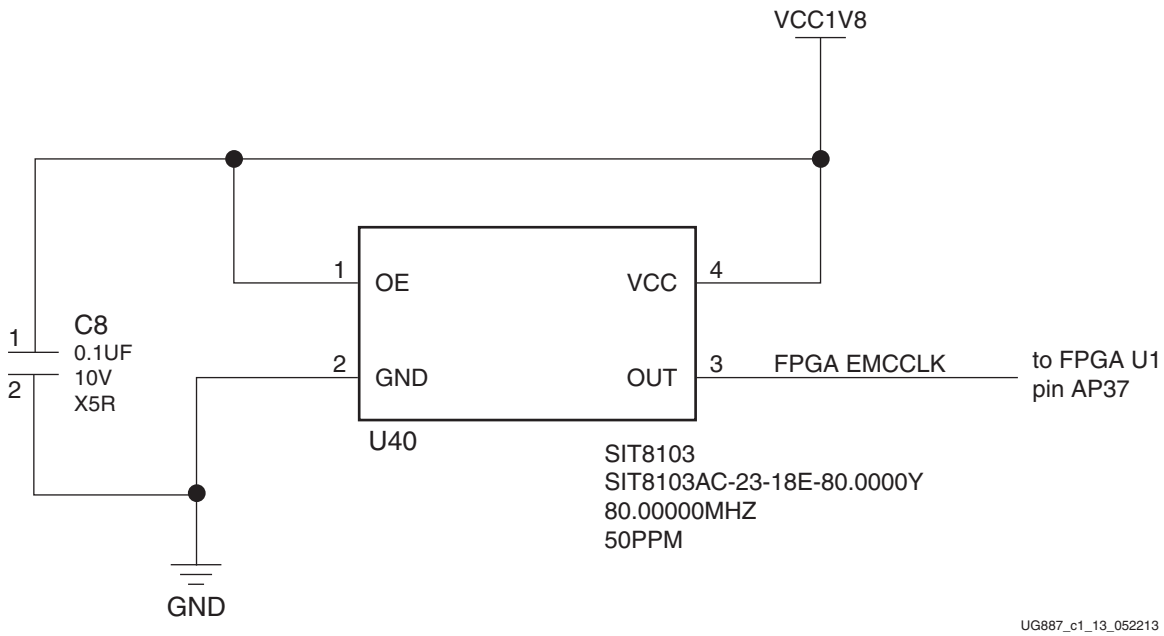


*Figure 1-13:* **FPGA External EMCC Clock**

## GTH Transceivers

[Figure 1-2, callout 10]

The VC709 board provides access to 22 GTH transceivers:

- Eight of the GTH transceivers are wired to the PCI Express x8 endpoint edge connector (P1) fingers.
- Ten of the GTH transceivers are wired to the FMC HPC connector (J35).
- Four of the GTH transceivers are wired to the four SFP/SFP+ connectors (P2, P3, P4, P5).

The GTH transceivers in 7 series FPGAs are grouped into four channels described as Quads. The reference clock for a Quad can be sourced from the Quad above or Quad below the GTH Quad of interest. There are six GTH Quads on the VC709 board with connectivity as shown here:

- Quad 113:
  - MGTREFCLK0 - Si5324 jitter attenuator
  - MGTREFCLK1 - SMA clock
  - Contains 4 GTH transceivers with one each allocated to SFP 1 through 4
- Quad 114:
  - MGTREFCLK0 - No clock
  - MGTREFCLK1 - No clock
  - Contains 4 GTH transceivers for PCIe lanes 4–7
- Quad 115:
  - MGTREFCLK0 - No clock
  - MGTREFCLK1 - PCIe edge connector clock

    - Contains 4 GTH transceivers for PCIe lanes 0–3
- Quad 117:
    - MGTREFCLK0 - No clock
    - MGTREFCLK1 - No clock
    - Contains 2 GTH transceivers for FMC1 HPC (DP8–DP9)
- Quad 118:
    - MGTREFCLK0 - FMC1 HPC GBTCLK1
    - MGTREFCLK1 - FMC1 HPC GBTCLK0
    - Contains 4 GTH transceivers for FMC1 HPC (DP4–DP7)
- Quad 119:
    - MGTREFCLK0 - No clock
    - MGTREFCLK1 - No clock
    - Contains 4 GTH transceivers for FMC1 HPC (DP0–DP3)

Table 1-19 lists the GTH quad channel and clock connection assignments.

*Table 1-9:* **GTH Quad Connection Assignments**

| Transceiver Bank | Channel/Clock | Connections |
|---|---|---|
| MGT_BANK_113 | GTHE2_CHANNEL_X1Y15 | SFP/SFP+ 4 |
| | GTHE2_CHANNEL_X1Y14 | SFP/SFP+ 3 |
| | GTHE2_CHANNEL_X1Y13 | SFP/SFP+ 2 |
| | GTHE2_CHANNEL_X1Y12 | SFP/SFP+ 1 |
| | MGTREFCLK0 | Si5324 jitter attenuator |
| | MGTREFCLK1 | SMA_MGT_REFCLK |
| MGT_BANK_114 | GTHE2_CHANNEL_X1Y19 | PCIe4 |
| | GTHE2_CHANNEL_X1Y18 | PCIe5 |
| | GTHE2_CHANNEL_X1Y17 | PCIe6 |
| | GTHE2_CHANNEL_X1Y16 | PCIe7 |
| | MGTREFCLK0 | NC |
| | MGTREFCLK1 | NC |
| MGT_BANK_115 | GTHE2_CHANNEL_X1Y23 | PCIe0 |
| | GTHE2_CHANNEL_X1Y22 | PCIe1 |
| | GTHE2_CHANNEL_X1Y21 | PCIe2 |
| | GTHE2_CHANNEL_X1Y20 | PCIe3 |
| | MGTREFCLK0 | NC |
| | MGTREFCLK1 | PCIe_CLK |
| MGT_BANK_117 | GTHE2_CHANNEL_X1Y31 | NC |
| | GTHE2_CHANNEL_X1Y30 | NC |

*Table 1-9:* **GTH Quad Connection Assignments *(Cont'd)***

| Transceiver Bank | Channel/Clock | Connections |
|---|---|---|
| | GTHE2_CHANNEL_X1Y29 | FMC1 HPC DP8 |
| | GTHE2_CHANNEL_X1Y28 | FMC1 HPC DP9 |
| | MGTREFCLK0 | NC |
| | MGTREFCLK1 | NC |
| MGT_BANK_118 | GTHE2_CHANNEL_X1Y35 | FMC1 HPC DP7 |
| | GTHE2_CHANNEL_X1Y34 | FMC1 HPC DP6 |
| | GTHE2_CHANNEL_X1Y33 | FMC1 HPC DP5 |
| | GTHE2_CHANNEL_X1Y32 | FMC1 HPC DP4 |
| | MGTREFCLK0 | FMC1 HPC GBT_CLK1 |
| | MGTREFCLK1 | FMC1 HPC GBT_CLK0 |
| MGT_BANK_119 | GTHE2_CHANNEL_X1Y39 | FMC1 HPC DP3 |
| | GTHE2_CHANNEL_X1Y38 | FMC1 HPC DP2 |
| | GTHE2_CHANNEL_X1Y37 | FMC1 HPC DP1 |
| | GTHE2_CHANNEL_X1Y36 | FMC1 HPC DP0 |
| | MGTREFCLK0 | NC |
| | MGTREFCLK1 | NC |

For more information on the GTH transceivers see *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476) [Ref 6].

## PCI Express Endpoint Connectivity

[Figure 1-2, callout 11]

The 8-lane PCI Express edge connector performs data transfers at the rate of 2.5 GT/s for a Gen1 application, 5.0 GT/s for a Gen2 application, and 8.0 GT/s for a Gen3 application. The PCIe transmit and receive signal datapaths have a characteristic impedance of 85Ω ±10%. The PCIe clock is routed as a 100Ω differential pair. The 7 series FPGAs GTH transceivers are used for multi-gigabit per second serial interfaces.

The XC7VX690T-2FFG1761C FPGA (-2 speed grade) included with the VC709 board supports up to Gen3 x8.

The PCIe clock is input from the edge connector. It is AC coupled to the FPGA through the MGTREFCLK1 pins of Quad 115. PCIE_CLK_Q0_P is connected to FPGA U1 pin AB8, and the _N net is connected to pin AB7. The PCI Express clock circuit is shown in Figure 1-14.

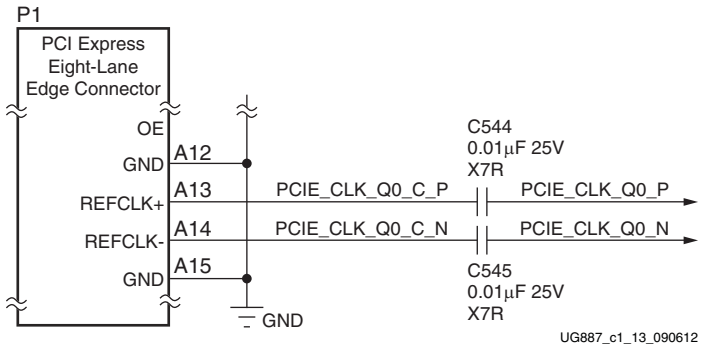


*Figure 1-14:* **PCI Express Clock**

PCIe lane width/size is selected through jumper J49 (Figure 1-15). The default lane size selection is 1-lane (J49 pins 1 and 2 jumpered).

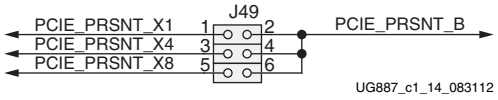


*Figure 1-15:* **PCI Express Lane Size Select Jumper J49**

Table 1-10 lists the PCIe edge connector connections at P1.

*Table 1-10:* **PCIe Edge Connector Connections**

| Net Name | FPGA (U1) Pin | PCIe Edge Connector (P1) | | Function | FFG1761 Placement |
|---|---|---|---|---|---|
| | | Pin | Name | | |
| PCIE_RX0_P | Y4 | B14 | PETp0 | Integrated Endpoint block receive pair | GTHE2_CHANNEL_X1Y23 |
| PCIE_RX0_N | Y3 | B15 | PETn0 | Integrated Endpoint block receive pair | GTHE2_CHANNEL_X1Y23 |
| PCIE_RX1_P | AA6 | B19 | PETp1 | Integrated Endpoint block receive pair | GTHE2_CHANNEL_X1Y22 |
| PCIE_RX1_N | AA5 | B20 | PETn1 | Integrated Endpoint block receive pair | GTHE2_CHANNEL_X1Y22 |
| PCIE_RX2_P | AB4 | B23 | PETp2 | Integrated Endpoint block receive pair | GTHE2_CHANNEL_X1Y21 |
| PCIE_RX2_N | AB3 | B24 | PETn2 | Integrated Endpoint block receive pair | GTHE2_CHANNEL_X1Y21 |
| PCIE_RX3_P | AC6 | B27 | PETp3 | Integrated Endpoint block receive pair | GTHE2_CHANNEL_X1Y20 |
| PCIE_RX3_N | AC5 | B28 | PETn3 | Integrated Endpoint block receive pair | GTHE2_CHANNEL_X1Y20 |
| PCIE_RX4_P | AD4 | B33 | PETp4 | Integrated Endpoint block receive pair | GTHE2_CHANNEL_X1Y19 |
| PCIE_RX4_N | AD3 | B34 | PETn4 | Integrated Endpoint block receive pair | GTHE2_CHANNEL_X1Y19 |
| PCIE_RX5_P | AE6 | B37 | PETp5 | Integrated Endpoint block receive pair | GTHE2_CHANNEL_X1Y18 |
| PCIE_RX5_N | AE5 | B38 | PETn5 | Integrated Endpoint block receive pair | GTHE2_CHANNEL_X1Y18 |
| PCIE_RX6_P | AF4 | B41 | PETp6 | Integrated Endpoint block receive pair | GTHE2_CHANNEL_X1Y17 |
| PCIE_RX6_N | AF3 | B42 | PETn6 | Integrated Endpoint block receive pair | GTHE2_CHANNEL_X1Y17 |
| PCIE_RX7_P | AG6 | B45 | PETp7 | Integrated Endpoint block receive pair | GTHE2_CHANNEL_X1Y16 |
| PCIE_RX7_N | AG5 | B46 | PETn7 | Integrated Endpoint block receive pair | GTHE2_CHANNEL_X1Y16 |
| PCIE_TX0_P | W2 | A16 | PERp0 | Integrated Endpoint block transmit pair | GTHE2_CHANNEL_X1Y23 |
| PCIE_TX0_N | W1 | A17 | PERn0 | Integrated Endpoint block transmit pair | GTHE2_CHANNEL_X1Y23 |

Table 1-10: **PCIe Edge Connector Connections *(Cont'd)***

| Net Name | FPGA (U1) Pin | PCIe Edge Connector (P1) | | Function | FFG1761 Placement |
|---|---|---|---|---|---|
| | | Pin | Name | | |
| PCIE_TX1_P | AA2 | A21 | PERp1 | Integrated Endpoint block transmit pair | GTHE2_CHANNEL_X1Y22 |
| PCIE_TX1_N | AA1 | A22 | PERn1 | Integrated Endpoint block transmit pair | GTHE2_CHANNEL_X1Y22 |
| PCIE_TX2_P | AC2 | A25 | PERp2 | Integrated Endpoint block transmit pair | GTHE2_CHANNEL_X1Y21 |
| PCIE_TX2_N | AC1 | A26 | PERn2 | Integrated Endpoint block transmit pair | GTHE2_CHANNEL_X1Y21 |
| PCIE_TX3_P | AE2 | A29 | PERp3 | Integrated Endpoint block transmit pair | GTHE2_CHANNEL_X1Y20 |
| PCIE_TX3_N | AE1 | A30 | PERn3 | Integrated Endpoint block transmit pair | GTHE2_CHANNEL_X1Y20 |
| PCIE_TX4_P | AG2 | A35 | PERp4 | Integrated Endpoint block transmit pair | GTHE2_CHANNEL_X1Y19 |
| PCIE_TX4_N | AG1 | A36 | PERn4 | Integrated Endpoint block transmit pair | GTHE2_CHANNEL_X1Y19 |
| PCIE_TX5_P | AH4 | A39 | PERp5 | Integrated Endpoint block transmit pair | GTHE2_CHANNEL_X1Y18 |
| PCIE_TX5_N | AH3 | A40 | PERn5 | Integrated Endpoint block transmit pair | GTHE2_CHANNEL_X1Y18 |
| PCIE_TX6_P | AJ2 | A43 | PERp6 | Integrated Endpoint block transmit pair | GTHE2_CHANNEL_X1Y17 |
| PCIE_TX6_N | AJ1 | A44 | PERn6 | Integrated Endpoint block transmit pair | GTHE2_CHANNEL_X1Y17 |
| PCIE_TX7_P | AK4 | A47 | PERp7 | Integrated Endpoint block transmit pair | GTHE2_CHANNEL_X1Y16 |
| PCIE_TX7_N | AK3 | A48 | PERn7 | Integrated Endpoint block transmit pair | GTHE2_CHANNEL_X1Y16 |
| PCIE_CLK_Q0_P | AB8 | A13 | REFCLK+ | Integrated Endpoint block differential clock pair from PCIe | MGT_BANK_115 |
| PCIE_CLK_Q0_N | AB7 | A14 | REFCLK- | Integrated Endpoint block differential clock pair from PCIe | MGT_BANK_115 |
| PCIE_PRSNT_B | J49 2, 4, 6 | A1 | PRSNT#1 | J49 Lane Size Select jumper | NA |
| PCIE_WAKE_B | AV33 | B11 | WAKE# | Integrated Endpoint block wake signal | U1 FPGA Bank13 Pin AV33 |
| PCIE_PERST_B | AV35 | A11 | PERST | Integrated Endpoint block reset signal | U1 FPGA Bank13 Pin AV35 |

Table 1-11 lists the PCIe edge connector connections for Quad 115.

*Table 1-11:* **GTH Quad 115 PCIe Edge Connector Connections**

| Quad 115 Pin Name | FPGA (U1) Pin | Net Name | PCIe Edge Connector (P1) | | FFG1761 Placement |
|---|---|---|---|---|---|
| | | | Pin | Pin Name | |
| MGTXTXP0_115_AE2 | AE2 | PCIE_TX3_P | A29 | PERp3 | GTHE2_CHANNEL_X1Y20 |
| MGTXTXN0_115_AE1 | AE1 | PCIE_TX3_N | A30 | PERn3 | GTHE2_CHANNEL_X1Y20 |
| MGTXRXP0_115_AC6 | AC6 | PCIE_RX3_P | B27 | PETp3 | GTHE2_CHANNEL_X1Y20 |
| MGTXRXN0_115_AC5 | AC5 | PCIE_RX3_N | B28 | PETn3 | GTHE2_CHANNEL_X1Y20 |
| MGTXTXP1_115_AC2 | AC2 | PCIE_TX2_P | A25 | PERp2 | GTHE2_CHANNEL_X1Y21 |
| MGTXTXN1_115_AC1 | AC1 | PCIE_TX2_N | A26 | PERn2 | GTHE2_CHANNEL_X1Y21 |
| MGTXRXP1_115_AB4 | AB4 | PCIE_RX2_P | B23 | PETp2 | GTHE2_CHANNEL_X1Y21 |
| MGTXRXN1_115_AB3 | AB3 | PCIE_RX2_N | B24 | PETn2 | GTHE2_CHANNEL_X1Y21 |
| MGTXTXP2_115_AA2 | AA2 | PCIE_TX1_P | A21 | PERp1 | GTHE2_CHANNEL_X1Y22 |
| MGTXTXN2_115_AA1 | AA1 | PCIE_TX1_N | A22 | PERn1 | GTHE2_CHANNEL_X1Y22 |
| MGTXRXP2_115_AA6 | AA6 | PCIE_RX1_P | B19 | PETp1 | GTHE2_CHANNEL_X1Y22 |
| MGTXRXN2_115_AA5 | AA5 | PCIE_RX1_N | B20 | PETn1 | GTHE2_CHANNEL_X1Y22 |
| MGTXTXP3_115_W2 | W2 | PCIE_TX0_P | A16 | PERp0 | GTHE2_CHANNEL_X1Y23 |
| MGTXTXN3_115_W1 | W1 | PCIE_TX0_N | A17 | PERn0 | GTHE2_CHANNEL_X1Y23 |
| MGTXRXP3_115_Y4 | Y4 | PCIE_RX0_P | B14 | PETp0 | GTHE2_CHANNEL_X1Y23 |
| MGTXRXN3_115_Y3 | Y3 | PCIE_RX0_N | B15 | PETn0 | GTHE2_CHANNEL_X1Y23 |
| MGTREFCLK0P_115_Y8 | Y8 | NC | | | MGT_BANK_115 |
| MGTREFCLK0N_115_Y7 | Y7 | NC | | | MGT_BANK_115 |
| MGTREFCLK1P_115_AB8 | AB8 | PCIE_CLK_Q0_N | A13 | REFCLK- | MGT_BANK_115 |
| MGTREFCLK1N_115_AB7 | AB7 | PCIE_CLK_Q0_P | A14 | REFCLK+ | MGT_BANK_115 |

Table 1-12 lists the PCIe edge connector connections for Quad 114.

*Table 1-12:* **GTH Quad 114 PCIe Edge Connector Connections**

| Quad 114 Pin Name | FPGA (U1) Pin | Net Name | PCIe Edge Connector (P1) | | FFG1761 Placement |
|---|---|---|---|---|---|
| | | | Pin | Pin Name | |
| MGTXTXP0_114_AK4 | AK4 | PCIE_TX7_P | A47 | PERp7 | GTHE2_CHANNEL_X1Y16 |
| MGTXTXN0_114_AK3 | AK3 | PCIE_TX7_N | A48 | PERn7 | GTHE2_CHANNEL_X1Y16 |
| MGTXRXP0_114_AG6 | AG6 | PCIE_RX7_P | B45 | PETp7 | GTHE2_CHANNEL_X1Y16 |
| MGTXRXN0_114_AG5 | AG5 | PCIE_RX7_N | B46 | PETn7 | GTHE2_CHANNEL_X1Y16 |
| MGTXTXP1_114_AJ2 | AJ2 | PCIE_TX6_P | A43 | PERp6 | GTHE2_CHANNEL_X1Y17 |
| MGTXTXN1_114_AJ1 | AJ1 | PCIE_TX6_N | A44 | PERn6 | GTHE2_CHANNEL_X1Y17 |
| MGTXRXP1_114_AF4 | AF4 | PCIE_RX6_P | B41 | PETp6 | GTHE2_CHANNEL_X1Y17 |
| MGTXRXN1_114_AF3 | AF3 | PCIE_RX6_N | B42 | PETn6 | GTHE2_CHANNEL_X1Y17 |
| MGTXTXP2_114_AH4 | AH4 | PCIE_TX5_P | A39 | PERp5 | GTHE2_CHANNEL_X1Y18 |
| MGTXTXN2_114_AH3 | AH3 | PCIE_TX5_N | A40 | PERn5 | GTHE2_CHANNEL_X1Y18 |
| MGTXRXP2_114_AE6 | AE6 | PCIE_RX5_P | B37 | PETp5 | GTHE2_CHANNEL_X1Y18 |
| MGTXRXN2_114_AE5 | AE5 | PCIE_RX5_N | B38 | PETn5 | GTHE2_CHANNEL_X1Y18 |
| MGTXTXP3_114_AG2 | AG2 | PCIE_TX4_P | A35 | PERp4 | GTHE2_CHANNEL_X1Y19 |
| MGTXTXN3_114_AG1 | AG1 | PCIE_TX4_N | A36 | PERn4 | GTHE2_CHANNEL_X1Y19 |
| MGTXRXP3_114_AD4 | AD4 | PCIE_RX4_P | B33 | PETp4 | GTHE2_CHANNEL_X1Y19 |
| MGTXRXN3_114_AD3 | AD3 | PCIE_RX4_N | B34 | PETn4 | GTHE2_CHANNEL_X1Y19 |
| MGTREFCLK0P_114_AD8 | AD8 | NC | | | MGT_BANK_114 |
| MGTREFCLK0N_114_AD7 | AD7 | NC | | | MGT_BANK_114 |
| MGTREFCLK1P_114_AF8 | AF8 | NC | | | MGT_BANK_114 |
| MGTREFCLK1N_114_AF7 | AF7 | NC | | | MGT_BANK_114 |

The PCIe edge connector P1 has two LVCMOS18 signals connected to the XCVX690T FPGA U1. The nets PCIE_PERST (P1.A11) and PCIE_WAKE_B (P1.B11) are level-shifted to 1.8V at U38, and are connected to the XCVX690T FPGA U1 bank 13 pins AV35 and AV33, respectively.

For more information refer to *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476) [Ref 6] and *7 Series FPGAs Integrated Block for PCI Express User Guide (*PG054) [Ref 7].

## SFP/SFP+ Module Connectors

[Figure 1-2, callout 12]

The VC709 board supports four small form-factor pluggable (SFP+) connector and cage assemblies P2–P5 that accept SFP or SFP+ modules. Figure 1-16 shows an example of the SFP+ module connector circuitry replicated for each module.

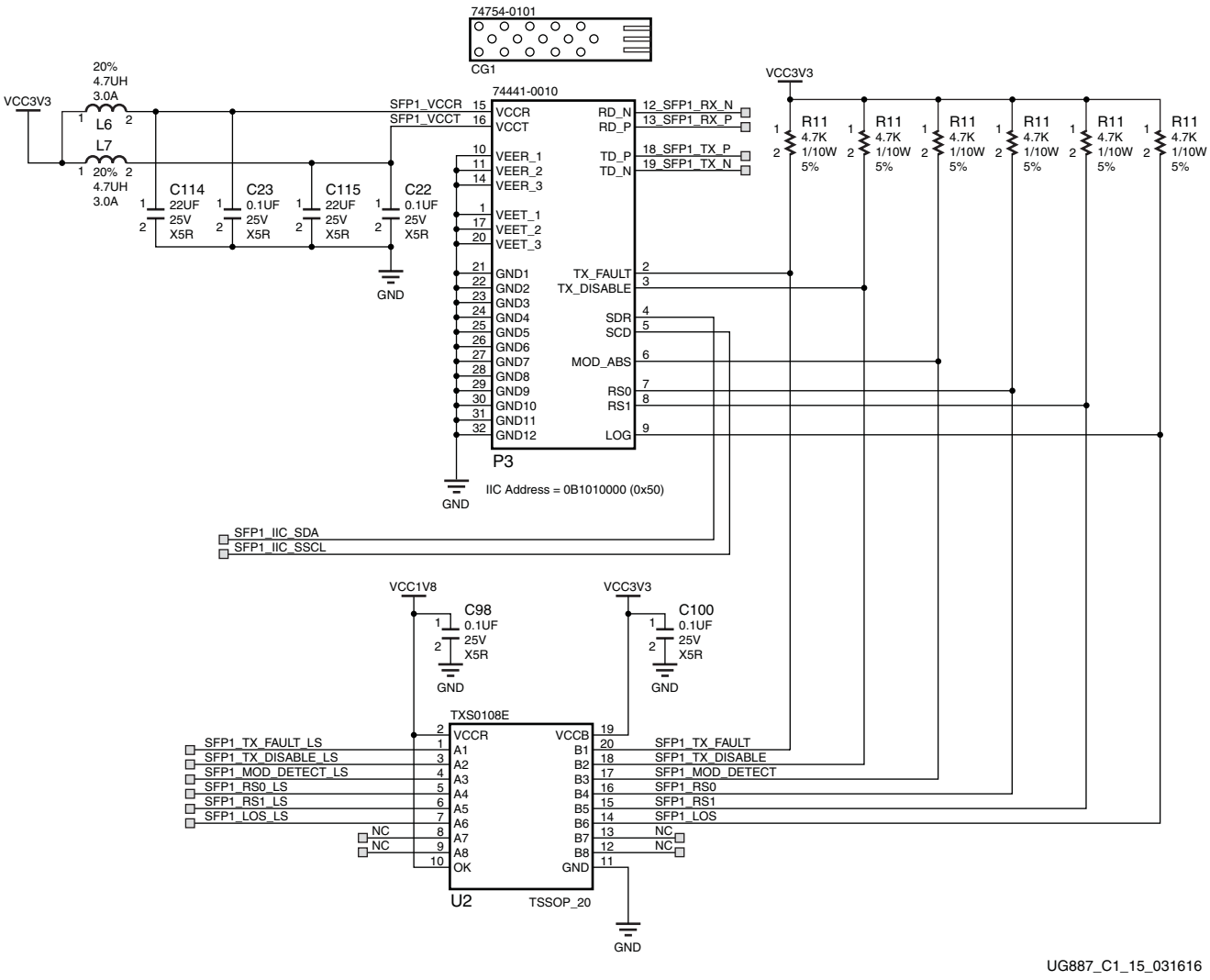


*Figure 1-16:* **SFP+ Module Connector Circuit (Typical at Four Locations)**

Table 1-13 lists the SFP+ module RX and TX connections to the FPGA.

*Table 1-13:* **FPGA U1 to SFP+ Module Connections**

| XCVX690T (U1) Pin | Net Name | SFP+ Module | |
|---|---|---|---|
| | | Pin Number | Pin Name |
| **SFP+ Module 1 (P3)** | | | |
| AP4 | SFP1_TX_P | 18 | TX_P |
| AP3 | SFP1_TX_N | 19 | TX_N |
| AN6 | SFP1_RX_P | 13 | RD_P |
| AN5 | SFP1_RX_N | 12 | RD_N |
| **SFP+ Module 2 (P2)** | | | |
| AN2 | SFP2_TX_P | 18 | TX_P |
| AN1 | SFP2_TX_N | 19 | TX_N |
| AM8 | SFP2_RX_P | 13 | RD_P |
| AM7 | SFP2_RX_N | 12 | RD_N |
| **SFP+ Module 3 (P4)** | | | |
| AM4 | SFP3_TX_P | 18 | TX_P |
| AM3 | SFP3_TX_N | 19 | TX_N |
| AL6 | SFP3_RX_P | 13 | RD_P |
| AL5 | SFP3_RX_N | 12 | RD_N |
| **SFP+ Module 4 (P5)** | | | |
| AL2 | SFP4_TX_P | 18 | TX_P |
| AL1 | SFP4_TX_N | 19 | TX_N |
| AJ6 | SFP4_RX_P | 13 | RD_P |
| AJ5 | SFP4_RX_N | 12 | RD_N |

Table 1-14 lists the SFP+ module control and status connections to the FPGA.

*Table 1-14:* **SFP+ Module Control and Status**

| XCVX690T (U1) Pin | Net Name | I/O Standard | SFP+ Module | |
|---|---|---|---|---|
| | | | Pin Number | Pin Name |
| **SFP+ Module 1 (P3)** | | | | |
| Y38 | SFP1_TX_FAULT | LVCMOS18 | 2 | TX_FAULT |
| AB42 | SFP1_MOD_DETECT | LVCMOS18 | 6 | MOD_ABS |
| W40 | SFP1_RS0 | LVCMOS18 | 7 | RS0 |
| Y40 | SFP1_RS1 | LVCMOS18 | 9 | RS1 |
| Y39 | SFP1_LOS | LVCMOS18 | 8 | LOS |
| AB41 | SFP1_TX_DISABLE | LVCMOS18 | 3 | TX_DISABLE |
| **SFP+ Module 2 (P2)** | | | | |
| AA39 | SFP2_TX_FAULT | LVCMOS18 | 2 | TX_FAULT |
| AA42 | SFP2_MOD_DETECT | LVCMOS18 | 6 | MOD_ABS |
| AB38 | SFP2_RS0 | LVCMOS18 | 7 | RS0 |
| AB39 | SFP2_RS1 | LVCMOS18 | 9 | RS1 |
| AA40 | SFP2_LOS | LVCMOS18 | 8 | LOS |
| Y42 | SFP2_TX_DISABLE | LVCMOS18 | 3 | TX_DISABLE |
| **SFP+ Module 3 (P4)** | | | | |
| AA41 | SFP3_TX_FAULT | LVCMOS18 | 2 | TX_FAULT |
| AC39 | SFP3_MOD_DETECT | LVCMOS18 | 6 | MOD_ABS |
| AD42 | SFP3_RS0 | LVCMOS18 | 7 | RS0 |
| AE42 | SFP3_RS1 | LVCMOS18 | 9 | RS1 |
| AD38 | SFP3_LOS | LVCMOS18 | 8 | LOS |
| AC38 | SFP3_TX_DISABLE | LVCMOS18 | 3 | TX_DISABLE |
| **SFP+ Module 4 (P5)** | | | | |
| AE38 | SFP4_TX_FAULT | LVCMOS18 | 2 | TX_FAULT |
| AC41 | SFP4_MOD_DETECT | LVCMOS18 | 6 | MOD_ABS |
| AE39 | SFP4_RS0 | LVCMOS18 | 7 | RS0 |
| AE40 | SFP4_RS1 | LVCMOS18 | 9 | RS1 |
| AD40 | SFP4_LOS | LVCMOS18 | 8 | LOS |
| AC40 | SFP4_TX_DISABLE | LVCMOS18 | 3 | TX_DISABLE |

***Note:*** The six control/status signals to/from each SFP+ connector are routed through a level shifter.

## USB-to-UART Bridge

[Figure 1-2, callout 13]

The VC709 board contains a Silicon Labs CP2103GM USB-to-UART bridge device (U44) which allows a connection to a host computer with a USB port. The USB cable is supplied in the VC709 evaluation kit (type-A end to host computer, type mini-B end to VC709 board connector J17). The CP2103GM is powered by the USB 5V provided by the host PC when the USB cable is plugged into the USB port on the VC709 board.

Xilinx UART IP is expected to be implemented in the FPGA fabric. The FPGA supports the USB-to-UART bridge using four signal pins: Transmit (TX), Receive (RX), Request to Send (RTS), and Clear to Send (CTS).

Silicon Labs provides royalty-free Virtual COM Port (VCP) drivers for the host computer. These drivers permit the CP2103GM USB-to-UART bridge to appear as a COM port to communications application software (for example, TeraTerm or HyperTerm) that runs on the host computer. The VCP device drivers must be installed on the host PC prior to establishing communications with the VC709 board.

The USB Connector pin assignments and signal definitions between J17 and U44 are listed in Table 1-15.

*Table 1-15:* **USB Connector J17 Pin Assignments and Signal Definitions**

| USB Connector (J17) | | Net Name | Description | CP2103GM (U44) | |
|---|---|---|---|---|---|
| Pin | Name | | | Pin | Name |
| 1 | VBUS | USB_UART_VBUS | +5V VBUS powered | 7 | REGIN |
| | | | | 8 | VBUS |
| 2 | D_N | USB_D_N | Bidirectional differential serial data (N-side) | 4 | D – |
| 3 | D_P | USB_D_P | Bidirectional differential serial data (P-side) | 3 | D + |
| 4 | GND | USB_UART_GND | Signal ground | 2 | GND1 |
| | | | | 29 | CNR_GND |

Table 1-16 shows the USB connections between the FPGA and the UART.

*Table 1-16:* **FPGA to UART Connections**

| FPGA (U1) | | | | Schematic Net Name | CP2103GM UART (U44) | | |
|---|---|---|---|---|---|---|---|
| Pin | Function | Direction | I/O Standard | | Pin | Function | Direction |
| AR34 | RTS | Output | LVCMOS18 | USB_UART_CTS | 22 | CTS | Input |
| AT32 | CTS | Input | LVCMOS18 | USB_UART_RTS | 23 | RTS | Output |
| AU36 | TX | Output | LVCMOS18 | USB_UART_RX | 24 | RXD | Input |
| AU33 | RX | Input | LVCMOS18 | USB_UART_TX | 25 | TXD | Output |

Refer to the Silicon Labs website for technical information on the CP2103GM and the VCP drivers.

## I2C Bus

[Figure 1-2, callout 14, 15]

The VC709 board implements a single I$^2$C port on the FPGA (IIC_SDA_MAIN, pin AU32; IIC_SDA_SCL, pin AT35), which is routed through a TI Semiconductor PCA9548A 1-to-8 channel I$^2$C bus switch (U52). The bus switch can operate at speeds up to 400 kHz.

The bus switch I$^2$C address is `0x74` (`0b01110100`) and must be addressed and configured to select the desired downstream device.

The four SFP+ connectors SFP1 (P3), SFP2 (P2), SFP3 (P4), and SFP4 (P5) are addressed through a secondary PCA9546A 1-to-4 channel I$^2$C bus switch (U14). The VC709 board I$^2$C bus topology is shown in Figure 1-17.

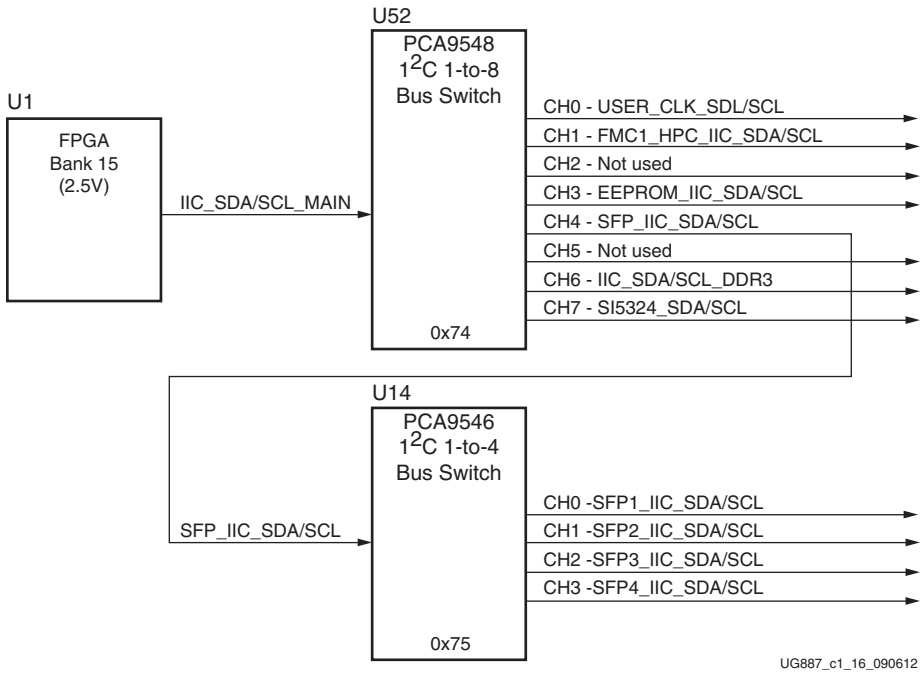


*Figure 1-17:* **I$^2$C Bus Topology**

User applications that communicate with devices on one of the downstream I$^2$C buses must first set up a path to the desired bus through the U52 bus switch at I$^2$C address `0x74` (`0b1110100`). Table 1-17 lists the address for each bus. The secondary (SFP+ access) bus switch U14 is at I$^2$C address `0x75` (`0b1110101`) and the SFP+ modules all have the same address `0x50` (`0b1010000`).

*Table 1-17:* **I$^2$C Bus Addresses**

| I$^2$C Bus | I$^2$C Switch Position | I$^2$C Address |
|---|---|---|
| PCA9548 | NA | `0b1110100` |
| USER_CLK_SDL/SCL | 0 | `0b1011101` |
| FMC1_HPC_IIC_SDA/SCL | 1 | `0bxxxxx00` |
| NOT USED | 2 | `NOT USED` |

*Table 1-17:* **I²C Bus Addresses *(Cont'd)***

| I²C Bus | I²C Switch Position | I²C Address |
|---|---|---|
| EEPROM_IIC_SDA/SCL | 3 | 0b1010100 |
| PCA9546 (SFP1–SFP4) | 4 | 0b1110101 |
| NOT USED | 5 | NOT USED |
| IIC_SDA/SCL_DDR3 J1<br>IIC_SDA/SCL_DDR3 J3 | 6 | 0b1010001, 0b0011001<br>0b1010010, 0b0011010 |
| Si5324_SDA/SCL | 7 | 0b1101000 |

**Notes:**

1. Use the PCA9548 (U52) at I²C address 0x74 (0b01110100) to set up the path to these buses.

The U52 PCA9548 I2C bus MUX has three LVCMOS18 connections to the XCVC190T FPGA U1.

- U52 pin 19 net IIC_SCL_MAIN is level-shifted to 1.8V by Q16 and is connected to U1 bank 13 pin AT35.
- U52 pin 20 net IIC_SDA_MAIN is level-shifted to 1.8V by Q17 and is connected to U1 bank 13 pin AU32.
- U52 pin 24 net IIC_MUX_RESET_B is level-shifted to 1.8V by U70 and is connected to U1 bank 15 pin AY42. Both I2C switches U52 and U14 have a common reset net IIC_MUX_RESET_B. This is an active-Low signal and must be driven High (FPGA U1 pin AY42) to enable I2C bus transactions between the FPGA U1 and the other components on the I2C bus.

Information about the PCA9546A and PCA9548A is available on the Texas Instruments website.

## Status LEDs

[Figure 1-2, callout 24]

Table 1-18 defines the status LEDs. For user-controlled LEDs, see User I/O.

*Table 1-18:* **Status LEDs**

| Reference Designator | Signal Name | Color | Description |
|---|---|---|---|
| DS1 | FPGA_INIT_B | GREEN/RED | GREEN: FPGA initialization successful<br>RED: FPGA initialization in progress or configuration CRC failure |
| DS10 | FPGA_DONE | GREEN | FPGA configured successfully |
| DS14 | PWRCTL1_VCC4A_PG | GREEN | FMC1 HPC power good |
| DS16 | VCC12_P_IN | GREEN | 12V power ON |
| DS17 | PWRCTL_PWRGOOD | GREEN | TI power system power good |
| DS18 | LINEAR_POWER_GOOD | GREEN | DDR3 SODIMMs VTT power good |

## User I/O

[Figure 1-2, callout 16, 18]

The VC709 board provides the following user and general purpose I/O capabilities:

- Eight user LEDs (callout 16)
  - GPIO_LED_[7-0]: DS9, DS8, DS7, DS6, DS5, DS4, DS3, DS2
- Five user pushbuttons and reset switch (callout 17)
  - GPIO_SW_[NESWC]: SW3, SW4, SW5, SW7, SW6
  - CPU_RESET: SW8
- 8-position user DIP switch (callout 18)
  - GPIO_DIP_SW[7-0]: SW2

### User LEDs

Figure 1-18 shows the user LED circuits.

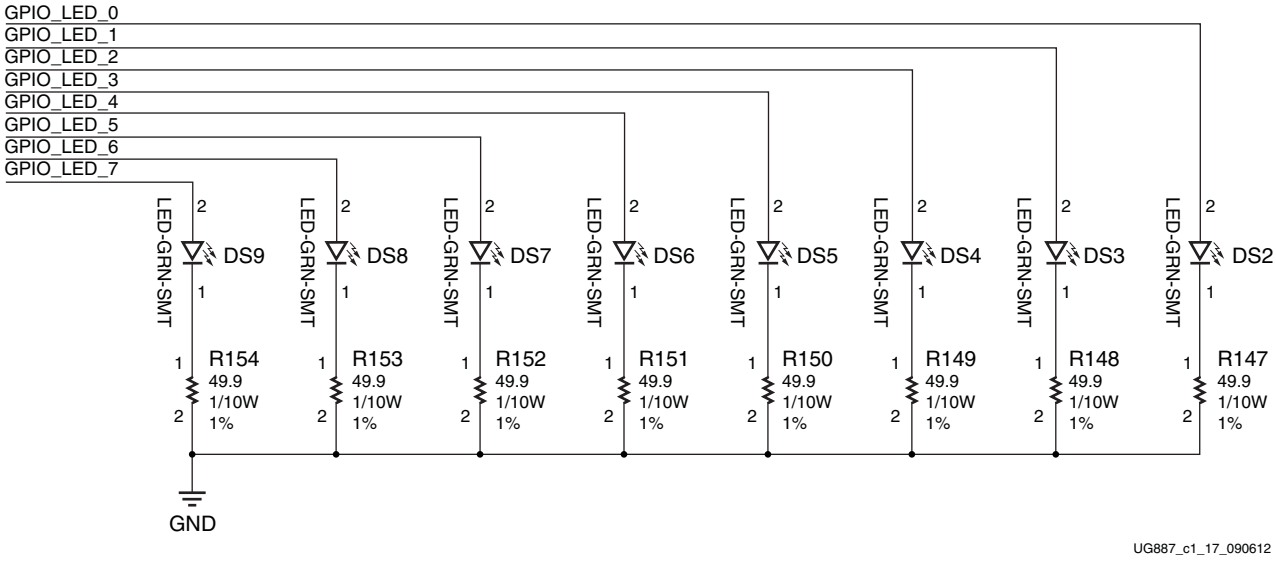


*Figure 1-18:* **User LEDs**

## User Pushbuttons

Figure 1-19 shows the user pushbutton switch circuits.

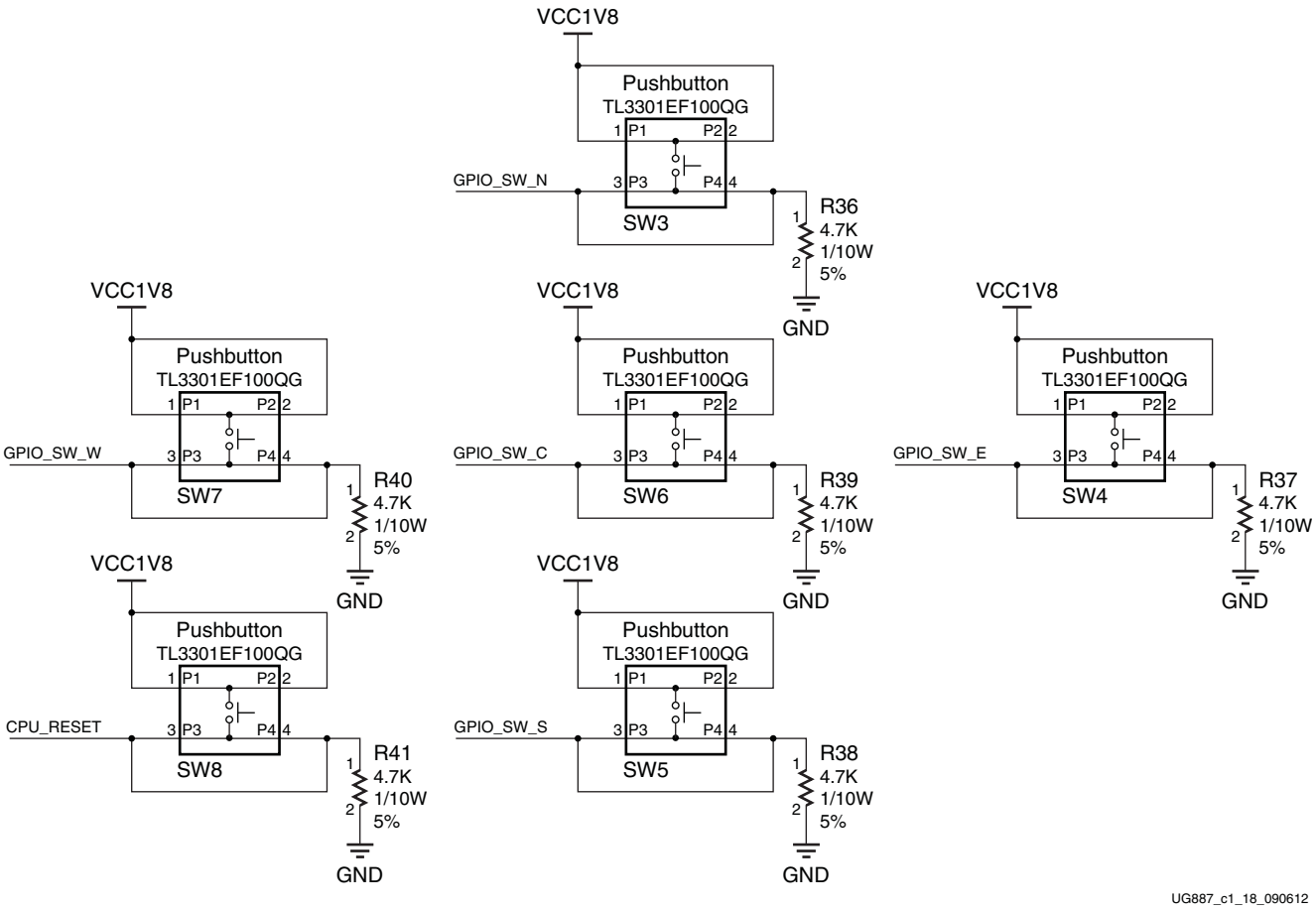


*Figure 1-19:* **User Pushbuttons**

Figure 1-20 shows the GPIO DIP switch circuit.

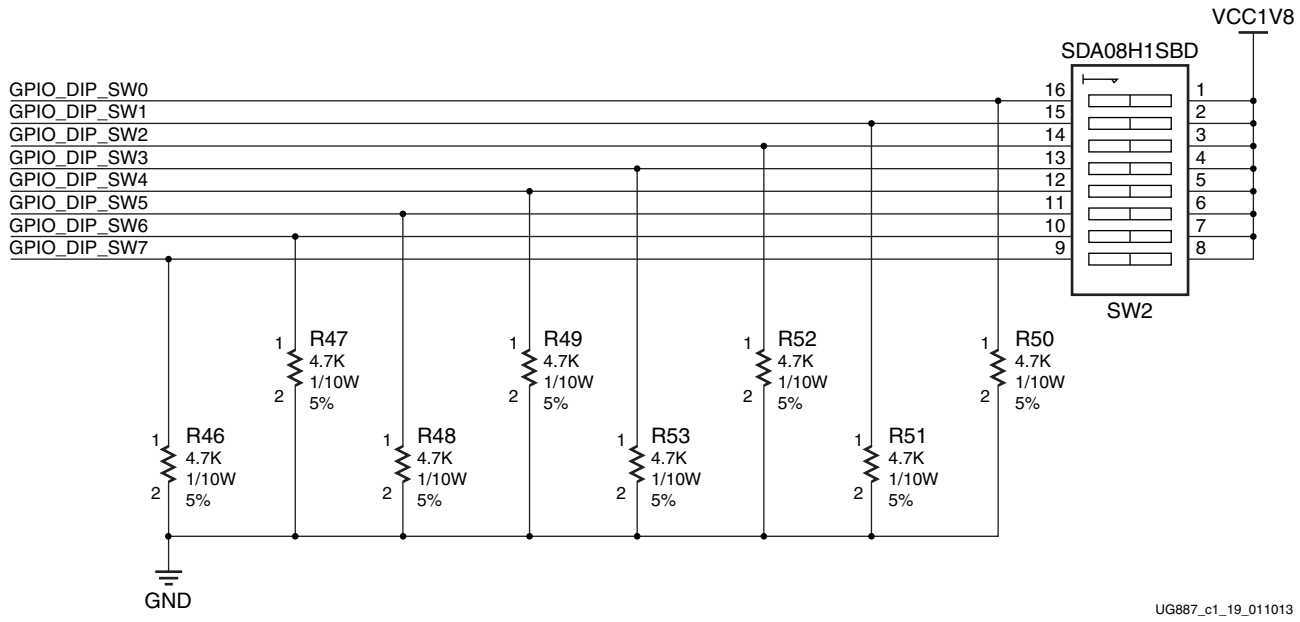


*Figure 1-20:* **GPIO DIP Switch**

Table 1-19 lists the GPIO connections to FPGA U1.

*Table 1-19:* **GPIO Connections to FPGA U1**

| XCVX690T (U1) Pin | Net Name | I/O Standard | GPIO Pin |
|---|---|---|---|
| **Indicator LEDs (Active-High)** | | | |
| AM39 | GPIO_LED_0 | LVCMOS18 | DS2.2 |
| AN39 | GPIO_LED_1 | LVCMOS18 | DS3.2 |
| AR37 | GPIO_LED_2 | LVCMOS18 | DS4.2 |
| AT37 | GPIO_LED_3 | LVCMOS18 | DS5.2 |
| AR35 | GPIO_LED_4 | LVCMOS18 | DS6.2 |
| AP41 | GPIO_LED_5 | LVCMOS18 | DS7.2 |
| AP42 | GPIO_LED_6 | LVCMOS18 | DS8.2 |
| AU39 | GPIO_LED_7 | LVCMOS18 | DS9.2 |
| **Directional Pushbutton Switches** | | | |
| AR40 | GPIO_SW_N | LVCMOS18 | SW3.3 |
| AU38 | GPIO_SW_E | LVCMOS18 | SW4.3 |
| AP40 | GPIO_SW_S | LVCMOS18 | SW5.3 |
| AW40 | GPIO_SW_W | LVCMOS18 | SW7.3 |
| AV39 | GPIO_SW_C | LVCMOS18 | SW6.3 |
| **8-Pole DIP Switch** | | | |

*Table 1-19:* **GPIO Connections to FPGA U1 *(Cont'd)***

| XCVX690T (U1) Pin | Net Name | I/O Standard | GPIO Pin |
|---|---|---|---|
| AV30 | GPIO_DIP_SW0 | LVCMOS18 | SW2.16 |
| AY33 | GPIO_DIP_SW1 | LVCMOS18 | SW2.15 |
| BA31 | GPIO_DIP_SW2 | LVCMOS18 | SW2.14 |
| BA32 | GPIO_DIP_SW3 | LVCMOS18 | SW2.13 |
| AW30 | GPIO_DIP_SW4 | LVCMOS18 | SW2.12 |
| AY30 | GPIO_DIP_SW5 | LVCMOS18 | SW2.11 |
| BA30 | GPIO_DIP_SW6 | LVCMOS18 | SW2.10 |
| BB31 | GPIO_DIP_SW7 | LVCMOS18 | SW2.9 |
| **Reset Pushbutton Switch** | | | |
| AV40 | CPU_RESET | LVCMOS18 | SW8.3 |

## Switches

[Figure 1-2, callout 19, 20, and 21]

The VC709 board includes a power and a configuration switch:

- FPGA_PROG_B, active-Low pushbutton switch SW9 (callout 19)
- Configuration mode DIP switch SW11 (callout 20)
- Power on/off slide switch SW12 (callout 21)

### FPGA_PROG_B Pushbutton SW9 (Active-Low)

[Figure 1-2, callout 19]

Switch SW9 grounds the FPGA PROG_B pin when pressed. This action initiates an FPGA reconfiguration. The FPGA_PROG_B signal is connected to FPGA U1 pin AJ11.

See *7 Series FPGAs Configuration User Guide* (UG470) [Ref 3]for further details on configuring the 7 series FPGAs.

Figure 1-21 shows SW9.

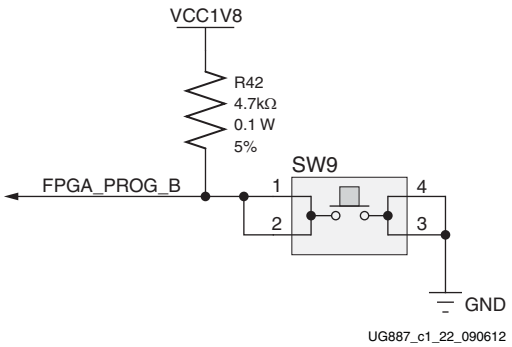


*Figure 1-21:* **FPGA_PROG_B Pushbutton SW9**

## Configuration Mode and Upper Linear Flash Address Switch (SW11)

[Figure 1-2, callout 20]

**FPGA Configuration Mode:** The mode signals FPGA_M2, _M1, and _M0 are connected to FPGA U1 pins AJ10, AK10, and AL10, respectively. Configuration mode is used at power-up or when the PROG pushbutton is pressed.

**Linear BPI Flash Upper Addresses:** DIP switch SW11 positions 1 and 2 control the setting of address bits FLASH_A25 and FLASH_A24.

Figure 1-22 shows the SW11 circuit.

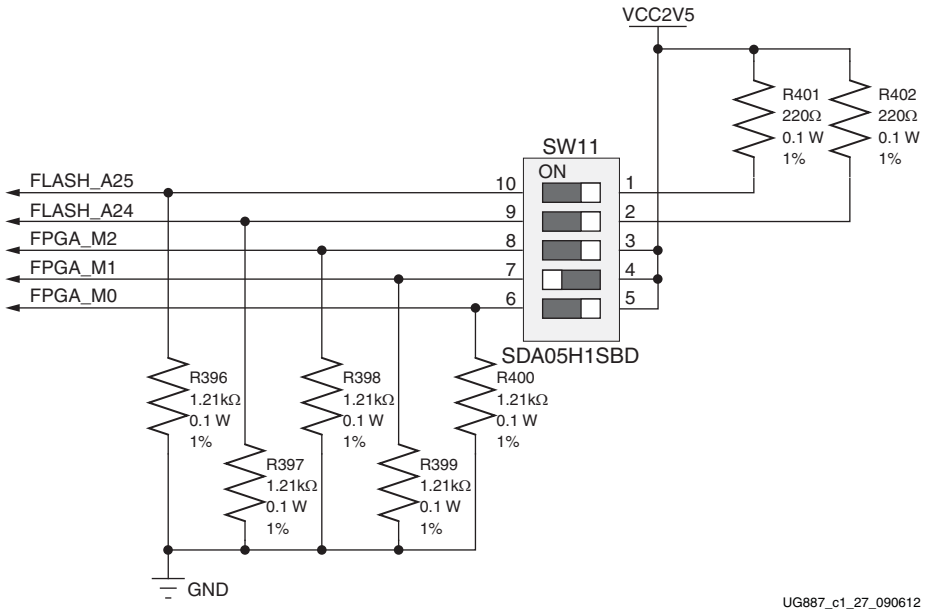


*Figure 1-22:* **Configuration Mode and Upper Linear Flash Address Switch**

## Power On/Off Slide Switch SW12

[Figure 1-2, callout 21]

The VC709 board power switch is SW12. Sliding the switch actuator from the Off to On position applies 12V power from J18, a 6-pin mini-fit connector. Green LED DS16 illuminates when the VC709 board 12V power is on. See Power Management for details on the onboard power system.

> ***Caution!*** Do NOT plug a PC ATX power supply 6-pin connector into J18 on the VC709 board. The ATX 6-pin connector has a different pinout than J18. Connecting an ATX 6-pin connector into J18 damages the VC709 board and voids the board warranty.

The VC709 evaluation kit provides the adapter cable shown in Figure 1-23 for powering the VC709 board from the ATX power supply 4-pin peripheral connector. The Xilinx part number for this cable is 2600304, and is equivalent to Sourcegate Technologies part number AZCBL-WH-1109. For information on ordering this cable, see [Ref 21].

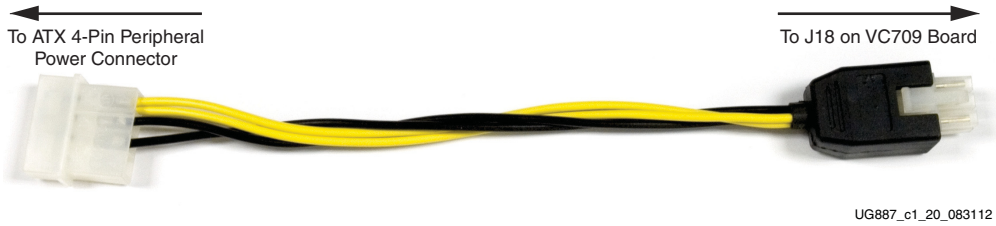


*Figure 1-23:* **ATX Power Supply Adapter Cable**

Figure 1-24 shows the power connector J18, power switch SW12, and indicator LED DS16.

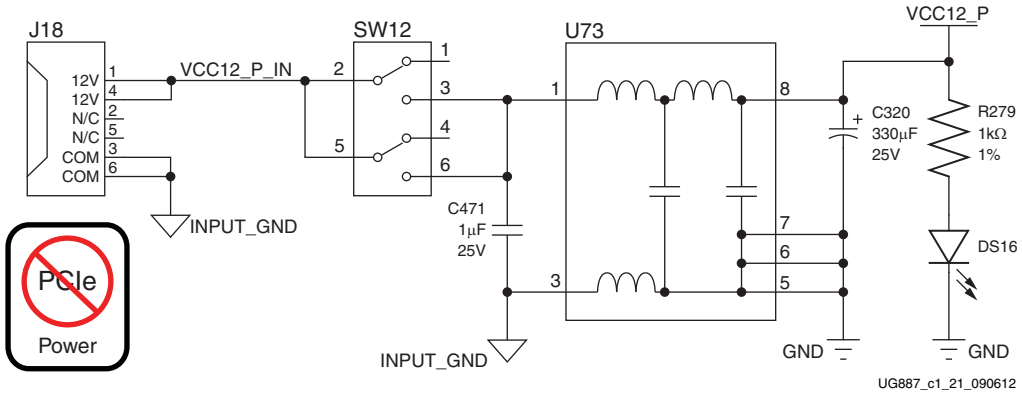


*Figure 1-24:* **Power On/Off Switch SW15**

## VITA 57.1 FMC1 HPC Connector (Partially Populated)

[Figure 1-2, callout 22]

The VC709 board implements one instance of the FMC HPC VITA 57.1 specification connector. This section discusses the FMC1 HPC J35 connector.

***Note:*** The FMC1 HPC J35 connector is a keyed connector oriented so that a plug-on card faces away from the VC709 board.

The VITA 57.1 FMC standard calls a high pin count (HPC), 400 pin 10 x 40 position form factor connector. The 10 x 40 rows of an FMC HPC connector provides pins for up to:

- 160 single-ended or 80 differential user-defined signals
- 10 GTH transceivers
- 2 GTH clocks
- 4 differential clocks
- 159 ground and 15 power connections

The VC709 board FMC1 HPC connector J35 implements a subset of the maximum signal and clock connectivity capabilities:

- 80 differential user-defined pairs:
  - 34 LA pairs (LA00-LA33)
  - 24 HA pairs (HA00-HA23)
  - 22 HB pairs (HB00-HB21)

- 10 GTH transceivers
- 2 GTH clocks
- 2 differential clocks

The FMC1 HPC signals are distributed across GTH Quads 117, 118, and 119.

The VC709 board VADJ voltage for the FMC1 HPC (J35) connector is fixed at 1.8V.

Signaling speed ratings:

- Single-ended: 9 GHz (18 Gb/s)
- Differential
  - Optimal vertical: 9 GHz (18 Gb/s)
  - Optimal horizontal: 16 GHz (32 Gb/s)
  - High Density Vertical: 7 GHz (15 Gb/s)

Mechanical specifications:

- Samtec SEAM/SEAF Series
- 1.27 mm x 1.27 mm (0.050-inch x 0.050-inch) pitch

The Samtec connector system is rated for signaling speeds up to 9 GHz (18 Gb/s) based on a –3 dB insertion loss point within a two-level signaling environment.

Table 1-20 shows the FMC HPC connector J35 connections to FPGA U1.

*Table 1-20:* **VITA 57.1 FMC HPC J35 Connections to FPGA U1**

| J35 FMC1 HPC Pin | Net Name | I/O Standard | XCVX690T (U1) Pin | J35 FMC1 HPC Pin | Net Name | I/O Standard | XCVX690T (U1) Pin |
|---|---|---|---|---|---|---|---|
| A2 | FMC1_HPC_DP1_M2C_P | (1) | C6 | B1 | NC | NA | NA |
| A3 | FMC1_HPC_DP1_M2C_N | (1) | C5 | B4 | FMC1_HPC_DP9_M2C_P | (1) | N6 |
| A6 | FMC1_HPC_DP2_M2C_P | (1) | B8 | B5 | FMC1_HPC_DP9_M2C_N | (1) | N5 |
| A7 | FMC1_HPC_DP2_M2C_N | (1) | B7 | B8 | FMC1_HPC_DP8_M2C_P | (1) | P8 |
| A10 | FMC1_HPC_DP3_M2C_P | (1) | A6 | B9 | FMC1_HPC_DP8_M2C_N | (1) | P7 |
| A11 | FMC1_HPC_DP3_M2C_N | (1) | A5 | B12 | FMC1_HPC_DP7_M2C_P | (1) | E6 |
| A14 | FMC1_HPC_DP4_M2C_P | (1) | H8 | B13 | FMC1_HPC_DP7_M2C_N | (1) | E5 |
| A15 | FMC1_HPC_DP4_M2C_N | (1) | H7 | B16 | FMC1_HPC_DP6_M2C_P | (1) | F8 |
| A18 | FMC1_HPC_DP5_M2C_P | (1) | G6 | B17 | FMC1_HPC_DP6_M2C_N | (1) | F7 |
| A19 | FMC1_HPC_DP5_M2C_N | (1) | G5 | B20 | FMC1_HPC_GBTCLK1_M2C_P | (1) | E10 |
| A22 | FMC1_HPC_DP1_C2M_P | (1) | D4 | B21 | FMC1_HPC_GBTCLK1_M2C_N | (1) | E9 |
| A23 | FMC1_HPC_DP1_C2M_N | (1) | D3 | B24 | FMC1_HPC_DP9_C2M_P | (1) | M4 |
| A26 | FMC1_HPC_DP2_C2M_P | (1) | C2 | B25 | FMC1_HPC_DP9_C2M_N | (1) | M3 |
| A27 | FMC1_HPC_DP2_C2M_N | (1) | C1 | B28 | FMC1_HPC_DP8_C2M_P | (1) | N2 |
| A30 | FMC1_HPC_DP3_C2M_P | (1) | B4 | B29 | FMC1_HPC_DP8_C2M_N | (1) | N1 |
| A31 | FMC1_HPC_DP3_C2M_N | (1) | B3 | B32 | FMC1_HPC_DP7_C2M_P | (1) | F4 |
| A34 | FMC1_HPC_DP4_C2M_P | (1) | J2 | B33 | FMC1_HPC_DP7_C2M_N | (1) | F3 |
| A35 | FMC1_HPC_DP4_C2M_N | (1) | J1 | B36 | FMC1_HPC_DP6_C2M_P | (1) | G2 |

Table 1-20: **VITA 57.1 FMC HPC J35 Connections to FPGA U1 *(Cont'd)***

| J35 FMC1 HPC Pin | Net Name | I/O Standard | XCVX690T (U1) Pin | J35 FMC1 HPC Pin | Net Name | I/O Standard | XCVX690T (U1) Pin |
|---|---|---|---|---|---|---|---|
| A38 | FMC1_HPC_DP5_C2M_P | (1) | H4 | B37 | FMC1_HPC_DP6_C2M_N | (1) | G1 |
| A39 | FMC1_HPC_DP5_C2M_N | (1) | H3 | B40 | NC | | NA |
| | | | | | | | |
| C2 | FMC1_HPC_DP0_C2M_P | (1) | E2 | D1 | PWRCTL1_VCC4B_PG | LVCMOS18 | AL32 |
| C3 | FMC1_HPC_DP0_C2M_N | (1) | E1 | D4 | FMC1_HPC_GBTCLK0_M2C_P | (1) | G10 |
| C6 | FMC1_HPC_DP0_M2C_P | (1) | D8 | D5 | FMC1_HPC_GBTCLK0_M2C_N | (1) | G9 |
| C7 | FMC1_HPC_DP0_M2C_N | (1) | D7 | D8 | FMC1_HPC_LA01_CC_P | LVCMOS18 | J40 |
| C10 | FMC1_HPC_LA06_P | LVCMOS18 | K42 | D9 | FMC1_HPC_LA01_CC_N | LVCMOS18 | J41 |
| C11 | FMC1_HPC_LA06_N | LVCMOS18 | J42 | D11 | FMC1_HPC_LA05_P | LVCMOS18 | M41 |
| C14 | FMC1_HPC_LA10_P | LVCMOS18 | N38 | D12 | FMC1_HPC_LA05_N | LVCMOS18 | L41 |
| C15 | FMC1_HPC_LA10_N | LVCMOS18 | M39 | D14 | FMC1_HPC_LA09_P | LVCMOS18 | R42 |
| C18 | FMC1_HPC_LA14_P | LVCMOS18 | N39 | D15 | FMC1_HPC_LA09_N | LVCMOS18 | P42 |
| C19 | FMC1_HPC_LA14_N | LVCMOS18 | N40 | D17 | FMC1_HPC_LA13_P | LVCMOS18 | H39 |
| C22 | FMC1_HPC_LA18_CC_P | LVCMOS18 | M32 | D18 | FMC1_HPC_LA13_N | LVCMOS18 | G39 |
| C23 | FMC1_HPC_LA18_CC_N | LVCMOS18 | L32 | D20 | FMC1_HPC_LA17_CC_P | LVCMOS18 | L31 |
| C26 | FMC1_HPC_LA27_P | LVCMOS18 | J31 | D21 | FMC1_HPC_LA17_CC_N | LVCMOS18 | K32 |
| C27 | FMC1_HPC_LA27_N | LVCMOS18 | H31 | D23 | FMC1_HPC_LA23_P | LVCMOS18 | P30 |
| C30 | FMC1_HPC_IIC_SCL | NA | U52.4 | D24 | FMC1_HPC_LA23_N | LVCMOS18 | N31 |
| C31 | FMC1_HPC_IIC_SDA | NA | U52.3 | D26 | FMC1_HPC_LA26_P | LVCMOS18 | J30 |
| C34 | GND | NA | NA | D27 | FMC1_HPC_LA26_N | LVCMOS18 | H30 |
| C35 | VCC12_P | NA | NA | D29 | FMC1_HPC_TCK_BUF | NA | U19.14 |
| C37 | VCC12_P | NA | NA | D30 | FMC1_TDI_BUF | NA | U19.18 |
| C39 | VCC3V3 | NA | NA | D31 | FMC1_TDO_FPGA_TDI | NA | T10 |
| | | | | D32 | VCC3V3 | NA | NA |
| | | | | D33 | FMC1_HPC_TMS_BUF | NA | U19.17 |
| | | | | D34 | NC | NA | NA |
| | | | | D35 | GND | NA | NA |
| | | | | D36 | VCC3V3 | NA | NA |
| | | | | D38 | VCC3V3 | NA | NA |
| | | | | D40 | VCC3V3 | NA | NA |
| | | | | | | | |
| E2 | FMC1_HPC_HA01_CC_P | LVCMOS18 | D35 | F1 | FMC1_HPC_PG_M2C | LVCMOS18 | AN34 |
| E3 | FMC1_HPC_HA01_CC_N | LVCMOS18 | D36 | F4 | FMC1_HPC_HA00_CC_P | LVCMOS18 | E34 |
| E6 | FMC1_HPC_HA05_P | LVCMOS18 | G32 | F5 | FMC1_HPC_HA00_CC_N | LVCMOS18 | E35 |
| E7 | FMC1_HPC_HA05_N | LVCMOS18 | F32 | F7 | FMC1_HPC_HA04_P | LVCMOS18 | F34 |

*Table 1-20:* **VITA 57.1 FMC HPC J35 Connections to FPGA U1 *(Cont'd)***

| J35 FMC1 HPC Pin | Net Name | I/O Standard | XCVX690T (U1) Pin | J35 FMC1 HPC Pin | Net Name | I/O Standard | XCVX690T (U1) Pin |
|---|---|---|---|---|---|---|---|
| E9 | FMC1_HPC_HA09_P | LVCMOS18 | E32 | F8 | FMC1_HPC_HA04_N | LVCMOS18 | F35 |
| E10 | FMC1_HPC_HA09_N | LVCMOS18 | D32 | F10 | FMC1_HPC_HA08_P | LVCMOS18 | J36 |
| E12 | FMC1_HPC_HA13_P | LVCMOS18 | B36 | F11 | FMC1_HPC_HA08_N | LVCMOS18 | H36 |
| E13 | FMC1_HPC_HA13_N | LVCMOS18 | A37 | F13 | FMC1_HPC_HA12_P | LVCMOS18 | B37 |
| E15 | FMC1_HPC_HA16_P | LVCMOS18 | B39 | F14 | FMC1_HPC_HA12_N | LVCMOS18 | B38 |
| E16 | FMC1_HPC_HA16_N | LVCMOS18 | A39 | F16 | FMC1_HPC_HA15_P | LVCMOS18 | C33 |
| E18 | FMC1_HPC_HA20_P | LVCMOS18 | B34 | F17 | FMC1_HPC_HA15_N | LVCMOS18 | C34 |
| E19 | FMC1_HPC_HA20_N | LVCMOS18 | A34 | F19 | FMC1_HPC_HA19_P | LVCMOS18 | B32 |
| E21 | FMC1_HPC_HB03_P | LVCMOS18 | G28 | F20 | FMC1_HPC_HA19_N | LVCMOS18 | B33 |
| E22 | FMC1_HPC_HB03_N | LVCMOS18 | G29 | F22 | FMC1_HPC_HB02_P | LVCMOS18 | K28 |
| E24 | FMC1_HPC_HB05_P | LVCMOS18 | K27 | F23 | FMC1_HPC_HB02_N | LVCMOS18 | J28 |
| E25 | FMC1_HPC_HB05_N | LVCMOS18 | J27 | F25 | FMC1_HPC_HB04_P | LVCMOS18 | H24 |
| E27 | FMC1_HPC_HB09_P | LVCMOS18 | H23 | F26 | FMC1_HPC_HB04_N | LVCMOS18 | G24 |
| E28 | FMC1_HPC_HB09_N | LVCMOS18 | G23 | F28 | FMC1_HPC_HB08_P | LVCMOS18 | H25 |
| E30 | FMC1_HPC_HB13_P | LVCMOS18 | P25 | F29 | FMC1_HPC_HB08_N | LVCMOS18 | H26 |
| E31 | FMC1_HPC_HB13_N | LVCMOS18 | P26 | F31 | FMC1_HPC_HB12_P | LVCMOS18 | K24 |
| E33 | FMC1_HPC_HB19_P | LVCMOS18 | L25 | F32 | FMC1_HPC_HB12_N | LVCMOS18 | K25 |
| E34 | FMC1_HPC_HB19_N | LVCMOS18 | L26 | F34 | FMC1_HPC_HB16_P | LVCMOS18 | N25 |
| E36 | FMC1_HPC_HB21_P | LVCMOS18 | P22 | F35 | FMC1_HPC_HB16_N | LVCMOS18 | N26 |
| E37 | FMC1_HPC_HB21_N | LVCMOS18 | P23 | F37 | FMC1_HPC_HB20_P | LVCMOS18 | P21 |
| E39 | VCC1V8 | NA | NA | F38 | FMC1_HPC_HB20_N | LVCMOS18 | N21 |
| | | | | F40 | VCC1V8 | NA | NA |
| | | | | | | | |
| G2 | FMC1_HPC_CLK1_M2C_P | LVCMOS18 | N30 | H1 | NC | NA | NA |
| G3 | FMC1_HPC_CLK1_M2C_N | LVCMOS18 | M31 | H2 | FMC1_HPC_PRSNT_M2C | LVCMOS18 | AM31 |
| G6 | FMC1_HPC_LA00_CC_P | LVCMOS18 | K39 | H4 | FMC1_HPC_CLK0_M2C_P | LVCMOS18 | L39 |
| G7 | FMC1_HPC_LA00_CC_N | LVCMOS18 | K40 | H5 | FMC1_HPC_CLK0_M2C_N | LVCMOS18 | L40 |
| G9 | FMC1_HPC_LA03_P | LVCMOS18 | M42 | H7 | FMC1_HPC_LA02_P | LVCMOS18 | P41 |
| G10 | FMC1_HPC_LA03_N | LVCMOS18 | L42 | H8 | FMC1_HPC_LA02_N | LVCMOS18 | N41 |
| G12 | FMC1_HPC_LA08_P | LVCMOS18 | M37 | H10 | FMC1_HPC_LA04_P | LVCMOS18 | H40 |
| G13 | FMC1_HPC_LA08_N | LVCMOS18 | M38 | H11 | FMC1_HPC_LA04_N | LVCMOS18 | H41 |
| G15 | FMC1_HPC_LA12_P | LVCMOS18 | R40 | H13 | FMC1_HPC_LA07_P | LVCMOS18 | G41 |
| G16 | FMC1_HPC_LA12_N | LVCMOS18 | P40 | H14 | FMC1_HPC_LA07_N | LVCMOS18 | G42 |
| G18 | FMC1_HPC_LA16_P | LVCMOS18 | K37 | H16 | FMC1_HPC_LA11_P | LVCMOS18 | F40 |
| G19 | FMC1_HPC_LA16_N | LVCMOS18 | K38 | H17 | FMC1_HPC_LA11_N | LVCMOS18 | F41 |

Table 1-20: **VITA 57.1 FMC HPC J35 Connections to FPGA U1 *(Cont'd)***

| J35 FMC1 HPC Pin | Net Name | I/O Standard | XCVX690T (U1) Pin | J35 FMC1 HPC Pin | Net Name | I/O Standard | XCVX690T (U1) Pin |
|---|---|---|---|---|---|---|---|
| G21 | FMC1_HPC_LA20_P | LVCMOS18 | Y29 | H19 | FMC1_HPC_LA15_P | LVCMOS18 | M36 |
| G22 | FMC1_HPC_LA20_N | LVCMOS18 | Y30 | H20 | FMC1_HPC_LA15_N | LVCMOS18 | L37 |
| G24 | FMC1_HPC_LA22_P | LVCMOS18 | R28 | H22 | FMC1_HPC_LA19_P | LVCMOS18 | W30 |
| G25 | FMC1_HPC_LA22_N | LVCMOS18 | P28 | H23 | FMC1_HPC_LA19_N | LVCMOS18 | W31 |
| G27 | FMC1_HPC_LA25_P | LVCMOS18 | K29 | H25 | FMC1_HPC_LA21_P | LVCMOS18 | N28 |
| G28 | FMC1_HPC_LA25_N | LVCMOS18 | K30 | H26 | FMC1_HPC_LA21_N | LVCMOS18 | N29 |
| G30 | FMC1_HPC_LA29_P | LVCMOS18 | T29 | H28 | FMC1_HPC_LA24_P | LVCMOS18 | R30 |
| G31 | FMC1_HPC_LA29_N | LVCMOS18 | T30 | H29 | FMC1_HPC_LA24_N | LVCMOS18 | P31 |
| G33 | FMC1_HPC_LA31_P | LVCMOS18 | M28 | H31 | FMC1_HPC_LA28_P | LVCMOS18 | L29 |
| G34 | FMC1_HPC_LA31_N | LVCMOS18 | M29 | H32 | FMC1_HPC_LA28_N | LVCMOS18 | L30 |
| G36 | FMC1_HPC_LA33_P | LVCMOS18 | U31 | H34 | FMC1_HPC_LA30_P | LVCMOS18 | V30 |
| G37 | FMC1_HPC_LA33_N | LVCMOS18 | T31 | H35 | FMC1_HPC_LA30_N | LVCMOS18 | V31 |
| G39 | VCC1V8 | NA | NA | H37 | FMC1_HPC_LA32_P | LVCMOS18 | V29 |
| | | | | H38 | FMC1_HPC_LA32_N | LVCMOS18 | U29 |
| | | | | H40 | VCC1V8 | NA | NA |
| | | | | | | | |
| J2 | NC | NC | NA | K1 | NC | NA | NA |
| J3 | NC | NC | NA | K4 | NC | NA | NA |
| J6 | FMC1_HPC_HA03_P | LVCMOS18 | H33 | K5 | NC | NA | NA |
| J7 | FMC1_HPC_HA03_N | LVCMOS18 | G33 | K7 | FMC1_HPC_HA02_P | LVCMOS18 | E33 |
| J9 | FMC1_HPC_HA07_P | LVCMOS18 | C38 | K8 | FMC1_HPC_HA02_N | LVCMOS18 | D33 |
| J10 | FMC1_HPC_HA07_N | LVCMOS18 | C39 | K10 | FMC1_HPC_HA06_P | LVCMOS18 | G36 |
| J12 | FMC1_HPC_HA11_P | LVCMOS18 | J37 | K11 | FMC1_HPC_HA06_N | LVCMOS18 | G37 |
| J13 | FMC1_HPC_HA11_N | LVCMOS18 | J38 | K13 | FMC1_HPC_HA10_P | LVCMOS18 | H38 |
| J15 | FMC1_HPC_HA14_P | LVCMOS18 | E37 | K14 | FMC1_HPC_HA10_N | LVCMOS18 | G38 |
| J16 | FMC1_HPC_HA14_N | LVCMOS18 | E38 | K16 | FMC1_HPC_HA17_CC_P | LVCMOS18 | C35 |
| J18 | FMC1_HPC_HA18_P | LVCMOS18 | F39 | K17 | FMC1_HPC_HA17_CC_N | LVCMOS18 | C36 |
| J19 | FMC1_HPC_HA18_N | LVCMOS18 | E39 | K19 | FMC1_HPC_HA21_P | LVCMOS18 | D37 |
| J21 | FMC1_HPC_HA22_P | LVCMOS18 | F36 | K20 | FMC1_HPC_HA21_N | LVCMOS18 | D38 |
| J22 | FMC1_HPC_HA22_N | LVCMOS18 | F37 | K22 | FMC1_HPC_HA23_P | LVCMOS18 | A35 |
| J24 | FMC1_HPC_HB01_P | LVCMOS18 | H28 | K23 | FMC1_HPC_HA23_N | LVCMOS18 | A36 |
| J25 | FMC1_HPC_HB01_N | LVCMOS18 | H29 | K25 | FMC1_HPC_HB00_CC_P | LVCMOS18 | J25 |
| J27 | FMC1_HPC_HB07_P | LVCMOS18 | G26 | K26 | FMC1_HPC_HB00_CC_N | LVCMOS18 | J26 |
| J28 | FMC1_HPC_HB07_N | LVCMOS18 | G27 | K28 | FMC1_HPC_HB06_CC_P | LVCMOS18 | K23 |
| J30 | FMC1_HPC_HB11_P | LVCMOS18 | K22 | K29 | FMC1_HPC_HB06_CC_N | LVCMOS18 | J23 |

*Table 1-20:* **VITA 57.1 FMC HPC J35 Connections to FPGA U1 *(Cont'd)***

| J35 FMC1 HPC Pin | Net Name | I/O Standard | XCVX690T (U1) Pin | | J35 FMC1 HPC Pin | Net Name | I/O Standard | XCVX690T (U1) Pin |
|---|---|---|---|---|---|---|---|---|
| J31 | FMC1_HPC_HB11_N | LVCMOS18 | J22 | | K31 | FMC1_HPC_HB10_P | LVCMOS18 | M22 |
| J33 | FMC1_HPC_HB15_P | LVCMOS18 | M21 | | K32 | FMC1_HPC_HB10_N | LVCMOS18 | L22 |
| J34 | FMC1_HPC_HB15_N | LVCMOS18 | L21 | | K34 | FMC1_HPC_HB14_P | LVCMOS18 | J21 |
| J36 | FMC1_HPC_HB18_P | LVCMOS18 | G21 | | K35 | FMC1_HPC_HB14_N | LVCMOS18 | H21 |
| J37 | FMC1_HPC_HB18_N | LVCMOS18 | G22 | | K37 | FMC1_HPC_HB17_CC_P | LVCMOS18 | M24 |
| J39 | FMC1_VIO_B_M2C (1) (3) | | | | K38 | FMC1_HPC_HB17_CC_N | LVCMOS18 | L24 |
| | | | | | K40 | FMC1_VIO_B_M2C | | |

**Notes:**

1. No I/O standards are associated with MGT connections.
2. FMC1_VIO_B_M2C is sourced by a FMC card which supports the HB bus, when plugged onto the HPC connector J35.
3. FMC1_VIO_B_M2C is a variable voltage but it cannot exceed the fixed VADJ 1.8V value.

## Power Management

[Figure 1-2, callout 26]

The VC709 board power distribution diagram is shown in Figure 1-25.

The PCB layout and power system have been designed to meet the recommended criteria described in *7 Series FPGAs PCB Design and Pin Planning Guide* (UG483) [Ref 8].

The J5 keyed PMBus connector has three LVCMOS18 connections to the XCVC190T FPGA U1.

- J5 pin 9 net PMBUS_CLK is level-shifted to 1.8V by Q8 and is connected to U1 bank 15 pin AW37.
- J5 pin 10 net PMBUS_DATA is level-shifted to 1.8V by Q6 and is connected to U1 bank 15 pin AY39.
- J5 pin 8 net PMBUS_ALERT is level-shifted to 1.8V by Q7 and is connected to U1 bank 15 pin AV38.

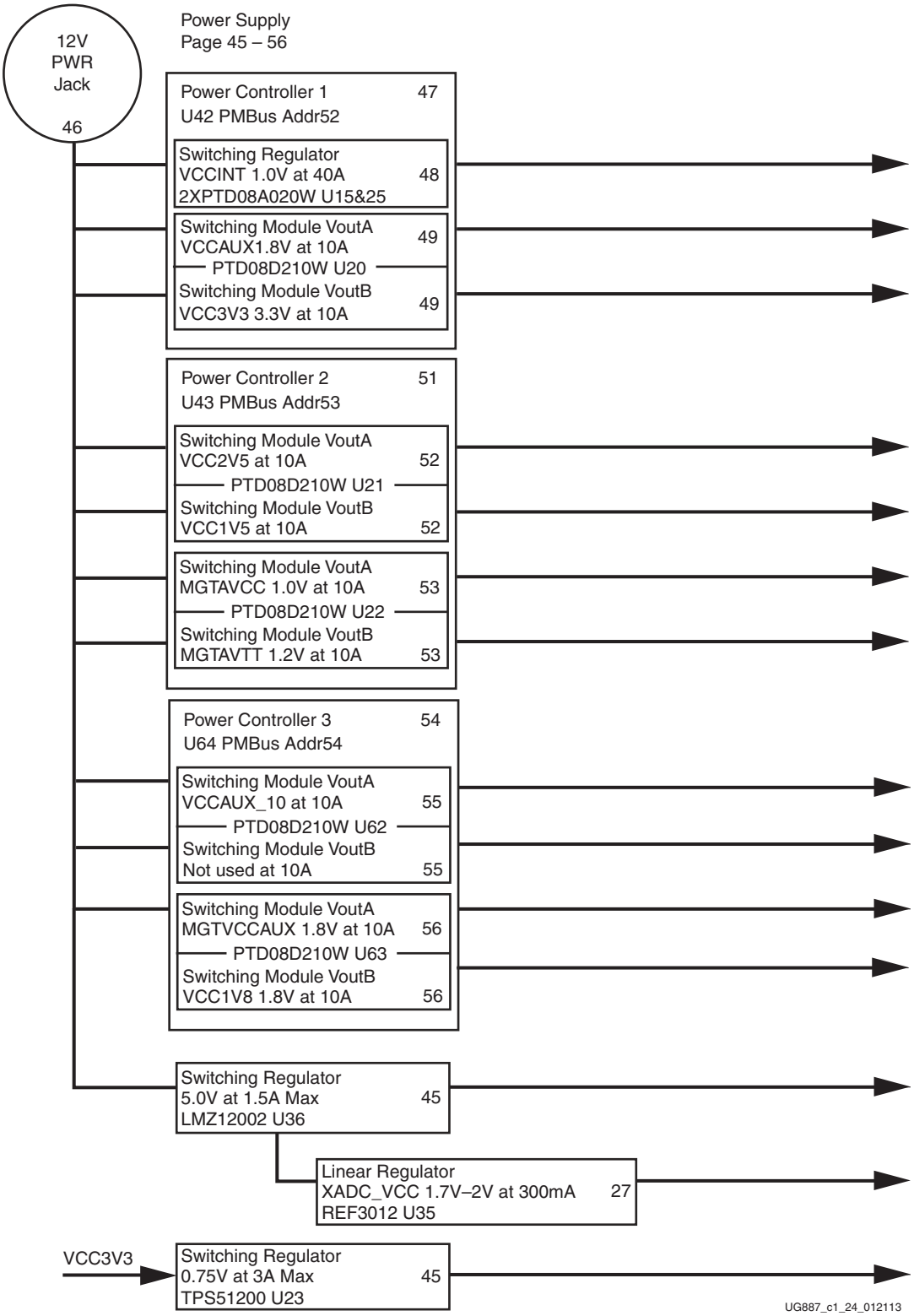


*Figure 1-25:* **Onboard Power Regulators**

The VC709 board uses power regulators and PMBus compliant digital PWM system controllers from Texas Instrument digital power to supply the core and auxiliary voltages listed in Table 1-21. U10 is an ADP123 linear regulator from Analog Devices.

*Table 1-21:* **Onboard Power System Devices**

| Device Type | Reference Designator | Description | Power Rail Net Name | Power Rail Voltage | Schematic Page |
|---|---|---|---|---|---|
| **Core voltage controller and regulators** | | | | | |
| UCD9248PFC(1) | U42 | PMBus Controller (Addr = 52) | | | 47 |
| PTD08A020W | U25/U15 | Dual adjustable switching regulators 40A, 0.6V to 3.6V | VCCINT_FPGA | 1.00V | 48 |
| PTD08D210W ($V_{OUT}$ A) | U20 | ½ of adjustable switching regulator dual 10A, 0.6V to 3.6V | VCCAUX | 1.80V | 49 |
| PTD08D210W ($V_{OUT}$ B) | | ½ of adjustable switching regulator dual 10A, 0.6V to 3.6V | VCC3V3 | 3.30V | 49 |
| **Auxiliary voltage controller and regulators** | | | | | |
| UCD9248PFC(2) | U43 | PMBus Controller (Addr = 53) | | | 51 |
| PTD08D210W ($V_{OUT}$ A) | U21 | ½ of adjustable switching regulator dual 10A, 0.6V to 3.6V | VCC2V5_FPGA | 2.50V | 52 |
| PTD08D210W ($V_{OUT}$ B) | | ½ of adjustable switching regulator dual 10A, 0.6V to 3.6V | VCC1V5_FPGA | 1.50V | 52 |
| PTD08D210W ($V_{OUT}$ A) | U22 | ½ of adjustable switching regulator dual 10A, 0.6V to 3.6V | MGTAVCC | 1.00V | 53 |
| PTD08D210W ($V_{OUT}$ B) | | ½ of adjustable switching regulator dual 10A, 0.6V to 3.6V | MGTAVTT | 1.20V | 53 |
| | | | | | |
| UCD9248PFC(3) | U64 | PMBus Controller (Addr = 54) | | | 54 |
| PTD08D210W ($V_{OUT}$ A) | U62 | ½ of adjustable switching regulator dual 10A, 0.6V to 3.6V | VCCAUX_IO | 2.00V | 55 |
| PTD08D210W ($V_{OUT}$ B) | | ½ of adjustable switching regulator dual 10A, 0.6V to 3.6V | NOT USED | 1.00V | 55 |
| PTD08D210W ($V_{OUT}$ A) | U63 | ½ of adjustable switching regulator dual 10A, 0.6V to 3.6V | MGTVCCAUX | 1.80V | 56 |
| PTD08D210W ($V_{OUT}$ B) | | ½ of adjustable switching regulator dual 10A, 0.6V to 3.6V | VCC1V8_FPGA (4) | 1.80V | 56 |
| **Linear regulators** | | | | | |
| LMZ12002 | U36 | Fixed linear regulator 2A | VCC5V0 | 5.00V | 45 |
| TPS51200DR | U23 | Tracking regulator, 3A | VTTDDR | 0.75V | 45 |
| ADP123 | U10 | Fixed linear regulator, 300 mA | XADC_VCC | 1.80V | 27 |

*Table 1-21:* **Onboard Power System Devices *(Cont'd)***

| Device Type | Reference Designator | Description | Power Rail Net Name | Power Rail Voltage | Schematic Page |
|---|---|---|---|---|---|
| REF3012 | U35 | Fixed linear voltage reference | XADC_VREF | 1.25V | 27 |

**Notes:**

1. See Table 1-22.
2. See Table 1-23.
3. See Table 1-24.
4. The FMC VADJ rail is fixed at 1.8V.

## FMC_VADJ Voltage

The FMC VADJ rail is fixed at 1.8V (U63 $V_{OUT}$B VCC1V8).

### Monitoring Voltage and Current

Voltage and current monitoring and control are available for selected power rails through Texas Instruments' Fusion Digital Power graphical user interface. The three onboard TI power controllers (U42 at address 52, U43 at address 53, and U64 at address 54) are wired to the same PMBus. The PMBus connector, J5, is provided for use with the TI USB Interface Adapter PMBus pod (TI part number EVM USB-TO-GPIO), which can be ordered from the Texas Instruments Xilinx USB website and the associated TI Fusion Digital Power Designer GUI also downloadable from Texas Instruments fusion tools. This is the simplest and most convenient way to monitor the voltage and current values for the power rail listed in Table 1-22, Table 1-23, and Table 1-24.

In each of these the three tables (one per controller), the Power Good (PG) On Threshold is the set-point at or above which the particular rail is deemed "good". The PG Off Threshold is the set-point at or below which the particular rail is no longer deemed "good". The controller internally OR's these PG conditions together and drives an output PG pin high only if all active rail PG states are "good". The On and Off Delay and rise and fall times are relative to when the board power on-off slide switch SW12 is turned on and off.

Table 1-22 defines the voltage and current values for each power rail controlled by the UCD9248 PMBus controller at address 52 (U42).

*Table 1-22:* **Power Rail Specifications for UCD9248 PMBus Controller at Address 52**

| Rail Number | Rail Name | Schematic Rail Name | Nominal $V_{OUT}$ (V) | PG On Threshold (V) | PG Off Threshold (V) | On Delay (ms) | Rise Time (ms) | Off Delay (ms) | Fall Time (ms) | Shutdown Threshold[1] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | $V_{OUT}$ Over Fault (V) | $I_{OUT}$ Over Fault (A) | Temp Over Fault (°C) |
| 1 | Rail #1 | VCCINT_FPGA | 1 | 0.9 | 0.85 | 5 | 4 | 35 | 4 | 1.15 | 35 | 84 |
| 2 | Rail #2 | VCCAUX | 1.8 | 1.62 | 1.53 | 20 | 4 | 20 | 4 | 2.07 | 9.5 | 84 |
| 3 | Rail #3 | VCC3V3 | 3.3 | 2.97 | 2.805 | 35 | 5 | 5 | 5 | 3.795 | 9.5 | 84 |

**Notes:**

1. The values defined in these columns are the voltage, current, and temperature thresholds that cause the regulator to shut down if the value is exceeded.

Table 1-23 defines the voltage and current values for each power rail controlled by the UCD9248 PMBus controller at address 53 (U43).

*Table 1-23:* **Power Rail Specifications for UCD9248 PMBus Controller at Address 53**

| Rail Number | Rail Name | Schematic Rail Name | Nominal $V_{OUT}$ (V) | PG On Threshold (V) | PG Off Threshold (V) | On Delay (ms) | Rise Time (ms) | Off Delay (ms) | Fall Time (ms) | Shutdown Threshold[1] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | $V_{OUT}$ Over Fault (V) | $I_{OUT}$ Over Fault (A) | Temp Over Fault (°C) |
| 1 | Rail #1 | VCC2V5_FPGA | 2.5 | 2.25 | 2.125 | 35 | 5 | 5 | 1 | 2.875 | 9.5 | 84 |
| 2 | Rail #2 | VCC1V5 | 1.5 | 1.35 | 1.275 | 30 | 5 | 10 | 1 | 1.725 | 9.5 | 84 |
| 3 | Rail #3 | MGTAVCC | 1 | 0.9 | 0.85 | 10 | 4 | 35 | 4 | 1.45 | 9.5 | 84 |
| 4 | Rail #4 | MGTAVTT | 1.2 | 1.08 | 1.02 | 15 | 4 | 25 | 4 | 1.38 | 9.5 | 84 |

**Notes:**

1. The values defined in these columns are the voltage, current, and temperature thresholds that cause the regulator to shut down if the value is exceeded.

Table 1-24 defines the voltage and current values for each power rail controlled by the UCD9248 PMBus controller at address 54 (U64).

*Table 1-24:* **Power Rail Specifications for UCD9248 PMBus Controller at Address 54**

| Rail Number | Rail Name | Schematic Rail Name | Nominal $V_{OUT}$ (V) | PG On Threshold (V) | PG Off Threshold (V) | On Delay (ms) | Rise Time (ms) | Off Delay (ms) | Fall Time (ms) | Shutdown Threshold[1] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | $V_{OUT}$ Over Fault (V) | $I_{OUT}$ Over Fault (A) | Temp Over Fault (°C) |
| 1 | Rail #1 | VCCAUX_IO | 2 | 1.8 | 1.7 | 25 | 5 | 15 | 5 | 2.3 | 9.5 | 84 |
| 2 | Rail #2 | NOT USED | 1 | 0.9 | 0.85 | 35 | 4 | 5 | 4 | 1.15 | 9.5 | 84 |
| 3 | Rail #3 | MGTVCCAUX | 1.8 | 1.62 | 1.53 | 15 | 4 | 25 | 4 | 2.07 | 9.5 | 84 |
| 4 | Rail #4 | VCC1V8_FPGA | 1.8 | 1.62 | 1.53 | 30 | 4 | 10 | 4 | 2.07 | 9.5 | 84 |

**Notes:**

1. The values defined in these columns are the voltage, current, and temperature thresholds that cause the regulator to shut down if the value is exceeded.

### FPGA Cooling Fan Operation

The FPGA cooling fan control circuit has its PWM signal wired to a dual-use FPGA bank 15 pin BA37. After configuration, this pin is expected to be toggled by user-provided fan speed control IP to control fan speed. The fan tachometer feedback signal is wired to FPGA bank 15 pin BB37.

FPGA U1 pin BA37 is alternately an unused BPI flash memory address pin (A28). During FPGA configuration in BPI mode, the BPI flash memory address lines are driven. The BA37 pin is held low during BPI configuration and thus the fan PWM signal is not active and the cooling fan is off during the FPGA BPI configuration process.

After configuration is complete, the dual-use FPGA pin BA37 is available for use by user-provided fan speed control IP. If no IP is implemented, this pin should be driven High or placed into high impedance mode so pull-up resistor R198 can pull SM_FAN_PWM high to turn the fan on.

More information about the power system components used by the VC709 board is available from the Texas Instrument digital power website.

Documentation describing PMBus programming for the UCD9248 digital power controller is available at the Texas Instruments fusion tools documentation website.

***Note:*** It has been noted that power modules on the VC709 evaluation board that operate at moderate to high current levels (due to a customer design) might generate substantial heat that can result in unexpected power module shutdowns from over-temperature conditions. This then turns off the FPGA on the development board. Refer to the Virtex-7 VC709 Evaluation Kit Master Answer Record (AR 51901) concerning the solution.

## XADC Analog-to-Digital Converter

The 7 series FPGAs provide an Analog Front End XADC block. The XADC block includes a dual 12-bit, 1 MSPS Analog-to-Digital Convertor (ADC) and on-chip sensors. See *7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* (UG480) [Ref 9] for details on the capabilities of the analog front end. Figure 1-26 shows the XADC block diagram.

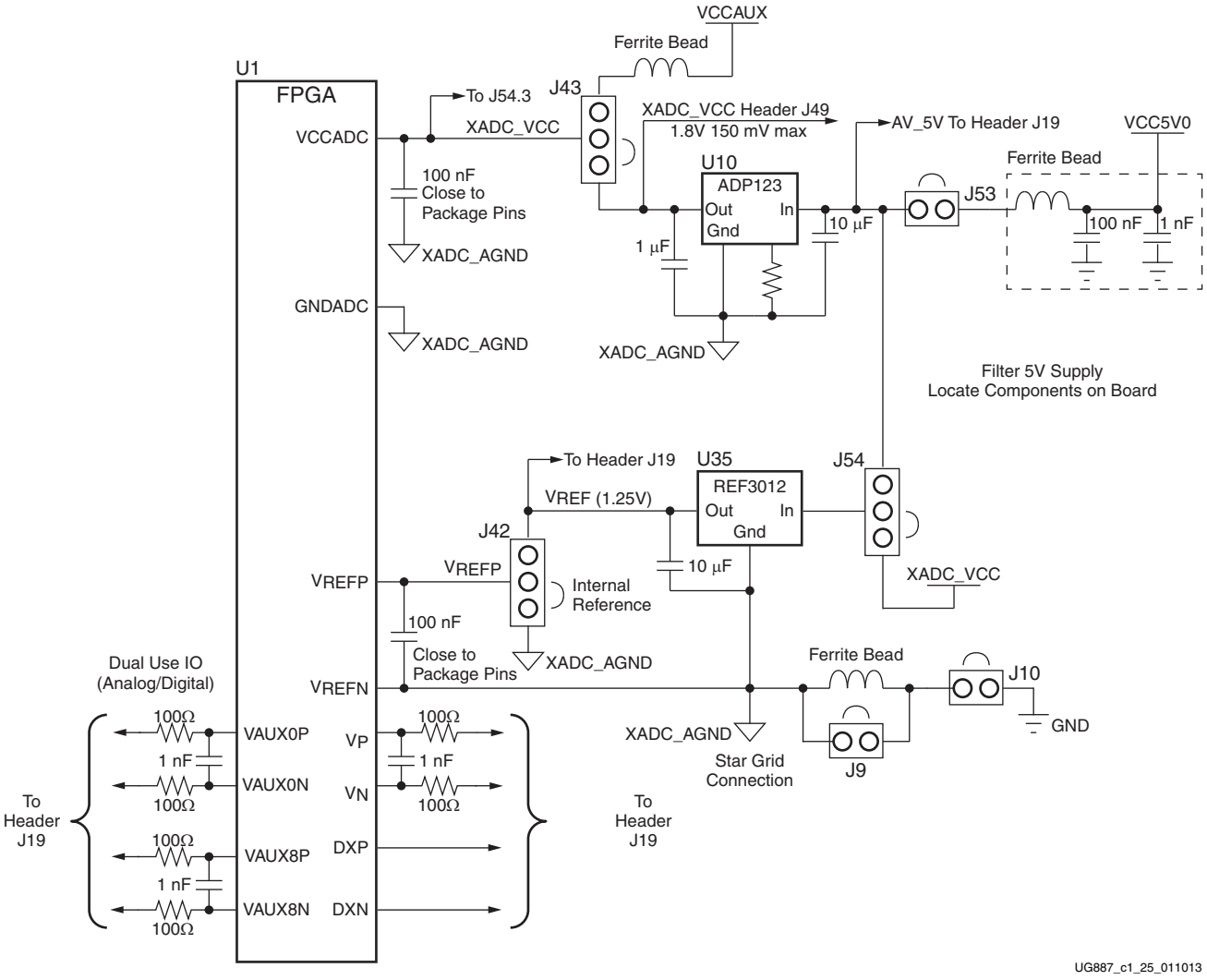


*Figure 1-26:* **XADC Block Diagram**

The VC709 board supports both the internal FPGA sensor measurements and the external measurement capabilities of the XADC. Internal measurements of the die temperature, $V_{CCINT}$, $V_{CCAUX}$, and $V_{CCBRAM}$ are available. The VC709 board $V_{CCINT}$ and $V_{CCBRAM}$ are provided by a common 1.0 V supply.

Jumper J42 can be used to select either an external differential voltage reference (VREF) or on-chip voltage reference for the analog-to-digital converter.

For external measurements an XADC header (J19) is provided. This header can be used to provide analog inputs to the FPGA dedicated VP/VN channel, and to the VAUXP[0]/VAUXN[0], VAUXP[8]/VAUXN[8] auxiliary analog input channels. Simultaneous sampling of Channel 0 and Channel 8 is supported.

A user-provided analog signal multiplexer card can be used to sample additional external analog inputs using the 4 GPIO pins available on the XADC header as multiplexer address lines. Figure 1-27 shows the XADC header connections (Figure 1-2, callout 23).

***Note:*** VADJ is fixed at 1.8V on the VC709 board.

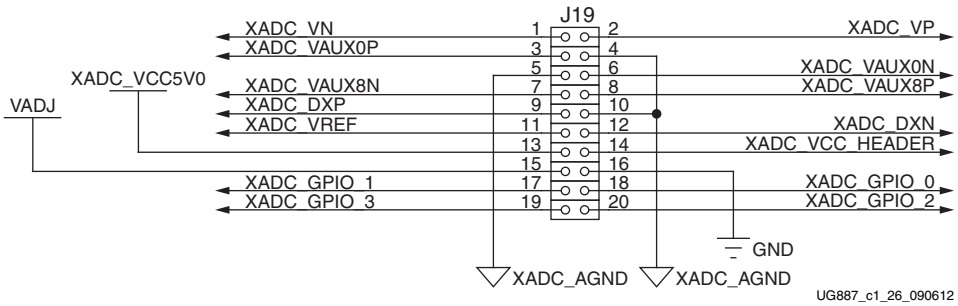


*Figure 1-27:* **XADC header (J19)**

Table 1-25 describes the XADC header J19 pin functions.

*Table 1-25:* **XADC Header J19 Pinout**

| Net Name | J19 Pin Number | Description |
|---|---|---|
| VN, VP | 1, 2 | Dedicated analog input channel for the XADC. |
| XADC_VAUX0P, N | 3, 6 | Auxiliary analog input channel 0. Also supports use as I/O inputs when anti-alias capacitor is not present. |
| XADC_VAUX8N, P | 7, 8 | Auxiliary analog input channel 8. Also supports use as I/O inputs when anti-alias capacitor is not present. |
| DXP, DXN | 9, 12 | Access to thermal diode. |
| XADC_AGND | 4, 5, 10 | Analog ground reference. |
| XADC_VREF | 11 | 1.25V reference from the board. |
| XADC_VCC5V0 | 13 | Filtered 5V supply from board. |
| XADC_VCC_HEADER | 14 | Analog 1.8V supply for XADC. |
| VADJ | 15 | $V_{CCO}$ supply for bank which is the source of DIO pins. |
| GND | 16 | Digital ground (board) reference |
| XADC_GPIO_3, 2, 1, 0 | 19, 20, 17, 18 | Digital I/O. These LVCMOS18 pins are connected to U1 bank 15 pins AN41, AN40, AR39, and AR38, respectively. These I/Os should not be shared with other functions because they are required to support 3-state operation. |

# Configuration Options

The FPGA on the VC709 board can be configured by the following methods:

- Master BPI (uses the linear BPI flash).
- JTAG (Digilent USB-to-JTAG Bridge only). See USB JTAG for more information.

See *7 Series FPGAs Configuration User Guide* (UG470) [Ref 3] for further details on configuration modes.

The method used to configure the FPGA is controlled by the mode pin (M2, M1, M0) settings selected through DIP switch SW11. Table 1-26 lists the supported mode switch settings.

*Table 1-26:* **Mode Switch SW11 Settings**

| Mode Pins (M2, M1, M0) | Configuration Mode |
|---|---|
| 010 | Master BPI |
| 101 | JTAG |

Figure 1-28 shows mode switch SW13.

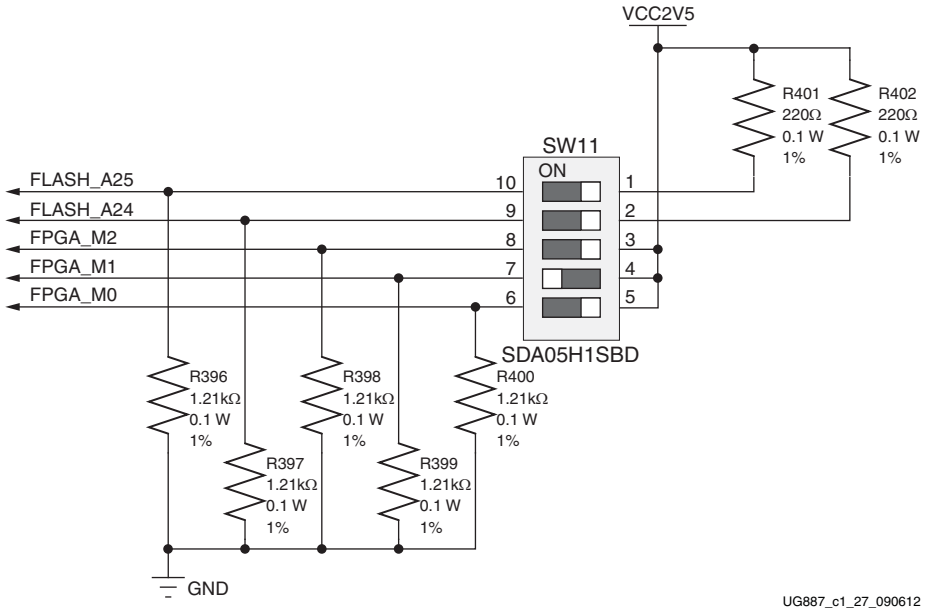


*Figure 1-28:* **Mode Switch**

The mode pins settings on SW11 determine if the linear BPI flash is used for configuring the FPGA. DIP switch. SW11 also provides the upper two address bits for the linear BPI flash and can be used to select one of multiple stored configuration bitstreams. Figure 1-29 shows the connectivity between the onboard nonvolatile flash devices used for configuration and the FPGA.

To obtain the fastest configuration speed, an external 80 MHz oscillator is wired to the EMCCLK pin of the FPGA. This allows users to create bitstreams that configure the FPGA over the 16-bit datapath from the linear BPI flash memory at a maximum synchronous read rate of 80 MHz.

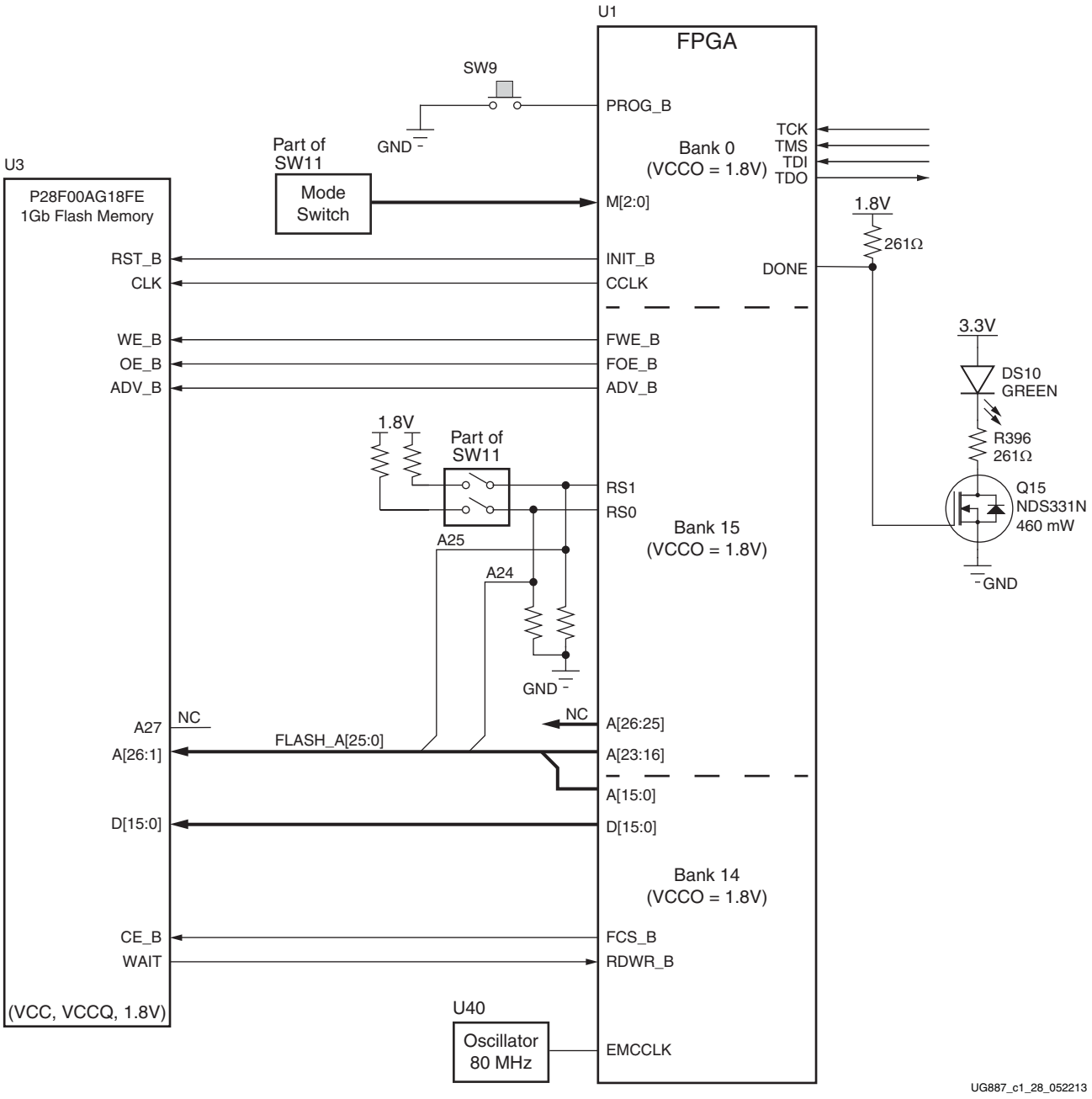


*Figure 1-29:* **VC709 Board Configuration Circuit**

Appendix A

# Default Switch and Jumper Settings

## GPIO DIP Switch SW2

See Figure 1-2 Item 24 for the location of SW2. Default settings are shown in Figure A-1 and details are listed in Table A-1.

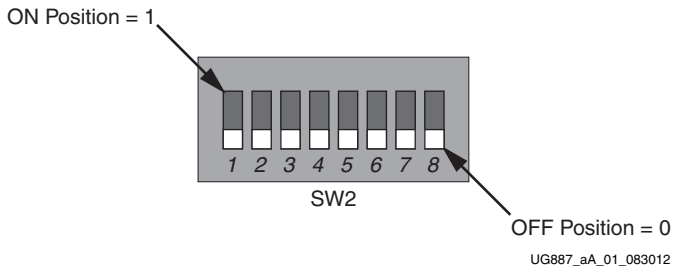


*Figure A-1:* **SW2 Default Settings**

*Table A-1:* **SW2 Default Switch Settings**

| Position | Function | Default |
|---|---|---|
| 1 | GPIO_DIP_SW0 | Off |
| 2 | GPIO_DIP_SW1 | Off |
| 3 | GPIO_DIP_SW2 | Off |
| 4 | GPIO_DIP_SW3 | Off |
| 5 | GPIO_DIP_SW4 | Off |
| 6 | GPIO_DIP_SW5 | Off |
| 7 | GPIO_DIP_SW6 | Off |
| 8 | GPIO_DIP_SW7 | Off |

# Configuration DIP Switch SW11

See Figure 1-2 Item 29 for the location of SW11. Default settings are shown in Figure A-2 and details are listed in Table A-2.

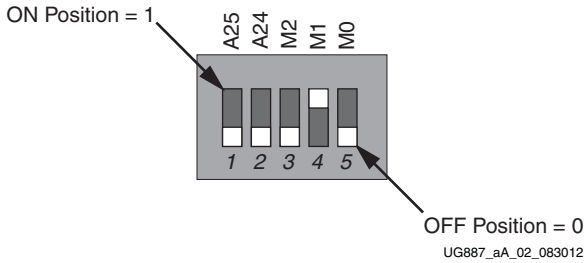


*Figure A-2:* **SW11 Default Settings**

The default mode setting M[2:0] = `010` selects Master BPI configuration at board power-on.

*Table A-2:* **SW11 Default Switch Settings**

| Position | Function | | Default |
|---|---|---|---|
| 1 | FLASH_A25 | A25 | Off |
| 2 | FLASH_A24 | A24 | Off |
| 3 | FPGA_M2 | M0 | Off |
| 4 | FPGA_M1 | M1 | On |
| 5 | FPGA_M0 | M3 | Off |

# Default Jumper Settings

See Figure A-3 for locations of jumpers listed in Table A-3.

*Table A-3:* **Default Jumper Settings**

| Jumper Callout | Jumper | Function | Default Jumper Position | Schematic 0381499 Page Number |
|---|---|---|---|---|
| 1 | J9 | XADC GND ferrite filter bypass jumper | None | 27 |
| 2 | J10 | XADC GND-to-XADC_AGND jumper | 1-2 | 27 |
| 3 | J11 | TI controller U42 Addr 52 Reset jumper | None | 47 |
| 4 | J12 | TI controller U43 Addr 53 Reset jumper | None | 51 |
| 5 | J42 | XADC external 1.2V or internal VREFP selector | 1-2 | 27 |
| 6 | J43 | XADC VCC select header | 2-3 | 27 |
| 7 | J50 | TI controller U64 Addr 54 Reset jumper | None | 54 |
| 8 | J53 | XADC VCC5V0-to-XADC_VCC5V0 jumper | 1-2 | 27 |
| 9 | J54 | XADC REF3012 U35 VIN select | 1-2 | 27 |
| 10 | J49 | PCIe bus width select header | 1-2 | 35 |

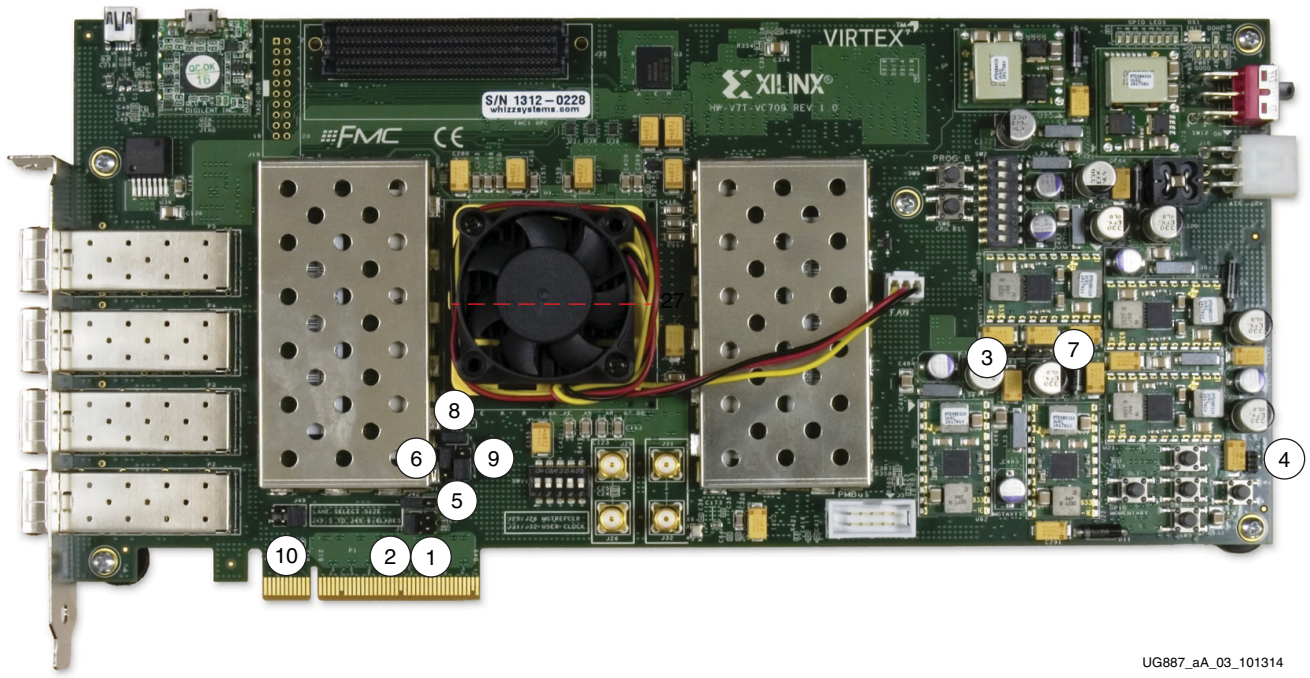


*Figure A-3:* **VC709 Board Jumper Locations**

# VITA 57.1 FMC Connector Pinouts

Figure B-1 shows the pinout of the FPGA mezzanine card (FMC) high pin count (HPC) connector defined by the VITA 57.1 FMC specification. For a description of how the VC709 board implements the FMC specification, see VITA 57.1 FMC1 HPC Connector (Partially Populated).

| | K | J | H | G | F | E | D | C | B | A |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | VREF_B_M2C | GND | VREF_A_M2C | GND | PG_M2C | GND | PG_C2M | GND | RES1 | GND |
| 2 | GND | CLK3_M2C_P | PRSNT_M2C_L | CLK1_M2C_P | GND | HA01_P_CC | GND | DP0_C2M_P | GND | DP1_M2C_P |
| 3 | GND | CLK3_M2C_N | GND | CLK1_M2C_N | GND | HA01_N_CC | GND | DP0_C2M_N | GND | DP1_M2C_N |
| 4 | CLK2_M2C_P | GND | CLK0_M2C_P | GND | HA00_P_CC | GND | GBTCLK0_M2C_P | GND | DP9_M2C_P | GND |
| 5 | CLK2_M2C_N | GND | CLK0_M2C_N | GND | HA00_N_CC | GND | GBTCLK0_M2C_N | GND | DP9_M2C_N | GND |
| 6 | GND | HA03_P | GND | LA00_P_CC | GND | HA05_P | GND | DP0_M2C_P | GND | DP2_M2C_P |
| 7 | HA02_P | HA03_N | LA02_P | LA00_N_CC | HA04_P | HA05_N | GND | DP0_M2C_N | GND | DP2_M2C_N |
| 8 | HA02_N | GND | LA02_N | GND | HA04_N | GND | LA01_P_CC | GND | DP8_M2C_P | GND |
| 9 | GND | HA07_P | GND | LA03_P | GND | HA09_P | LA01_N_CC | GND | DP8_M2C_N | GND |
| 10 | HA06_P | HA07_N | LA04_P | LA03_N | HA08_P | HA09_N | GND | LA06_P | GND | DP3_M2C_P |
| 11 | HA06_N | GND | LA04_N | GND | HA08_N | GND | LA05_P | LA06_N | GND | DP3_M2C_N |
| 12 | GND | HA11_P | GND | LA08_P | GND | HA13_P | LA05_N | GND | DP7_M2C_P | GND |
| 13 | HA10_P | HA11_N | LA07_P | LA08_N | HA12_P | HA13_N | GND | GND | DP7_M2C_N | GND |
| 14 | HA10_N | GND | LA07_N | GND | HA12_N | GND | LA09_P | LA10_P | GND | DP4_M2C_P |
| 15 | GND | HA14_P | GND | LA12_P | GND | HA16_P | LA09_N | LA10_N | GND | DP4_M2C_N |
| 16 | HA17_P_CC | HA14_N | LA11_P | LA12_N | HA15_P | HA16_N | GND | GND | DP6_M2C_P | GND |
| 17 | HA17_N_CC | GND | LA11_N | GND | HA15_N | GND | LA13_P | GND | DP6_M2C_N | GND |
| 18 | GND | HA18_P | GND | LA16_P | GND | HA20_P | LA13_N | LA14_P | GND | DP5_M2C_P |
| 19 | HA21_P | HA18_N | LA15_P | LA16_N | HA19_P | HA20_N | GND | LA14_N | GND | DP5_M2C_N |
| 20 | HA21_N | GND | LA15_N | GND | HA19_N | GND | LA17_P_CC | GND | GBTCLK1_M2C_P | GND |
| 21 | GND | HA22_P | GND | LA20_P | GND | HB03_P | LA17_N_CC | GND | GBTCLK1_M2C_N | GND |
| 22 | HA23_P | HA22_N | LA19_P | LA20_N | HB02_P | HB03_N | GND | LA18_P_CC | GND | DP1_C2M_P |
| 23 | HA23_N | GND | LA19_N | GND | HB02_N | GND | LA23_P | LA18_N_CC | GND | DP1_C2M_N |
| 24 | GND | HB01_P | GND | LA22_P | GND | HB05_P | LA23_N | GND | DP9_C2M_P | GND |
| 25 | HB00_P_CC | HB01_N | LA21_P | LA22_N | HB04_P | HB05_N | GND | GND | DP9_C2M_N | GND |
| 26 | HB00_N_CC | GND | LA21_N | GND | HB04_N | GND | LA26_P | LA27_P | GND | DP2_C2M_P |
| 27 | GND | HB07_P | GND | LA25_P | GND | HB09_P | LA26_N | LA27_N | GND | DP2_C2M_N |
| 28 | HB06_P_CC | HB07_N | LA24_P | LA25_N | HB08_P | HB09_N | GND | GND | DP8_C2M_P | GND |
| 29 | HB06_N_CC | GND | LA24_N | GND | HB08_N | GND | TCK | GND | DP8_C2M_N | GND |
| 30 | GND | HB11_P | GND | LA29_P | GND | HB13_P | TDI | SCL | GND | DP3_C2M_P |
| 31 | HB10_P | HB11_N | LA28_P | LA29_N | HB12_P | HB13_N | TDO | SDA | GND | DP3_C2M_N |
| 32 | HB10_N | GND | LA28_N | GND | HB12_N | GND | 3P3VAUX | GND | DP7_C2M_P | GND |
| 33 | GND | HB15_P | GND | LA31_P | GND | HB19_P | TMS | GND | DP7_C2M_N | GND |
| 34 | HB14_P | HB15_N | LA30_P | LA31_N | HB16_P | HB19_N | TRST_L | GA0 | GND | DP4_C2M_P |
| 35 | HB14_N | GND | LA30_N | GND | HB16_N | GND | GA1 | 12P0V | GND | DP4_C2M_N |
| 36 | GND | HB18_P | GND | LA33_P | GND | HB21_P | 3P3V | GND | DP6_C2M_P | GND |
| 37 | HB17_P_CC | HB18_N | LA32_P | LA33_N | HB20_P | HB21_N | GND | 12P0V | DP6_C2M_N | GND |
| 38 | HB17_N_CC | GND | LA32_N | GND | HB20_N | GND | 3P3V | GND | GND | DP5_C2M_P |
| 39 | GND | VIO_B_M2C | GND | VADJ | GND | VADJ | GND | 3P3V | GND | DP5_C2M_N |
| 40 | VIO_B_M2C | GND | VADJ | GND | VADJ | GND | 3P3V | GND | RES0 | GND |

UG887_aB_01_083012

*Figure B-1:* **FMC1 HPC Connector Pinout**

XILINX

*Appendix C*

# *Xilinx Design Constraints*

The VC709 board Xilinx design constraints (XDC) file template provides for designs targeting the VC709 board. Net names in the constraints correlate with net names on the latest VC709 board schematic. Users must identify the appropriate pins and replace the net names listed here with net names in the user RTL. See the *Vivado Design Suite User Guide Using Constraints* (UG903) [Ref 10] for more information.

The FMC connector J35 is connected to 1.8V $V_{CCO}$ banks. Because each user's FMC card implements customer-specific circuitry, the FMC bank I/O standards must be uniquely defined by each customer.

Refer to the boards file on the Virtex-7 FPGA VC709 Evaluation Kit documentation page (www.xilinx.com/vc709), for the latest version of the FPGA xdc constraint file.

# Board Setup

## Installing the VC709 Board in a PC Chassis

Installation of the VC709 board inside a computer chassis is required when developing or testing PCI Express functionality.

When the VC709 board is used inside a computer chassis (that is, plugged in to the PCIe® slot), power is provided from the ATX power supply 4-pin peripheral connector *only* through the ATX adapter cable shown in Figure D-1 to J18 on the VC709 board. The Xilinx part number for this cable is 2600304. For information on ordering this cable, see [Ref 21].

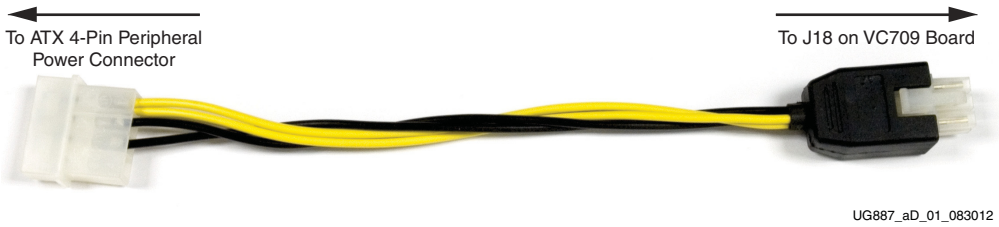


*Figure D-1:* **ATX Power Supply Adapter Cable**

To install the VC709 board in a PC chassis:

1. On the VC709 board, remove all five rubber feet and standoffs. The standoffs and feet are affixed to the board by screws on the top side of the board. Remove all five screws. Re-attach the PCIe bracket with two screws.
2. Power down the host computer and remove the AC power cord from the PC.
3. Open the PC chassis following the instructions provided with the PC.
4. Select a vacant PCIe expansion slot and remove the expansion cover (at the back of the chassis) by removing the screw on the top of the cover.
5. Plug the VC709 board into the PCIe connector at this slot.
6. Secure the card PCIe mounting bracket on the VC709 board with the expansion cover screw.

   ***Note:*** The VC709 board is taller than standard PCIe cards. Ensure that the height of the card is free of obstructions.
7. Connect the ATX power supply to the VC709 board using the ATX power supply adapter cable as shown in Figure D-1:
   a. Plug the 6-pin 2 x 3 Molex connector on the adapter cable into J18 on the VC709 board.
   b. Plug the 4-pin 1 x 4 Molex connector on the opposite end of the adapter cable into an ATX power supply cable bundle mating 4-pin 1 x 4 peripheral power connector.

***Caution!*** Do NOT plug a PC ATX power supply 6-pin connector into J18 on the VC709 board. The ATX 6-pin connector has a different pinout than J18. Connecting an ATX 6-pin connector into J18 may damage the VC709 board and void the board warranty.

8. Slide the VC709 board power switch SW12 to the ON position. The PC can now be plugged in and powered on.

XILINX

*Appendix E*

# *Board Specifications*

## Dimensions

Height: 5.5 inch (14.0 cm)

Thickness (±10%): 0.062 inch (0.1575 cm)

Length: 10.5 inch (26.7 cm)

***Note:*** The VC709 board height exceeds the standard 4.376 inch (11.15 cm) height of a PCI Express card.

## Environmental

### Temperature

Operating: 0°C to +45°C

Storage: –25°C to +60°C

### Humidity

10% to 90% non-condensing

### Operating Voltage

+12 $V_{DC}$

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*Appendix F*

# *Regulatory and Compliance Information*

This product is designed and tested to conform to the European Union directives and standards described in this section.

Refer to the VC709 board master answer record concerning the CE requirements for the PC Test Environment:

Virtex-7 VC709 Evaluation Kit Master Answer Record 51901

## CE Directives

2006/95/EC, *Low Voltage Directive (LVD)*

2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*

## CE Standards

EN standards are maintained by the European Committee for Electrotechnical Standardization (CENELEC). IEC standards are maintained by the International Electrotechnical Commission (IEC).

### Electromagnetic Compatibility

EN 55022:2010, *Information Technology Equipment Radio Disturbance Characteristics – Limits and Methods of Measurement*

EN 55024:2010, *Information Technology Equipment Immunity Characteristics – Limits and Methods of Measurement*

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This is a Class A product and can cause radio interference. In a domestic environment, the user might be required to take adequate corrective measures.

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### Safety

IEC 60950-1:2005, *Information technology equipment – Safety, Part 1: General requirements*

EN 60950-1:2006, *Information technology equipment – Safety, Part 1: General requirements*

# Markings

In August of 2005, the European Union (EU) implemented the EU WEEE Directive 2002/96/EC and later the WEEE Recast Directive 2012/19/EU requiring Producers of electronic and electrical equipment (EEE) to manage and finance the collection, reuse, recycling and to appropriately treat WEEE that the Producer places on the EU market after August 13, 2005. The goal of this directive is to minimize the volume of electrical and electronic waste disposal and to encourage re-use and recycling at the end of life.

Xilinx has met its national obligations to the EU WEEE Directive by registering in those countries to which Xilinx is an importer. Xilinx has also elected to join WEEE Compliance Schemes in some countries to help manage customer returns at end-of-life.

If you have purchased Xilinx-branded electrical or electronic products in the EU and are intending to discard these products at the end of their useful life, please do not dispose of them with your other household or municipal waste. Xilinx has labeled its branded electronic products with the WEEE Symbol to alert our customers that products bearing this label should not be disposed of in a landfill or with municipal or household waste in the EU.

This product complies with Directive 2002/95/EC on the restriction of hazardous substances (RoHS) in electrical and electronic equipment.

This product complies with CE Directives 2006/95/EC, *Low Voltage Directive (LVD) and 2004/108/EC, Electromagnetic Compatibility (EMC) Directive.*

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*Appendix G*

# *Additional Resources*

## Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see the Xilinx Support website.

For continual updates, add the Answer Record to your myAlerts.

## Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

## References

The most up to date information related to the VC709 evaluation kit and its documentation is available on these websites:

Virtex-7 FPGA VC709 Connectivity Kit

Virtex-7 FPGA VC709 Connectivity Kit Documentation website

Virtex-7 VC709 Evaluation Kit Master Answer Record 51901

These Xilinx documents and sites provide supplemental material useful with this guide:

1. *7 Series FPGAs Overview* (DS180)
2. *Virtex-7 T and XT FPGAs Data Sheet: DC and AC Switching Characteristics* (DS183)
3. *7 Series FPGAs Configuration User Guide* (UG470)
4. *7 Series FPGAs Memory Interface Solutions User Guide* (UG586)
5. *7 Series FPGAs Memory Resources User Guide* (UG473)
6. *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476)
7. *7 Series FPGAs Integrated Block for PCI Express User Guide (*PG054)
8. *7 Series FPGAs PCB Design and Pin Planning Guide* (UG483)
9. *7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* (UG480)
10. *Vivado Design Suite User Guide Using Constraints* (UG903)
11. *7 Series FPGAs Packaging and Pinout Product Specification (*UG475)
12. *XC7VX690T (*UG886)

These external websites provide supplemental material useful with this guide: Use the website search function to find information for the items listed with each link:

13. Micron Technology
    PC28F00AG18FE/MT28GU01GAAA1EGC-0SIT, MT8KTF51264HZ-1G9
14. Si Time
    SiT9102, SiT9122
15. Silicon Labs
    Si570, Si5324C, CP2103GM, VCP Drivers
16. Texas Instruments
    UCD9248PFC, PTD08A010W, PTD08A020W, PTD08D021W, LMZ12002, TL1962ADC, TPS51200DR, PCA9548, PCA9546
17. Texas Instrument digital power
    Digital power solutions webpage
18. Texas Instruments fusion tools
    Fusion Digital Power Designer graphical user interface software
19. Texas Instruments Xilinx USB
    USB to GPIO Interface Adapter
20. Analog Devices
    ADP123
21. Sourcegate Technologies

    To order the custom Sourcegate cable, contact sgt-sales@sourcegate.net, +65 6483 2878 for price and availability.

    ***Note:*** The Xilinx ATX cable part number 2600304 is manufactured by Sourcegate Technologies and is equivalent to the Sourcegate Technologies part number AZCBL-WH-11009. Sourcegate only manufactures the latest revision. This is a custom cable and cannot be ordered from the Sourcegate website.

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