Analog Front-end Chip for Multi-cells Li+ Battery Pack AP9107

General Description

AP9107 is an analog front-end chip especially for multi-cells Li-ion/Polymer battery pack application. It includes 8-Channels analog switch, builds in passive balancing circuit for 6 channels with 65Ω discharge resistor, and linear regulator with 5mA capability which can offer low noise voltage reference for post ADC circuit.

AP9107 has four logic selection inputs (A/B/C/D). When all logic pins are set low, no channel is selected and the chip is turned off with shutdown mode. The A, B, C and D selection pins are compatible with TTL/CMOS logic level, can be connected to MCU I/O port directly to select the right channel respectively. The VOUT is analog output pin to indicate exactly the voltage of each channel.

AUX7, AUX8 pins are auxiliary channels, which can be connected to the NTC and/or PTC resistor to measure the battery pack temperature.

AP9107 has 4 logic output pins as ALO, BLO, CLO and DLO, which can transfer control logic for the upper chip if used in dual or triple chips in serial.

AP9107 is available in standard package of TSSOP-24 (EDP).

Features

- ±6mV Cell Voltage Matching Error between Any 2 CHs after Software Correlation
- Integrated Internal Balancing Circuit with 65Ω Discharge Resistor
- Built-in V_{REF}, 5.0V/5.0mA with 1%
- Built-in Logic Transfer with Level Shift for Application with 2 or 3 Chips in Serial
- Ultra Low Current in Shutdown Mode, 4.5μA
- Up to 6-cells in Serial Battery Pack Application with Single Chip
- Up to 11-cells in Serial Battery Pack Application with Dual Chips
- Up to 16-cells in Serial Battery Pack Application with Triple Chips
- Compatible with TTL/CMOS Logic Level

Applications

- E-Bike Battery Pack
- E-Moto Battery Pack

TSSOP-24 (EDP)

Figure 1. Package Type of AP9107

Pin Configuration

G Package
(TSSOP-24 (EDP))

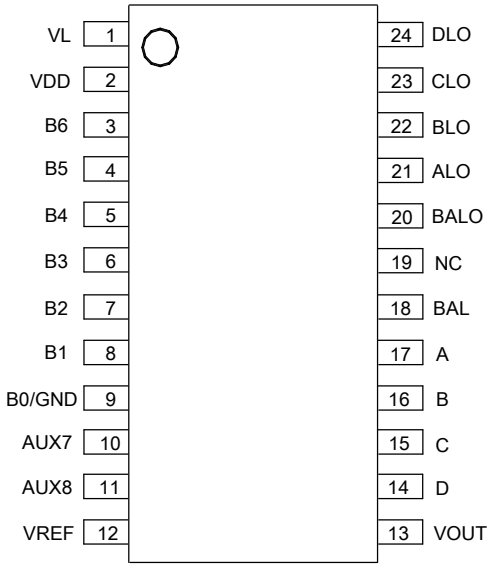


Figure 2. Pin Configuration of AP9107 (Top View)

Pin Descriptions (Note 1)

Pin Number	Pin Name	Function
1	VL	Level shift logic power supply
2	VDD	Power supply
3	B6	Positive node of sixth battery cell
4	B5	Positive node of fifth battery cell & negative node of sixth battery cell
5	B4	Positive node of fourth battery cell & negative node of fifth battery cell
6	B3	Positive node of third battery cell & negative node of fourth battery cell
7	B2	Positive node of second battery cell & negative node of third battery cell
8	B1	Positive node of first battery cell & negative node of second battery cell
9	B0(GND)	Ground and negative node of first battery cell
10	AUX7	Auxiliary channel 7
11	AUX8	Auxiliary channel 8
12	VREF	Reference voltage output 5V/5mA with 1%, connect 1.0μF capacitor at least to GND
13	VOUT	Cell voltage output pin
14	D	Channel selection logic input D
15	C	Channel selection logic input C
16	B	Channel selection logic input B
17	A	Channel selection logic input A
18	BAL	Balance selection logic input, active high. Set BAL high, the chip is in balance mode; in this mode, V_{OUT} is forced to 0V. Set BAL low, the chip is in normal mode; V_{OUT} indicates channel input voltage respectively based on channel selection
19	NC	No connected
20	BALO	Balance selection logic output
21	ALO	Channel selection logic output A
22	BLO	Channel selection logic output B
23	CLO	Channel selection logic output C
24	DLO	Channel selection logic output D

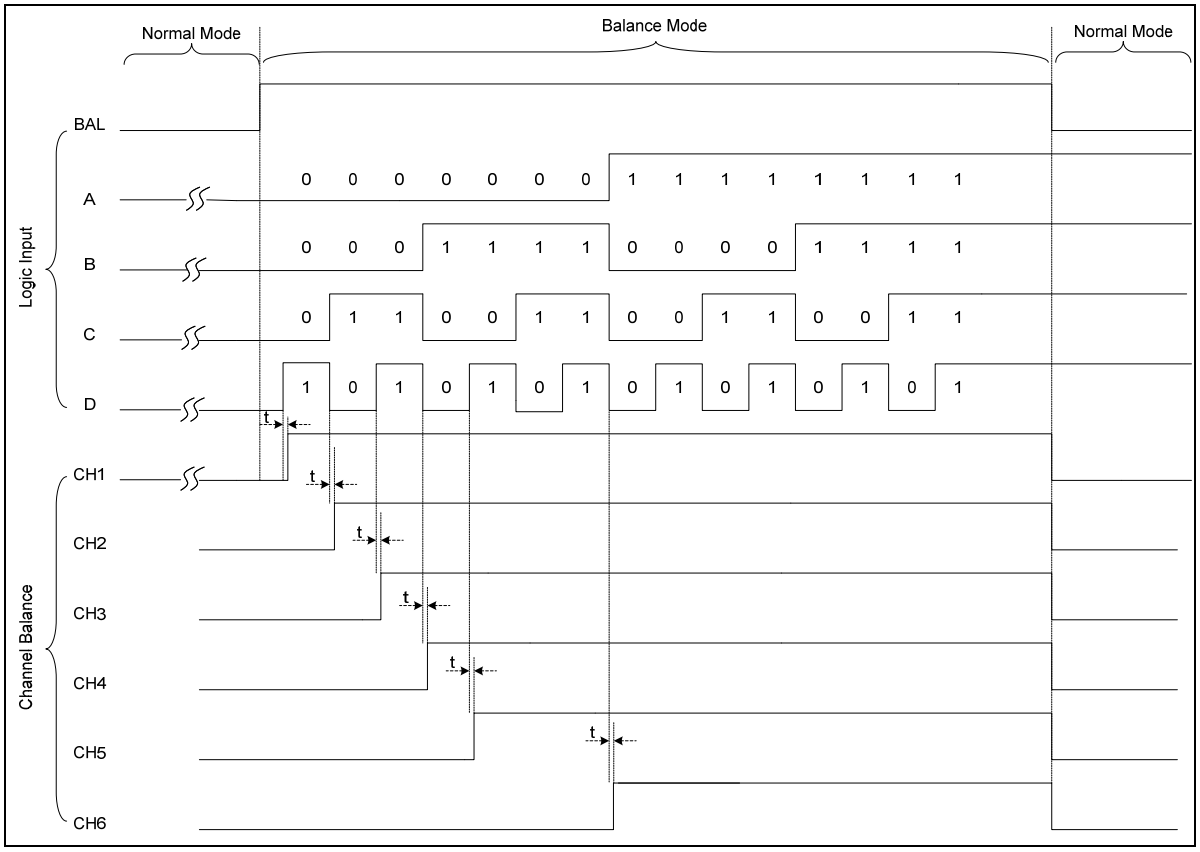
Note 1: VDD pin should always be connected to the positive node of top battery; Voltage of VL pin should be equal to or larger than that of the VDD pin, and should not exceed V_{DD}+5.0V.

Truth Table and Relationship between Input Logic, Output Logic and Active Channel (Note 2)

V_{DD}=21.6V, V_L=V_{DD}+4.4V=26V.

Logic Input					Logic Output					Balance Status	Active Channel	Output Voltage (V_{OUT})
BAL	A	B	C	D	BALO	ALO	BLO	CLO	DLO			
0	0	0	0	0	0	0	0	0	0	Close (Shutdown Mode)	N/A	0V (Shutdown Mode)
0	0	0	0	1	0	0	1	1	1	Close	QD1	B1 vs. B0
0	0	0	1	0	0	0	1	1	1	Close	QD2	B2 vs. B1
0	0	0	1	1	0	0	1	1	1	Close	QD3	B3 vs. B2
0	0	1	0	0	0	0	1	1	1	Close	QD4	B4 vs. B3
0	0	1	0	1	0	0	1	1	1	Close	QD5	B5 vs. B4
0	0	1	1	0	0	0	1	1	1	Close	QD7	4*(AUX7 vs. GND)
0	0	1	1	1	0	0	1	1	1	Close	QD8	4*(AUX8 vs. GND)
0	1	0	0	0	0	1	0	0	0	Close	QD6	B6 vs. B5
0	1	0	0	1	0	0	0	0	1	Close	QD6	B6 vs. B5
0	1	0	1	0	0	0	0	1	0	Close	QD6	B6 vs. B5
0	1	0	1	1	0	0	0	1	1	Close	QD6	B6 vs. B5
0	1	1	0	0	0	0	1	0	0	Close	QD6	B6 vs. B5
0	1	1	0	1	0	0	1	0	1	Close	QD6	B6 vs. B5
0	1	1	1	0	0	0	1	1	0	Close	QD6	B6 vs. B5
0	1	1	1	1	0	0	1	1	1	Close	QD6	B6 vs. B5
1	0	0	0	0	1	0	0	0	0	N/A	N/A	0V
1	0	0	0	1	1	0	1	1	1	B1 vs. B0	QD1	0V
1	0	0	1	0	1	0	1	1	1	B2 vs. B1	QD2	0V
1	0	0	1	1	1	0	1	1	1	B3 vs. B2	QD3	0V
1	0	1	0	0	1	0	1	1	1	B4 vs. B3	QD4	0V
1	0	1	0	1	1	0	1	1	1	B5 vs. B4	QD5	0V
1	0	1	1	0	1	0	1	1	1	N/A	N/A	0V
1	0	1	1	1	1	0	1	1	1	N/A	N/A	0V
1	1	0	0	0	1	1	0	0	0	B6 vs. B5	QD6	0V
1	1	0	0	1	1	0	0	0	1	B6 vs. B5	QD6	0V
1	1	0	1	0	1	0	0	1	0	B6 vs. B5	QD6	0V
1	1	0	1	1	1	0	0	1	1	B6 vs. B5	QD6	0V
1	1	1	0	0	1	0	1	0	0	B6 vs. B5	QD6	0V
1	1	1	0	1	1	0	1	0	1	B6 vs. B5	QD6	0V
1	1	1	1	0	1	0	1	1	0	B6 vs. B5	QD6	0V
1	1	1	1	1	1	0	1	1	1	B6 vs. B5	QD6	0V

Channel Balance Chart (Note 2)



Note 2:
In balance mode, output voltage (VOUT pin) is forced to 0V, and it does not indicate the channel input voltage. Balance current between selected channels is active until BAL is set low. Once BAL is set low, V_{OUT} will indicate selected channel input voltage correctly. Make sure the set up time of channel selection is 1.0ms at least. Balance current is generated after 't' period, 500μs in typical.

Functional Block Diagram

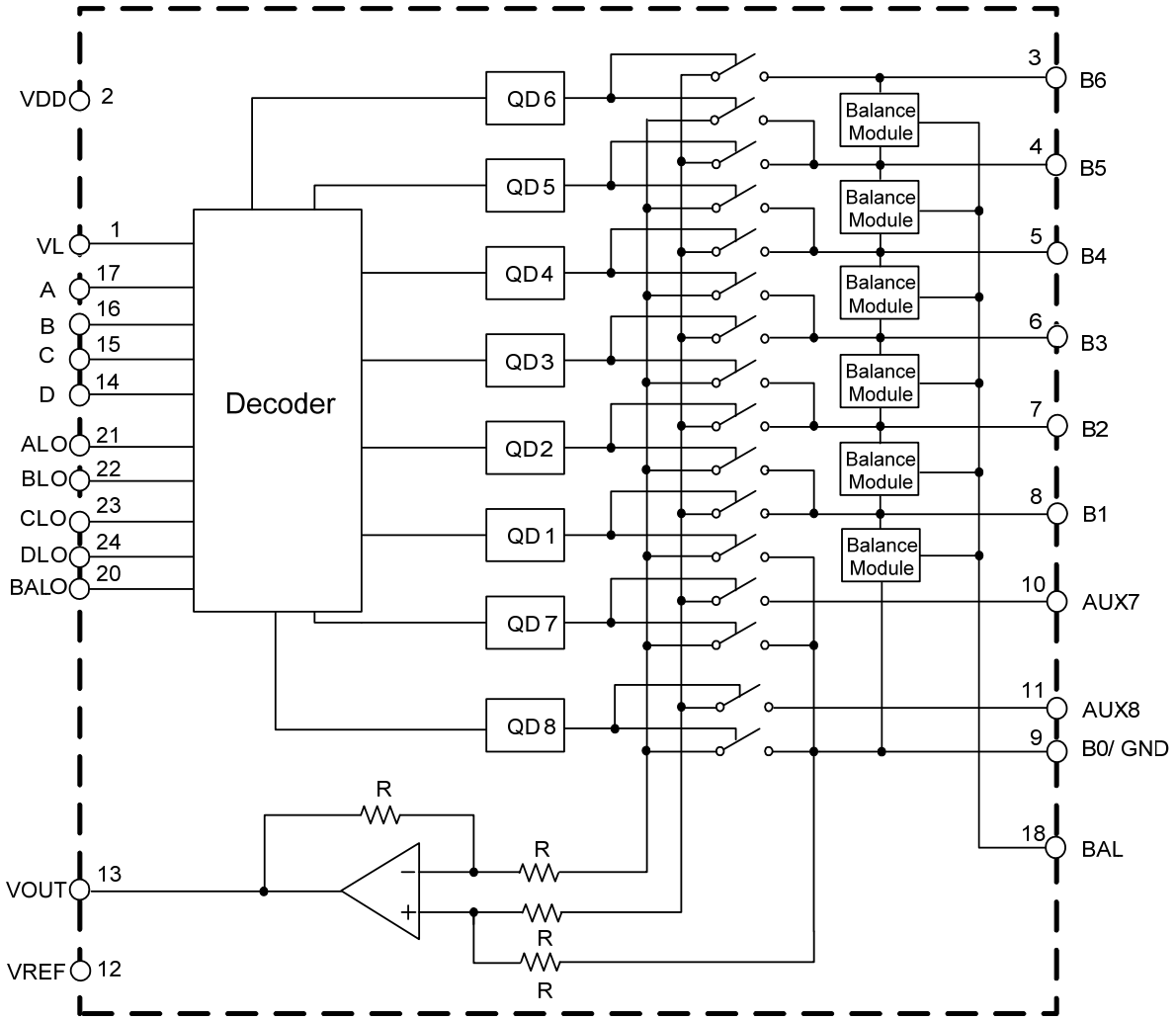
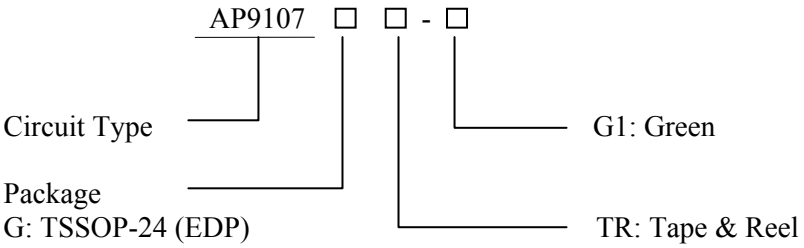


Figure 3. Functional Block Diagram of AP9107

Ordering Information



Package	Temperature Range	Part Number	Marking ID	Packing Type
TSSOP-24 (EDP) (Note 3)	-40 to 85°C	AP9107GTR-G1	AP9107G-G1	Tape & Reel

BCD Semiconductor's Pb-free products, as designated with "G1" suffix in the part number, are RoHS compliant and green.

Note 3: For the thermal pad size, please see the Option 2 of Mechanical Dimensions in Page 16.

Absolute Maximum Ratings (Note 4)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3 to 36	V
Logic Voltage	VL to VDD	-0.3 to 5	V
	VL to GND	-0.3 to 36	V
Voltage between B_N and B_{N+1}	V_{CELL}	-0.3 to 5	V
Voltage between AUX7/AUX8 and GND	V_{AUX}	-0.3 to 1.25	V
Operating Junction Temperature Range	T_J	150	ºC
Storage Temperature Range	T_{STG}	-65 to 150	ºC
Lead Temperature (Soldering, 10sec)	T_{LEAD}	260	ºC
Thermal Resistance (Note 5)	θ_{JA}	40	ºC/W
ESD (Machine Model)		200	V
ESD (Human Body Model)		2000	V

Note 4: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.
Note 5: Chip is soldered to copper (1oz, 100mm^2) with 10*phi 0.5mm vias.

Recommended Operating Conditions

Parameter		Symbol	Min	Max	Unit
Supply Voltage		V_{DD}	6.0	27	V
Battery Cell Voltage		V_{CELL}	2.0	4.5	V
Input Voltage	(B6 vs. B5, B5 vs. B4, B4 vs. B3, B3 vs. B2, B2 vs. B1, B1 vs. GND)	V_{IN}	2.0	4.5	V
	AUX7/8 vs. GND		0.5	1.125	
Operating Ambient Temperature		T_A	-40	85	°C
Input Logic Level		V_{IL}/V_{IH}	0	5.0	V

Electrical Characteristics

V_{DD}=21.6V, V_L=V_{DD}+4.4V=26V, T_A=25°C, **Bold** typeface applies over full temperature -40°C≤T_A≤85°C ranges, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		6.0		27	V
Quiescent Current	I_Q			0.28	0.4	mA
Logic Current	I_L			8.0		μA
Shutdown Current	I_{SHUT}	Set A, B, C, D and BAL low		4.5	8.0	μA
VREF Output Voltage	V_{REF}		4.95	5.0	5.05	V
VREF Output Current	I_{REF}		3	5		mA
Balance Discharge Resistor	R_{BAL}			65		Ω
Switch						
Bias Current	I_{BIAS}	For B1, B2, B3, B4, B5 and B6 Pin		25	40	μA
		For AUX7, AUX8 Pin			1.0	
Channel Matching Error between any 2 Channels after Correlations	E_{MATCH}	Set all channels DC: 2.5V to 4.2V, (V_{MAX}-V_{MIN})/average(CH1 to CH8)	**-6**		**6**	mV
Gain (Note 6)	GAIN	CH1, CH2, CH3, CH4, CH5, CH6		1.0		V/V
		CH7, CH8		0.25		
Channel Switching and Set-up Time	t_{SET}			1.0		ms
Logic Input (Voltage Mode)						
Logic Input High Level	V_{IH}	A, B, C, D, BAL	1.2		5.0	V
Logic Input Low Level	V_{IL}	A, B, C, D, BAL	0		0.5	V
Input Leakage Current	I_{LEAK}	Set A, B, C, D BAL 0V	-1.0		1.0	μA
Pull Down Current	$I_{PULL-DOWN}$	Set A, B, C, D BAL 5.0V			1.0	μA
Logic Output (Voltage Mode)						
Logic Input Low Level	V_{OL}	ALO, BLO, CLO, DLO, BALO	V_{DD}			V
Logic Input High Level	V_{OH}	ALO, BLO, CLO, DLO, BALO			V_L	V

Note 6: CH1-B1 vs. B0; CH2-B2 vs. B1; CH3-B3 vs. B2; CH4-B4 vs. B3; CH5-B5 vs. B4; CH6-B6 vs. B5; CH7-AUX7 vs. B0; CH8-AUX8 vs. B0.

Typical Application

AP9107 can be used for multi-cells (3 to 6-cells in serial) battery pack application. Below is the recommended typical application circuit for 6 cells in series.

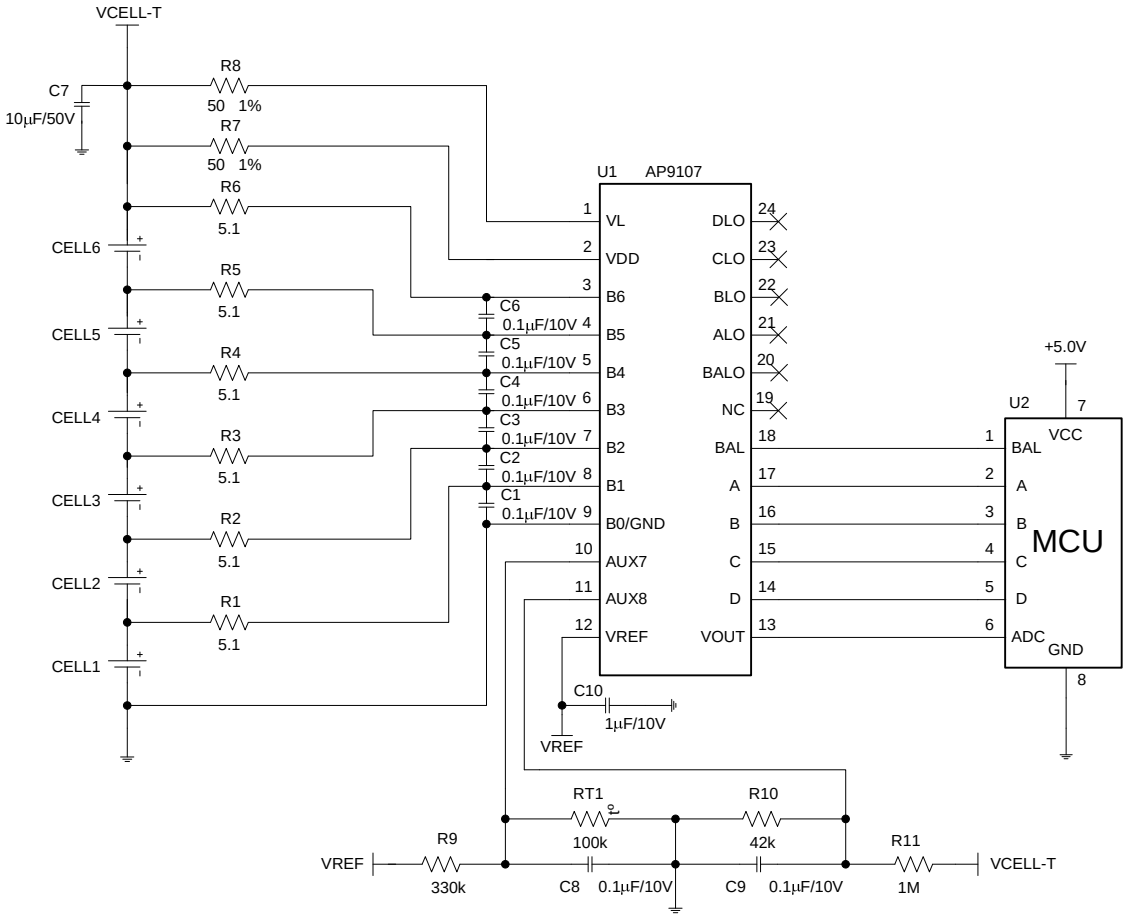


Figure 4. 6-cells Battery (Single Chip) Application for AP9107

Truth Table for 6-cells (Single Chip) Battery Application

Logic Input					Balance Status	Output Voltage
BAL	A	B	C	D		
0	0	0	0	0	Close (Shutdown Mode)	0V (Shutdown Mode)
0	0	0	0	1	Close	VCELL1
0	0	0	1	0	Close	VCELL2
0	0	0	1	1	Close	VCELL3
0	0	1	0	0	Close	VCELL4
0	0	1	0	1	Close	VCELL5
0	0	1	1	0	Close	4*(AUX7)
0	0	1	1	1	Close	4*(AUX8)
0	1	0	0	0	Close	VCELL6
0	1	0	0	1	Close	VCELL6
0	1	0	1	0	Close	VCELL6
0	1	0	1	1	Close	VCELL6
0	1	1	0	0	Close	VCELL6
0	1	1	0	1	Close	VCELL6
0	1	1	1	0	Close	VCELL6
0	1	1	1	1	Close	VCELL6
1	0	0	0	0	N/A	0V
1	0	0	0	1	VCELL1	0V
1	0	0	1	0	VCELL2	0V
1	0	0	1	1	VCELL3	0V
1	0	1	0	0	VCELL4	0V
1	0	1	0	1	VCELL5	0V
1	0	1	1	0	N/A	0V
1	0	1	1	1	N/A	0V
1	1	0	0	0	VCELL6	0V
1	1	0	0	1	VCELL6	0V
1	1	0	1	0	VCELL6	0V
1	1	0	1	1	VCELL6	0V
1	1	1	0	0	VCELL6	0V
1	1	1	0	1	VCELL6	0V
1	1	1	1	0	VCELL6	0V
1	1	1	1	1	VCELL6	0V

Typical Application (Continued)

AP9107 can be used for up to 11-cells in serial battery pack application with dual chips. Below is the recommended typical application circuit for 11 cells in series battery pack.

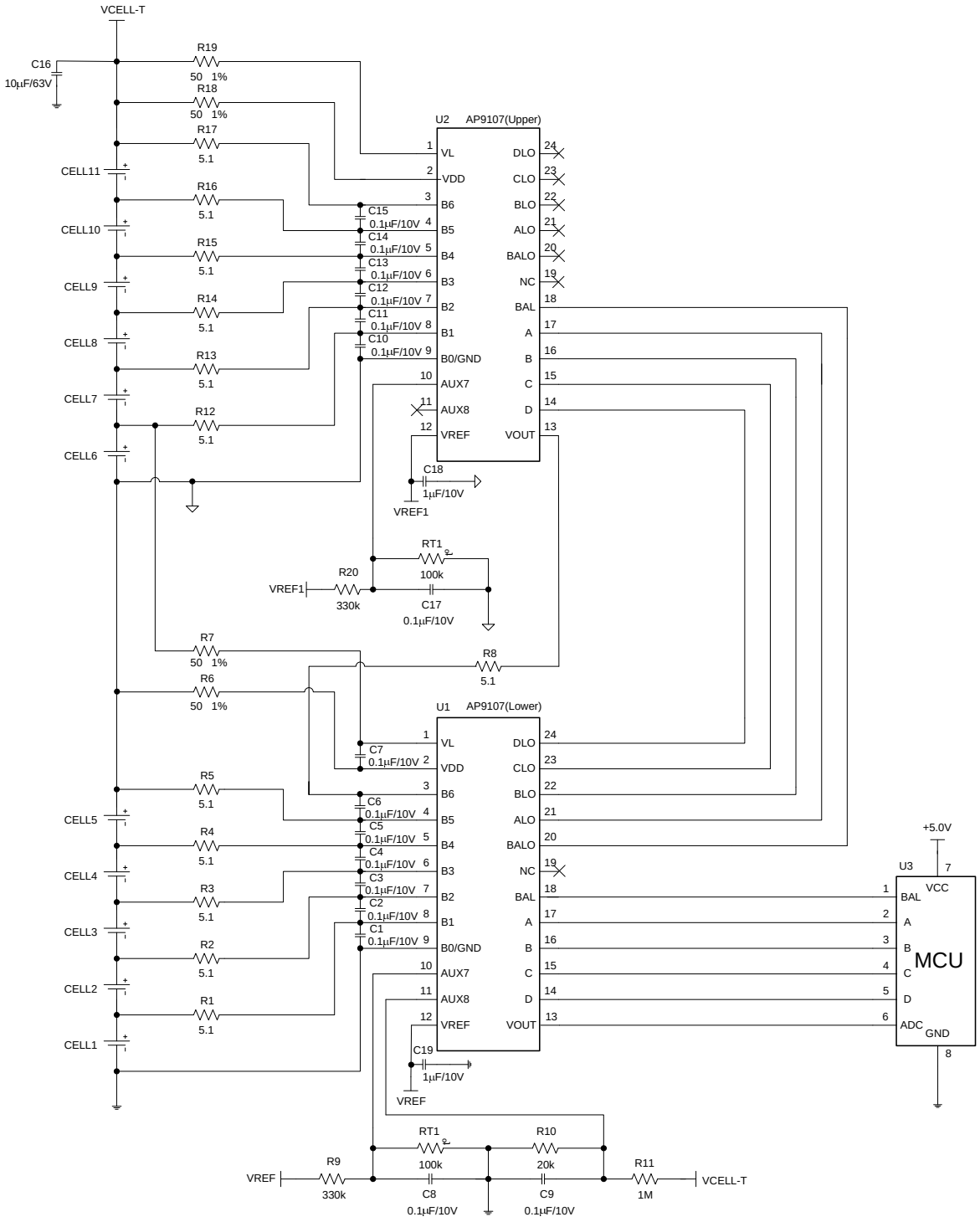


Figure 5. 11-cells Battery (Dual Chips) Application for AP9107

Truth Table for 11-cells (Dual Chips) Battery Application

Logic Input (Lower)					Logic Input (Upper)					Balance Status	Output Voltage
BAL	A	B	C	D	BAL	A	B	C	D		
0	0	0	0	0	0	0	0	0	0	Close (Shutdown Mode)	0V (Shutdown Mode)
0	0	0	0	1	0	0	1	1	1	Close	VCELL1
0	0	0	1	0	0	0	1	1	1	Close	VCELL2
0	0	0	1	1	0	0	1	1	1	Close	VCELL3
0	0	1	0	0	0	0	1	1	1	Close	VCELL4
0	0	1	0	1	0	0	1	1	1	Close	VCELL5
0	0	1	1	0	0	0	1	1	1	Close	4*(AUX7)(Lower)
0	0	1	1	1	0	0	1	1	1	Close	4*(AUX8) (Lower)
0	1	0	0	0	0	1	0	0	0	Close	VCELL11
0	1	0	0	1	0	0	0	0	1	Close	VCELL6
0	1	0	1	0	0	0	0	1	0	Close	VCELL7
0	1	0	1	1	0	0	0	1	1	Close	VCELL8
0	1	1	0	0	0	0	1	0	0	Close	VCELL9
0	1	1	0	1	0	0	1	0	1	Close	VCELL10
0	1	1	1	0	0	0	1	1	0	Close	4*(AUX7)(Upper)
0	1	1	1	1	0	0	1	1	1	Close	4*(AUX8)(Upper)
1	0	0	0	0	1	0	0	0	0	N/A	0V
1	0	0	0	1	1	0	1	1	1	VCELL1	0V
1	0	0	1	0	1	0	1	1	1	VCELL2	0V
1	0	0	1	1	1	0	1	1	1	VCELL3	0V
1	0	1	0	0	1	0	1	1	1	VCELL4	0V
1	0	1	0	1	1	0	1	1	1	VCELL5	0V
1	0	1	1	0	1	0	1	1	1	N/A	0V
1	0	1	1	1	1	0	1	1	1	N/A	0V
1	1	0	0	0	1	1	0	0	0	VCELL11	0V
1	1	0	0	1	1	0	0	0	1	VCELL6	0V
1	1	0	1	0	1	0	0	1	0	VCELL7	0V
1	1	0	1	1	1	0	0	1	1	VCELL8	0V
1	1	1	0	0	1	0	1	0	0	VCELL9	0V
1	1	1	0	1	1	0	1	0	1	VCELL10	0V
1	1	1	1	0	1	0	1	1	0	N/A	0V
1	1	1	1	1	1	0	1	1	1	N/A	0V

Typical Application (Continued)

AP9107 can be used for up to 16-cells in serial battery pack application with triple chips. Below is the recommended typical application circuit for 16 cells in series battery pack.

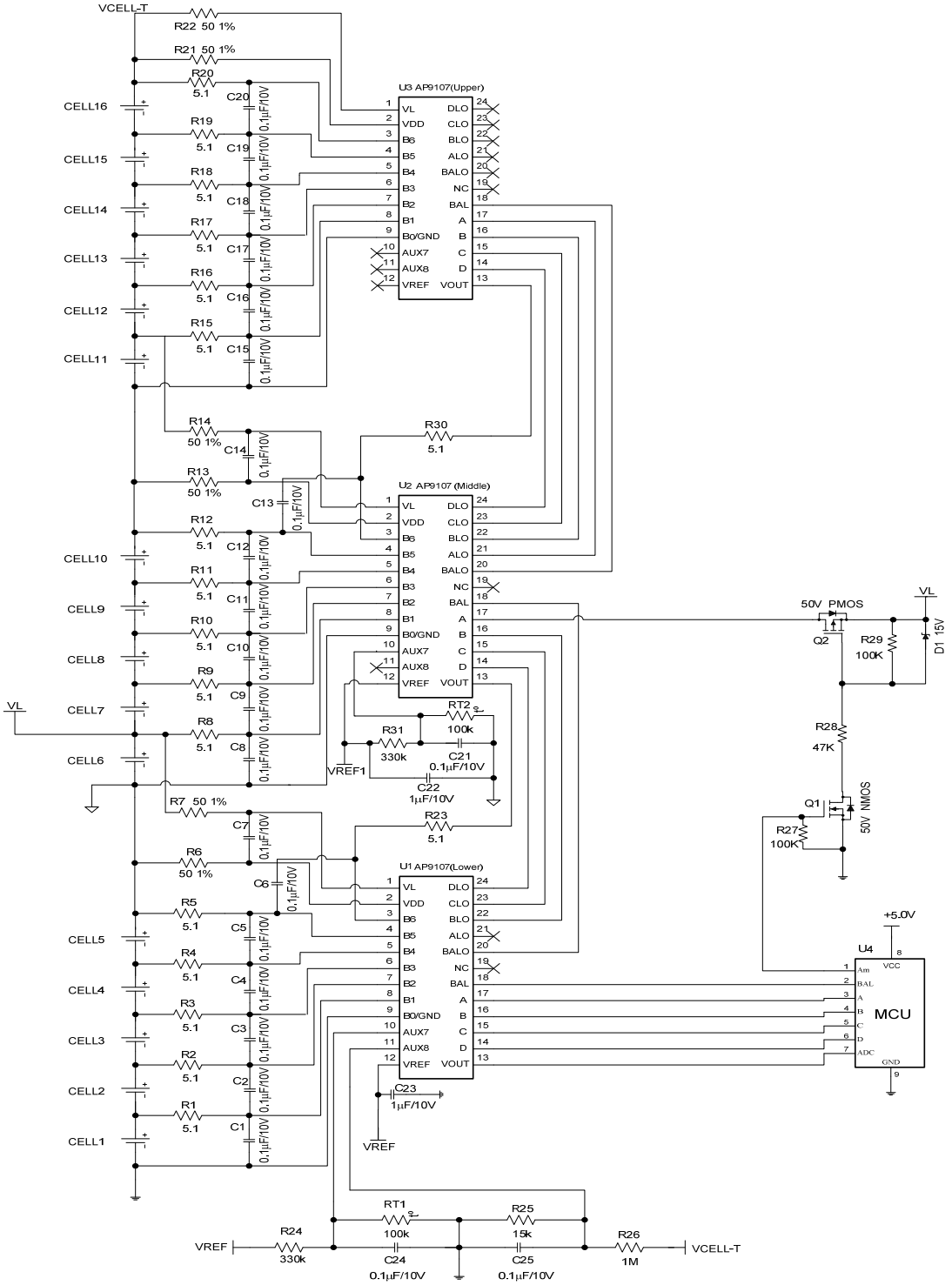


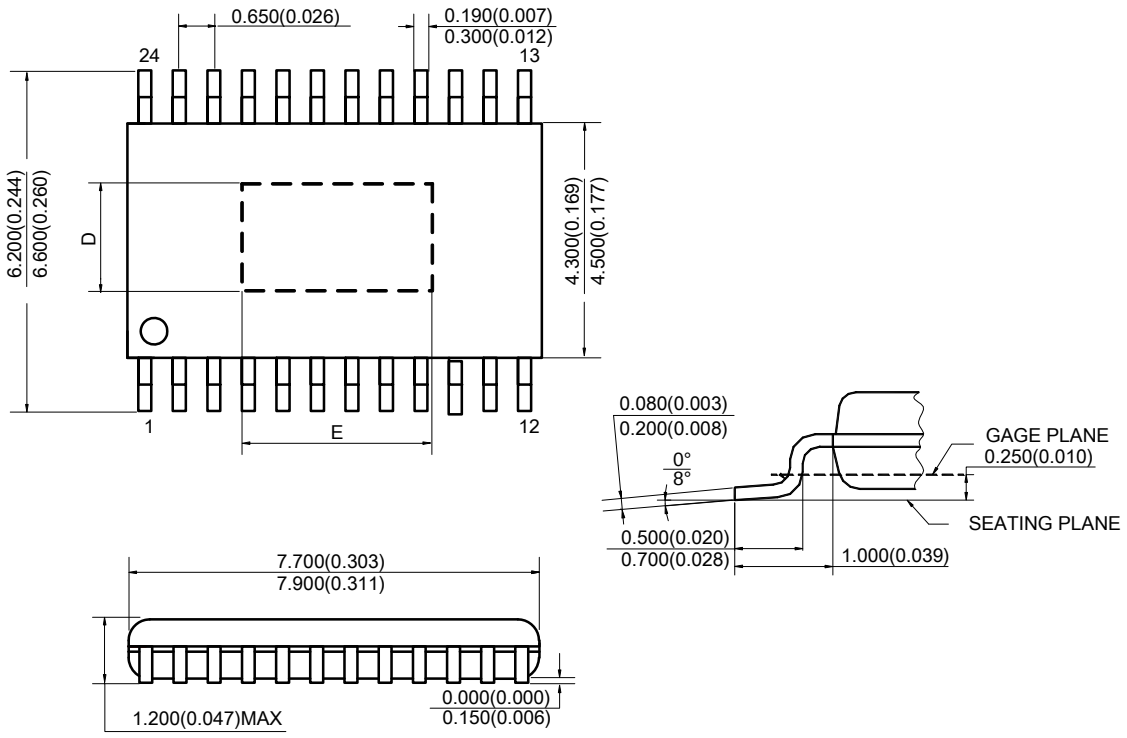
Figure 6. 16-cells Battery (Triple Chips) Application for AP9107

Truth Table for 16-cells (Triple Chips) Battery Application

Logic Input(Lower)					Logic Input (Middle)					Logic Input (Upper)					Balance Status	Output Voltage
BAL	A	B	C	D	BAL	A	B	C	D	BAL	A	B	C	D		
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Close (Shutdown Mode)	0V (Shutdown Mode)
0	0	0	0	1	0	0	1	1	1	0	0	1	1	1	Close	VCELL1
0	0	0	1	0	0	0	1	1	1	0	0	1	1	1	Close	VCELL2
0	0	0	1	1	0	0	1	1	1	0	0	1	1	1	Close	VCELL3
0	0	1	0	0	0	0	1	1	1	0	0	1	1	1	Close	VCELL4
0	0	1	0	1	0	0	1	1	1	0	0	1	1	1	Close	VCELL5
0	0	1	1	0	0	0	1	1	1	0	0	1	1	1	Close	4*(AUX7)(Lower)
0	0	1	1	1	0	0	1	1	1	0	0	1	1	1	Close	4*(AUX8)(Lower)
0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	Close	VCELL16
0	1	0	0	1	0	0	0	0	1	0	0	1	1	1	Close	VCELL6
0	1	0	1	0	0	0	0	1	0	0	0	1	1	1	Close	VCELL7
0	1	0	1	1	0	0	0	1	1	0	0	1	1	1	Close	VCELL8
0	1	1	0	0	0	0	1	0	0	0	0	1	1	1	Close	VCELL9
0	1	1	0	1	0	0	1	0	1	0	0	1	1	1	Close	VCELL10
0	1	1	1	0	0	0	1	1	0	0	0	1	1	1	Close	4*(AUX7)(Middle)
0	1	1	1	1	0	0	1	1	1	0	0	1	1	1	Close	4*(AUX8)(Middle)
0	1	0	0	1	0	1	0	0	1	0	0	0	0	1	Close	VCELL11
0	1	0	1	0	0	1	0	1	0	0	0	0	1	0	Close	VCELL12
0	1	0	1	1	0	1	0	1	1	0	0	0	1	1	Close	VCELL13
0	1	1	0	0	0	1	1	0	0	0	0	1	0	0	Close	VCELL14
0	1	1	0	1	0	1	1	0	1	0	0	1	0	1	Close	VCELL15
0	1	1	1	0	0	1	1	1	0	0	0	1	1	0	Close	4*(AUX7)(Upper)
0	1	1	1	1	0	1	1	1	0	0	0	1	1	1	Close	4*(AUX8)(Upper)
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	N/A	0V
1	0	0	0	1	0	0	1	1	1	0	0	1	1	1	VCELL1	0V
1	0	0	1	0	0	0	1	1	1	0	0	1	1	1	VCELL2	0V
1	0	0	1	1	0	0	1	1	1	0	0	1	1	1	VCELL3	0V
1	0	1	0	0	0	0	1	1	1	0	0	1	1	1	VCELL4	0V
1	0	1	0	1	0	0	1	1	1	0	0	1	1	1	VCELL5	0V
1	0	1	1	0	0	0	1	1	1	0	0	1	1	1	N/A	0V
1	0	1	1	1	0	0	1	1	1	0	0	1	1	1	N/A	0V
1	1	0	0	0	0	1	0	0	0	0	1	0	0	0	VCELL16	0V
1	1	0	0	1	0	0	0	0	1	0	0	1	1	1	VCELL6	0V
1	1	0	1	0	0	0	0	1	0	0	0	1	1	1	VCELL7	0V
1	1	0	1	1	0	0	0	1	1	0	0	1	1	1	VCELL8	0V
1	1	1	0	0	0	0	1	0	0	0	0	1	1	1	VCELL9	0V
1	1	1	0	1	0	0	1	0	1	0	0	1	1	1	VCELL10	0V
1	1	1	1	0	0	0	1	1	0	0	0	1	1	1	N/A	0V
1	1	1	1	1	0	0	1	1	1	0	0	1	1	1	N/A	0V
1	1	0	0	1	0	1	0	0	1	0	0	0	0	1	VCELL11	0V
1	1	0	1	0	0	1	0	1	0	0	0	0	1	0	VCELL12	0V
1	1	0	1	1	0	1	0	1	1	0	0	0	1	1	VCELL13	0V
1	1	1	0	0	0	1	1	0	0	0	0	1	0	0	VCELL14	0V
1	1	1	0	1	0	1	1	0	1	0	0	1	0	1	VCELL15	0V
1	1	1	1	0	0	1	1	1	0	0	0	1	1	0	N/A	0V
1	1	1	1	1	0	1	1	1	0	0	0	1	1	1	N/A	0V

Mechanical Dimensions

TSSOP-24 (EDP) Unit: mm(inch)



Symbol	D				E			
	min(mm)	max(mm)	min(inch)	max(inch)	min(mm)	max(mm)	min(inch)	max(inch)
Option1	1.500	1.800	0.059	0.071	2.700	3.000	0.106	0.118
Option2	2.700	3.000	0.106	0.118	3.900	4.200	0.154	0.165

Note: Eject hole, oriented hole and mold mark is optional.

BCD Semiconductor Manufacturing Limited

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