

## Clock Synthesizer with Differential CPU Outputs

### Features

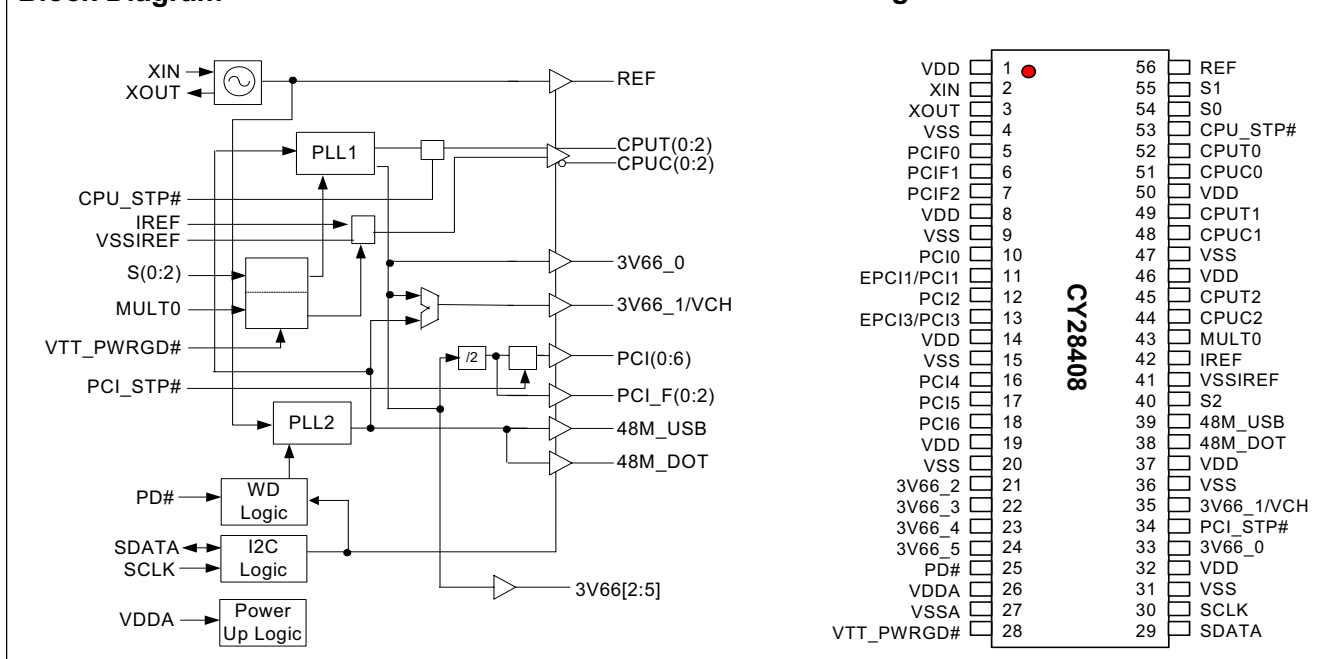
- Compatible to Intel® CK 408 Mobile Clock Synthesizer
- Support Intel P4 and Brookdale CPU
- Specifications
- 3.3V power supply
- Three differential CPU clocks
- Ten copies of PCI clocks
- Six copies of 3V66 clocks
- SMBus support with read back capabilities
- Spread Spectrum electromagnetic interference (EMI) reduction
- Dial-A-Frequency® features
- Dial-A-dB™ features
- 56-pin TSSOP package

**Table 1. Frequency Table<sup>[1]</sup>**

| S2 | S1 | S0 | CPU(0:2) | 3V66   | PCI_PCIF | REF        | USB/DOT |
|----|----|----|----------|--------|----------|------------|---------|
| 1  | 0  | 0  | 100 MHz  | 66 MHz | 33 MHz   | 14.318 MHz | 48 MHz  |
| 1  | 0  | 1  | 133 MHz  | 66 MHz | 33 MHz   | 14.318 MHz | 48 MHz  |
| 1  | 1  | 0  | Reserved |        |          |            |         |
| 1  | 1  | 1  | 166 MHz  | 66 MHz | 33 MHz   | 14.318 MHz | 48 MHz  |
| 0  | 0  | 0  | 66 MHz   | 66 MHz | 33 MHz   | 14.318 MHz | 48 MHz  |
| 0  | 0  | 1  | 100 MHz  | 66 MHz | 33 MHz   | 14.318 MHz | 48 MHz  |
| 0  | 1  | 0  | Reserved |        |          |            |         |
| 0  | 1  | 1  | 133 MHz  | 66 MHz | 33 MHz   | 14.318 MHz | 48 MHz  |
| M  | 0  | 0  | Hi-Z     | Hi-Z   | Hi-Z     | Hi-Z       | Hi-Z    |
| M  | 0  | 1  | TCLK/2   | TCLK/4 | TCLK/8   | TCLK       | TCLK/2  |

### Block Diagram

### Pin Configuration



### Note:

1. TCLK is a test clock driven on the XTAL\_IN input during test mode. M = driven to a level between 1.0V and 1.8V. If the S2 pin is at a M level during power-up, an 0 state will be latched into the device's internal state register.

**Pin Description**

| Pin                          | Name                 | PWR   | I/O       | Description   |
|------------------------------|----------------------|-------|-----------|---|
| 2                            | XIN                  | VDD   | I         | <b>Oscillator buffer input.</b> Connect to a crystal or to an external clock.   |
| 3                            | XOUT                 | VDD   | O         | <b>Oscillator buffer output.</b> Connect to a crystal. Do not connect when an external clock is applied at XIN.   |
| 52, 51, 49, 48, 45, 44       | CPUT(0:2), CPUC(0:2) | VDD   | O         | <b>Differential host output clock pairs.</b> See <i>Table 1</i> for frequencies and functionality.  |
| 10, 12, 16, 17, 18           | PCI(0,2)/(3:5)       | VDDP  | O         | <b>PCI clock outputs.</b> Synchronous to the 3V66 clock. See <i>Table 1</i> .   |
| 11, 13                       | EPCI/PCI(1,3)        | VDD   | I/O<br>PD | <b>Early or normal PCI clock outputs.</b> There is an internal 250k $\Omega$ pull-down resistor. See <i>Table 8</i> .   |
| 5, 6, 7                      | PCIF (0:2)           | VDD   | O         | <b>33-MHz PCI clocks</b> , which are $\pm 2$ copies of 3V66 clocks, may be free running (not stopped when PCI_STP# is asserted LOW) or may be stoppable depending on the programming of SMBus register Byte3, Bits (3:5).                   |
| 56                           | REF                  | VDD   | O         | <b>Buffered output copy of the device's XIN clock.</b>  |
| 42                           | IREF                 | VDD   | I         | <b>Current reference programming input for CPU buffers.</b> A resistor is connected between this pin and VSSIREF.   |
| 28                           | VTT_PWRGD#           | VDD   | I         | <b>Qualifying input that latches S(0:2) and MULT0.</b> When this input is at a logic low, the S(0:2) and MULT0 are latched  |
| 39                           | 48M_USB              | VDD48 | O         | <b>Fixed 48-MHz USB clock outputs.</b>  |
| 38                           | 48M_DOT              | VDD48 | O         | <b>Fixed 48-MHz DOT clock outputs.</b>  |
| 33                           | 3V66_0               | VDD   | O         | <b>3.3V 66-MHz fixed frequency clock.</b>   |
| 35                           | 3V66_1/VCH           | VDD   | O         | <b>3.3V clock selectable with SMBus byte0, Bit5, when Byte5, Bit5.</b> When Byte 0 Bit 5 is at a logic 1, then this pin is a 48M output clock. When byte0, Bit5 is a logic 0, then this is a 66-MHz output clock (default).                 |
| 21, 22, 23, 24               | 3V66(2:5)            | VDD   | O         | <b>3.3V 66-MHz fixed frequency clock.</b>   |
| 25                           | PD#                  | VDD   | I<br>PU   | <b>This pin is a power-down mode pin.</b> A logic LOW level causes the device to enter a power-down state. All internal logic is turned off except for the SMBus logic. All output buffers are stopped.                                     |
| 43                           | MULT0                | VDD   | I<br>PU   | <b>Programming input selection for CPU clock current multiplier.</b><br>0 = 4 * IREF, 1 = 6 * IREF  |
| 55, 54                       | S(0,1)               | VDD   | I         | <b>Frequency select inputs.</b> See <i>Table 1</i>  |
| 29                           | SDATA                | VDD   | I/O<br>PU | <b>Serial data input.</b> Conforms to the SMBus specification of a Slave Receive/Transmit device. It is an input when receiving data. It is an open drain output when acknowledging or transmitting data.                                   |
| 30                           | SCLK                 | VDD   | I<br>PU   | <b>Serial clock input.</b> Conforms to the SMBus specification.   |
| 40                           | S2                   | VDD   | I<br>T    | <b>Frequency select input.</b> See <i>Table 1</i> . This is a tri-level input that is driven HIGH, LOW, or driven to a intermediate level.  |
| 34                           | PCI_STP#             | VDD   | I<br>PU   | <b>PCI clock disable input.</b> When asserted LOW, PCI (0:6) clocks are synchronously disabled in a LOW state. This pin does not effect PCIF (0:2) clock outputs if they are programmed to be PCIF clocks via the device's SMBus interface. |
| 53                           | CPU_STP#             | VDD   | I<br>PU   | <b>CPU clock disable input.</b> When asserted LOW, CPUT (0:2) clocks are synchronously disabled in a HIGH state and CPUC(0:2) clocks are synchronously disabled in a LOW state.   |
| 1, 8, 14, 19, 32, 37, 46, 50 | VDD                  | –     | PWR       | 3.3V power supply.  |
| 4, 9, 15, 20, 27, 31, 36, 47 | VSS                  | –     | PWR       | Common ground.  |
| 41                           | VSSIREF              | –     | PWR       | <b>Current reference programming input for CPU buffers.</b> A resistor is connected between this pin and IREF. This pin should also be returned to device VSS.  |
| 26                           | VDDA                 | –     | PWR       | <b>Analog power input.</b> Used for PLL and internal analog circuits. It is also specifically used to detect and determine when power is at an acceptable level to enable the device to operate.  |

## Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers, can be individually enabled or disabled. The registers associated with the Serial Data Interface initialize to their default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface can also be used during system operation for power management functions.

**Table 2. Command Code Definition**

| Bit   | Description   |
|-------|---|
| 7     | 0 = Block read or block write operation, 1 = Byte read or byte write operation  |
| (6:0) | Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '0000000' |

## Data Protocol

The clock driver serial protocol accepts block write and block read operations from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred.

The block write and block read protocol is outlined in *Table 3* while *Table 4* outlines the corresponding byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

**Table 3. Block Read and Block Write Protocol**

| Block Write Protocol |  | Block Read Protocol |                                     |
|----------------------|--|---------------------|-------------------------------------|
| Bit                  | Description  | Bit                 | Description                         |
| 1                    | Start  | 1                   | Start                               |
| 8:2                  | Slave address – 7 bits   | 8:2                 | Slave address – 7 bits              |
| 9                    | Write  | 9                   | Write                               |
| 10                   | Acknowledge from slave   | 10                  | Acknowledge from slave              |
| 18:11                | Command Code – 8 Bits  | 18:11               | Command Code – 8 Bits               |
| 19                   | Acknowledge from slave   | 19                  | Acknowledge from slave              |
| 27:20                | Byte Count – 8 bits<br>(Skip this step if I <sup>2</sup> C_EN bit set) | 20                  | Repeat start                        |
| 28                   | Acknowledge from slave   | 27:21               | Slave address – 7 bits              |
| 36:29                | Data byte 1 – 8 bits   | 28                  | Read = 1                            |
| 37                   | Acknowledge from slave   | 29                  | Acknowledge from slave              |
| 45:38                | Data byte 2 – 8 bits   | 37:30               | Byte Count from slave – 8 bits      |
| 46                   | Acknowledge from slave   | 38                  | Acknowledge                         |
| ....                 | Data Byte /Slave Acknowledges  | 46:39               | Data byte 1 from slave – 8 bits     |
| ....                 | Data Byte N –8 bits  | 47                  | Acknowledge                         |
| ....                 | Acknowledge from slave   | 55:48               | Data byte 2 from slave – 8 bits     |
| ....                 | Stop   | 56                  | Acknowledge                         |
|                      |  | ....                | Data bytes from slave / Acknowledge |
|                      |  | ....                | Data Bte N from slave – 8 bits      |
|                      |  | ....                | NOT Acknowledge                     |
|                      |  | ...                 | Stop                                |

**Table 4. Byte Read and Byte Write Protocol**

| Byte Write Protocol |                        | Byte Read Protocol |                        |
|---------------------|------------------------|--------------------|------------------------|
| Bit                 | Description            | Bit                | Description            |
| 1                   | Start                  | 1                  | Start                  |
| 8:2                 | Slave address – 7 bits | 8:2                | Slave address – 7 bits |
| 9                   | Write                  | 9                  | Write                  |
| 10                  | Acknowledge from slave | 10                 | Acknowledge from slave |
| 18:11               | Command Code – 8 bits  | 18:11              | Command Code – 8 bits  |

**Table 4. Byte Read and Byte Write Protocol (continued)**

| Byte Write Protocol |                        | Byte Read Protocol |                          |
|---------------------|------------------------|--------------------|--------------------------|
| Bit                 | Description            | Bit                | Description              |
| 19                  | Acknowledge from slave | 19                 | Acknowledge from slave   |
| 27:20               | Data byte – 8 bits     | 20                 | Repeated start           |
| 28                  | Acknowledge from slave | 27:21              | Slave address – 7 bits   |
| 29                  | Stop                   | 28                 | Read                     |
|                     |                        | 29                 | Acknowledge from slave   |
|                     |                        | 37:30              | Data from slave – 8 bits |
|                     |                        | 38                 | NOT Acknowledge          |
|                     |                        | 39                 | Stop                     |

**Byte 0: CPU Clock Register<sup>[2]</sup>**

| Bit | @Pup   | Name       | Description   |
|-----|--------|------------|---|
| 7   | 0      |            | Spread Spectrum Enable, 0 = Spread Off, 1 = Spread On<br>This is a Read and Write control bit.  |
| 6   | 0      |            | CPU clock Power-down Mode Select. 0 = Drive CPUT to 4 or 6 IREF and drive CPUC to low when PD# is asserted LOW. 1 = Three-state all CPU outputs. This is only applicable when PD# is LOW. It is not applicable to CPU_STP#.   |
| 5   | 0      | 3V66_1/VCH | 3V66_1/VCH frequency Select, 0 = 66M selected, 1 = 48M selected<br>This is a Read and Write control bit.  |
| 4   | Pin 53 | CPU_STP#   | Reflects the current value of the external CPU_STP#. This bit is Read-only.   |
| 3   | Pin 34 | PCI_STP#   | Reflects the current value of the internal PCI_STP# function when read. Internally PCI_STP# is a logical AND function of the internal SMBus register bit and the external PCI_STP# pin. This is a Read and Write control bit. |
| 2   | Pin 40 | SEL2       | Frequency Select Bit 2. Reflects the value of SEL2. This bit is Read-only.  |
| 1   | Pin 55 | SEL1       | Frequency Select Bit 1. Reflects the value of SEL1. This bit is Read-only.  |
| 0   | Pin 54 | SEL0       | Frequency Select Bit 0. Reflects the value of SEL0. This bit is Read-only.  |

**Byte 1: CPU Clock Register**

| Bit | @Pup   | Name    | Description   |
|-----|--------|---------|---|
| 7   | Pin 43 |         | MULT0 Value. This bit is Read-only.   |
| 6   | 0      |         | Controls functionality of CPUT/C outputs when CPU_STP# is asserted. 0 = Drive CPUT to 4 or 6 IREF and drive CPUC to low when CPU_STP# is asserted LOW. 1 = Tri-state all CPU outputs when CPU_STP# is asserted. This bit will override Byte0, Bit6 such that even if it is a 0, when PD# goes low the CPU outputs will be tri-stated. |
| 5   | 0      |         | Controls CPU2 functionality when CPU_STP# is asserted LOW<br>1 = Free Running, 0 = Stopped LOW with CPU_STP# asserted LOW<br>This is a Read and Write control bit.  |
| 4   | 0      |         | Controls CPU1 functionality when CPU_STP# is asserted LOW<br>1 = Free Running, 0 = Stopped LOW with CPU_STP# asserted LOW<br>This is a Read and Write control bit.  |
| 3   | 0      |         | Controls CPUT0 functionality when CPU_STP# is asserted LOW<br>1 = Free Running, 0 = Stopped LOW with CPU_STP# asserted LOW<br>This is a Read and Write control bit.   |
| 2   | 1      | CPUT/C2 | CPUT/C2 Output Control<br>1 = enabled, 0 = three-state CPUT/C2<br>This is a Read and Write control bit.   |

**Note:**

2. PU = Internal Pull-up. PD = Internal Pull-down. T = Tri-level logic input.

**Byte 1: CPU Clock Register (continued)**

| Bit | @Pup | Name    | Description   |
|-----|------|---------|---|
| 1   | 1    | CPUT/C1 | CPUT/C1 Output Control<br>1 = enabled, 0 = three-state CPUT/C1<br>This is a Read and Write control bit. |
| 0   | 1    | CPUT/C0 | CPUT/C0 Output Control<br>1 = enabled, 0 = three-state CPUT/C0<br>This is a Read and Write control bit. |

**Byte 2: PCI Clock Control Register (all bits are read- and write-functional)**

| Bit | @Pup | Name | Description  |
|-----|------|------|--|
| 7   | 0    | REF  | REF Output Control.<br>0 = high strength, 1 = low strength |
| 6   | 1    | PCI6 | PCI6 Output Control<br>1 = enabled, 0 = forced LOW         |
| 5   | 1    | PCI5 | PCI5 Output Control<br>1 = enabled, 0 = forced LOW         |
| 4   | 1    | PCI4 | PCI4 Output Control<br>1 = enabled, 0 = forced LOW         |
| 3   | 1    | PCI3 | PCI3 Output Control<br>1 = enabled, 0 = forced LOW         |
| 2   | 1    | PCI2 | PCI2 Output Control<br>1 = enabled, 0 = forced LOW         |
| 1   | 1    | PCI1 | PCI1 Output Control<br>1 = enabled, 0 = forced LOW         |
| 0   | 1    | PCI0 | PCI0 Output Control<br>1 = enabled, 0 = forced LOW         |

**Byte 3: PCI\_F Clock and 48M Control Register (all bits are read- and write-functional)**

| Bit | @Pup | Name    | Description  |
|-----|------|---------|--|
| 7   | 1    | 48M_DOT | 48M_DOT Output Control<br>1 = enabled, 0 = forced LOW                              |
| 6   | 1    | 48M_USB | 48M_USB Output Control<br>1 = enabled, 0 = forced LOW                              |
| 5   | 0    |         | PCI_STP#, control of PCI_F2.<br>0 = Free Running, 1 = Stopped when PCI_STP# is LOW |
| 4   | 0    |         | PCI_STP#, control of PCI_F1.<br>0 = Free Running, 1 = Stopped when PCI_STP# is LOW |
| 3   | 0    |         | PCI_STP#, control of PCI_F0.<br>0 = Free Running, 1 = Stopped when PCI_STP# is LOW |
| 2   | 1    | PCI_F2  | PCI_F2 Output Control<br>1 = running, 0 = forced LOW                               |
| 1   | 1    | PCI_F1  | PCI_F1 Output Control<br>1 = running, 0 = forced LOW                               |
| 0   | 1    | PCI_F0  | PCI_F0 Output Control<br>1 = running, 0 = forced LOW                               |

**Byte 4: 3V66 Control Register** (all bits are read- and write-functional)

| Bit | @Pup | Name       | Description  |
|-----|------|------------|--|
| 7   | 0    |            | SS2 Spread Spectrum control bit (0 = down spread, 1 = center spread) |
| 6   | 0    |            | Reserved   |
| 5   | 1    | 3V66_0     | 3V66_0 Output Enabled, 1 = enabled, 0 = disabled                     |
| 4   | 1    | 3V66_1/VCH | 3V66_1/VCH Output Enable 1 = enabled, 0 = disabled                   |
| 3   | 1    | 3V66_5     | 3V66_5 Output Enable 1 = enabled, 0 = disabled                       |
| 2   | 1    | 3V66_4     | 3V66_4 Output Enabled 1 = enabled, 0 = disabled                      |
| 1   | 1    | 3V66_3     | 3V66_3 Output Enabled 1 = enabled, 0 = disabled                      |
| 0   | 1    | 3V66_2     | 3V66_2 Output Enabled 1 = enabled, 0 = disabled                      |

**Byte 5: Spread Spectrum Control Register** (all bits are read and write functional)

| Bit | @Pup | Name | Description  |
|-----|------|------|--|
| 7   | 0    |      | SS1 Spread Spectrum control bit                                      |
| 6   | 1    |      | SS0 Spread Spectrum control bit                                      |
| 5   | 0    |      | Reserved   |
| 4   | 0    |      | Reserved   |
| 3   | 0    |      | Reserved   |
| 2   | 0    |      | 48M_DOT edge rate control. When set to 1, the edge is slowed by 40%. |
| 1   | 0    |      | Reserved   |
| 0   | 0    |      | USB edge rate control. When set to 1, the edge is slowed by 40%.     |

**Spread Spectrum Clock Generation (SSCG)**

Spread Spectrum is a modulation technique used to minimizing EMI reduction generated by repetitive digital signals. A clock presents the generated EMI energy at the center frequency it is generating. Spread Spectrum distributes this energy over a specific and controlled frequency bandwidth therefore causing the average energy at any point in this band to decrease in value. This technique is achieved by modulating the clock away from its resting frequency by a certain percentage (which also determines the amount of EMI reduction). In this device, Spread Spectrum is enabled by setting specific register bits in the SMBus control bytes. *Table 5* is a listing of the modes and percentages of Spread Spectrum modulation that this device incorporates.

**Table 5. Spread Spectrum**

| SS2 | SS1 | SS0 | Spread Mode | Spread%      |
|-----|-----|-----|-------------|--------------|
| 0   | 0   | 0   | Down        | +0.00, -0.25 |
| 0   | 0   | 1   | Down        | +0.00, -0.50 |
| 0   | 1   | 0   | Down        | +0.00, -0.75 |
| 0   | 1   | 1   | Down        | +0.00, -1.00 |
| 1   | 0   | 0   | Center      | +0.13, -0.13 |
| 1   | 0   | 1   | Center      | +0.25, -0.25 |
| 1   | 1   | 0   | Center      | +0.37, -0.37 |
| 1   | 1   | 1   | Center      | +0.50, -1.50 |

**Byte 6: Silicon Signature Register** (all bits are read-only)

| Bit | @Pup | Name              | Description       |
|-----|------|-------------------|-------------------|
| 7   | 0    | Revision ID Bit 3 | Revision ID Bit 3 |
| 6   | 0    | Revision ID Bit 2 | Revision ID Bit 2 |
| 5   | 0    | Revision ID Bit 1 | Revision ID Bit 1 |
| 4   | 0    | Revision ID Bit 0 | Revision ID Bit 0 |
| 3   | 1    | Vendor ID Bit 3   | Vendor ID Bit 3   |
| 2   | 0    | Vendor ID Bit 2   | Vendor ID Bit 2   |
| 1   | 0    | Vendor ID Bit 1   | Vendor ID Bit 1   |
| 0   | 0    | Vendor ID Bit 0   | Vendor ID Bit 0   |

**Byte 7: Reserved**

| Bit | @Pup | Name | Description |
|-----|------|------|-------------|
| 7   | 0    |      | Reserved    |
| 6   | 0    |      | Reserved    |
| 5   | 0    |      | Reserved    |
| 4   | 0    |      | Reserved    |
| 3   | 1    |      | Reserved    |
| 2   | 1    |      | Reserved    |
| 1   | 1    |      | Reserved    |
| 0   | 0    |      | N8, MSB     |

**Byte 8: Dial-a-Frequency Control Register N** (all bits are read and write functional)

| Bit | @Pup | Name | Description |
|-----|------|------|-------------|
| 7   | 0    |      | N7          |
| 6   | 0    |      | N6          |
| 5   | 0    |      | N5          |
| 4   | 0    |      | N4          |
| 3   | 0    |      | N3          |
| 2   | 0    |      | N2          |
| 1   | 0    |      | N3          |
| 0   | 0    |      | N0, LSB     |

**Byte 9: Dial-a-Frequency™ Control Register R** (all bits are read and write functional)

| Bit | @Pup | Name | Description   |
|-----|------|------|---|
| 7   | 0    |      | R6 MSB  |
| 6   | 0    |      | R5  |
| 5   | 0    |      | R4  |
| 4   | 0    |      | R3  |
| 3   | 0    |      | R2  |
| 2   | 0    |      | R1  |
| 1   | 0    |      | R0, LSB   |
| 0   | 0    |      | R and N register mux selection. 0 = R and N values come from the ROM.<br>1 = data is loaded from DAF (SMBus) registers. |

**Dial-a-Frequency Feature**

SMBus Dial-a-Frequency feature is available in this device via Byte8 and Byte9. See our App Note AN-0025 for details on our Dial-a-Frequency feature.

P is a large value PLL constant that depends on the frequency selection achieved through the hardware selectors (S1, S0). P value may be determined from *Table 6*.

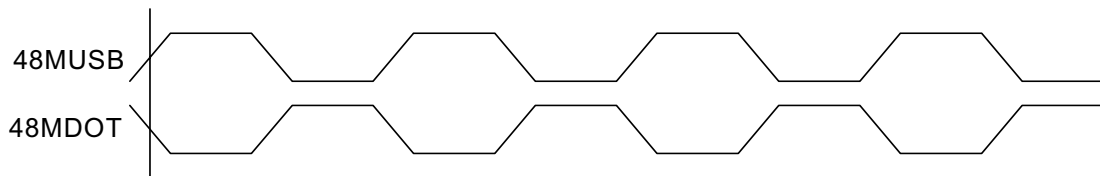
**Table 6. P Value**

| S(1:0) | P        |
|--------|----------|
| 0 0    | 32005333 |
| 0 1    | 48008000 |
| 1 0    | 96016000 |
| 1 1    | 64010667 |

**USB and DOT 48M Phase Relationship**

The 48M\_USB and 48M\_DOT clocks are normally in phase. It is understood that the difference in edge rate will introduce some inherent offset. When 3V66\_1/VCH clock is configured for VCH (48-MHz) operation it is also in phase with the USB and DOT outputs. See *Figure 1*.

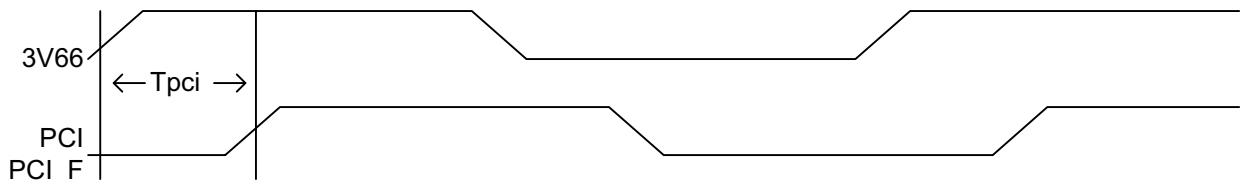




**Figure 1. 48M\_USB and 48M\_DOT Phase Relationship**

**Table 7. Group Timing Relationship and Tolerances**

| Description             | Offset       | Tolerance | Conditions     |
|-------------------------|--------------|-----------|----------------|
| 3V66 to PCI             | 2.5 ns       | ±1.0 ns   | 3V66 Leads PCI |
| 48M_USB to 48M_DOT Skew | 0 or 10.4 ns | ±1.0 ns   |                |



**Figure 2. 3V66 to PCI and PCI\_F Phase Relationship**

**Table 8. Early PCI Select Functions<sup>[3]</sup>**

| EPCI3 | EPCI1 | EPCI(3,1) |
|-------|-------|-----------|
| 0     | 0     | 0.0 ns    |
| 1     | 0     | 0.8 ns    |
| 1     | 1     | 1.6 ns    |

## Special Functions

### PCI\_F and IOAPIC Clock Outputs

The PCIF clock outputs are intended to be used, if required, for systems IOAPIC clock functionality. ANY two of the PCI\_F clock outputs can be used as IOAPIC 33-MHz clock outputs. They are 3.3V outputs will be divided down via a simple resistive voltage divider to meet specific system IOAPIC clock voltage requirements. In the event these clocks are not required, then these clocks can be used as general PCI clocks or disabled via the assertion of the PCI\_STP# pin.

**Note:**

3. 0 = 10K Pull-down resistor, 1 = 10k Pull-up resistor.

### 3V66\_1/VCH Clock Output

The 3V66\_1/VCH pin has a dual functionality that is selectable via SMBus. If Byte0, Bit 5 = '1', then the output is configured as a 48-MHz non-spread spectrum output. This output is phase aligned with the other 48M outputs (USB and DOT), to within 1 ns pin-to-pin skew. The switching of 3V66\_1/VCH into VCH mode occurs at system power on. When the SMBus Bit 5 of Byte 0 is programmed from a '0' to a '1', the 3V66\_1/VCH output may glitch while transitioning to 48M output mode.

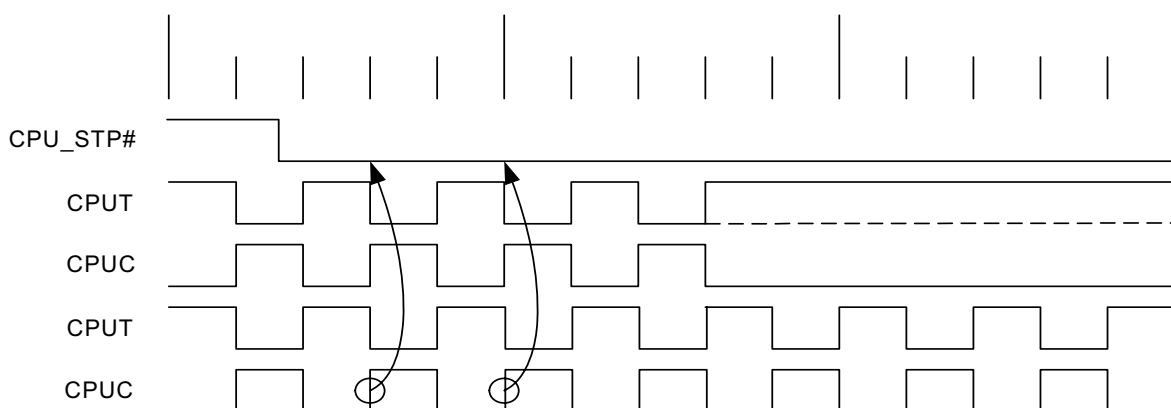
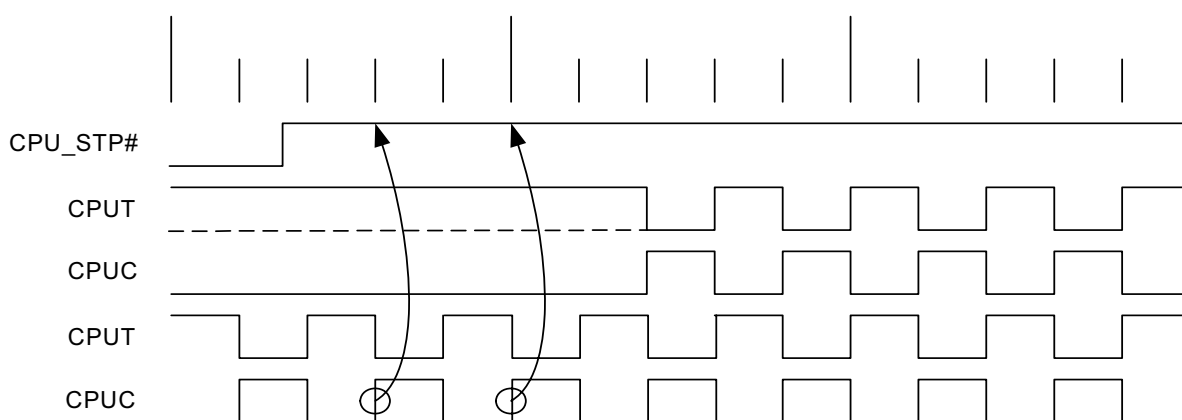
### CPU\_STP# Clarification

The CPU\_STP# signal is an active LOW input used for synchronous stopping and starting the CPU output clocks while the rest of the clock generator continues to function.

### CPU\_STP# – Assertion

When CPU\_STP# pin is asserted, all CPUT/C outputs that are set with the SMBus configuration to be stoppable via assertion of CPU\_STP# will be stopped after being sampled by two falling CPUT/C clock edges. The final state of the stopped CPU signals is CPUT = HIGH and CPU0C = LOW. There is no change to the output drive current values during the stopped state. The CPUT is driven HIGH with a current value equal to (Mult 0 'select') x (Iref), and the CPUC signal will not be driven. Due to external pull-down circuitry CPUC will be LOW during this stopped state.




**Figure 3. CPU\_STP# Assertion Waveform**

**Figure 4. CPU\_STP# Deassertion Waveform**

### CPU\_STP# Deassertion

The deassertion of the CPU\_STP# signal will cause all CPUT/C outputs that were stopped to resume normal operation in a synchronous manner. Synchronous manner meaning that no short or stretched clock pulses will be produced when the clock resumes. The maximum latency from the deassertion to active outputs is no more than 2 CPUC clock cycles.

### Three-state Control of CPU Clocks Clarification

During CPU\_STP# and PD# modes, CPU clock outputs may be set to driven or undriven (three-state) by setting the corresponding SMBus entry in Bit6 of Byte0 and Bit6 of Byte1.

**Table 9. Cypress Clock Power Management Truth Table**

| B0b6 | B1b6 | PD# | CPU_STP# | Stoppable CPUT | Stoppable CPUC | Non-Stop CPUT | Non-Stop CPUC |
|------|------|-----|----------|----------------|----------------|---------------|---------------|
| 0    | 0    | 1   | 1        | Running        | Running        | Running       | Running       |
| 0    | 0    | 1   | 0        | Iref x6        | Iref x6        | Running       | Running       |
| 0    | 0    | 0   | 1        | Iref x2        | Low            | Iref x2       | Low           |
| 0    | 0    | 0   | 0        | Iref x2        | Low            | Iref x2       | Low           |
| 0    | 1    | 1   | 1        | Running        | Running        | Running       | Running       |
| 0    | 1    | 1   | 0        | Hi Z           | Hi Z           | Running       | Running       |
| 0    | 1    | 0   | 1        | Hi Z           | Hi Z           | Hi Z          | Hi Z          |
| 0    | 1    | 0   | 0        | Hi Z           | Hi Z           | Hi Z          | Hi Z          |
| 1    | 0    | 1   | 1        | Running        | Running        | Running       | Running       |
| 1    | 0    | 1   | 0        | Iref x6        | Iref x6        | Running       | Running       |
| 1    | 0    | 0   | 1        | Hi Z           | Hi Z           | Hi Z          | Hi Z          |
| 1    | 0    | 0   | 0        | Hi Z           | Hi Z           | Hi Z          | Hi Z          |

**Table 9. Cypress Clock Power Management Truth Table (continued)**

| B0b6 | B1b6 | PD# | CPU_STP# | Stoppable CPUT | Stoppable CPUC | Non-Stop CPUT | Non-Stop CPUC |
|------|------|-----|----------|----------------|----------------|---------------|---------------|
| 1    | 1    | 1   | 1        | Running        | Running        | Running       | Running       |
| 1    | 1    | 1   | 0        | Hi Z           | Hi Z           | Running       | Running       |
| 1    | 1    | 0   | 1        | Hi Z           | Hi Z           | Hi Z          | Hi Z          |
| 1    | 1    | 0   | 0        | Hi Z           | Hi Z           | Hi Z          | Hi Z          |

**PCI\_STP# Assertion**

The PCI\_STP# signal is an active LOW input used for synchronous stopping and starting the PCI outputs while the rest of the clock generator continues to function. The set-up time for capturing PCI\_STP# going LOW is 10 ns ( $t_{\text{setup}}$ ) (see Figure 7). The PCI\_F clocks will not be affected by this pin if their control bits in the SMBus register are set to allow them to be free running.

**PCI\_STP# – Deassertion**

The deassertion of the PCI\_STP# signal will cause all PCI and stoppable PCI\_F clocks to resume running in a synchronous manner within two PCI clock periods after PCI\_STP# transitions to a high level.

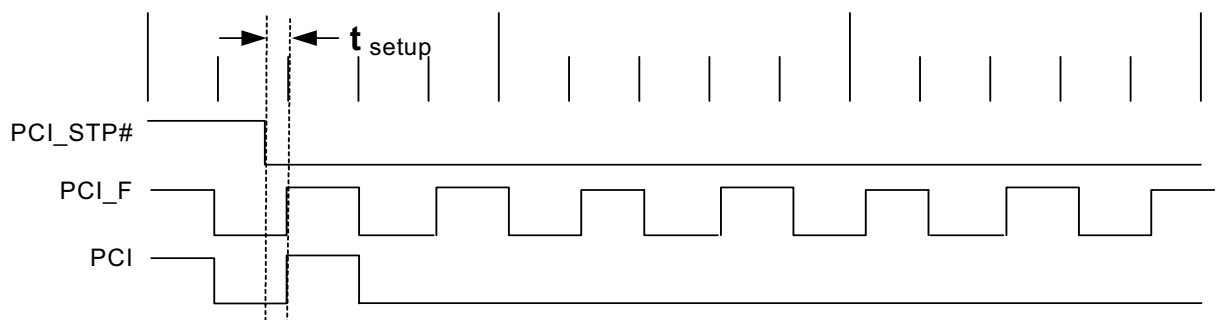
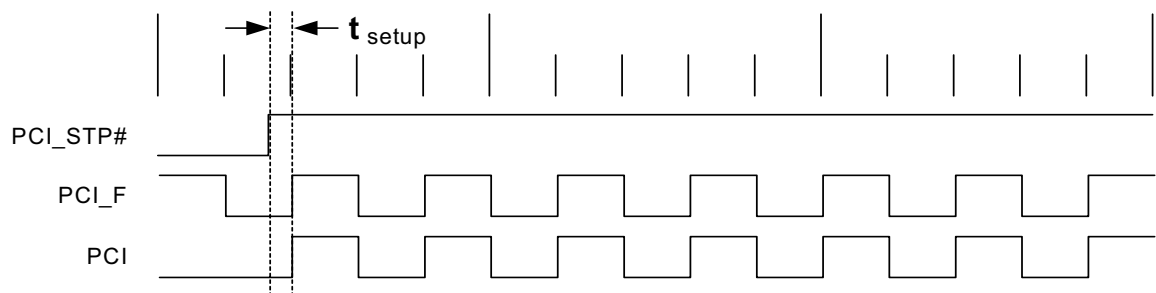
Note that the PCI STOP function is controlled by two inputs. One is the device PCI\_STP# pin number 34 and the other is SMBus byte 0 bit 3. These two inputs to the function are logically ANDed. If either the external pin or the internal SMBus register bit is set low then the stoppable PCI clocks will be stopped in a logic low state. Reading SMBus Byte 0 Bit 3 will return a 0 value if either of these control bits are set LOW thereby indicating the devices stoppable PCI clocks are not running.

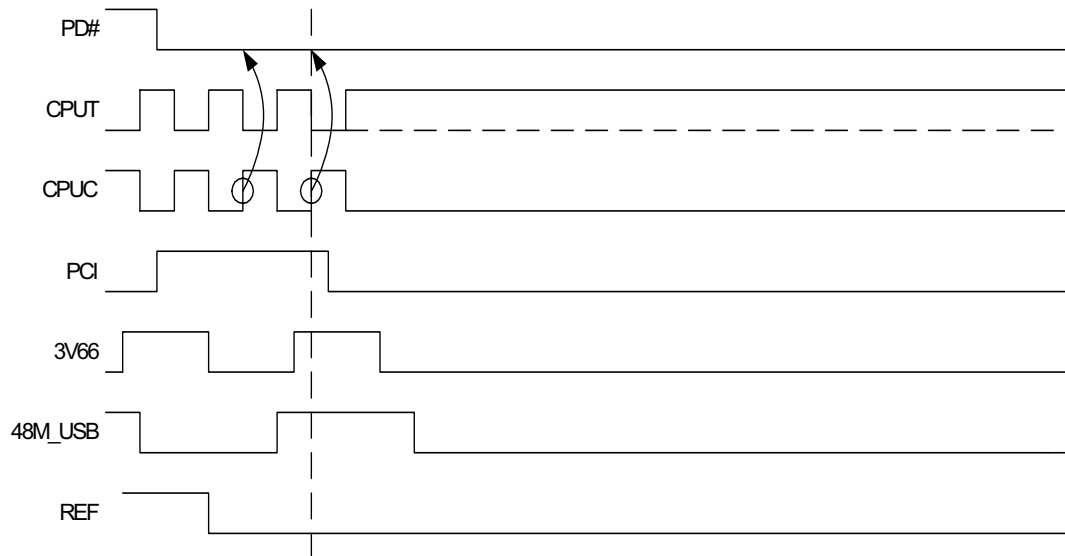
**PD# (Power-down) Clarification**

The PD# (Power-down) pin is used to shut off ALL clocks prior to shutting off power to the device. PD# is an asynchronous active LOW input. This signal is synchronized internally to the device powering down the clock synthesizer. PD# is an asynchronous function for powering up the system. When PD# is low, all clocks are driven to a LOW value and held there and the VCO and PLLs are also powered down. All clocks are shut down in a synchronous manner so has not to cause glitches while transitioning to the low 'stopped' state.

**PD# – Assertion**

When PD# is sampled LOW by two consecutive rising edges of the CPUC clock, then on the next HIGH-to-LOW transition of PCIF, the PCIF clock is stopped LOW. On the next HIGH-to-LOW transition of 66Buff, the 66Buff clock is stopped LOW. From this time, each clock will stop LOW on its next HIGH-to-LOW transition, except the CPUT clock. The CPU clocks are held with the CPUT clock pin driven HIGH with a value of  $2 \times I_{\text{ref}}$ , and CPUC undriven. After the last clock has stopped, the rest of the generator will be shut down.

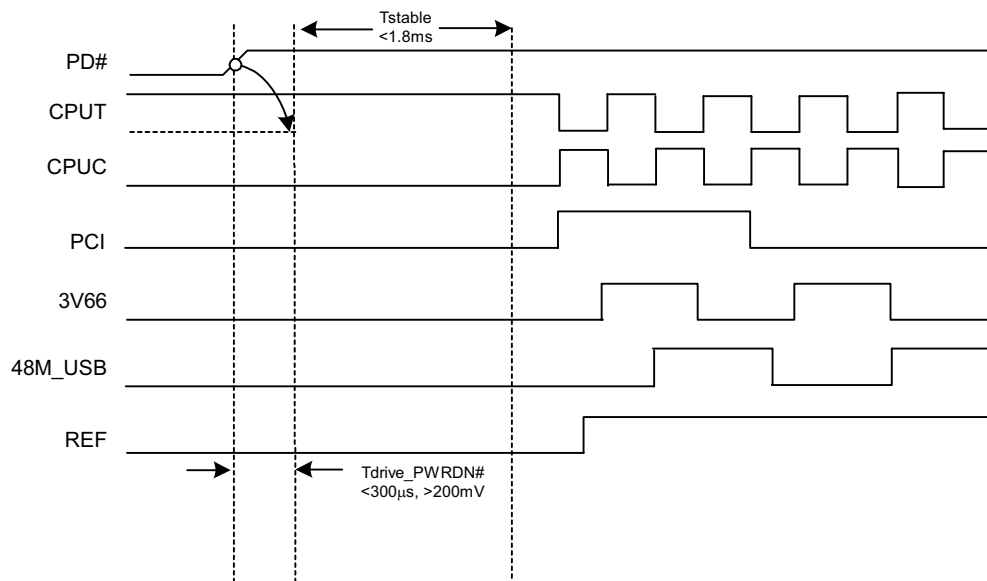

**Figure 5. PCI\_STP# Assertion Waveform**

**Figure 6. PCI\_STP# Deassertion Waveform**



**Figure 7. Power-down Assertion Timing Waveforms**

#### PD# – Deassertion

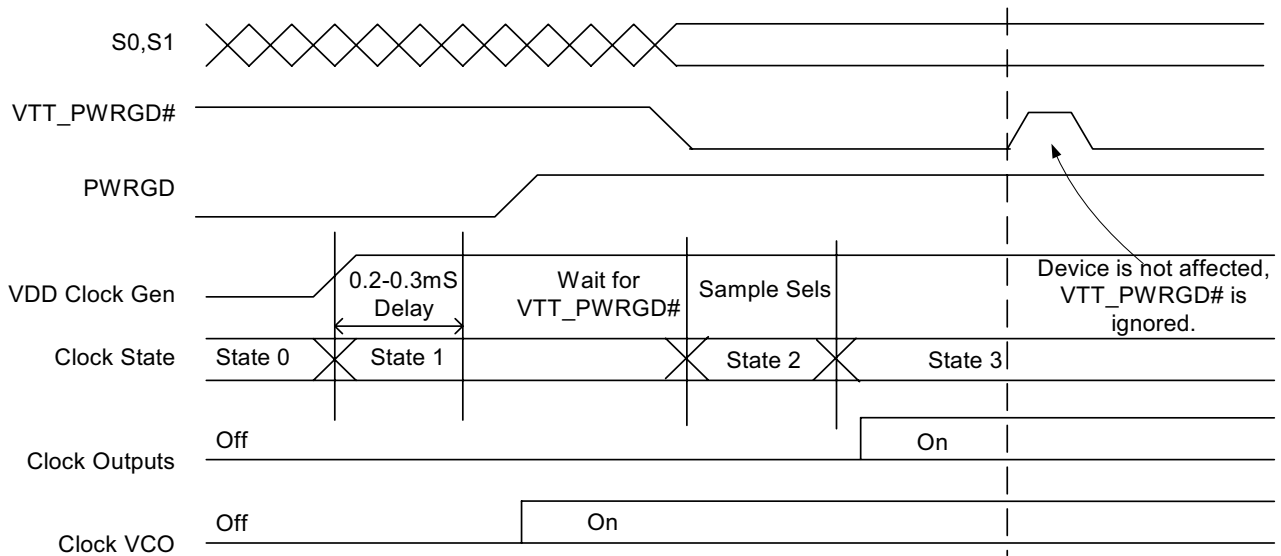
The power-up latency between PD# rising to a valid logic '1' level and the starting of all clocks is less than 1.8 ms.



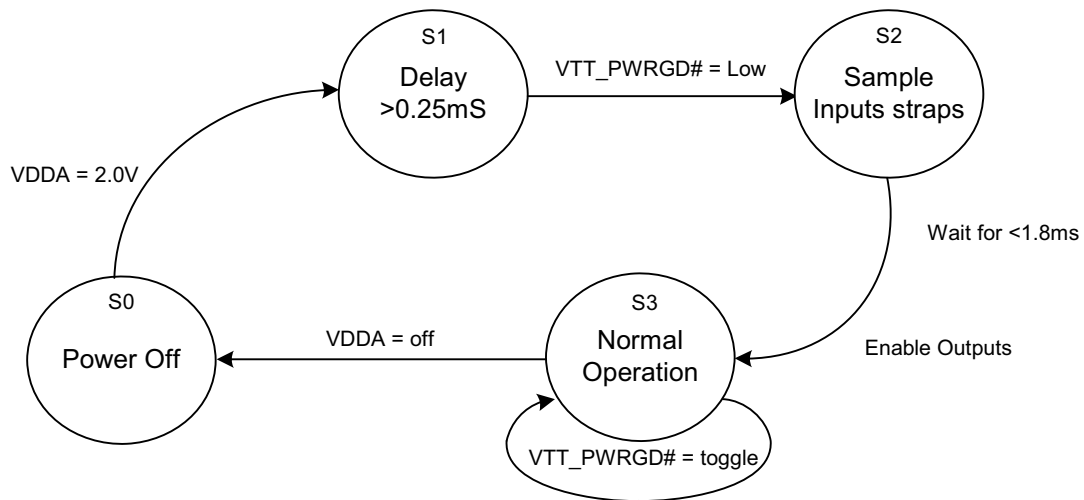
**Figure 8. Power-down Assertion Timing Waveforms**

**Table 10. PD# Functionality**

| PD# | 3V66   | PCI_F  | PCI    | USB/DOT |
|-----|--------|--------|--------|---------|
| 1   | 66 MHz | 33 MHz | 33 MHz | 48 MHz  |
| 0   | Low    | Low    | Low    | Low     |



**Figure 9. VTT\_PWRGD# Timing Diagram**



**Figure 10. Clock Generator Power-up/Run State Diagram**

**Absolute Maximum Conditions**

| Parameter          | Description                       | Condition                  | Min.  | Max.         | Unit |
|--------------------|-----------------------------------|----------------------------|-------|--------------|------|
| $V_{DD}$           | Core Supply Voltage               |                            | -0.5  | 4.6          | V    |
| $V_{DD\_A}$        | Analog Supply Voltage             |                            | -0.5  | 4.6          | V    |
| $V_{IN}$           | Input Voltage                     | Relative to $V_{SS}$       | -0.5  | $V_{DD}+0.5$ | VDC  |
| $T_S$              | Temperature, Storage              | Non-functional             | -65   | 150          | °C   |
| $T_A$              | Temperature, Operating Ambient    | Functional                 | 0     | 70           | °C   |
| $T_J$              | Temperature, Junction             | Functional                 | –     | 150          | °C   |
| ESD <sub>HBM</sub> | ESD Protection (Human Body Model) | MIL-STD-883, Method 3015   | 2000  | –            | V    |
| $\theta_{JC}$      | Dissipation, Junction to Case     | Mil-STD-883E Method 1012.1 | 20.62 |              | °C/W |
| $\theta_{JA}$      | Dissipation, Junction to Ambient  | JEDEC (JESD 51)            | 62.26 |              | °C/W |
| UL-94              | Flammability Rating               | @1/8 in.                   | V-0   |              |      |
| MSL                | Moisture Sensitivity Level        |                            | 1     |              |      |

**DC Electrical Specifications**

| Parameter         | Description                   | Conditions   | Min.           | Max.           | Unit |
|-------------------|-------------------------------|--|----------------|----------------|------|
| $V_{DD}, V_{DDA}$ | 3.3 Operating Voltage         | $3.3V \pm 5\%$   | 3.135          | 3.465          | V    |
| $V_{IL12C}$       | Input Low Voltage             | SDATA, SCLK  | –              | –              | 1.0  |
| $V_{IH12C}$       | Input High Voltage            | SDATA, SCLK  | 2.2            | –              | –    |
| $V_{IL}$          | Input Low Voltage             |  | $V_{SS} - 0.5$ | 0.8            | V    |
| $V_{IH}$          | Input High Voltage            |  | 2.0            | $V_{DD} + 0.5$ | V    |
| $V_{ILS2}$        | S2 Input Low Voltage          | $V_{DD} = 3.3V$  | $V_{SS} - 0.5$ | 0.7            | V    |
| $V_{IMS2}$        | S2 Input Mid Voltage          | $V_{DD} = 3.3V$  | 1.2            | 1.6            | V    |
| $V_{IHS2}$        | S2 Input High Voltage         | $V_{DD} = 3.3V$  | 2.0            | $V_{DD} + 0.5$ | V    |
| $I_{IL}$          | Input Leakage Current         | except Pull-ups or Pull downs<br>$0 < V_{IN} < V_{DD}$               | -5             | 5              | μA   |
| $V_{OL}$          | Output Low Voltage            | $I_{OL} = 1 \text{ mA}$  | –              | 0.4            | V    |
| $V_{OH}$          | Output High Voltage           | $I_{OH} = -1 \text{ mA}$   | 2.4            | –              | V    |
| $I_{OZ}$          | High-Impedance Output Current |  | -10            | 10             | μA   |
| $C_{IN}$          | Input Pin Capacitance         |  | 2              | 5              | pF   |
| $C_{OUT}$         | Output Pin Capacitance        |  | 3              | 6              | pF   |
| $L_{IN}$          | Pin Inductance                |  | –              | 7              | nH   |
| $V_{XIH}$         | Xin High Voltage              |  | $0.7V_{DD}$    | $V_{DD}$       | V    |
| $V_{XIL}$         | Xin Low Voltage               |  | 0              | $0.3V_{DD}$    | V    |
| $I_{DD}$          | Dynamic Supply Current        | At 166 MHz and all outputs loaded per Table 11 and Figures 11 and 12 | –              | 280            | mA   |
| $I_{PD}$          | Power-down Supply Current     | PD# Asserted, Byte0 bit 6="1"  | –              | 2.0            | mA   |

**AC Electrical Specifications**

| Parameter      | Description               | Condition                                    | Min.   | Max. | Unit |
|----------------|---------------------------|--|--------|------|------|
| <b>Crystal</b> |                           |  |        |      |      |
| $T_{DC}$       | XIN Duty Cycle            | When driven from external source             | 47.5   | 52.5 | %    |
| $T_{PERIOD}$   | XIN period                | Measured at $V_{DD}/2$                       | 69.841 | 71.0 | ns   |
| $T_R / T_F$    | XIN Rise and Fall Times   | Measured between $0.3V_{DD}$ and $0.7V_{DD}$ | –      | 10.0 | ns   |
| $T_{CCJ}$      | XIN Cycle to Cycle Jitter | When driven from external source             | –      | 500  | ps   |

**AC Electrical Specifications** (continued)

| Parameter                       | Description                                       | Condition                                  | Min.   | Max. | Unit |
|---------------------------------|---|--|--------|------|------|
| <b>CPU at 0.7V</b>              |   |  |        |      |      |
| T <sub>DC</sub>                 | CPUT and CPUC Duty Cycle                          | Measured at VOX                            | 45     | 55   | %    |
| T <sub>PERIOD</sub>             | 100MHz CPUT and CPUC Period                       | Measured at VOX                            | 5.9    | 6.1  | ns   |
| T <sub>PERIOD</sub>             | 133 MHz CPUT and CPUC Period                      | Measured at VOX                            | 9.85   | 10.2 | ns   |
| T <sub>PERIOD</sub>             | 166 MHz CPUT and CPUC Period                      | Measured at VOX                            | 7.35   | 7.65 | ns   |
| T <sub>SKEW</sub>               | Any CPUT/C to CPUT/C Clock Skew                   | See Figure 12                              | –      | 100  | ps   |
| T <sub>CCJ</sub>                | CPUT/C Cycle to Cycle Jitter                      | See Figure 12                              | –      | 255  | ps   |
| T <sub>R</sub> / T <sub>F</sub> | CPUT and CPUC Rise and Fall Times                 | Measured from 0.175 to 0.525               | 175    | 1000 | ps   |
| T <sub>RFM</sub>                | Rise/Fall Matching                                | Fraction of $2x(T_R - T_F)/(T_R + T_F)$    | –      | 20   | %    |
| ΔT <sub>R</sub>                 | Rise Time Variation                               | Measured from 0.175 to 0.525               | –      | 150  | ps   |
| ΔT <sub>F</sub>                 | Fall Time Variation                               | Measured from 0.525 to 0.175               | –      | 150  | ps   |
| V <sub>OX</sub>                 | Crossing Point Voltage at 0.7V Swing              | See Figure 12                              | 280    | 430  | mv   |
| <b>CPU at 1.0V</b>              |   |  |        |      |      |
| T <sub>DC</sub>                 | CPUT and CPUC Duty Cycle                          | Measured at VOX                            | 45     | 55   | %    |
| T <sub>PERIOD</sub>             | 100MHz CPUT and CPUC Period                       | Measured at VOX                            | 5.9    | 6.1  | ns   |
| T <sub>PERIOD</sub>             | 133 MHz CPUT and CPUC Period                      | Measured at VOX                            | 9.85   | 10.2 | ns   |
| T <sub>PERIOD</sub>             | 166 MHz CPUT and CPUC Period                      | Measured at VOX                            | 7.35   | 7.65 | ns   |
| T <sub>SKEW</sub>               | Any CPUT/C to CPUT/C Clock Skew                   | See Figure 11                              | –      | 100  | ps   |
| T <sub>CCJ</sub>                | CPUT/C Cycle to Cycle Jitter                      | See Figure 11                              | –      | 255  | ps   |
| T <sub>R</sub> / T <sub>F</sub> | CPUT and CPUC Rise and Fall Times                 | Measured differentially from –0.35 to 0.35 | 175    | 1000 | ps   |
| V <sub>OX</sub>                 | Crossing Point Voltage at 0.7V Swing              | See Figure 11                              | 510    | 760  | mv   |
| ΔSlew                           | Absolute Single Ended Rise/Fall Waveform Symmetry | Measured from 0.41 to 0.36                 | –      | 325  | ps   |
| <b>3V66</b>                     |   |  |        |      |      |
| T <sub>DC</sub>                 | 3V66 Duty Cycle                                   | Measured at 1.5V                           | 45     | 55   | %    |
| T <sub>PERIOD</sub>             | 3V66 Period                                       | Measured at 1.5V                           | 15.0   | 15.3 | ns   |
| T <sub>HIGH</sub>               | 3V66 High Time                                    | Measured at 2.4V                           | 4.95   | –    | ns   |
| T <sub>LOW</sub>                | 3V66 Low Time                                     | Measured at 0.4V                           | 4.55   | –    | ns   |
| T <sub>R</sub> / T <sub>F</sub> | 3V66 Rise and Fall Times                          | Measured from 0.4V to 2.4V                 | 0.5    | 2.3  | ns   |
| T <sub>SKEW</sub>               | Any 3V66 to Any 3V66 Clock Skew                   | Measured at 1.5V                           | –      | 500  | ps   |
| T <sub>CCJ</sub>                | 3V66 Cycle to Cycle Jitter                        | Measured at 1.5V. See Table 11             | –      | 400  | ps   |
| <b>PCI/PCIF</b>                 |   |  |        |      |      |
| T <sub>DC</sub>                 | PCI /PCI_F Duty Cycle                             | Measure at 1.5V                            | 45     | 55   | %    |
| T <sub>PERIOD</sub>             | PCIF/PCI Period                                   | Measured at 1.5V                           |        | 30   | ns   |
| T <sub>HIGH</sub>               | PCIF and PCI high time                            | Measured at 1.5V                           | 12.0   | –    | ns   |
| T <sub>LOW</sub>                | PCIF and PCI low time                             | Measured at 0.4V                           | 12.0   | –    | ns   |
| T <sub>R</sub> / T <sub>F</sub> | PCIF and PCI rise and fall times                  | Measured at 0.4V to 2.4V                   | 0.5    | 2.3  | ns   |
| T <sub>SKEW</sub>               | Any PCI clock to Any PCI clock Skew               | Measured at 1.5V                           | –      | 500  | ps   |
| T <sub>CCJ</sub>                | PCIF and PCI Cycle to Cycle Jitter                | Measured at 1.5V. See Table 11             | –      | 325  | ps   |
| <b>48M_DOT</b>                  |   |  |        |      |      |
| T <sub>DC</sub>                 | Duty Cycle  | Measured at 1.5V                           | 45     | 55   | %    |
| T <sub>PERIOD</sub>             | Period  | Measured at 1.5V                           | 20.837 |      | ns   |
| T <sub>R</sub> / T <sub>F</sub> | Rise and Fall Times                               | Measured at 0.4 to 2.4V                    | 0.5    | 1.0  | ns   |
| T <sub>CCJ</sub>                | REF Cycle to Cycle Jitter                         | Measured at 1.5V. See Table 11             | –      | 350  | ps   |

**AC Electrical Specifications** (continued)

| Parameter                          | Description                        | Condition                             | Min.    | Max.    | Unit |
|------------------------------------|------------------------------------|---------------------------------------|---------|---------|------|
| <b>48M_USB</b>                     |                                    |                                       |         |         |      |
| T <sub>DC</sub>                    | Duty Cycle                         | Measured at 1.5V                      | 45      | 55      | %    |
| T <sub>PERIOD</sub>                | Period                             | Measured at 1.5V                      | 20.8299 | 20.8333 | ns   |
| T <sub>R</sub> / T <sub>F</sub>    | Rise and Fall Times                | Measured at 0.4 to 2.4V               | 1.0     | 2.0     | ns   |
| T <sub>CCJ</sub>                   | Cycle to Cycle Jitter              | Measured at 1.5V. See <i>Table 11</i> | –       | 350     | ps   |
| <b>REF</b>                         |                                    |                                       |         |         |      |
| T <sub>DC</sub>                    | REF Duty Cycle                     | Measured at 1.5V                      | 45      | 55      | %    |
| T <sub>PERIOD</sub>                | REF Period                         | Measured at 1.5V                      | 69.84   | 71.0    | ns   |
| T <sub>R</sub> / T <sub>F</sub>    | REF Rise and Fall Times            | Measured at 0.4 to 2.4V               | 0.5     | 2.0     | V/ns |
| T <sub>CCJ</sub>                   | REF Cycle to Cycle Jitter          | Measured at 1.5V. See <i>Table 11</i> | –       | 1000    | ps   |
| <b>ENABLE/DISABLE and SETUP</b>    |                                    |                                       |         |         |      |
| T <sub>PZL</sub> /T <sub>PZH</sub> | Output Enable Delay (all outputs)  |                                       | 1.0     | 10.0    | ns   |
| T <sub>PLZ</sub> /T <sub>PHZ</sub> | Output Disable Delay (all outputs) |                                       | 1.0     | 10.0    | ns   |
| T <sub>STABLE</sub>                | Clock Stabilization from Power-up  |                                       | –       | 3.0     | ms   |
| T <sub>SS</sub>                    | Stopclock Setup Time               |                                       | 10.0    | –       | ns   |
| T <sub>SH</sub>                    | Stopclock Hold Time                |                                       | 0       | –       | ns   |

**Table 11. Maximum Lumped Capacitive Output Loads**

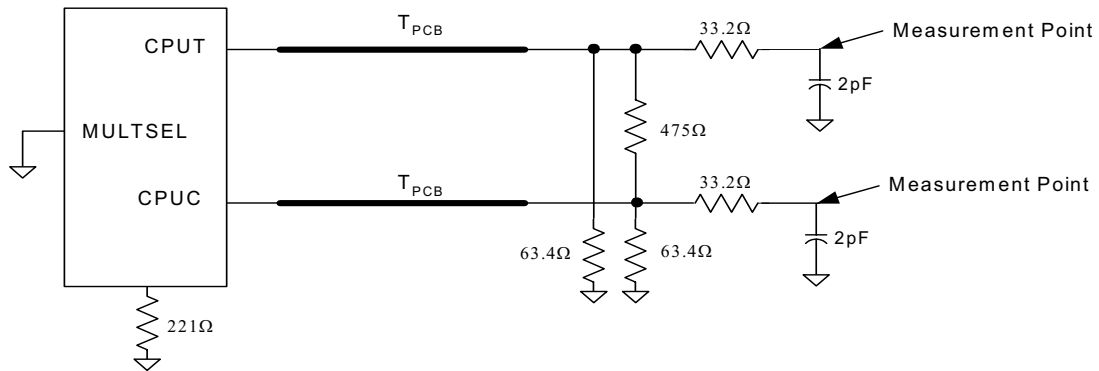
| Clock         | Max Load | Unit |
|---------------|----------|------|
| PCI Clocks    | 30       | pF   |
| 3V66          | 30       | pF   |
| 48M_USB Clock | 20       | pF   |
| 48M_DOT       | 10       | pF   |
| REF Clock     | 50       | pF   |



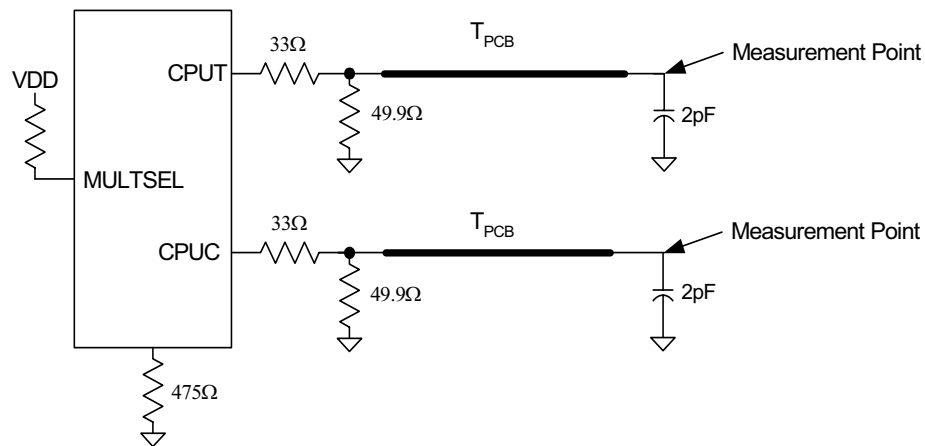
## Test and Measurement Set-up

### For Differential CPU Output Signals

The following diagram shows lumped test load configurations for the differential Host Clock Outputs.

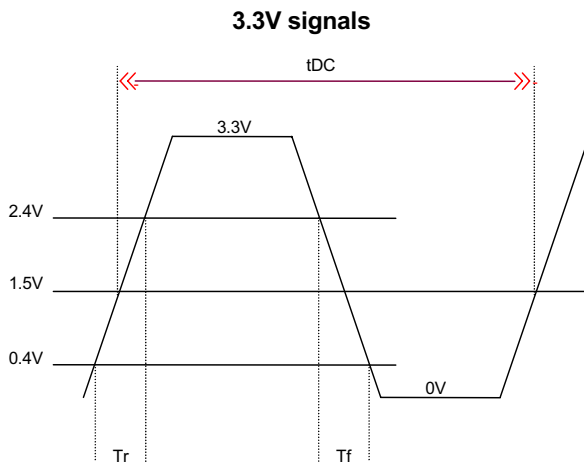
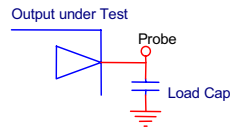


**Figure 11. 1.0V Test Load Termination**



**Figure 12. 0.7V Test Load Termination**

### For Single-Ended Output Signals



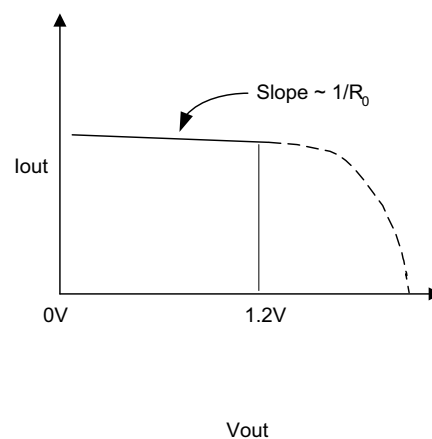
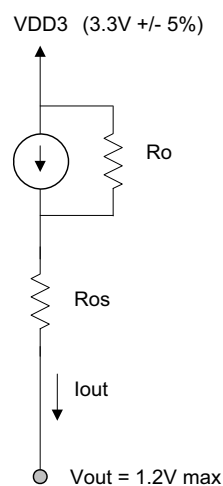
**Figure 13.**

### Buffer Characteristics

#### Current Mode CPU Clock Buffer Characteristics

The current mode output buffer detail and current reference circuit details are contained in the previous table of this data sheet. The following parameters are used to specify output buffer characteristics:

1. Output impedance of the current mode buffer circuit –  $R_o$  (see Figure 14).
2. Minimum and maximum required voltage operation range of the circuit –  $V_{op}$  (see Figure 14).
3. Series resistance in the buffer circuit –  $R_{os}$  (see Figure 14).
4. Current accuracy at given configuration into nominal test load for given configuration.



**Figure 14.**

**Table 12. Host Clock (HCSL) Buffer Characteristics**

| Characteristic | Minimum                 | Maximum |
|----------------|-------------------------|---------|
| Ro             | 3000 Ohms (recommended) | N/A     |
| Ros            |                         |         |
| Vout           | N/A                     | 1.2V    |

Iout is selectable depending on implementation. The parameters above apply to all configurations. Vout is the voltage at the pin of the device.

The various output current configurations are shown in the host swing select functions table. For all configurations, the deviation from the expected output current is  $\pm 7\%$  as shown in the current accuracy table.

**Table 13. CPU Clock Current Select Function**

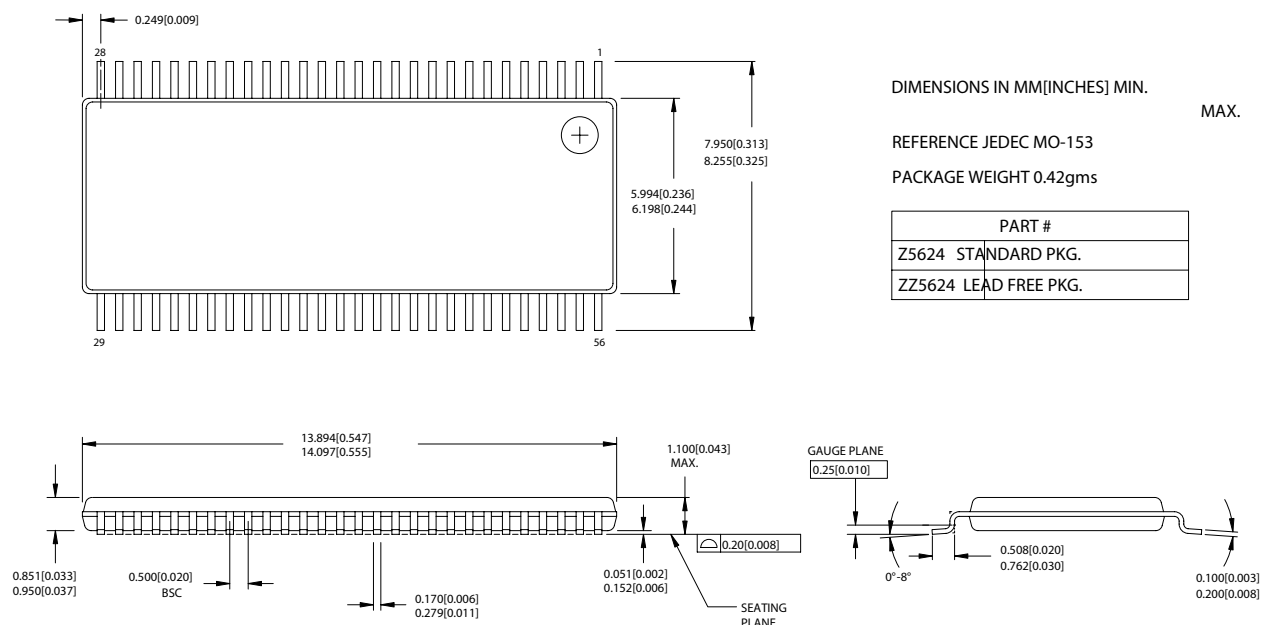
| Mult0 | Board Target Trace/Term Z | Reference R, Iref – Vdd (3*Rr) | Output Current | Voh @ Z   |
|-------|---------------------------|--------------------------------|----------------|-----------|
| 0     | 50 Ohms                   | Rr = 221 1%, Iref = 5.00mA     | Ioh = 4*Iref   | 1.0V @ 50 |
| 1     | 50 Ohms                   | Rr = 475 1%, Iref = 2.32mA     | Ioh = 6*Iref   | 0.7V @ 50 |

## Ordering Information

| Part Number | Package Type                 | Product Flow           |
|-------------|------------------------------|------------------------|
| CY28408ZC   | 56-Pin TSSOP                 | Commercial, 0° to 70°C |
| CY28408ZCT  | 56-Pin TSSOP - Tape and Reel | Commercial, 0° to 70°C |

## Package Drawings and Dimensions

### 56-Lead Thin Shrunk Small Outline Package, Type II (6 mm x 12 mm) Z56



While SLI has reviewed all information herein for accuracy and reliability, Spectra Linear Inc. assumes no responsibility for the use of any circuitry or for the infringement of any patents or other rights of third parties which would result from each use. This product is intended for use in normal commercial applications and is not warranted nor is it intended for use in life support, critical medical instruments, or any other application requiring extended temperature range, high reliability, or any other extraordinary environmental requirements unless pursuant to additional processing by Spectra Linear Inc., and expressed written agreement by Spectra Linear Inc. Spectra Linear Inc. reserves the right to change any circuitry or specification without notice.



**Стандарт  
Электрон  
Связь**

Мы молодая и активно развивающаяся компания в области поставок электронных компонентов. Мы поставляем электронные компоненты отечественного и импортного производства напрямую от производителей и с крупнейших складов мира.

Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию .

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России , а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

Минимальные сроки поставки, гибкие цены, неограниченный ассортимент и индивидуальный подход к клиентам являются основой для выстраивания долгосрочного и эффективного сотрудничества с предприятиями радиоэлектронной промышленности, предприятиями ВПК и научно-исследовательскими институтами России.

С нами вы становитесь еще успешнее!

**Наши контакты:**

**Телефон:** +7 812 627 14 35

**Электронная почта:** [sales@st-electron.ru](mailto:sales@st-electron.ru)

**Адрес:** 198099, Санкт-Петербург,  
Промышленная ул, дом № 19, литера Н,  
помещение 100-Н Офис 331