

# MC74VHCT74A

## Dual D-Type Flip-Flop with Set and Reset

The MC74VHCT74A is an advanced high speed CMOS D-type flip-flop fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The signal level applied to the D input is transferred to Q output during the positive going transition of the Clock pulse.

Reset ( $\overline{RD}$ ) and Set ( $\overline{SD}$ ) are independent of the Clock (CP) and are accomplished by setting the appropriate input Low.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3 V to 5.0 V, because it has full 5.0 V CMOS level output swings.

The VHCT74A input structures provide protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. The output structures also provide protection when  $V_{CC} = 0$  V. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

### Features

- High Speed:  $f_{max} = 60$  MHz (Typ) at  $V_{CC} = 5.0$  V
- Low Power Dissipation:  $I_{CC} = 2$   $\mu$ A (Max) at  $T_A = 25^\circ$ C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 4.5 V to 5.5 V Operating Range
- Low Noise:  $V_{OLP} = 0.8$  V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: 128 FETs or 32 Equivalent Gates
- Pb-Free Packages are Available

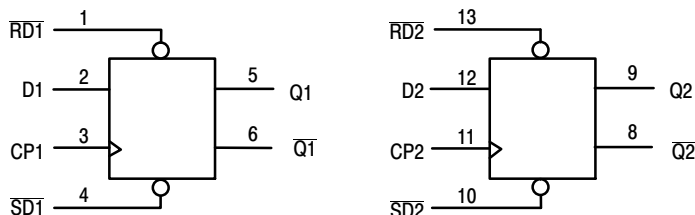


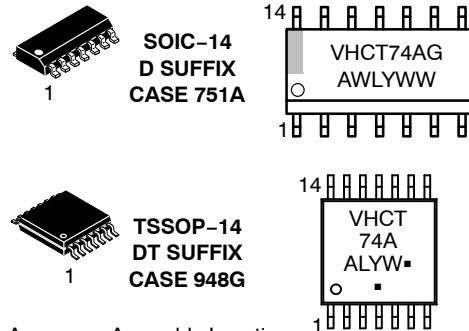
Figure 2. Logic Diagram



ON Semiconductor®

<http://onsemi.com>

### MARKING DIAGRAMS



A = Assembly Location  
 WL, L = Wafer Lot  
 Y = Year  
 WW, W = Work Week  
 G or  $\bullet$  = Pb-Free Package  
 (Note: Microdot may be in either location)

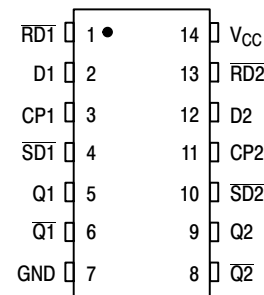


Figure 1. Pin Assignment

### FUNCTION TABLE

Inputs				Outputs	
SD	RD	CP	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↗	H	H	L
H	H	↘	L	L	H
H	H	L	X	No Change	No Change
H	H	H	X	No Change	No Change
H	H	↔	X	No Change	No Change

\*Both outputs will remain high as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

### ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

# MC74VHCT74A

## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage	-0.5 to + 7.0	V
$V_{in}$	DC Input Voltage	-0.5 to + 7.0	V
$V_{out}$	DC Output Voltage $V_{CC} = 0$ High or Low State	-0.5 to + 7.0 -0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	Input Diode Current	-20	mA
$I_{OK}$	Output Diode Current ( $V_{OUT} < GND$ ; $V_{OUT} > V_{CC}$ )	$\pm 20$	mA
$I_{out}$	DC Output Current, per Pin	$\pm 25$	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 50$	mA
$P_D$	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
$T_{stg}$	Storage Temperature	-65 to + 150	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Derating - SOIC Packages: - 7 mW/°C from 65° to 125°C  
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	DC Supply Voltage	4.5	5.5	V
$V_{in}$	DC Input Voltage	0	5.5	V
$V_{out}$	DC Output Voltage $V_{CC} = 0$ High or Low State	0 0	5.5 $V_{CC}$	V
$T_A$	Operating Temperature	-55	+ 125	°C
$t_r, t_f$	Input Rise and Fall Time $V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$	0	20	ns/V

## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	$V_{CC}$ V	$T_A = 25^\circ\text{C}$			$T_A = -55 \text{ to } 125^\circ\text{C}$		Unit
				Min	Typ	Max	Min	Max	
$V_{IH}$	Minimum High-Level Input Voltage		4.5 to 5.5	2.0			2.0		V
$V_{IL}$	Maximum Low-Level Input Voltage		4.5 to 5.5			0.8		0.8	V
$V_{OH}$	Minimum High-Level Output Voltage $V_{in} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50 \mu\text{A}$	4.5	4.4	4.5		4.4		V
		$I_{OH} = -8 \text{ mA}$	4.5	3.94			3.80		V
$V_{OL}$	Maximum Low-Level Output Voltage $V_{in} = V_{IH}$ or $V_{IL}$	$I_{OL} = 50 \mu\text{A}$	4.5		0.0	0.1		0.1	V
		$I_{OL} = 8 \text{ mA}$	4.5			0.36		0.44	V
$I_{in}$	Maximum Input Leakage Current	$V_{in} = 5.5 \text{ V}$ or GND	0 to 5.5			$\pm 0.1$		$\pm 1.0$	$\mu\text{A}$
$I_{CC}$	Maximum Quiescent Supply Current	$V_{in} = V_{CC}$ or GND	5.5			2.0		20.0	$\mu\text{A}$
$I_{CCT}$	Quiescent Supply Current	Per Input: $V_{IN} = 3.4 \text{ V}$ Other Input: $V_{CC}$ or GND	5.5			1.35		1.50	mA
$I_{OPD}$	Output Leakage Current	$V_{OUT} = 5.5 \text{ V}$	0			0.5		5.0	$\mu\text{A}$

# MC74VHCT74A

## AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0\text{ns}$ )

Symbol	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$			$T_A = -55 \text{ to } 125^\circ\text{C}$		Unit
			Min	Typ	Max	Min	Max	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, CP to Q or $\bar{Q}$	$V_{CC} = 5.0 \pm 0.5\text{V}$ $C_L = 15 \text{ pF}$ $C_L = 50 \text{ pF}$		5.8 6.3	7.8 8.8	1.0 1.0	9.0 10.0	ns
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, $\bar{SD}$ or $\bar{RD}$ to Q or $\bar{Q}$	$V_{CC} = 5.0 \pm 0.5\text{V}$ $C_L = 15 \text{ pF}$ $C_L = 50 \text{ pF}$		7.6 8.1	10.4 11.4	1.0 1.0	12.0 13.0	ns
$f_{max}$	Maximum Clock Frequency (50% Duty Cycle)	$V_{CC} = 5.0 \pm 0.5\text{V}$ $C_L = 15 \text{ pF}$ $C_L = 50 \text{ pF}$	100 80	160 140		80 65		MHz
$C_{in}$	Maximum Input Capacitance			4	10		10	pF

Symbol	Parameter	Typical @ $25^\circ\text{C}$ , $V_{CC} = 5.0 \text{ V}$		Unit
		24		
$C_{PD}$	Power Dissipation Capacitance (Note 1)			pF

1.  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:  $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}/2$  (per flip-flop).  $C_{PD}$  is used to determine the no-load dynamic power consumption;  $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$ .

## TIMING REQUIREMENTS (Input $t_r = t_f = 3.0 \text{ ns}$ )

Symbol	Parameter	$V_{CC}$ V	Guaranteed Limit		Unit
			$T_A = 25^\circ\text{C}$	$T_A = -55 \text{ to } 125^\circ\text{C}$	
$t_w$	Minimum Pulse Width, CP	$5.0 \pm 0.5$	5.0	5.0	ns
$t_w$	Minimum Pulse Width, $\bar{RD}$ or $\bar{SD}$	$5.0 \pm 0.5$	5.0	5.0	ns
$t_{su}$	Minimum Setup Time, D to CP	$5.0 \pm 0.5$	5.0	5.0	ns
$t_h$	Minimum Hold Time, D to CP	$5.0 \pm 0.5$	0.0	0.0	ns
$t_{rec}$	Minimum Recovery Time, $\bar{SD}$ or $\bar{RD}$ to CP	$5.0 \pm 0.5$	3.5	3.5	ns

## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
MC74VHCT74AD	SOIC-14	55 Units / Rail
MC74VHCT74ADR2	SOIC-14	2500 / Tape & Reel
MC74VHCT74ADR2G	SOIC-14 (Pb-Free)	2500 / Tape & Reel
MC74VHCT74ADT	TSSOP-14*	96 Units / Rail
MC74VHCT74ADTR2	TSSOP-14*	2500 / Tape & Reel
MC74VHCT74ADTR2G	TSSOP-14*	2500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*This package is inherently Pb-Free.

# MC74VHCT74A

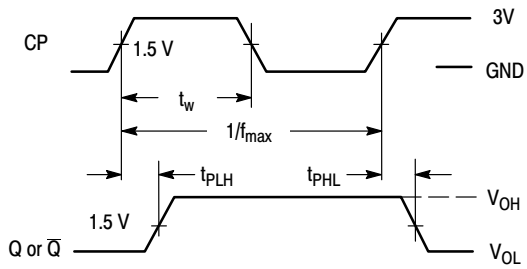


Figure 3. Switching Waveform

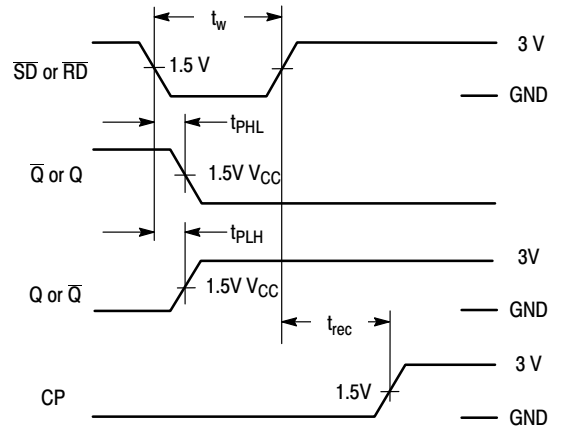


Figure 4. Switching Waveform

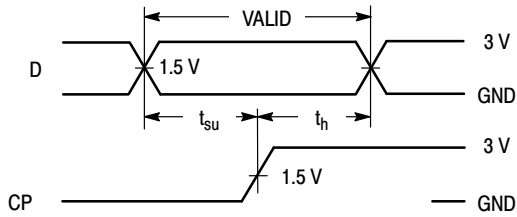
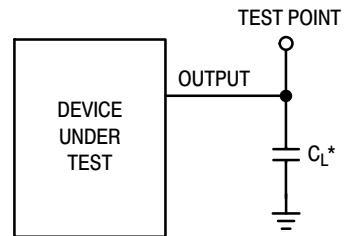


Figure 5. Switching Waveform



\*Includes all probe and jig capacitance

Figure 6. Switching Waveform

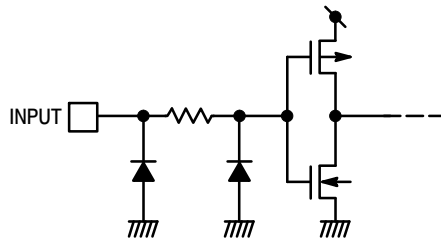
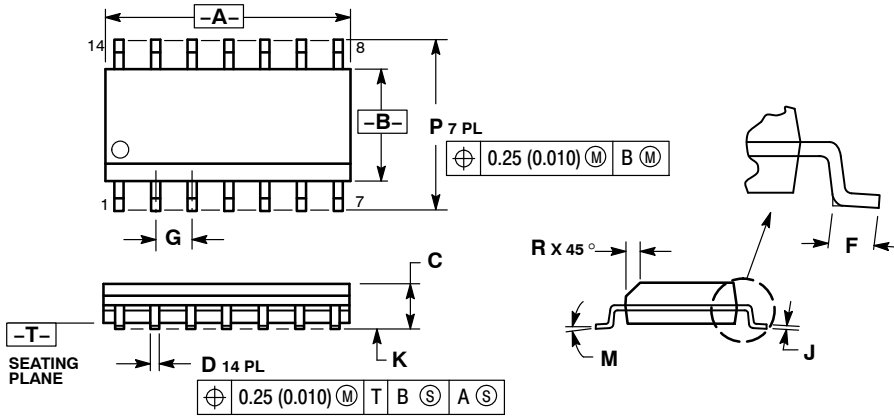


Figure 7. Input Equivalent Circuit

# MC74VHCT74A

## PACKAGE DIMENSIONS

SOIC-14  
D SUFFIX  
CASE 751A-03  
ISSUE G



**NOTES:**

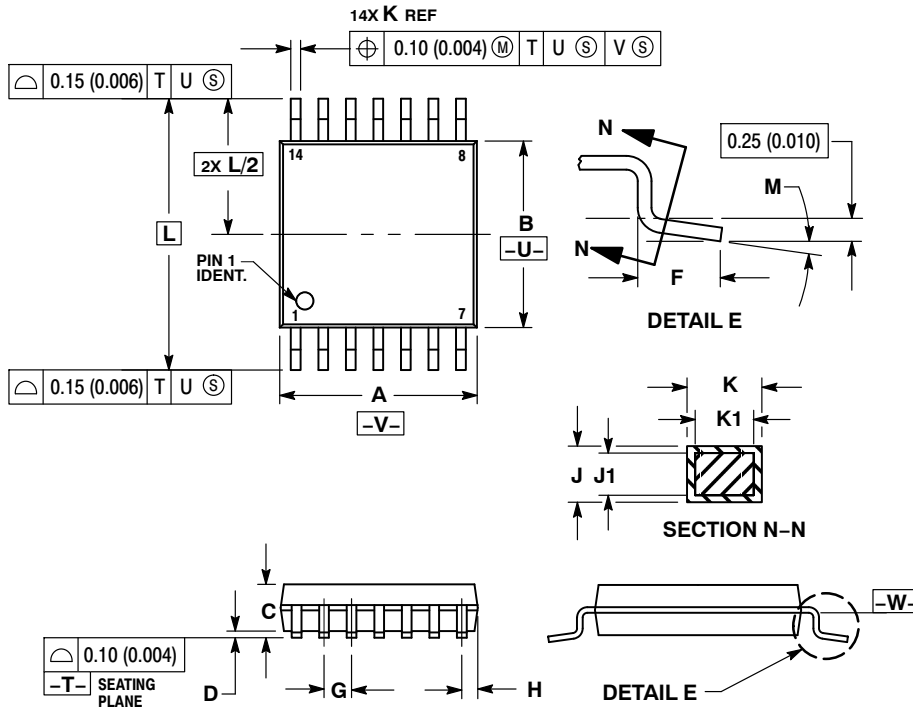
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

# MC74VHCT74A

## PACKAGE DIMENSIONS

TSSOP-14  
DT SUFFIX  
CASE 948G-01  
ISSUE A



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -V-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.80	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5773-3850

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>  
For additional information, please contact your local Sales Representative



## Стандарт Электрон Связь

Мы молодая и активно развивающаяся компания в области поставок электронных компонентов. Мы поставляем электронные компоненты отечественного и импортного производства напрямую от производителей и с крупнейших складов мира.

Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию .

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России , а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

Минимальные сроки поставки, гибкие цены, неограниченный ассортимент и индивидуальный подход к клиентам являются основой для выстраивания долгосрочного и эффективного сотрудничества с предприятиями радиоэлектронной промышленности, предприятиями ВПК и научно-исследовательскими институтами России.

С нами вы становитесь еще успешнее!

### Наши контакты:

**Телефон:** +7 812 627 14 35

**Электронная почта:** [sales@st-electron.ru](mailto:sales@st-electron.ru)

**Адрес:** 198099, Санкт-Петербург,  
Промышленная ул, дом № 19, литера Н,  
помещение 100-Н Офис 331