

International IR Rectifier

- Logic Level Gate Drive
- Ultra Low On-Resistance
- Surface Mount (IRLR3410)
- Straight Lead (IRLU3410)
- Advanced Process Technology
- Fast Switching
- Fully Avalanche Rated
- Lead-Free

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

The D-PAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.

Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	17	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	12	
I_{DM}	Pulsed Drain Current ①⑤	60	
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation	79	W
	Linear Derating Factor	0.53	W/°C
V_{GS}	Gate-to-Source Voltage	± 16	V
E_{AS}	Single Pulse Avalanche Energy②③	150	mJ
I_{AR}	Avalanche Current①⑤	9.0	A
E_{AR}	Repetitive Avalanche Energy①⑤	7.9	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

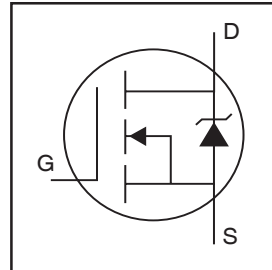
	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.9	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount) **	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

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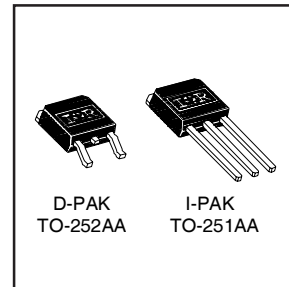
PD - 95087A

IRLR/U3410PbF

HEXFET® Power MOSFET



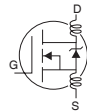
$V_{DSS} = 100\text{V}$
$R_{DS(on)} = 0.105\Omega$
$I_D = 17\text{A}$



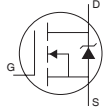
D-PAK
TO-252AA

I-PAK
TO-251AA

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	100	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.122	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.105	W	V _{GS} = 10V, I _D = 10A ④
		—	—	0.125		V _{GS} = 5.0V, I _D = 10A ④
		—	—	0.155		V _{GS} = 4.0V, I _D = 9.0A ④
V _{GS(th)}	Gate Threshold Voltage	1.0	—	2.0	V	V _{DS} = V _{GS} , I _D = 250μA
g _{fs}	Forward Transconductance	7.7	—	—	S	V _{DS} = 25V, I _D = 9.0A⑤
I _{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V _{DS} = 100V, V _{GS} = 0V
		—	—	250		V _{DS} = 80V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 16V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -16V
Q _g	Total Gate Charge	—	—	34	nC	I _D = 9.0A
Q _{gs}	Gate-to-Source Charge	—	—	4.8		V _{DS} = 80V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	20		V _{GS} = 5.0V, See Fig. 6 and 13 ④⑤
t _{d(on)}	Turn-On Delay Time	—	7.2	—	ns	V _{DD} = 50V
t _r	Rise Time	—	53	—		I _D = 9.0A
t _{d(off)}	Turn-Off Delay Time	—	30	—		R _G = 6.0Ω, V _{GS} = 5.0V
t _f	Fall Time	—	26	—		R _D = 5.5Ω, See Fig. 10 ④⑤
L _D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact⑥
L _S	Internal Source Inductance	—	7.5	—		
C _{iss}	Input Capacitance	—	800	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	160	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	90	—		f = 1.0MHz, See Fig. 5⑤

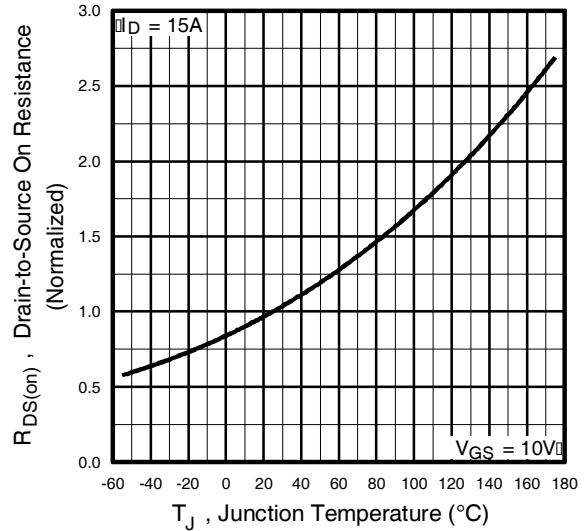
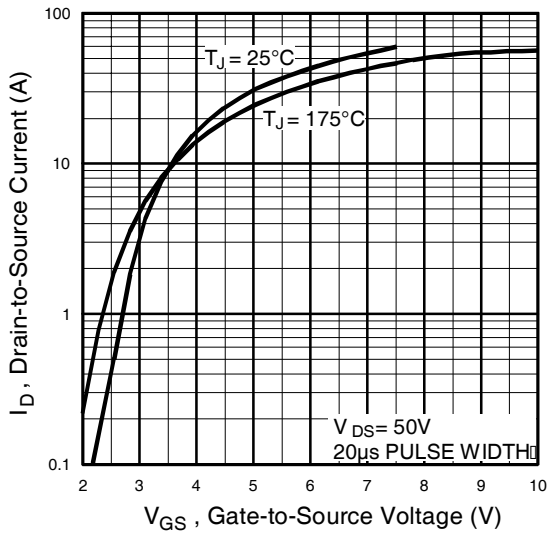
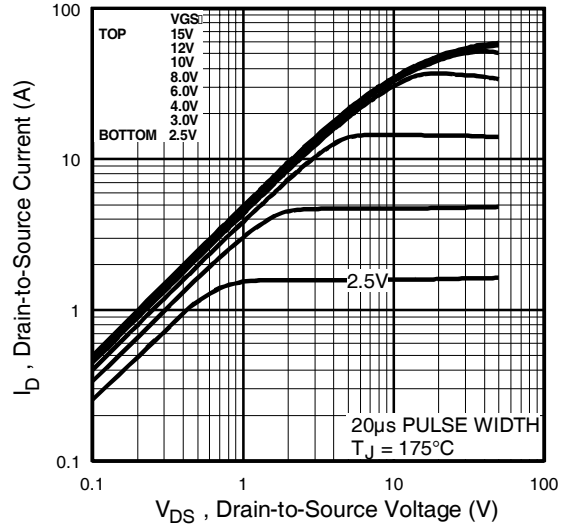
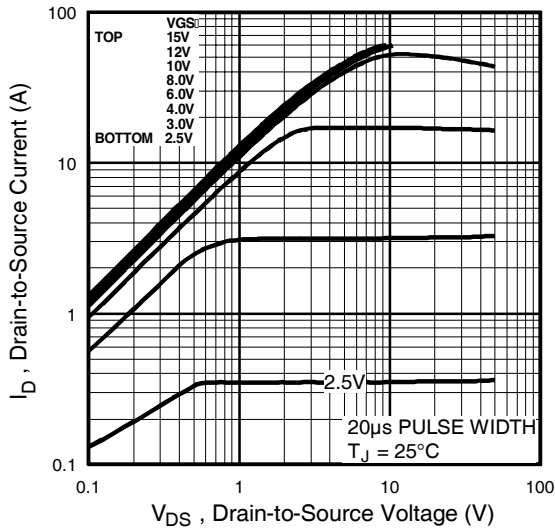
Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	17	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①⑤	—	—	60		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 9.0A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	140	210	ns	T _J = 25°C, I _F = 9.0A
Q _{rr}	Reverse Recovery Charge	—	740	1100	nC	di/dt = 100A/μs ④⑤
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② V_{DD} = 25V, starting T_J = 25°C, L = 3.1mH
R_G = 25Ω, I_{AS} = 9.0A. (See Figure 12)
- ③ I_{SD} ≤ 9.0A, di/dt ≤ 540A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 175°C
- ④ Pulse width ≤ 300μs; duty cycle ≤ 2%
- ⑤ Uses IRL530N data and test conditions
- ⑥ This is applied for I-PAK, L_S of D-PAK is measured between lead and center of die contact

** When mounted on 1" square PCB (FR-4 or G-10 Material) .
For recommended footprint and soldering techniques refer to application note #AN-994



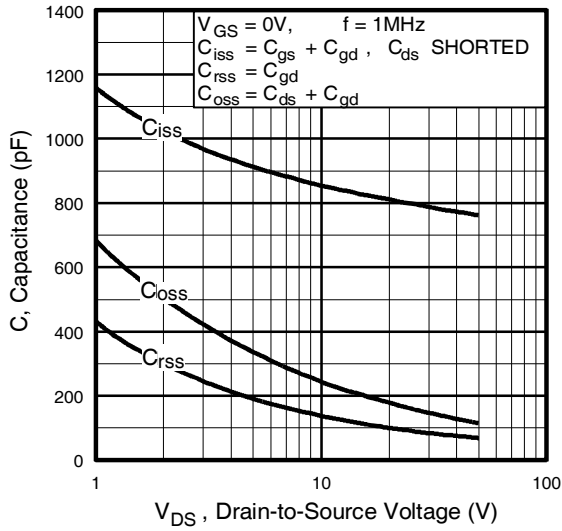


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

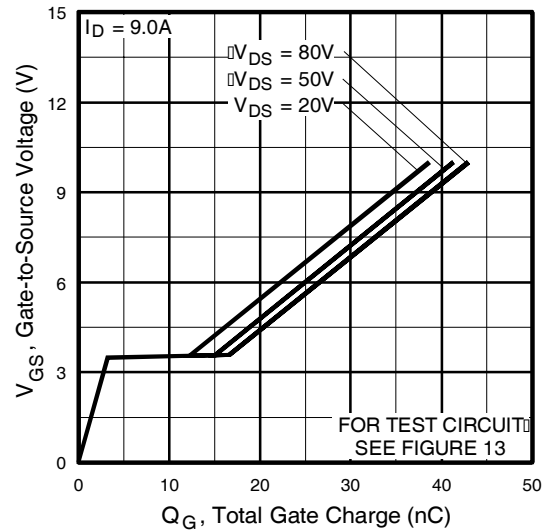


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

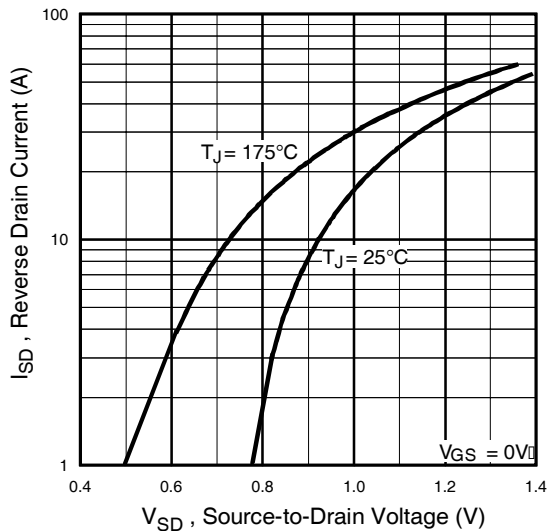


Fig 7. Typical Source-Drain Diode Forward Voltage

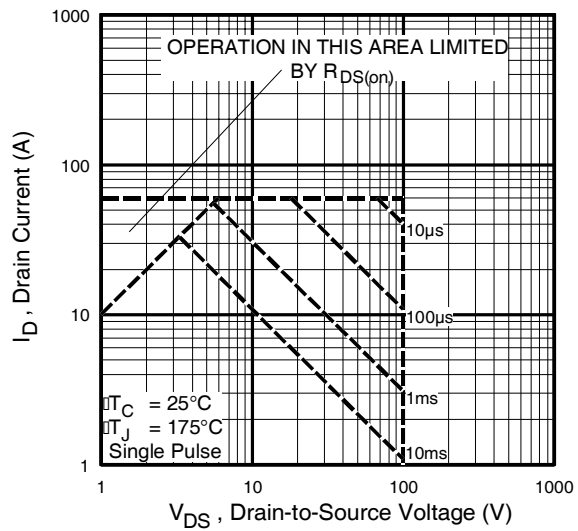


Fig 8. Maximum Safe Operating Area

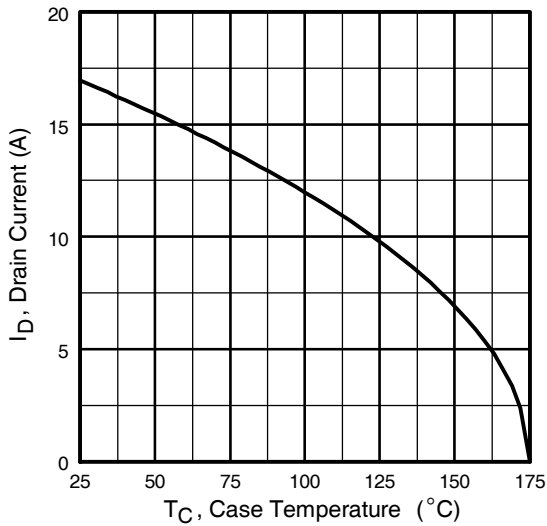


Fig 9. Maximum Drain Current Vs. Case Temperature

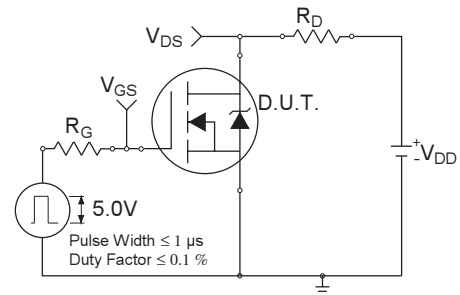


Fig 10a. Switching Time Test Circuit

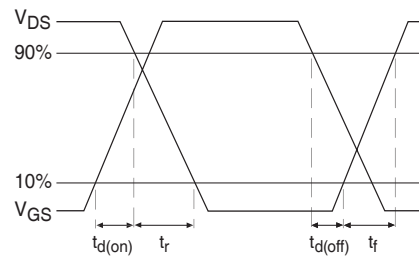


Fig 10b. Switching Time Waveforms

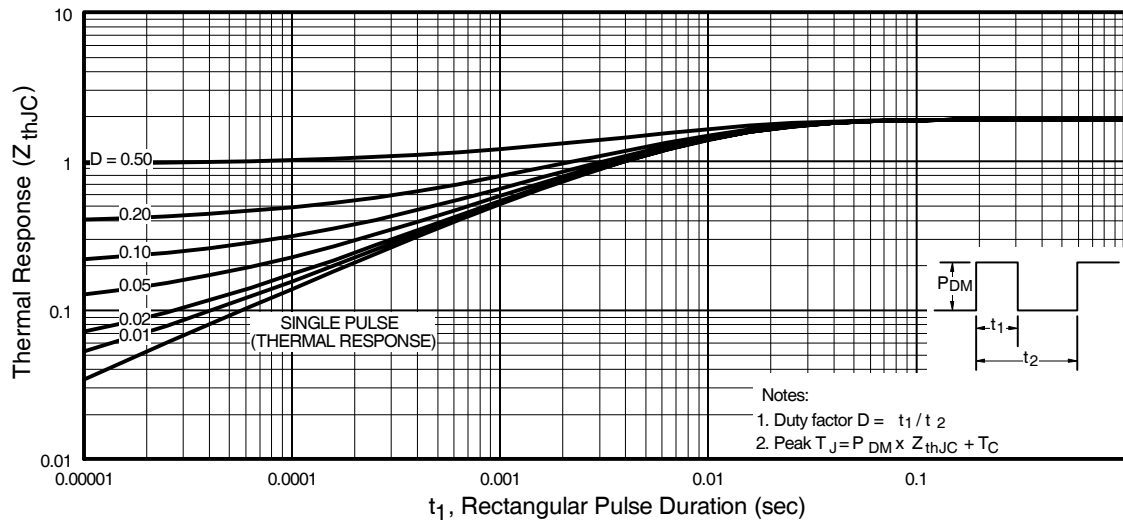


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

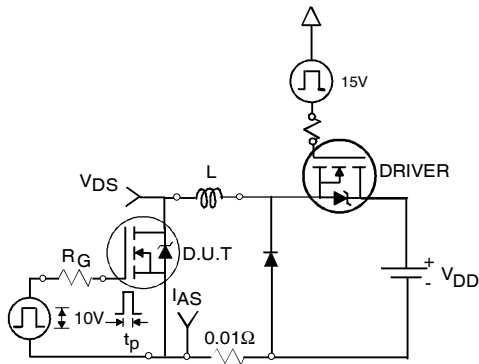


Fig 12a. Unclamped Inductive Test Circuit

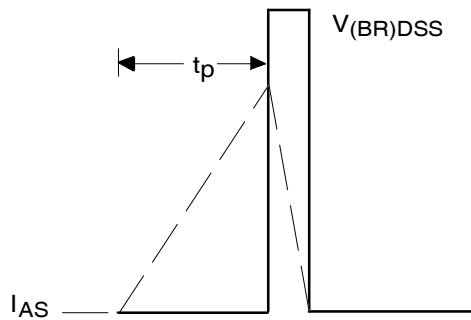


Fig 12b. Unclamped Inductive Waveforms

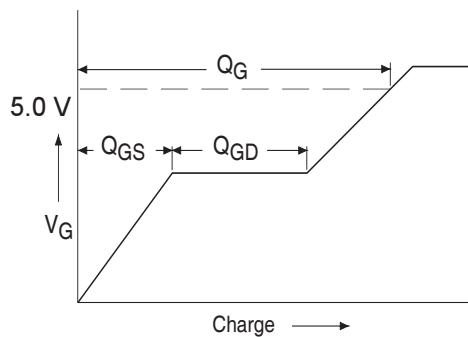


Fig 13a. Basic Gate Charge Waveform

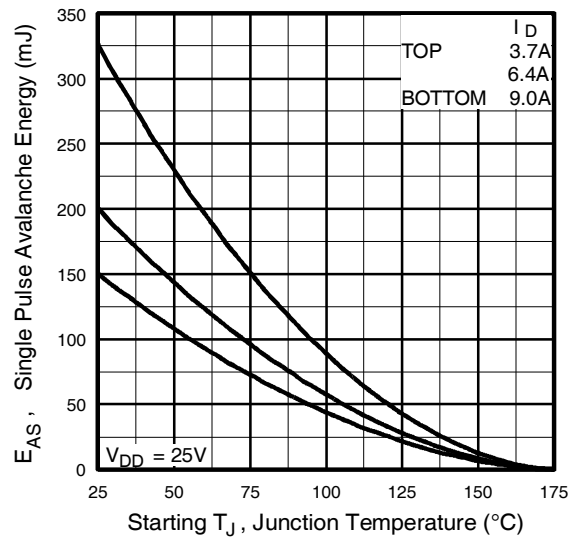


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

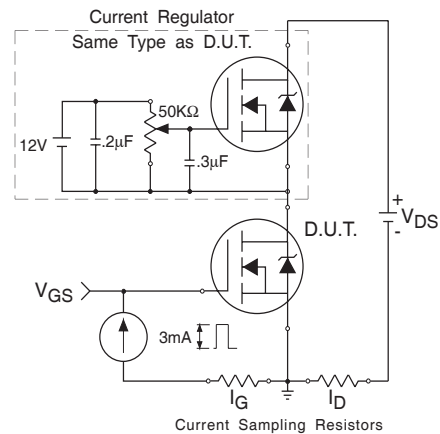
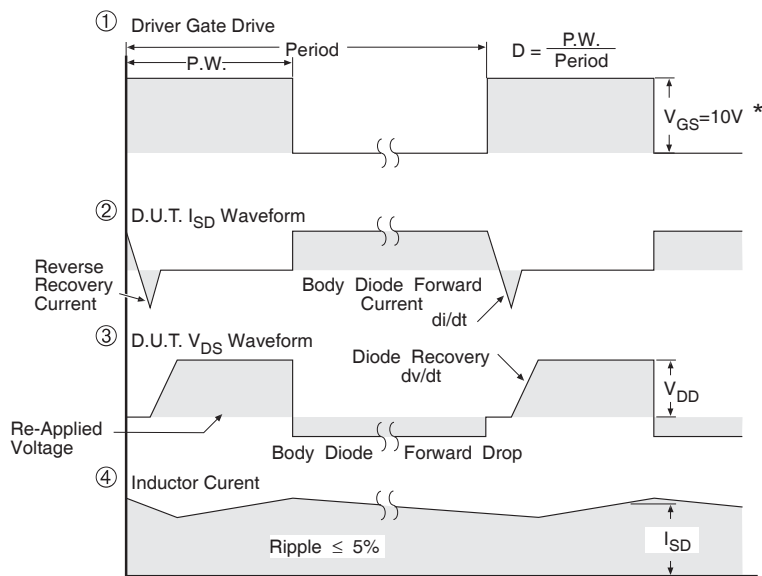
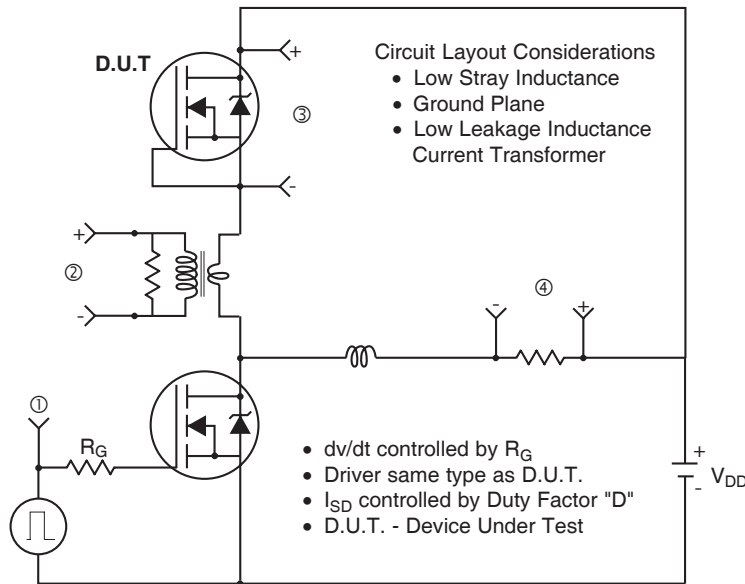


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

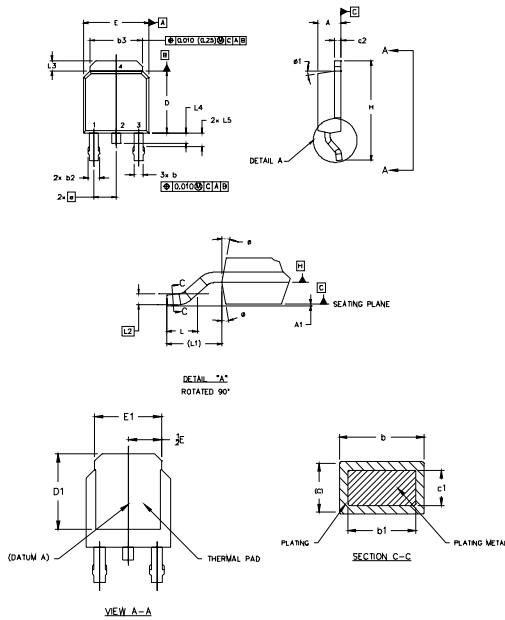
Fig 14. For N-Channel HEXFETS

IRLR/U3410PbF



D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

- 1.0 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
- 2.0 DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
- 3.0 LEAD DIMENSION UNCONTROLLED IN L5.
- 4.0 DIMENSION D1 AND E1 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
- 5.0 SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 [0.127] AND .010 [0.254] FROM THE LEAD TIP.
- 6.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 7.0 OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	Min.	Max.	Min.	Max.	
A	2.18	2.29	.086	.094	
A1	0.13	0.13	.005	.005	
B	0.84	0.99	.033	.039	5
B1	0.84	0.99	.033	0.037	5
B2	0.78	1.14	.030	.045	
B3	4.96	5.46	.195	.215	
C	0.96	0.81	.038	.034	5
C1	0.41	0.36	.016	.014	5
C2	.046	0.89	.018	.035	5
D	3.87	6.22	.152	.245	6
D1	5.21	-	.205	-	4
E	6.25	6.73	.246	.265	6
E1	4.52	-	.178	-	4
F	2.29	-	.090	MSC	
H	8.49	10.41	.334	.410	
L	1.40	1.78	.055	.070	
L1	2.74	MSC	.108	REF	
L2	0.91	MSC	.036	MSC	
L3	0.89	1.27	.035	.050	
L4	1.02	1.02	.040	.040	
L5	1.14	1.52	.045	.060	3
W	0"	10"	0"	10"	
H1	0"	10"	0"	10"	

LEAD ASSIGNMENTS

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE
- 4 - DRAIN

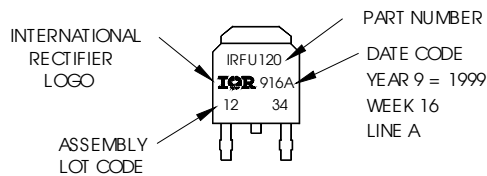
JEDEC GUPACK

- 1 - GATE
- 2 - COLLECTOR
- 3 - EMITTER
- 4 - COLLECTOR

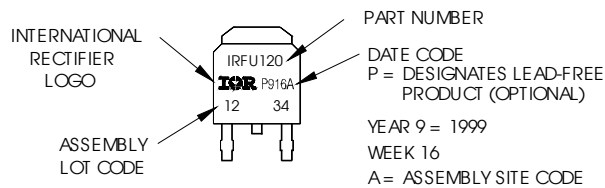
D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 1234
ASSEMBLED ON VVW 16, 1999
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position
indicates "Lead-Free"

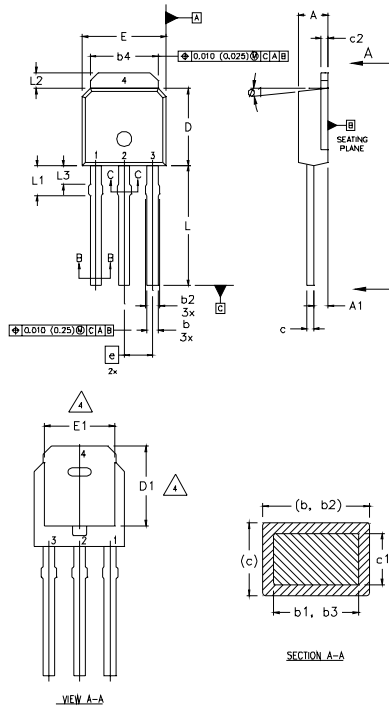


OR



I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



- NOTES:
- 1 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
 - 2 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
 - 3 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
 - 4 THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
 - 5 LEAD DIMENSION UNCONTROLLED IN L3.
 - 6 DIMENSION b1, b3 APPLY TO BASE METAL ONLY.
 - 7 OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA.
 - 8 CONTROLLING DIMENSION : INCHES.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	0.086	.094	
A1	0.89	1.14	0.035	0.045	
b	0.64	0.89	0.025	0.035	
b1	0.64	0.79	0.025	0.031	4
b2	0.76	1.14	0.030	0.045	
b3	0.76	1.04	0.030	0.041	
b4	5.00	5.46	0.195	0.215	4
c	0.46	0.61	0.018	0.024	
c1	0.41	0.56	0.016	0.022	
c2	.046	0.86	0.018	0.035	
D	5.97	6.22	0.235	0.245	3, 4
D1	5.21	-	0.205	-	4
E	6.36	6.73	0.250	0.265	3, 4
E1	4.32	-	0.170	-	4
e	2.29		0.090 BSC		
L	8.89	9.60	0.350	0.380	
L1	1.91	2.29	0.075	0.090	
L2	0.89	1.27	0.035	0.050	4
L3	1.14	1.52	0.045	0.060	5
e1	Ø	15'	Ø	15'	

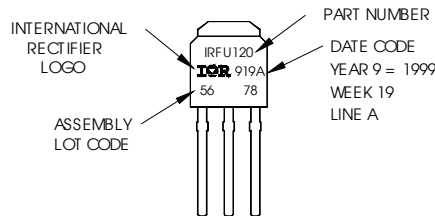
LEAD ASSIGNMENTS

- HEXFET
- 1.- GATE
 - 2.- DRAIN
 - 3.- SOURCE
 - 4.- DRAIN

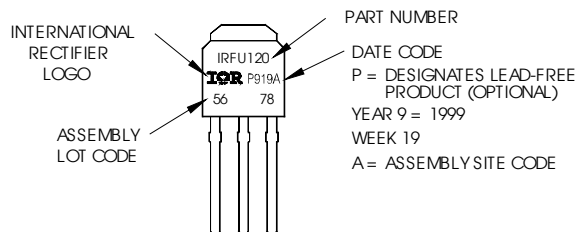
I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120 WITH ASSEMBLY LOT CODE 5678 ASSEMBLED ON WW 19, 1999 IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position indicates "Lead-Free"

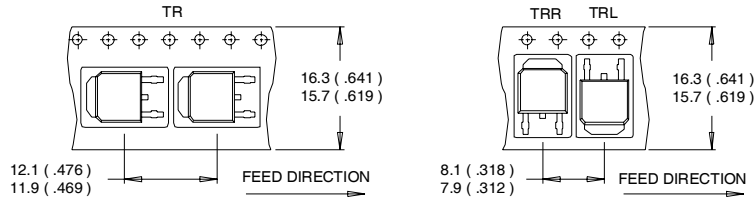


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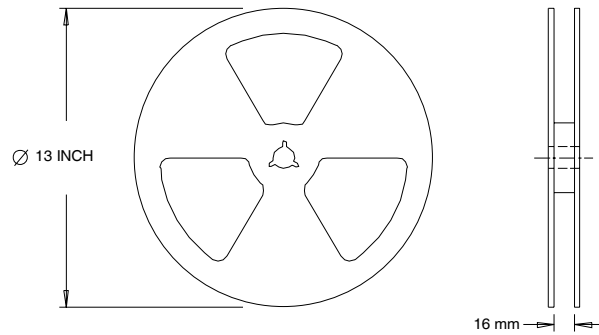


D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



- NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
 2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
 3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



- NOTES :
1. OUTLINE CONFORMS TO EIA-481.

Data and specifications subject to change without notice.

International
IR Rectifier

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Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>



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помещение 100-Н Офис 331