

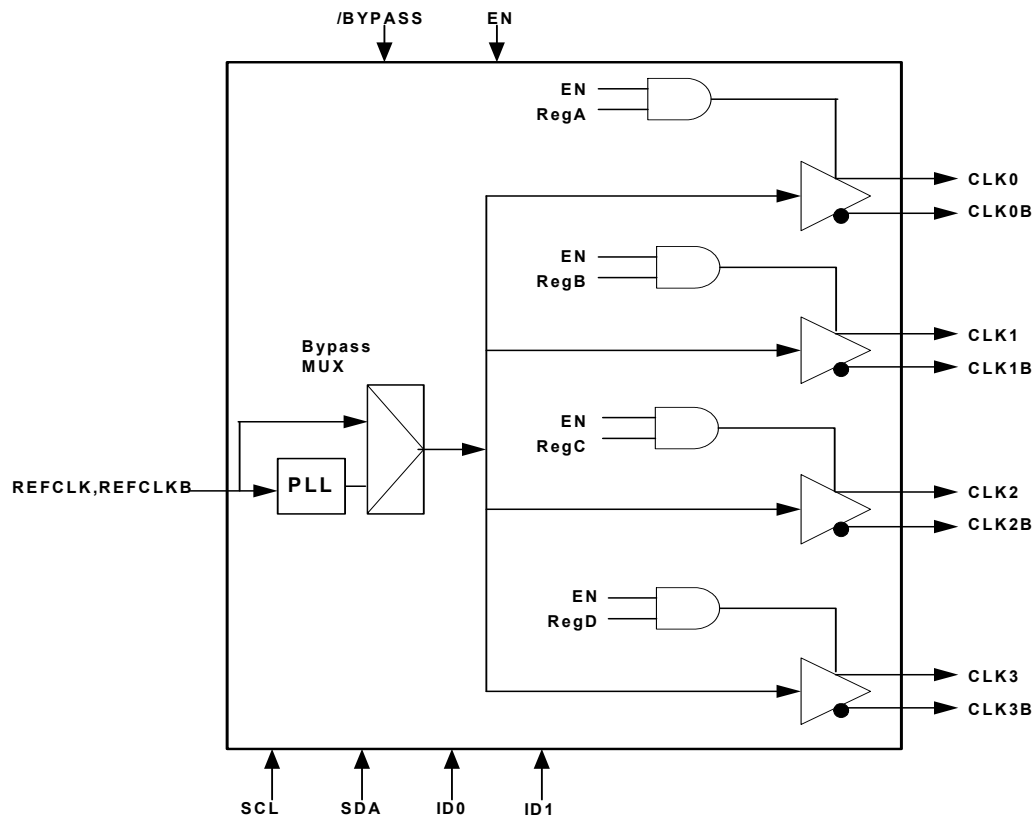
## Features

- Meets Rambus® Extended Data Rate (XDR™) clocking requirements
- 25 ps typical cycle-to-cycle jitter
  - 135 dBc/Hz typical phase noise at 20 MHz offset
- 100 or 133 MHz differential clock input
- 300–800 MHz high speed clock support
- Quad (open drain) differential output drivers
- Supports frequency multipliers: 3, 4, 5, 6, 8, 9/2, 15/2, and 15/4
- Spread Aware™
- 2.5 V operation
- 28-pin TSSOP package

## Functional Description

For a complete list of related documentation, click [here](#).

## Logic Block Diagram

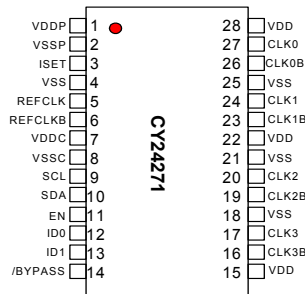


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## Pinouts

Figure 1. 28-pin TSSOP pinout



## Pin Definitions

28-pin TSSOP

| Pin No. | Name    | I/O | Description   |
|---------|---------|-----|---|
| 1       | VDDP    | PWR | 2.5 V power supply for phased lock loop (PLL)           |
| 2       | VSSP    | GND | Ground  |
| 3       | ISET    | I   | Set clock driver current (external resistor)            |
| 4       | VSS     | GND | Ground  |
| 5       | REFCLK  | I   | Reference clock input (connect to clock source)         |
| 6       | REFCLKB | I   | Complement of reference clock (connect to clock source) |
| 7       | VDDC    | PWR | 2.5 V power supply for core                             |
| 8       | VSSC    | GND | Ground  |
| 9       | SCL     | I   | SMBus clock (connect to smbus)                          |
| 10      | SDA     | I   | SMBus data (connect to smbus)                           |
| 11      | EN      | I   | Output Enable (CMOS signal)                             |
| 12      | ID0     | I   | Device ID (CMOS signal)                                 |
| 13      | ID1     | I   | Device ID (CMOS signal)                                 |
| 14      | /BYPASS | I   | REFCLK bypassing PLL (CMOS signal)                      |
| 15      | VDD     | PWR | Power supply for outputs                                |
| 16      | CLK3B   | O   | Complement clock output                                 |
| 17      | CLK3    | O   | Clock output  |
| 18      | VSS     | GND | Ground  |
| 19      | CLK2B   | O   | Complement clock output                                 |
| 20      | CLK2    | O   | Clock output  |
| 21      | VSS     | GND | Ground  |
| 22      | VDD     | PWR | Power supply for outputs                                |
| 23      | CLK1B   | O   | Complement clock output                                 |
| 24      | CLK1    | O   | Clock output  |
| 25      | VSS     | GND | Ground  |

**Pin Definitions** *(continued)*

28-pin TSSOP

| Pin No. | Name  | I/O | Description              |
|---------|-------|-----|--------------------------|
| 26      | CLK0B | O   | Complement clock output  |
| 27      | CLK0  | O   | Clock output             |
| 28      | VDD   | PWR | Power supply for outputs |

**Functional Overview**
**PLL Multiplier**

Table 1 shows the frequency multipliers in the PLL, selectable by programming the SMBus registers MULT0, MULT1, and MULT2. Default multiplier at power up is 4.

**Table 1. PLL Multiplier Selection**

| Register |       |       | Frequency Multiplier | Output Frequency (MHz)                       |  |
|----------|-------|-------|----------------------|--|--|
| MULT2    | MULT1 | MULT0 |                      | REFCLK = 100 MHz <sup>[1]</sup> , REFSEL = 0 | REFCLK = 133 MHz <sup>[1]</sup> , REFSEL = 1 |
| 0        | 0     | 0     | 3                    | 300  | 400  |
| 0        | 0     | 1     | 4                    | 400 <sup>[2]</sup>                           | 533 <sup>[3]</sup>                           |
| 0        | 1     | 0     | 5                    | 500  | 667  |
| 0        | 1     | 1     | 6                    | 600  | 800  |
| 1        | 0     | 0     | 8                    | 800  | 1067 <sup>[3]</sup>                          |
| 1        | 0     | 1     | 9/2                  | 450  | 600  |
| 1        | 1     | 0     | 15/2                 | 750  | 1000 <sup>[3]</sup>                          |
| 1        | 1     | 1     | 15/4                 | 375  | 500  |

**Device ID and SMBus Device Address**

The device ID (ID0 and ID1) is a part of the SMBus device 8-bit address. The least significant bit of the address designates a write or read operation. Table 2 shows the addresses for four CY24271 devices on the same SMBus.

**Table 2. SMBus Device Addresses for CY24271**

| XCG    |           | Hex Address | 8-bit SMBus Device Address Including Operation |   |   |   |   |     |     |          |
|--------|-----------|-------------|--|---|---|---|---|-----|-----|----------|
| Device | Operation |             | Five Most Significant Bits                     |   |   |   |   | ID1 | ID0 | WR# / RD |
| 0      | Write     | D8          | 1  | 1 | 0 | 1 | 1 | 0   | 0   | 0        |
|        | Read      | D9          |  |   |   |   |   | 1   |     |          |
| 1      | Write     | DA          |  |   |   |   |   | 0   | 1   | 0        |
|        | Read      | DB          |  |   |   |   |   | 1   |     |          |
| 2      | Write     | DC          |  |   |   |   |   | 1   | 0   | 0        |
|        | Read      | DD          |  |   |   |   |   | 1   |     |          |
| 3      | Write     | DE          |  |   |   |   |   | 1   | 1   | 0        |
|        | Read      | DF          |  |   |   |   |   | 1   |     |          |

**Notes**

- Output frequencies shown in Table 1 are based on nominal input frequencies of 100 MHz and 133.3 MHz. The PLL multipliers are applicable to spread spectrum modulated input clock with maximum and minimum input cycle time. The REFSEL bit in SMBus 81h is set correctly as shown.
- Default PLL multiplier at power up.
- Contact the factory if operation at these frequencies is required.

### Modes of Operation

The modes of operation are determined by the logic signals applied to the EN and /BYPASS pins and the values in the five SMBus Registers: RegTest, RegA, RegB, RegC, and RegD. Table 3 shows selection from one to all four of the outputs, the Outputs Disabled Mode (EN = low), and Bypass Mode

(EN = high, /BYPASS = low). There is an option reserved for vendor test. Disabled outputs are set to High Z.

At power up, the SMBus registers default to the last entry in Table 3. The value at RegTest is 0. The values at RegA, RegB, RegC, and RegD are all '1'. Thus, all outputs are controlled by the logic applied to EN and /or BYPASS.

**Table 3. Modes of Operation for CY24271**

| EN | /BYPASS | RegTest          | RegA             | RegB             | RegC             | RegD             | CLK0/CLK0B                        | CLK1/CLK1B         | CLK2/CLK2B         | CLK3/CLK3B         |
|----|---------|------------------|------------------|------------------|------------------|------------------|-----------------------------------|--------------------|--------------------|--------------------|
| L  | X       | X                | X                | X                | X                | X                | High Z                            | High Z             | High Z             | High Z             |
| H  | X       | 1                | X                | X                | X                | X                | Reserved for Vendor Test          |                    |                    |                    |
| H  | L       | 0                | X                | X                | X                | X                | REFCLK/<br>REFCLKB <sup>[4]</sup> | REFCLK/<br>REFCLKB | REFCLK/<br>REFCLKB | REFCLK/<br>REFCLKB |
| H  | H       | 0                | 0                | 0                | 0                | 0                | High Z                            | High Z             | High Z             | High Z             |
| H  | H       | 0                | 0                | 0                | 0                | 1                | High Z                            | High Z             | High Z             | CLK/CLKB           |
| H  | H       | 0                | 0                | 0                | 1                | 0                | High Z                            | High Z             | CLK/CLKB           | High Z             |
| H  | H       | 0                | 0                | 0                | 1                | 1                | High Z                            | High Z             | CLK/CLKB           | CLK/CLKB           |
| H  | H       | 0                | 0                | 1                | 0                | 0                | High Z                            | CLK/CLKB           | High Z             | High Z             |
| H  | H       | 0                | 0                | 1                | 0                | 1                | High Z                            | CLK/CLKB           | High Z             | CLK/CLKB           |
| H  | H       | 0                | 0                | 1                | 1                | 0                | High Z                            | CLK/CLKB           | CLK/CLKB           | High Z             |
| H  | H       | 0                | 0                | 1                | 1                | 1                | High Z                            | CLK/CLKB           | CLK/CLKB           | CLK/CLKB           |
| H  | H       | 0                | 1                | 0                | 0                | 0                | CLK/CLKB                          | High Z             | High Z             | High Z             |
| H  | H       | 0                | 1                | 0                | 0                | 1                | CLK/CLKB                          | High Z             | High Z             | CLK/CLKB           |
| H  | H       | 0                | 1                | 0                | 1                | 0                | CLK/CLKB                          | High Z             | CLK/CLKB           | High Z             |
| H  | H       | 0                | 1                | 0                | 1                | 1                | CLK/CLKB                          | High Z             | CLK/CLKB           | CLK/CLKB           |
| H  | H       | 0                | 1                | 1                | 0                | 0                | CLK/CLKB                          | CLK/CLKB           | High Z             | High Z             |
| H  | H       | 0                | 1                | 1                | 0                | 1                | CLK/CLKB                          | CLK/CLKB           | High Z             | CLK/CLKB           |
| H  | H       | 0                | 1                | 1                | 1                | 0                | CLK/CLKB                          | CLK/CLKB           | CLK/CLKB           | High Z             |
| H  | H       | 0 <sup>[5]</sup> | 1 <sup>[5]</sup> | 1 <sup>[5]</sup> | 1 <sup>[5]</sup> | 1 <sup>[5]</sup> | CLK/CLKB                          | CLK/CLKB           | CLK/CLKB           | CLK/CLKB           |

**Notes**

- 4. Bypass Mode: REFCLK bypasses the PLL to the output drivers.
- 5. Default mode of operation is at power up.

### SMBus Protocol

The CY24271 is a slave receiver supporting operations in the word and byte modes described in sections 5.5.4 and 5.5.5 of the SMBus Specification 2.0.

DC specifications are modified to RAMBUS standard to support 1.8, 2.5, and 3.3 volt devices. Time-out detection and packet error protocol SMBus features are not supported.

### Input Clock Signal

The XCG receives either a differential (REFCLK/REFCLKB) or a single-ended reference clocking input (REFCLK).

When the reference input clock is from a different clock source, it must meet the voltage levels and timing requirements listed in [DC Operating Conditions on page 8](#) and [AC Operating Conditions on page 10](#).

For a single-ended clock input, an external voltage divider and a supply voltage, as shown in [Figure 2 on page 7](#), provide a reference voltage  $V_{TH}$  at the REFCLKB pin. This determines the proper trip point of REFCLK. For the range of  $V_{TH}$  specified in [DC Operating Conditions on page 8](#), the outputs also meet the DC and AC Operating Conditions tables.

### SMBus Data Byte Definitions

Three data bytes are defined for the CY24271. Byte 0 is for programming the PLL multiplier registers and clock output registers.

The definition of Byte 2 is shown in [Table 4](#), [Table 5](#), and [Table 6 on page 7](#). The upper five bits are the revision numbers of the device and the lower three bits are the ID numbers assigned to the vendor by Rambus.

**Table 4. Command Code 80h** <sup>[6]</sup>

| Bit | Register | POD | Type | Description                     |
|-----|----------|-----|------|---------------------------------|
| 7   | Reserved | 0   | RW   | Reserved (no internal function) |
| 6   | MULT2    | 0   | RW   | PLL Multiplier Select           |
| 5   | MULT1    | 0   | RW   |                                 |
| 4   | MULT0    | 1   | RW   |                                 |
| 3   | RegA     | 1   | RW   | Clock 0 Output Select           |
| 2   | RegB     | 1   | RW   | Clock 1 Output Select           |
| 1   | RegC     | 1   | RW   | Clock 2 Output Select           |
| 0   | RegD     | 1   | RW   | Clock 3 Output Select           |

**Table 5. Command Code 81h** <sup>[6]</sup>

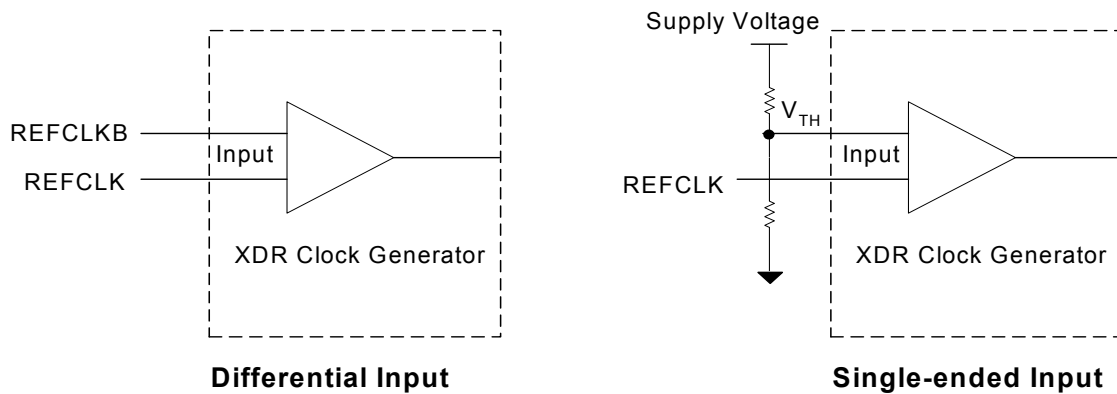
| Bit | Register | POD | Type | Description   |
|-----|----------|-----|------|---|
| 7   | Reserved | 0   | RW   | Reserved (no internal function)   |
| 6   | Reserved | 0   | RW   |   |
| 5   | Reserved | 0   | RW   |   |
| 4   | Reserved | 0   | RW   |   |
| 3   | Reserved | 1   | RW   | Reserved (must be set to '1' for proper operation)                        |
| 2   | REFSEL   | 0   | RW   | Reference Frequency Select (reference <a href="#">Table 1 on page 4</a> ) |
| 1   | Reserved | 0   | RW   | Reserved (must be set to '0' for proper operation)                        |
| 0   | RegTest  | 0   | RW   | Reserved (must be set to '0' for proper operation)                        |

**Note**

6. RW = Read and Write, RO = Read Only, POD = Power on default. See [Table 1 on page 4](#) for PLL multipliers and [Table 3 on page 5](#) for clock output selections.

**Table 6. Command Code 82h** <sup>[7]</sup>

| Bit | Register               | POD | Type | Description   |
|-----|------------------------|-----|------|---|
| 7   | Device Revision Number | ?   | RO   | Contact factory for Device Revision Number information. |
| 6   |                        | ?   | RO   |   |
| 5   |                        | ?   | RO   |   |
| 4   |                        | ?   | RO   |   |
| 3   |                        | ?   | RO   |   |
| 2   | Vendor ID              | 0   | RO   | RAMBUS assigned Vendor ID Code                          |
| 1   |                        | 1   | RO   |   |
| 0   |                        | 0   | RO   |   |

**Figure 2. Differential and Single-Ended Clock Inputs**

**Note**

7. RW = Read and Write, RO = Read Only, POD = Power on default. See [Table 1 on page 4](#) for PLL multipliers and [Table 3 on page 5](#) for clock output selections.

## Absolute Maximum Conditions

| Parameter          | Description                       | Condition                   | Min  | Max                   | Unit |
|--------------------|-----------------------------------|-----------------------------|------|-----------------------|------|
| V <sub>DD</sub>    | Clock Buffer Supply Voltage       |                             | -0.5 | 4.6                   | V    |
| V <sub>DDC</sub>   | Core Supply Voltage               |                             | -0.5 | 4.6                   | V    |
| V <sub>DDP</sub>   | PLL Supply Voltage                |                             | -0.5 | 4.6                   | V    |
| V <sub>IN</sub>    | Input Voltage (SCL and SDA)       | Relative to V <sub>SS</sub> | -0.5 | 4.6                   | V    |
|                    | Input Voltage (REFCLK/REFCLKB)    | Relative to V <sub>SS</sub> | -0.5 | V <sub>DD</sub> + 1.0 | V    |
|                    | Input Voltage                     | Relative to V <sub>SS</sub> | -0.5 | V <sub>DD</sub> + 0.5 | V    |
| T <sub>S</sub>     | Temperature, Storage              | Non-functional              | -65  | 150                   | °C   |
| T <sub>A</sub>     | Temperature, Operating Ambient    | Functional                  | 0    | 70                    | °C   |
| T <sub>J</sub>     | Temperature, Junction             | Functional                  | -    | 150                   | °C   |
| ESD <sub>HBM</sub> | ESD Protection (Human Body Model) | MIL-STD-883, Method 3015    | 2000 | -                     | V    |

## DC Operating Conditions

| Parameter                          | Description   | Condition  | Min                   | Max                   | Unit |
|------------------------------------|---|------------|-----------------------|-----------------------|------|
| V <sub>DDP</sub>                   | Supply Voltage for PLL                                  | 2.5 V ± 5% | 2.375                 | 2.625                 | V    |
| V <sub>DDC</sub>                   | Supply Voltage for Core                                 | 2.5 V ± 5% | 2.375                 | 2.625                 | V    |
| V <sub>DD</sub>                    | Supply Voltage for Clock Buffers                        | 2.5 V ± 5% | 2.375                 | 2.625                 | V    |
| V <sub>IHCLK</sub>                 | Input High Voltage, REFCLK/REFCLKB                      |            | 0.6                   | 0.95                  | V    |
| V <sub>ILCLK</sub>                 | Input Low Voltage, REFCLK/REFCLKB                       |            | -0.15                 | +0.15                 | V    |
| V <sub>IXCLK</sub> <sup>[8]</sup>  | Crossing Point Voltage, REFCLK/REFCLKB                  |            | 200                   | 550                   | mV   |
| ΔV <sub>IXCLK</sub> <sup>[8]</sup> | Difference in Crossing Point Voltage, REFCLK/REFCLKB    |            | -                     | 150                   | mV   |
| V <sub>IH</sub>                    | Input Signal High Voltage at ID0, ID1, EN, and /BYPASS  |            | 1.4                   | 2.625                 | V    |
| V <sub>IL</sub>                    | Input Signal Low Voltage at ID0, ID1, EN, and /BYPASS   |            | -0.15                 | 0.8                   | V    |
| V <sub>IH,SM</sub>                 | Input Signal High Voltage at SCL and SDA <sup>[9]</sup> |            | 1.4                   | 3.465                 | V    |
| V <sub>IL,SM</sub>                 | Input Signal Low Voltage at SCL and SDA                 |            | -0.15                 | 0.8                   | V    |
| V <sub>TH</sub> <sup>[10]</sup>    | Input Threshold Voltage for single-ended REFCLK         |            | 0.35                  | 0.5 × V <sub>DD</sub> | V    |
| V <sub>IH,SE</sub>                 | Input Signal High Voltage for single-ended REFCLK       |            | V <sub>TH</sub> + 0.3 | 2.625                 | V    |
| V <sub>IL,SE</sub>                 | Input Signal Low Voltage for single-ended REFCLK        |            | -0.15                 | V <sub>TH</sub> - 0.3 | V    |
| T <sub>A</sub>                     | Ambient Operating Temperature                           |            | 0                     | 70                    | °C   |

### Notes

8. Not 100% tested except V<sub>IXCLK</sub> and ΔV<sub>IXCLK</sub>. Parameters guaranteed by design and characterizations, not 100% tested in production.

9. This range of SCL and SDA input high voltage enables the 3.3 V, 2.5 V, or 1.8 V SMBus voltages to use CY24271.

10. Single-ended operation guaranteed only when  $0.8 < (V_{IH,SE} - V_{TH}) / (V_{TH} - V_{IL,SE}) < 1.2$ .



## DC Electrical Specifications

| Parameter        | Description  | Min  | Typ | Max  | Unit     |
|------------------|--|------|-----|------|----------|
| $V_{OX}^{[11]}$  | Differential output crossing point voltage <sup>[12]</sup>                               | 0.9  | 1.0 | 1.1  | V        |
| $V_{COS}^{[11]}$ | Output voltage swing (peak-to-peak single-ended) <sup>[13]</sup>                         | 300  | 325 | 350  | mV       |
| $V_{OL,ABS}$     | Absolute output low voltage at CLK[3:0], CLK[3:0]B <sup>[14]</sup>                       | 0.85 | –   | –    | V        |
| $V_{ISET}$       | Reference voltage for swing controlled current, $I_{REF}$                                | 0.98 | 1.0 | 1.02 | V        |
| $I_{DD}^{[11]}$  | Power Supply Current at 2.625 V, $f_{ref} = 100$ MHz, and $f_{out} = 300$ MHz            | –    | –   | 85   | mA       |
| $I_{DD}^{[11]}$  | Power Supply Current at 2.625 V, $f_{ref} = 133$ MHz, and $f_{out} = 667$ MHz            | –    | –   | 125  | mA       |
| $I_{DD}^{[11]}$  | Power Supply Current at 2.625 V, $f_{ref} = 133$ MHz, and $f_{out} = 800$ MHz            | –    | –   | 130  | mA       |
| $I_{OL}/I_{REF}$ | Ratio of output low current to reference current <sup>[15]</sup>                         | 6.8  | 7.0 | 7.2  |          |
| $I_{OL,ABS}$     | Minimum current at $V_{OL,ABS}^{[16]}$   | 45   | –   | –    | mA       |
| $V_{OL,SDA}$     | SDA output low voltage at test condition of SDA output low current = 4 mA                | –    | –   | 0.4  | V        |
| $I_{OL,SDA}$     | SDA output low current at test condition of SDA voltage = 0.8 V                          | 6    | –   | –    | mA       |
| $I_{OZ}$         | Current during High Z per pin at CLK[3:0], CLK[3:0]B                                     | –    | –   | 10   | $\mu$ A  |
| $Z_{OUT}$        | Output dynamic impedance when clock output signal is at $V_{OL} = 0.9$ V <sup>[17]</sup> | 1000 | –   | –    | $\Omega$ |

## Thermal Resistance

| Parameter <sup>[18]</sup> | Description                              | Test Conditions   | 28-pin TSSOP | Unit           |
|---------------------------|--|---|--------------|----------------|
| $\theta_{JA}$             | Thermal resistance (junction to ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51. | 78           | $^{\circ}$ C/W |
| $\theta_{JC}$             | Thermal resistance (junction to case)    |   | 17           | $^{\circ}$ C/W |

### Notes

11. Not 100% tested except  $V_{IXCLK}$  and  $\Delta V_{IXCLK}$ . Parameters guaranteed by design and characterizations, not 100% tested in production.
12.  $V_{OX}$  is measured on external divider network.
13.  $V_{COS}$  = (clock output high voltage – clock output low voltage), measured on the external divider network.
14.  $V_{OL,ABS}$  is measured at the clock output pins of the package.
15.  $I_{REF}$  is equal to  $V_{ISET}/R_{RC}$ .
16. Minimum  $I_{OL,ABS}$  is measured at the clock output pin with  $R_{RC} = 148$  ohms or less.
17.  $Z_{OUT}$  is defined at the output pins as  $(0.94\text{ V} - 0.90\text{ V}) / (I_{0.94} - I_{0.90})$  under conditions specified for  $I_{OL,ABS}$ .
18. These parameters are guaranteed by design and are not tested.

## AC Operating Conditions

The AC operating conditions follow.

| Parameter <sup>[19]</sup>                | Description   | Condition  | Min | Max                 | Unit               |
|--|---|--|-----|---------------------|--------------------|
| $t_{\text{CYCLE,IN}}$                    | REFCLK, REFCLKB input cycle time                                  | REFSEL = 0, /BYPASS = High   | 9   | 11                  | ns                 |
|  |   | REFSEL = 1, /BYPASS = High   | 7   | 8                   | ns                 |
|  |   | /BYPASS = Low  | 4   | –                   | ns                 |
| $t_{\text{JIT,IN(cc)}}$                  | Input Cycle to Cycle Jitter <sup>[20]</sup>                       |  | –   | 185                 | ps                 |
| $t_{\text{DCIN}}$ <sup>[21]</sup>        | Input Duty Cycle  | Over 10,000 cycles   | 40% | 60%                 | $t_{\text{CYCLE}}$ |
| $t_{\text{RIN}} / t_{\text{FIN}}$        | Rise and Fall Times   | Measured at 20%–80% of input voltage for REFCLK and REFCLKB inputs | 175 | 700                 | ps                 |
| $\Delta t_{\text{RIN}} / t_{\text{FIN}}$ | Rise and Fall Times Difference                                    |  | –   | 150                 | ps                 |
| $P_{\text{MIN}}$ <sup>[22]</sup>         | Modulation Index for triangular modulation                        |  | –   | 0.6                 | %                  |
|  | Modulation Index for non-triangular modulation                    |  | –   | 0.5 <sup>[23]</sup> | %                  |
| $f_{\text{MIN}}$ <sup>[22]</sup>         | Input Frequency Modulation  |  | 30  | 33                  | kHz                |
| $t_{\text{SR,IN}}$                       | Input Slew Rate (measured at 20%–80% of input voltage) for REFCLK |  | 1   | 4                   | V/ns               |
| $C_{\text{IN,REF}}$                      | Capacitance at REFCLK inputs                                      |  | –   | 7                   | pF                 |
| $C_{\text{IN,CMOS}}$                     | Capacitance at CMOS inputs  |  | –   | 10                  | pF                 |
| $f_{\text{SCL}}$                         | SMBus clock frequency input in SCL pin                            |  | DC  | 100                 | kHz                |

### Notes

19. Not 100% tested except  $V_{\text{IXCLK}}$  and  $\Delta V_{\text{IXCLK}}$ . Parameters guaranteed by design and characterizations, not 100% tested in production.

20. Jitter measured at crossing points and is the absolute value of the worst case deviation.

21. Measured at crossing points.

22. If input modulation is used; input modulation is allowed but not required.

23. The amount of allowed spreading for any non-triangular modulation is determined by the induced downstream tracking skew that cannot exceed the skew generated by the specified 0.6% triangular modulation. Typically, the amount of allowed non-triangular modulation is about 0.5%.

## AC Electrical Specifications

The AC Electrical specifications follow.

| Parameter <sup>[24]</sup>         | Description  | Min  | Typ  | Max  | Unit               |
|-----------------------------------|--|------|------|------|--------------------|
| t <sub>CYCLE</sub>                | Clock Cycle time <sup>[25]</sup>   | 1.25 | –    | 3.34 | ns                 |
| t <sub>JIT(cc)</sub>              | Jitter over 1-6 clock cycles at 400–635 MHz <sup>[26]</sup>  | –    | 25   | 40   | ps                 |
|                                   | Jitter over 1-6 clock cycles at 638–800 MHz  | –    | 25   | 30   | ps                 |
| L <sub>20</sub>                   | Phase noise SSB spectral purity L(f) at 20 MHz offset: 400–500 MHz<br>(In addition, device must not exceed<br>$L(f) = 10\log[1+(50 \times 10^6/f)^2 \cdot 4] - 138$ for $f = 1$ MHz to 100 MHz<br>except for the region near $f = \text{REFCLK}/Q$ where Q is the value of the<br>internal reference divider.) | –    | –135 | –128 | dBC/Hz             |
|                                   | 533 MHz and faster output  | –    | –    | TBD  |                    |
| t <sub>JIT(hper,cc)</sub>         | Cycle-to-cycle duty cycle error at 400–635 MHz   | –    | 25   | 40   | ps                 |
|                                   | Cycle-to-cycle duty cycle error at 636–800 MHz   | –    | 25   | 30   | ps                 |
| Δt <sub>SKEW</sub>                | Drift in t <sub>SKEW</sub> when ambient temperature varies between 0 °C and 70 °C and supply voltage varies between 2.375 V and 2.625 V. <sup>[27]</sup>   | –    | –    | 15   | ps                 |
| DC                                | Long term average output duty cycle  | 45%  | 50   | 55%  | t <sub>CYCLE</sub> |
| t <sub>EER,SCC</sub>              | PLL output phase error when tracking SSC   | –100 | –    | 100  | ps                 |
| t <sub>CR</sub> , t <sub>CF</sub> | Output rise and fall times at 400–800 MHz (measured at 20%–80% of output voltage)  | 120  | –    | 300  | ps                 |
| t <sub>CR,CF</sub>                | Difference between output rise and fall times on the same pin of the single device (20%–80%) of 400–800 MHz <sup>[28]</sup>  | –    | –    | 100  | ps                 |

### Notes

24. Not 100% tested except V<sub>I,CLK</sub> and ΔV<sub>I,CLK</sub>. Parameters guaranteed by design and characterizations, not 100% tested in production.

25. Max and min output clock cycle times are based on nominal outputs frequency of 300 and 800 MHz, respectively. For spread spectrum modulated differential or single-ended REFCLK, the output clock tracks the modulation of the input.

26. Output short term jitter spec is the absolute value of the worst case deviation.

27. t<sub>SKEW</sub> is the timing difference between any two of the four differential clocks and is measured at common mode voltage. Δt<sub>SKEW</sub> is the change in t<sub>SKEW</sub> when the operating temperature and supply voltage change.

28. t<sub>CR,CF</sub> applies only when appropriate R<sub>RC</sub> and output resistor network resistor values are selected to match pull up and pull down currents.

Test and Measurement Setup

Figure 3. Clock Outputs

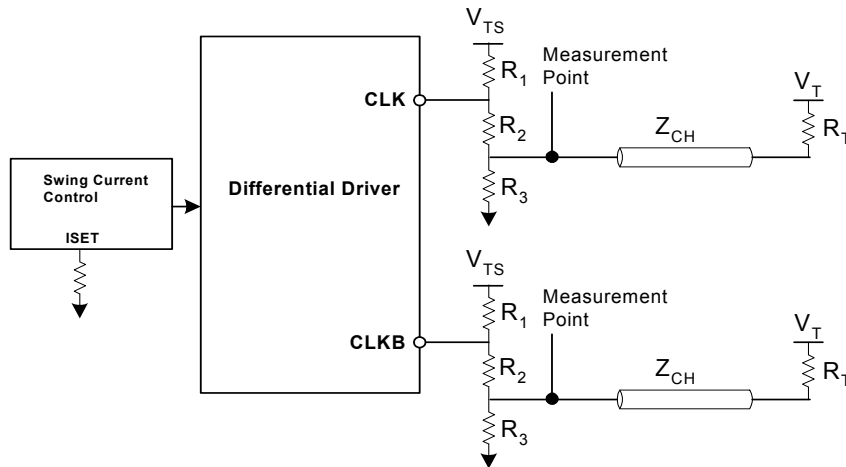


Table 7. Example External Resistor Values and Termination Voltages for a 50 Ω Channel

| Parameter      | Value | Unit |
|----------------|-------|------|
| R <sub>1</sub> | 39.2  | Ω    |
| R <sub>2</sub> | 66.5  | Ω    |
| R <sub>3</sub> | 93.1  | Ω    |

Table 7. Example External Resistor Values and Termination Voltages for a 50 Ω Channel

| Parameter       | Value | Unit |
|-----------------|-------|------|
| R <sub>T</sub>  | 49.9  | Ω    |
| R <sub>RC</sub> | 200   | Ω    |
| V <sub>TS</sub> | 2.5V  | V    |
| V <sub>T</sub>  | 1.2V  | V    |

### Signal Waveforms

A physical signal that appears at the pins of a device is deemed valid or invalid depending on its voltage and timing relations with other signals. Input and output voltage waveforms are defined as shown in Figure 4. Both rise and fall times are defined between the 20% and 80% points of the voltage swing, with the swing defined as  $V_H - V_L$ .

Figure 5 shows the definition of the output crossing point. The nominal crossing point between the complementary outputs is defined as the 50% point of the DC voltage levels. There are two crossing points defined:  $V_{x+}$  at the rising edge of CLK and  $V_{x-}$  at the falling edge of CLK. For some waveforms, both  $V_{x+}$  and  $V_{x-}$  are below  $V_{x,nom}$  (for example, if  $t_{CR}$  is larger than  $t_{CF}$ ).

Figure 4. Input and Output Waveforms

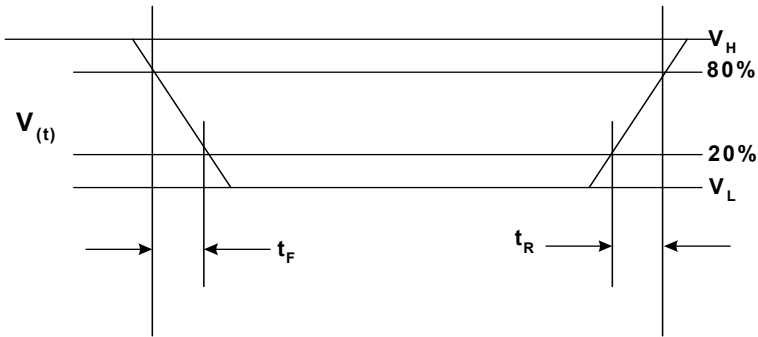
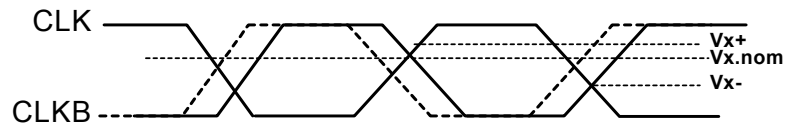


Figure 5. Crossing Point Voltage

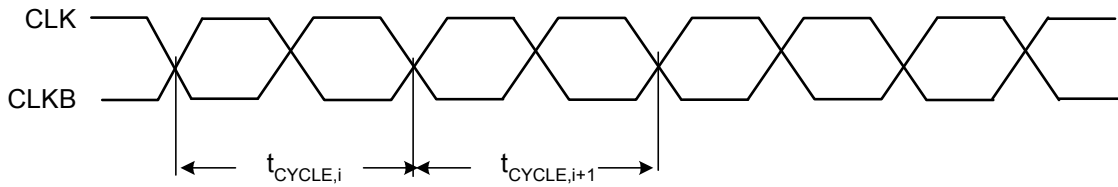


### Jitter

This section defines the specifications that relate to timing uncertainty (or jitter) of the input and output waveforms. Figure 6 shows the definition of cycle-to-cycle jitter with respect to the falling edge of the CLK signal. Cycle-to-cycle jitter is the difference between cycle times of adjacent cycles. Equal

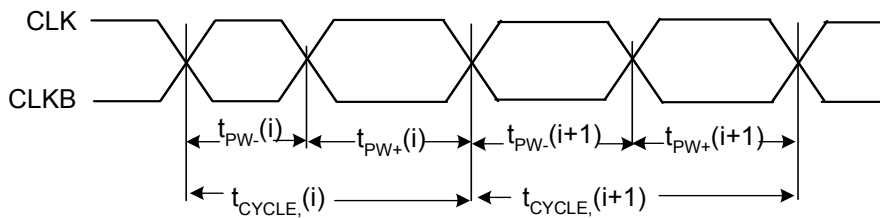
requirements apply rising edges of the CLK signal. Figure 7 shows the definition of cycle-to-cycle duty cycle error ( $t_{DC,ERR}$ ). Cycle-to-cycle duty cycle is defined as the difference between  $t_{PW+}$  (high times) of adjacent differential clock cycles. Equal requirements apply to  $t_{PW-}$ , low times of the differential clock cycles.

Figure 6. Cycle-to-cycle Jitter



$$t_J = t_{CYCLE,i} - t_{CYCLE,i+1} \text{ over 10,000 consecutive cycles}$$

Figure 7. Cycle-to-cycle Duty-cycle Error

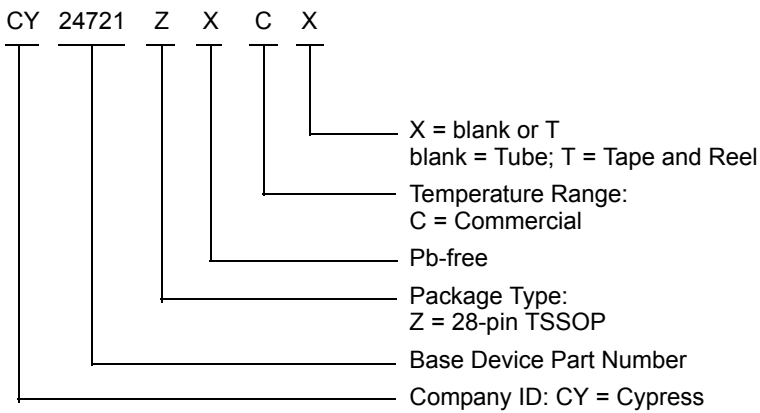


$$t_{DC,ERR} = t_{PW-,(i)} - t_{PW-,(i+1)} \text{ and } t_{PW-,(i+1)} - t_{PW+,(i+1)}$$

### Ordering Information

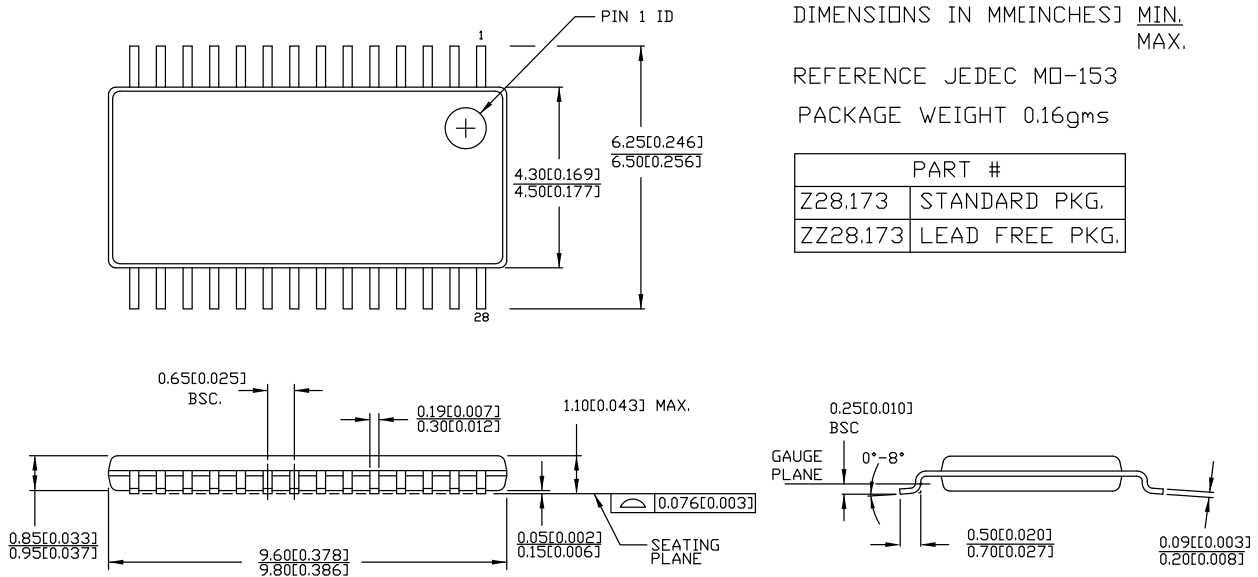
| Part Number    | Package Type                 | Product Flow              |
|----------------|------------------------------|---------------------------|
| <b>Pb-free</b> |                              |                           |
| CY24271ZXC     | 28-pin TSSOP                 | Commercial, 0 °C to 70 °C |
| CY24271ZXCT    | 28-pin TSSOP – Tape and Reel | Commercial, 0 °C to 70 °C |

### Ordering Code Definitions



### Package Drawing and Dimension

Figure 8. 28-pin TSSOP (4.40 mm Body) Z28.173/ZZ28.173 Package Outline, 51-85120



DIMENSIONS IN MM[INCHES] MIN. MAX.

REFERENCE JEDEC MO-153

PACKAGE WEIGHT 0.16gms

| PART #   |                |
|----------|----------------|
| Z28.173  | STANDARD PKG.  |
| ZZ28.173 | LEAD FREE PKG. |

51-85120 \*D



## Acronyms

| Acronym | Description                             |
|---------|---|
| CMOS    | Complementary Metal Oxide Semiconductor |
| ESD     | Electrostatic Discharge                 |
| PLL     | Phase Locked Loop                       |
| TSSOP   | Thin Shrunk Small Outline Package       |
| XDR     | Extended Data Rate                      |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C     | degree Celsius  |
| Hz     | hertz           |
| kHz    | kilohertz       |
| MHz    | megahertz       |
| μA     | microampere     |
| mA     | milliampere     |
| ms     | millisecond     |
| mV     | millivolt       |
| ns     | nanosecond      |
| Ω      | ohm             |
| %      | percent         |
| pF     | picofarad       |
| ps     | picosecond      |
| V      | volt            |

**Document History Page**

| Document Title: CY24271, Rambus® XDR™ Clock Generator<br>Document Number: 001-00411 |         |            |                 |  |
|---|---------|------------|-----------------|--|
| Rev.  | ECN No. | Issue Date | Orig. of Change | Description of Change  |
| **  | 378263  | See ECN    | RGL             | New data sheet.  |
| *A  | 492065  | See ECN    | KKV/TMP         | Replaced VSSC with VSS in all instances across the document.<br>Replaced VSSB with VSSC in all instances across the document.<br>Replaced SCLK with SCL in all instances across the document.<br>Replaced SDATA with SDA in all instances across the document.<br>Replaced BYPASSB with /BYPASS in all instances across the document.<br>Replaced VDDO with VDD in all instances across the document.<br>Replaced VSSO with VSS in all instances across the document.<br>Replaced VSSG with VSS in all instances across the document.<br>Updated <a href="#">Pin Definitions</a> . |
| *B  | 1333483 | See ECN    | FGA / SFV       | Updated <a href="#">DC Electrical Specifications</a> :<br>Added values for I <sub>DD</sub> parameter.  |
| *C  | 3162845 | 02/04/2011 | BASH            | Added <a href="#">Ordering Code Definitions</a> under <a href="#">Ordering Information</a> .<br>Updated <a href="#">Package Drawing and Dimension</a> .<br>Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> .<br>Updated to new template.   |
| *D  | 4292206 | 02/26/2014 | CINM            | Updated <a href="#">Package Drawing and Dimension</a> :<br>spec 51-85120 – Changed revision from *B to *C.<br>Updated to new template.<br>Completing Sunset Review.  |
| *E  | 4581659 | 11/27/2014 | AJU             | Updated <a href="#">Functional Description</a> :<br>Added “For a complete list of related documentation, click <a href="#">here</a> .” at the end.<br>Updated <a href="#">Package Drawing and Dimension</a> :<br>spec 51-85120 – Changed revision from *C to *D.   |
| *F  | 5279278 | 05/20/2016 | PSR             | Added <a href="#">Thermal Resistance</a> .<br>Updated to new template.   |
| *G  | 5660017 | 03/14/2017 | XHT             | No technical updates.<br>Completing Sunset Review.   |
| *H  | 5971807 | 11/20/2017 | AESATMP8        | Updated logo and Copyright.  |

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