



BUK9K89-100E

Dual N-channel TrenchMOS logic level FET

23 April 2013

Product data sheet

1. General description

Dual logic level N-channel MOSFET in a LPAK56D package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

2. Features and benefits

- Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with $V_{GS(th)} > 0.5 \text{ V @ } 175 \text{ °C}$

3. Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Start-stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

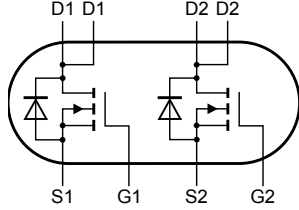
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25 \text{ °C}; T_j \leq 175 \text{ °C}$	-	-	100	V
I_D	drain current	$V_{GS} = 5 \text{ V}; T_{mb} = 25 \text{ °C}; \text{Fig. 1}$	-	-	12.5	A
P_{tot}	total power dissipation	$T_{mb} = 25 \text{ °C}; \text{Fig. 2}$	-	-	38	W
Static characteristics FET1 and FET2						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ °C}; \text{Fig. 12}$	-	75.8	89	mΩ
Dynamic characteristics FET1 and FET2						
Q_{GD}	gate-drain charge	$I_D = 5 \text{ A}; V_{DS} = 80 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ °C}; \text{Fig. 14}; \text{Fig. 15}$	-	4.2	-	nC

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 LFPAK56D (SOT1205)	 <i>mbk725</i>
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9K89-100E	LFPAK56D	Plastic single ended surface mounted package (LFPAK56D); 8 leads	SOT1205

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9K89-100E	98910E

8. Limiting values

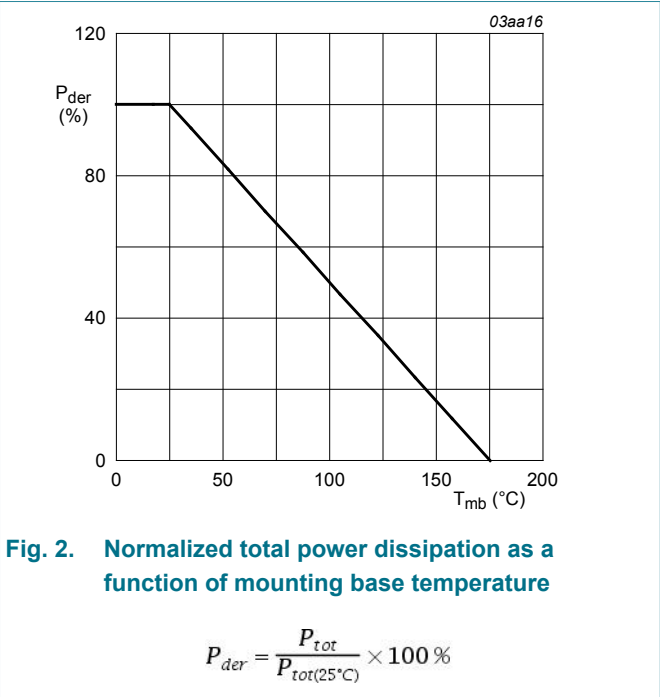
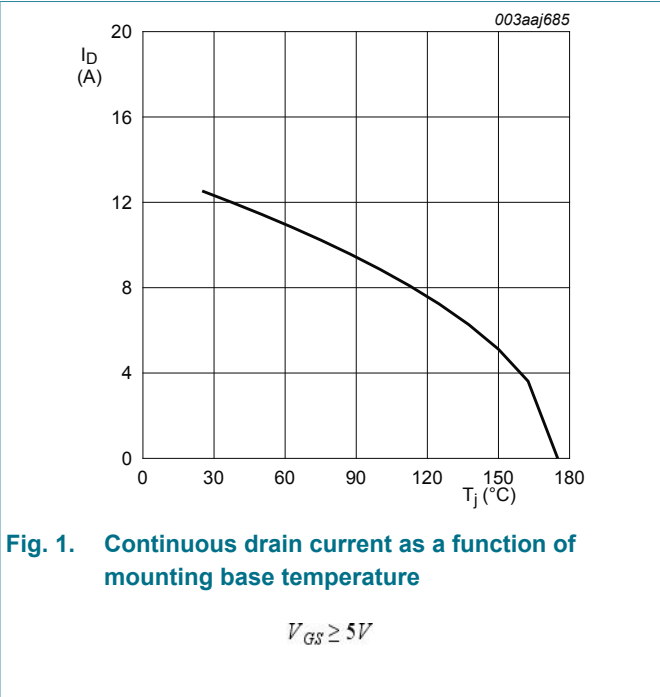
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	100	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$; $T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	100	V
V_{GS}	gate-source voltage	$T_j \leq 175\text{ °C}$; DC	-10	10	V
		$T_j \leq 175\text{ °C}$; Pulsed	[1][2] -15	15	V
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 5\text{ V}$; Fig. 1	-	12.5	A
		$T_{mb} = 100\text{ °C}$; $V_{GS} = 5\text{ V}$; Fig. 1	-	8.9	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Fig. 4	-	50	A

Symbol	Parameter	Conditions		Min	Max	Unit
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 2		-	38	W
T _{stg}	storage temperature			-55	175	°C
T _j	junction temperature			-55	175	°C
T _{sld(M)}	peak soldering temperature			-	260	°C
Source-drain diode FET1 and FET2						
I _S	source current	T _{mb} = 25 °C		-	12.5	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 µs; T _{mb} = 25 °C		-	50	A
Avalanche Ruggedness FET1 and FET2						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 12.5 A; V _{sup} ≤ 100 V; V _{GS} = 5 V; T _{j(init)} = 25 °C; Fig. 3	[3][4]	-	21	mJ

- [1] Accumulated Pulse duration up to 50 hours delivers zero defect ppm
- [2] Significantly longer life times are achieved by lowering T_j and or V_{GS}.
- [3] Refer to application note AN10273 for further information
- [4] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C



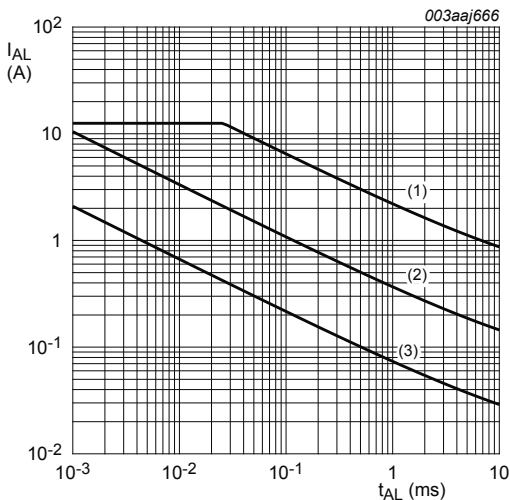


Fig. 3. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time, FET1 and FET2

- (1) Single-pulse; $T_j = 25\text{ }^{\circ}\text{C}$.
- (2) Single-pulse; $T_j = 150\text{ }^{\circ}\text{C}$.
- (3) Repetitive.

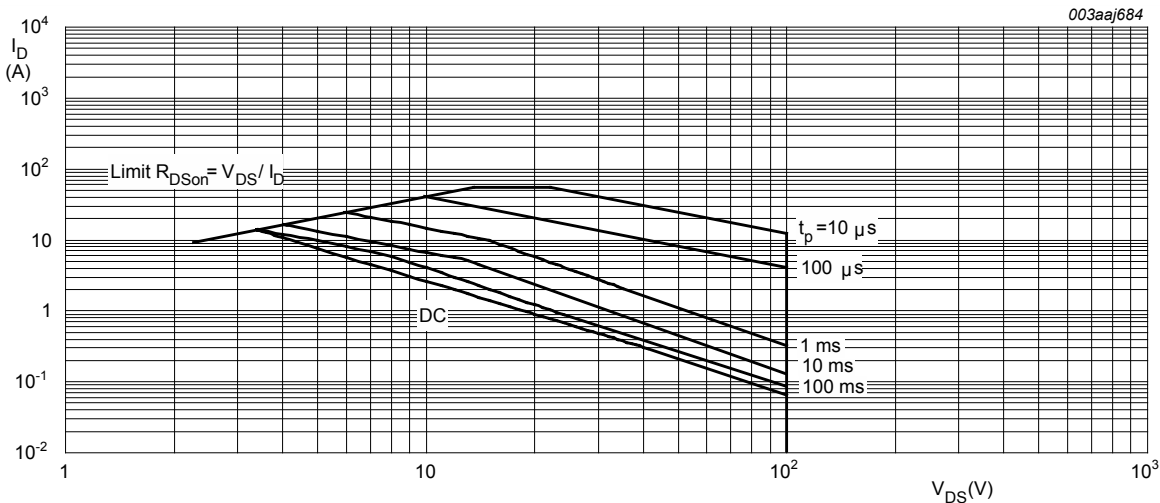


Fig. 4. Safe operating area; continuous and peak drain current as a function of drain-source voltage

$T_{mb} = 25\text{ }^{\circ}\text{C}$; I_{DM} is single pulse

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	-	3.96	K/W

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	95	-	K/W

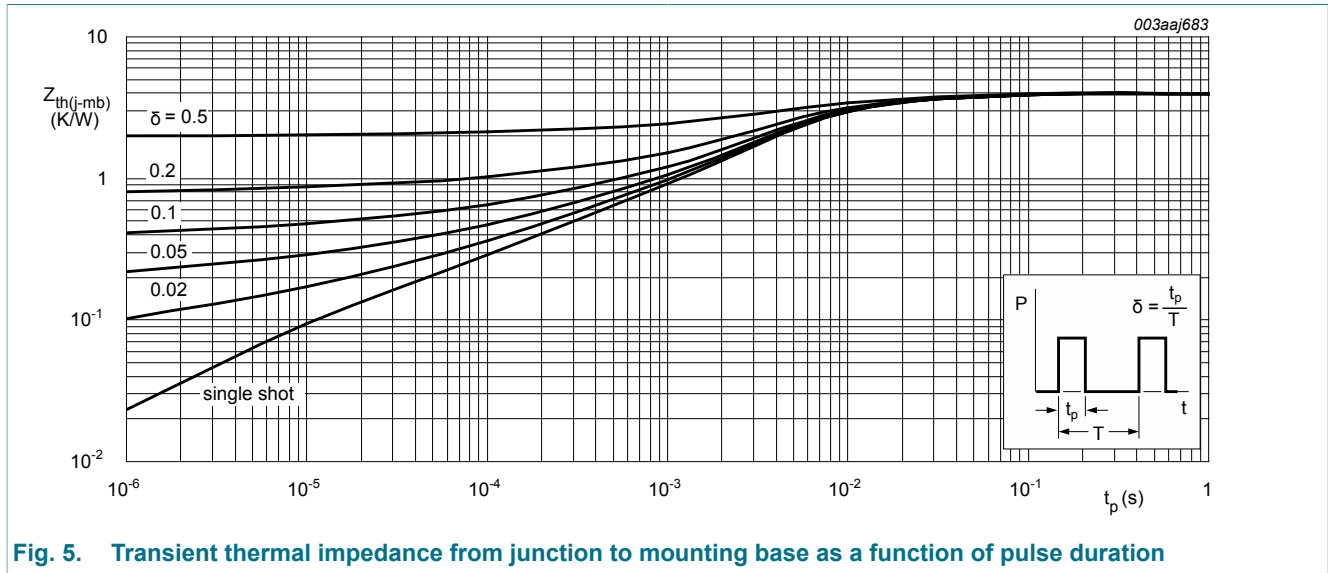


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics FET1 and FET2						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A$; $V_{GS} = 0 V$; $T_J = -55 ^\circ C$	90	-	-	V
		$I_D = 250 \mu A$; $V_{GS} = 0 V$; $T_J = 25 ^\circ C$	100	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 mA$; $V_{DS} = V_{GS}$; $T_J = 25 ^\circ C$; Fig. 10 ; Fig. 11	1.4	1.7	2.1	V
		$I_D = 1 mA$; $V_{DS} = V_{GS}$; $T_J = 175 ^\circ C$; Fig. 10 ; Fig. 11	0.5	-	-	V
		$I_D = 1 mA$; $V_{DS} = V_{GS}$; $T_J = -55 ^\circ C$; Fig. 10 ; Fig. 11	-	-	2.45	V
I_{DSS}	drain leakage current	$V_{DS} = 100 V$; $V_{GS} = 0 V$; $T_J = 25 ^\circ C$	-	0.02	1	μA
		$V_{DS} = 100 V$; $V_{GS} = 0 V$; $T_J = 175 ^\circ C$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = -10 V$; $V_{DS} = 0 V$; $T_J = 25 ^\circ C$	-	2	100	nA
		$V_{GS} = 10 V$; $V_{DS} = 0 V$; $T_J = 25 ^\circ C$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5 V$; $I_D = 5 A$; $T_J = 25 ^\circ C$; Fig. 12	-	75.8	89	m Ω
		$V_{GS} = 5 V$; $I_D = 5 A$; $T_J = 175 ^\circ C$; Fig. 12 ; Fig. 13	-	205.4	245	m Ω
		$V_{GS} = 10 V$; $I_D = 5 A$; $T_J = 25 ^\circ C$; Fig. 12	-	74.9	85	m Ω

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics FET1 and FET2							
Q _{G(tot)}	total gate charge	I _D = 5 A; V _{DS} = 80 V; V _{GS} = 10 V; T _j = 25 °C; Fig. 14 ; Fig. 15		-	16.8	-	nC
Q _{GS}	gate-source charge			-	1.7	-	nC
Q _{GD}	gate-drain charge			-	4.2	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz; T _j = 25 °C; Fig. 16		-	831	1108	pF
C _{oss}	output capacitance			-	81	97	pF
C _{rss}	reverse transfer capacitance			-	59	81	pF
t _{d(on)}	turn-on delay time	V _{DS} = 80 V; R _L = 16 Ω; V _{GS} = 10 V; R _{G(ext)} = 10 Ω; T _j = 25 °C; I _D = 5 A		-	3.6	-	ns
t _r	rise time			-	5.8	-	ns
t _{d(off)}	turn-off delay time			-	22.1	-	ns
t _f	fall time			-	12.1	-	ns
Source-drain diode FET1 and FET2							
V _{SD}	source-drain voltage	I _S = 10 A; V _{GS} = 0 V; T _j = 25 °C; Fig. 17		-	0.78	1.2	V
t _{rr}	reverse recovery time	I _S = 5 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 50 V; T _j = 25 °C		-	29.9	-	ns
Q _r	recovered charge			-	39.9	-	nC

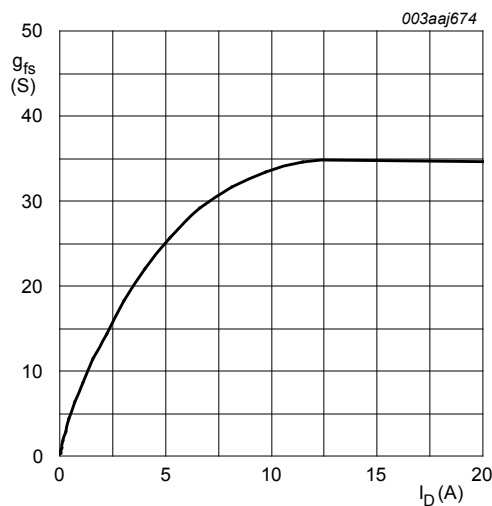


Fig. 6. Forward transconductance as a function of drain current; typical values

$$T_J = 25\text{ }^\circ\text{C}; V_{DS} = 15\text{ V}$$

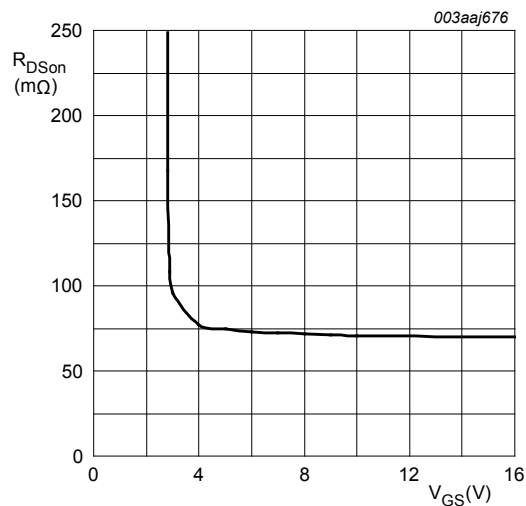


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$$T_J = 25\text{ }^\circ\text{C}; I_D = 5\text{ A}$$

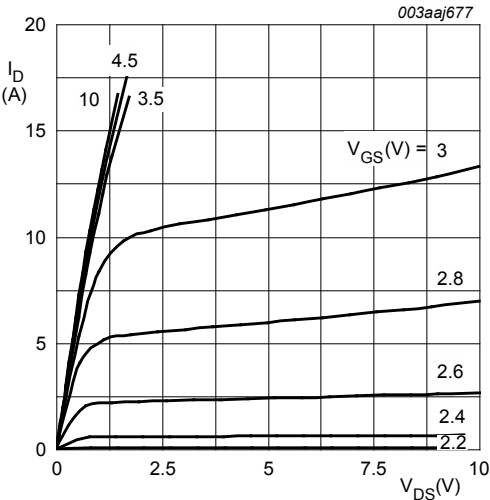


Fig. 8. Output characteristics: drain current as a function of drain-source voltage; typical values

$T_j = 25^\circ\text{C}$

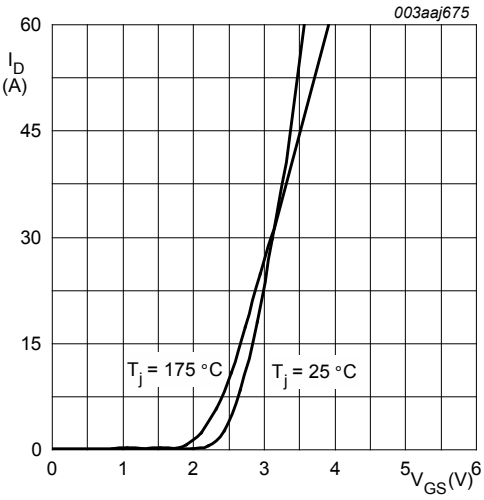


Fig. 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

$V_{DS} = 10\text{V}$

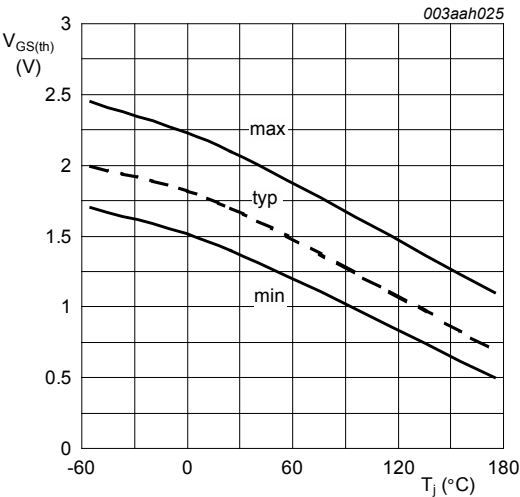


Fig. 10. Gate-source threshold voltage as a function of junction temperature

$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

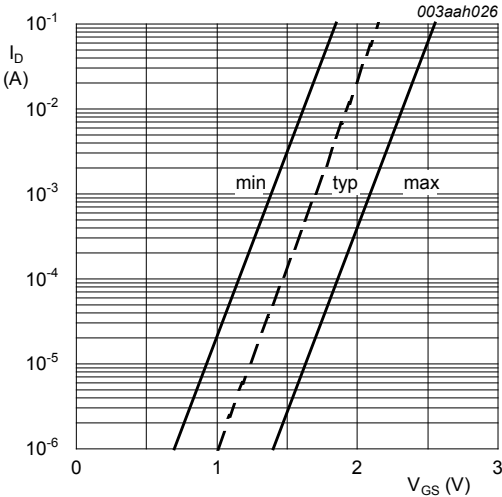


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$

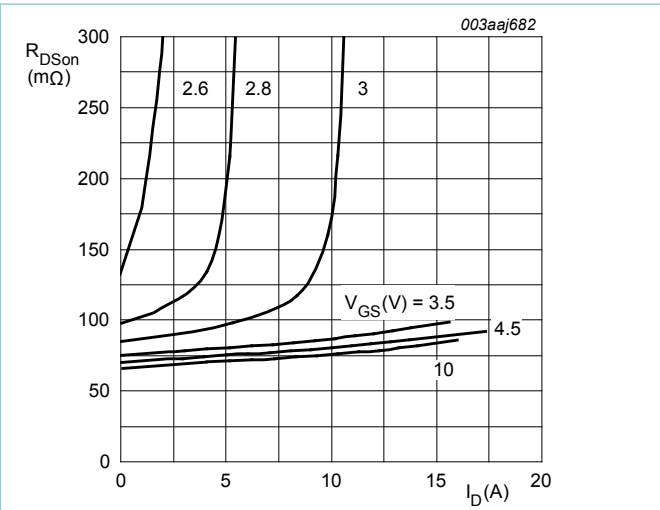


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25\text{ }^{\circ}\text{C}$

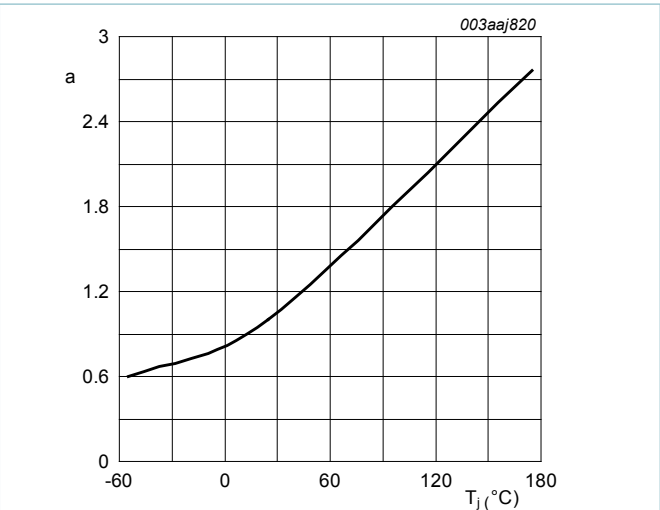


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon}(25^{\circ}\text{C})}$$

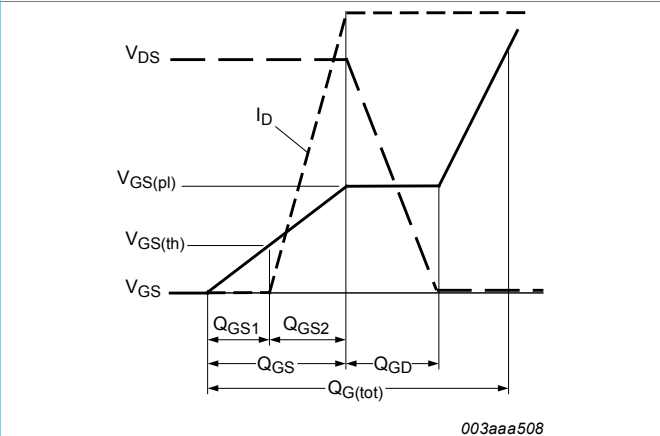


Fig. 14. Gate charge waveform definitions

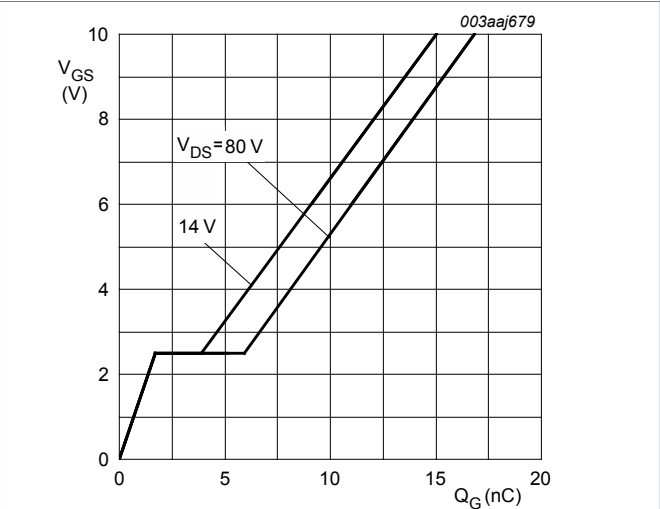


Fig. 15. Gate-source voltage as a function of gate charge; typical values

$T_j = 25\text{ }^{\circ}\text{C}; I_D = 5\text{ A}$

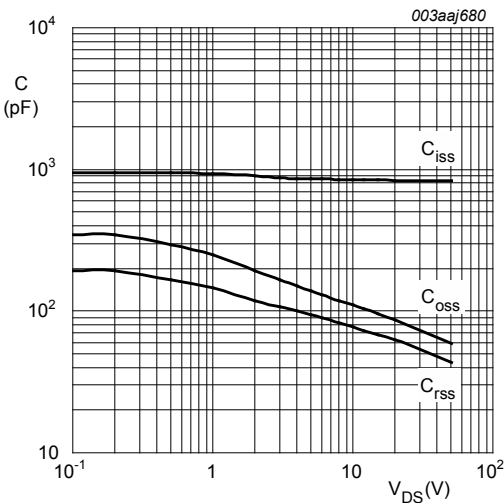


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS}=0\text{ V}; f=1\text{ MHz}$

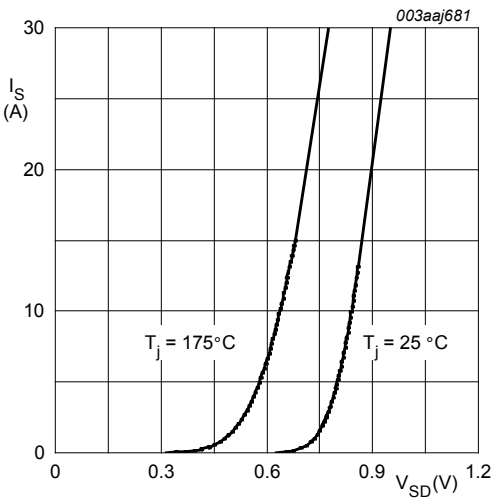


Fig. 17. Source current as a function of source-drain voltage; typical values

$V_{GS}=0\text{ V}$

11. Package outline

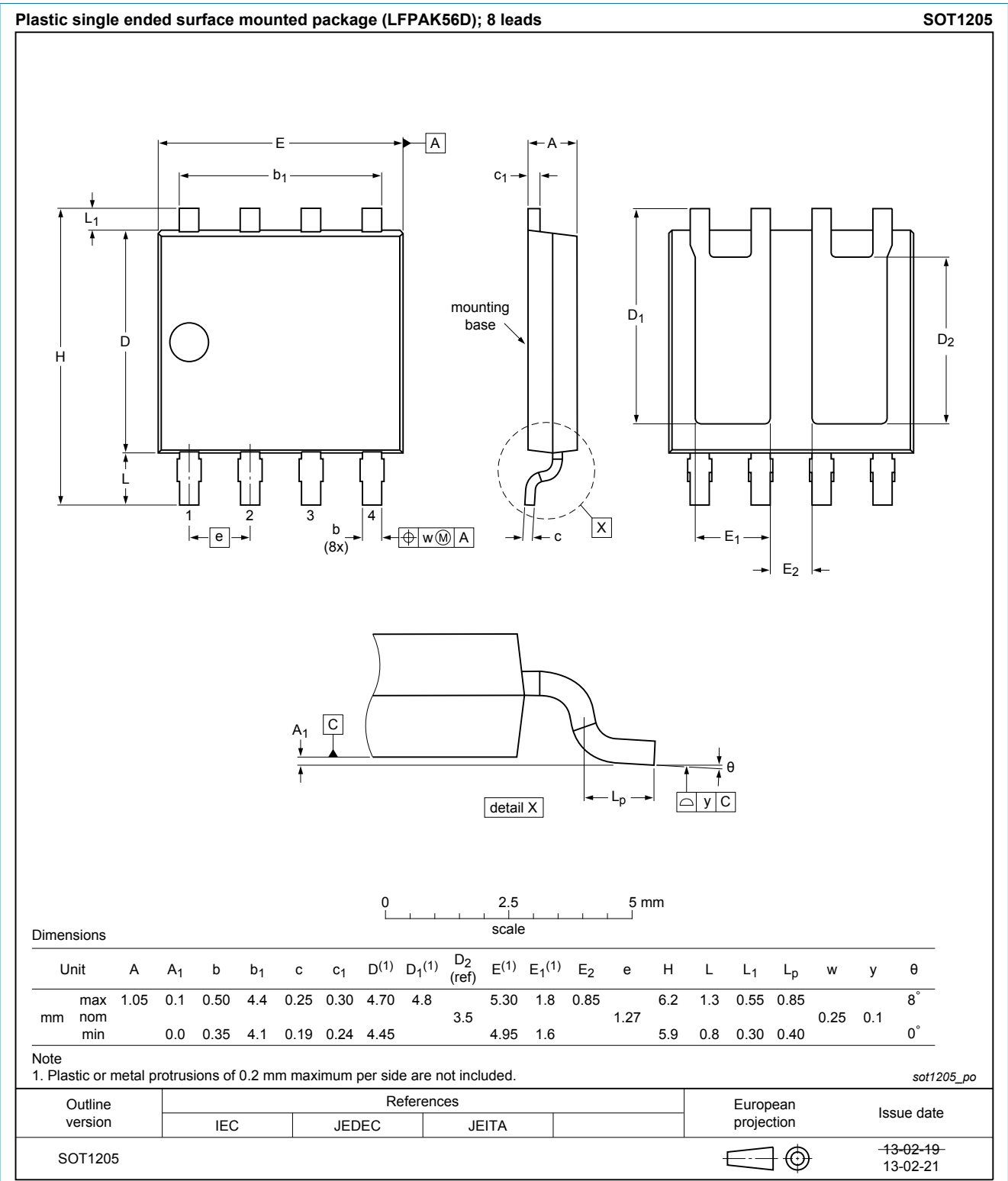


Fig. 18. Package outline LPAK56D (SOT1205)

12. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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