Unit: mm

TOSHIBA Diode Silicon Epitaxial Planar Type

# **1SS184**

### **Ultra High-Speed Switching Applications**

• AEC-Q101 Qualified (Note1)

Small package: SC-59

Low forward voltage:  $V_{F(3)} = 0.90 \text{ V (typ.)}$ 

Fast reverse recovery time:  $t_{rr} = 1.6$  ns (typ.)

Small total capacitance:  $C_T = 0.9 pF$  (typ.)

Note1: For detail information, please contact to our sales.

#### Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit	
Maximum (peak) reverse voltage	V <sub>RM</sub>	85	V	
Reverse voltage	VR	80	V	
Maximum (peak) forward current	I <sub>FM</sub>	300*	mA	
Average forward current	lo	100*	mA	
Surge current (10 ms)	IFSM	2*	Α	
Power dissipation	Р	150	mW	
Junction temperature	Tj	125	°C	
Storage temperature	T <sub>stg</sub>	-55 to 125	°C	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Unit rating. Total rating = unit rating  $\times$  1.5.

#### **Electrical Characteristics (Ta = 25°C)**

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Forward voltage	VF (1)	I <sub>F</sub> = 1 mA		0.60	_	٧
	VF (2)	IF = 10 mA		0.72	_	
	VF (3)	I <sub>F</sub> = 100 mA	_	0.90	1.20	
Reverse current	I <sub>R (1)</sub>	V <sub>R</sub> = 30 V	1	_	0.1	μА
	I <sub>R (2)</sub>	V <sub>R</sub> = 80 V	_	_	0.5	
Total capacitance	CT	V <sub>R</sub> = 0 V, f = 1 MHz		0.9	3.0	pF
Reverse recovery time	t <sub>rr</sub>	I <sub>F</sub> = 10 mA (Fig.1)		1.6	4.0	ns

2.9 ± 0.2 **→** 🔼 ANODE S-MINI TO-236MOD **JEDEC JEITA** SC-59 **TOSHIBA** 2-3F1S

Weight: 12 mg (typ.)

## Marking

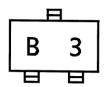
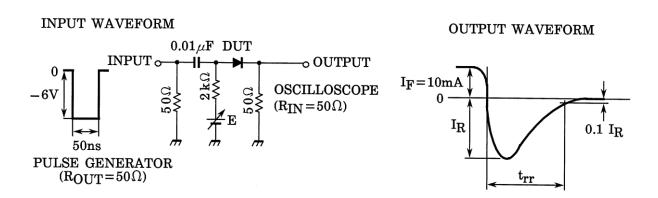
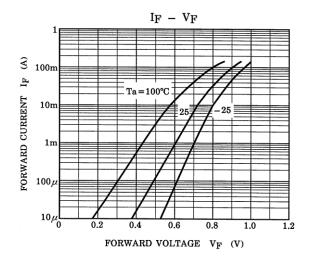
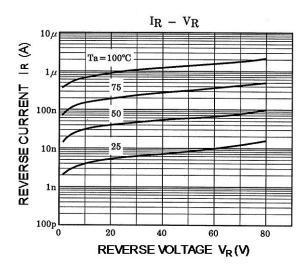


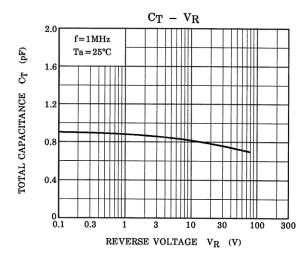
Fig.1 Reverse Recovery Time (trr) Test Circuit

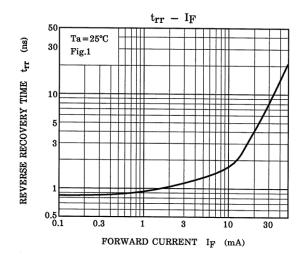


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