

LPC11Axx

32-bit ARM Cortex-M0 microcontroller; up to 32 kB flash, 8 kB SRAM, 4 kB EEPROM; configurable analog/mixed-signal

Rev. 3 — 7 September 2012

Product data sheet

1. General description

The LPC11Axx are an ARM Cortex-M0 based, low-cost 32-bit MCU family, designed for 8/16-bit microcontroller applications, offering performance, low power, simple instruction set and memory addressing together with reduced code size compared to existing 8/16-bit architectures.

The LPC11Axx operate at CPU frequencies of up to 50 MHz.

Analog/mixed-signal subsystems can be configured by software from interconnected digital and analog peripherals.

The digital peripherals on the LPC11Axx include up to 32 kB of flash memory, up to 4 kB of EEPROM data memory, up to 8 kB of SRAM data memory, a Fast-mode Plus I²C-bus interface, a RS-485/EIA-485 USART, two SSP controllers, four general purpose counter/timers, and up to 42 general purpose I/O pins.

Analog peripherals include a 10-bit ADC, a 10-bit DAC, an analog comparator, a temperature sensor, an internal voltage reference, and UnderVoltage LockOut (UVLO) protection.

2. Features and benefits

System:

- ◆ ARM Cortex-M0 processor, running at frequencies of up to 50 MHz.
- ARM Cortex-M0 built-in Nested Vectored Interrupt Controller (NVIC).
- ◆ Serial Wire Debug (SWD)
- JTAG boundary scan.
- System tick timer.

Memory:

- Up to 32 kB on-chip flash program memory.
- ◆ Up to 4 kB on-chip EEPROM data memory; byte erasable and byte programmable.
- Up to 8 kB SRAM data memory.
- ♦ 16 kB boot ROM.
- ◆ In-System Programming (ISP) for flash and In-Application Programming (IAP) for flash and EEPROM via on-chip bootloader software.
- ◆ Includes ROM-based 32-bit integer division and I²C-bus driver routines.
- Digital peripherals:
 - ◆ Up to 42 General Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors, repeater mode, and open-drain mode.



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- ◆ Up to 16 pins are configurable with a digital input glitch filter for removing glitches with widths of 10 ns or less and two pins are configurable for 50 ns glitch filters.
- ◆ GPIO pins can be used as edge and level sensitive interrupt sources.
- High-current source output driver (20 mA) on one pin (PIO0_21).
- ◆ High-current sink driver (20 mA) on true open-drain pins (PIO0_2 and PIO0_3).
- ◆ Four general purpose counter/timers with a total of up to 16 capture inputs and 14 match outputs.
- Programmable Windowed WatchDog Timer (WWDT) with a dedicated, internal low-power WatchDog Oscillator (WDOsc).

Analog peripherals:

- 10-bit ADC with input multiplexing among 8 pins.
- 10-bit DAC with flexible conversion triggering.
- Highly flexible analog comparator with a programmable voltage reference.
- ◆ Integrated temperature sensor.
- Internal voltage reference.
- UnderVoltage Lockout (UVLO) protection against power-supply droop below 2.4 V.

Serial interfaces:

- USART with fractional baud rate generation, internal FIFO, support for RS-485/9-bit mode and synchronous mode.
- Two SSP controllers with FIFO and multi-protocol capabilities. Support data rates of up to 25 Mbit/s.
- ◆ I²C-bus interface supporting the full I²C-bus specification and Fast-mode Plus with a data rate of 1 Mbit/s with multiple address recognition and monitor mode.

Clock generation:

- ◆ Crystal Oscillator (SysOsc) with an operating range of 1 MHz to 25 MHz.
- 12 MHz internal RC Oscillator (IRC) trimmed to 1% accuracy that can optionally be used as a system clock.
- Internal low-power, Low-Frequency Oscillator (LFOsc) with programmable frequency output.
- Clock input for external system clock (25 MHz typical).
- PLL allows CPU operation up to the maximum CPU rate with the IRC, the external clock, or the SysOsc as clock sources.
- Clock output function with divider that can reflect the SysOsc, the IRC, the main clock, or the LFOsc.

Power control:

- Supports one reduced power mode: The ARM Sleep mode.
- Power profiles residing in boot ROM allowing to optimize performance and minimize power consumption for any given application through one simple function call.
- Processor wake-up from reduced power mode using any interrupt.
- Power-On Reset (POR).
- Brown-Out Detect (BOD) with two programmable thresholds for interrupt and one hardware controlled reset trip point.
- POR and BOD are always enabled for rapid UVLO protection against power supply voltage droop below 2.4 V.
- Unique device serial number for identification.

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- Single 3.3 V power supply (2.6 V to 3.6 V).
- Temperature range –40 °C to +85 °C.
- Available as LQFP48 package, HVQFN33 (7 × 7) and HVQFN33 (5 × 5) packages, and in a very small WLCSP20 package.

3. Applications

- Power management
- Industrial control
- Remote monitoring
- Point-of-sale
- Test and measurement equipment
- Network appliances and services
- Factory automation

- Gaming equipment
- Motion control
- Medical instrumentation
- Fire and security
- Sensors
- Precision instrumentation
- HVAC and building control

4. Ordering information

Table 1. Ordering information

Type number	Package	Package											
	Name	Description	Version										
LPC11A02UK	WLCSP20	wafer level chip-size package; 20 bumps; $2.5 \times 2.5 \times 0.6$ mm	-										
LPC11A04UK	WLCSP20	wafer level chip-size package; 20 bumps; $2.5 \times 2.5 \times 0.6$ mm	-										
LPC11A11FHN33/001	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 \times 7 \times 0.85 mm	n/a										
LPC11A12FHN33/101	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 \times 7 \times 0.85 mm	n/a										
LPC11A13FHI33/201	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 \times 5 \times 0.85 mm	n/a										
LPC11A14FHN33/301	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 \times 7 \times 0.85 mm	n/a										
LPC11A12FBD48/101	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 \times 7 \times 1.4 mm	SOT313-2										
LPC11A14FBD48/301	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 \times 7 \times 1.4 mm	SOT313-2										

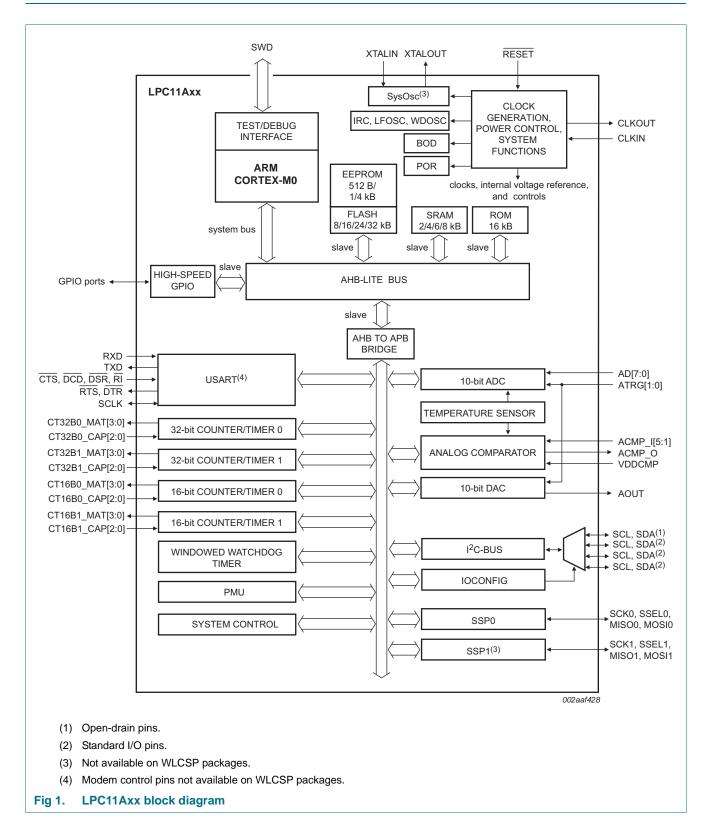


4.1 Ordering options

Table 2. Ordering options

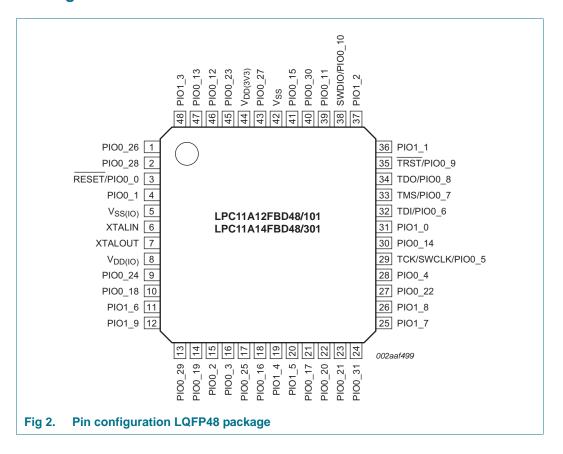
Type number	Flash	SRAM	EEPROM	10-bit ADC channels	10-bit DAC	Temperature sensor	Analog comparator	USART	SSP/SPI	1 ² C	GPIO	Package
LPC11A02UK	16 kB	4 kB	2 kB	8	1	1	1	1	1	1	18	WLCSP20
LPC11A04UK	32 kB	8 kB	4 kB	8	1	1	1	1	1	1	18	WLCSP20
LPC11A11FHN33/001	8 kB	2 kB	512 B	8	1	1	1	1	2	1	28	HVQFN33
LPC11A12FHN33/101	16 kB	4 kB	1 kB	8	1	1	1	1	2	1	28	HVQFN33
LPC11A12FBD48/101	16 kB	4 kB	1 kB	8	1	1	1	1	2	1	42	LQFP48
LPC11A13FHI33/201	24 kB	6 kB	2 kB	8	1	1	1	1	2	1	28	HVQFN33
LPC11A14FHN33/301	32 kB	8 kB	4 kB	8	1	1	1	1	2	1	28	HVQFN33
LPC11A14FBD48/301	32 kB	8 kB	4 kB	8	1	1	1	1	2	1	42	LQFP48

5. Block diagram

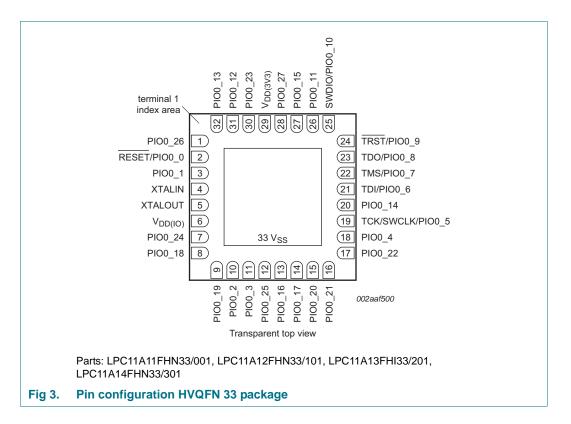


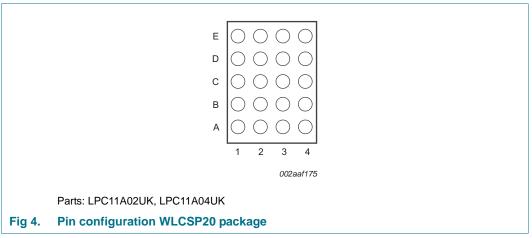
6. Pinning information

6.1 Pinning



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6.2 Pin description

All functional pins on the LPC11Axx are mapped to GPIO port 0 and port 1 (see <u>Table 4</u>). The port pins are multiplexed to accommodate more than one function (see <u>Table 3</u>).

The pin function is controlled by the pin's IOCON register (see the *LPC11Axx user manual*). The standard I/O pad configuration is illustrated in <u>Figure 31</u> and a detailed pin description is given in Table 4.

Table 3. Pin multiplexing

Function	Type			LQFP48	HVQFN33	WCSP20
		Port	Glitch filter	Pin	Pin	Ball
System clock	s, reset, and	d wake-up				
CLKIN	I	PIO0_1	no	4	3	B2
		PIO0_12	no	46	31	E1
		PIO0_19	no	14	9	-
		PIO0_24	no	9	7	-
CLKOUT	0	PIO0_1	no	4	3	B2
		PIO0_19	no	14	9	-
XTALIN	l (analog)	-	-	6	4	-
XTALOUT	O (analog)	-	-	7	5	-
RESET	I	PIO0_0	20 ns[1]	3	2	C1
Serial Wire D	ebug (SWD)	and JTAG				
TRST	I	PIO0_9	10 ns ²	35	24	D4
TCK	I	PIO0_5	10 ns ²	29	19	B3
TDI	I	PIO0_6	10 ns ^[2]	32	21	C3
TDO	0	PIO0_8	no	34	23	C2
TMS	I	PIO0_7	10 ns ²	33	22	C4
SWCLK	I	PIO0_2	50 ns ²	15	10	A1
		PIO0_5	10 ns ²	29	19	B3
SWDIO	I/O	PIO0_3	50 ns ^[2]	16	11	B1
		PIO0_10	10 ns ²	38	25	D3
Analog perip	herals (ADC	, DAC, comp	arator)			
ACMP_I1	l (analog)	PIO0_27	no	43	28	-
ACMP_I2	l (analog)	PIO0_13	no	47	32	D1
ACMP_I3	l (analog)	PIO0_16	no	18	13	A2
ACMP_I4	l (analog)	PIO0_17	no	21	14	A3
ACMP_I5	l (analog)	PIO0_22	no	27	17	-
ACMP_O	0	PIO0_2	no	15	10	A1
	(digital)	PIO0_3	no	16	11	B1
		PIO0_12	no	46	31	E1
		PIO0_21	no	23	16	-
		PIO0_23	no	45	30	-
AD0	l (analog)	PIO0_6	no	32	21	C3
AD1	l (analog)	PIO0_7	no	33	22	C4

Table 3. Pin multiplexing

Function	Type			LQFP48	HVQFN33	WCSP20
		Port	Glitch filter	Pin	Pin	Ball
AD2	l (analog)	PIO0_8	no	34	23	C2
AD3	l (analog)	PIO0_9	no	35	24	D4
AD4	l (analog)	PIO0_10	no	38	25	D3
AD5	l (analog)	PIO0_11	no	39	26	D2
AD6	l (analog)	PIO0_14	no	30	20	B4
AD7	l (analog)	PIO0_15	no	41	27	E4
AOUT	O (analog)	PIO0_4	no	28	18	A4
ATRG0	I	PIO0_16	10 ns[2]	18	13	A2
ATRG1	I	PIO0_17	10 ns ^[2]	21	14	A3
VDDCMP	I	PIO0_14	no	30	20	-
	(analog)	PIO0_5	no	-	-	B3
I ² C-bus interf	ace					
SCL	I/O	PIO0_2	50 ns[2]	15	10	A1
		PIO0_12	no	46	31	E1
		PIO0_16	10 ns[2]	18	13	A2
		PIO0_24	no	9	7	-
SDA	I/O	PIO0_3	50 ns ^[2]	16	11	B1
		PIO0_13	10 ns ^[2]	47	32	D1
		PIO0_15	10 ns[2]	41	27	E4
		PIO0_25	no	17	12	-
SSP0 control	ler					
MISO0	I/O	PIO0_6	10 ns ^[2]	32	21	C3
		PIO0_22	10 ns ^[2]	27	17	-
		PIO1_2	no	37	-	-
MOSI0	I/O	PIO0_4	10 ns ^[2]	28	18	A4
		PIO0_19	no	14	9	-
		PIO1_3	no	48	-	-
		PIO1_7	no	25	-	-
SCK0	I/O	PIO0_5	10 ns ^[2]	29	19	В3
		PIO0_20	no	22	15	-
		PIO1_0	no	31	-	-
SSEL0	I/O	PIO0_1	no	4	3	B2
		PIO0_18	no	10	8	-
		PIO1_1	no	36	_	_

Table 3. Pin multiplexing

Function	Туре			LQFP48	HVQFN33	WCSP20
		Port	Glitch filter	Pin	Pin	Ball
SSP1 contro	ller					
MISO1	I/O	PIO0_14	10 ns ²	30	20	-
		PIO0_26	no	1	1	-
		PIO1_8	no	26	-	-
MOSI1	I/O	PIO0_27	10 ns ^[2]	43	28	-
		PIO0_31	no	24	-	-
		PIO0_30	no	40	-	-
		PIO1_6	no	11	-	-
SCK1	I/O	PIO0_8	10 ns ^[2]	34	23	-
		PIO1_5	no	20	-	-
		PIO0_29	no	13	-	-
SSEL1	I/O	PIO0_25	no	17	12	-
		PIO1_4	no	19	-	-
		PIO0_28	no	2	-	-
USART						
RXD		PIO0_1	no	4	3	B2
		PIO0_12	no	46	31	E1
		PIO1_4	no	19	-	-
		PIO1_8	no	26	-	-
TXD	0	PIO0_13	no	47	32	D1
		PIO0_15	no	41	27	E4
		PIO0_26	no	1	1	-
		PIO1_5	no	20	-	-
SCLK	I/O	PIO0_11	10 ns[2]	39	26	D2
		PIO0_21	no	23	16	-
		PIO0_23	no	45	30	-
CTS	I	PIO0_9	10 ns[2]	35	24	D4
		PIO0_21	no	23	16	-
		PIO1_7	no	25	-	-
RTS	0	PIO0_10	no	38	25	D3
		PIO0_23	no	45	30	-
		PIO1_6	no	11	-	-
DCD	I	PIO1_9	no	12	-	-
		PIO1_0	no	31	-	-
DSR	I	PIO0_29	no	13	-	-
		PIO1_2	no	37	-	-
DTR	0	PIO0_28	no	2	-	-
		PIO1_1	no	36	_	-

Table 3. Pin multiplexing

Function	Туре			LQFP48	HVQFN33	WCSP20
		Port	Glitch filter	Pin	Pin	Ball
RI	I	PIO0_30	no	40	-	-
		PIO0_31	no	24	-	-
		PIO1_3	no	48	-	-
16-bit counter/t	imer CT16	B0				
CT16B0_CAP0	1	PIO0_2	50 ns ^[2]	15	10	A1
		PIO0_18	no	10	8	-
		PIO0_30	no	40	-	-
CT16B0_CAP1	1	PIO0_16	10 ns ^[2]	18	13	A2
		PIO1_4	no	19	-	-
CT16B0_CAP2	I	PIO0_17	10 ns ^[2]	21	14	A3
		PIO1_5	no	20	-	-
CT16B0_MAT0	0	PIO0_7	no	33	22	C4
		PIO0_17	no	21	14	A3
		PIO1_6	no	11	-	-
CT16B0_MAT1	0	PIO0_4	no	28	18	A4
		PIO0_9	no	35	24	D4
		PIO1_0	no	31	-	-
CT16B0_MAT2	0	PIO0_5	no	29	19	B3
		PIO0_10	no	38	25	D3
		PIO1_7	no	25	-	-
16-bit counter/	imer CT16	B1				
CT16B1_CAP0	I	PIO0_3	50 ns ^[2]	16	11	B1
		PIO0_24	no	9	7	-
		PIO1_3	no	48	-	-
CT16B1_CAP1	I	PIO0_18	no	10	8	-
		PIO0_26	no	1	1	-
		PIO0_31	no	24	-	-
CT16B1_CAP2	I	PIO0_27	10 ns ^[2]	43	28	-
		PIO1_7	no	25	-	-
CT16B1_MAT0	0	PIO0_19	no	14	9	-
		PIO0_25	no	17	12	-
		PIO1_1	no	36	-	-
CT16B1_MAT1	0	PIO0_14	no	30	20	B4
		PIO1_2	no	37	-	-
		PIO1_8	no	26	-	-
CT16B1_MAT2	0	PIO0_20	no	22	15	-
		PIO1_2	no	37	-	-
		PIO1_9	no	12	-	-

Table 3. Pin multiplexing

Function	Туре			LQFP48	HVQFN33	WCSP20
		Port	Glitch filter	Pin	Pin	Ball
32-bit counter/t	imer CT32	B0				
CT32B0_CAP0	I	PIO0_11	10 ns ²	39	26	D2
		PIO0_23	no	45	30	-
		PIO0_28	no	2	-	-
CT32B0_CAP1	I	PIO0_14	10 ns ²	30	20	B4
		PIO0_29	no	13	-	-
CT32B0_CAP2	I	PIO0_15	10 ns ²	41	27	E4
		PIO0_26	no	1	1	-
CT32B0_MAT0	0	PIO0_12	no	46	31	E1
		PIO0_30	no	40	-	-
CT32B0_MAT1	0	PIO0_13	no	47	32	D1
		PIO1_4	no	19	-	-
CT32B0_MAT2	0	PIO0_1	no	4	3	B2
		PIO1_5	no	20	-	-
CT32B0_MAT3	0	PIO0_6	no	32	21	C3
		PIO1_6	no	11	-	-
32-bit counter/t	imer CT32	B1				
CT32B1_CAP0	I	PIO0_7	10 ns ^[2]	33	22	C4
		PIO0_20	no	22	15	-
		PIO1_4	no	19	-	-
CT32B1_CAP1	I	PIO0_21	no	23	16	-
		PIO1_5	no	20	-	-
CT32B1_CAP2	I	PIO0_22	10 ns ^[2]	27	17	-
		PIO1_6	no	11	-	-
CT32B1_MAT0	0	PIO0_8	no	34	23	C2
		PIO0_31	no	24	-	-
		PIO1_8	no	26	-	-
CT32B1_MAT1	0	PIO0_9	no	35	24	D4
		PIO0_27	no	43	28	-
		PIO1_7	no	25	-	-
CT32B1_MAT2	0	PIO0_10	no	38	25	D3
		PIO0_22	no	27	17	-
		PIO1_9	no	12	-	-
CT32B1_MAT3	0	PIO0_11	no	39	26	D2
		PIO1_1	no	36	-	-
		PIO1_0	no	31	-	-
Supply and gro	und pins	1	1	1		
$V_{\rm DD(IO)}$	Supply	-	-	8	6	E2

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Table 3. Pin multiplexing

Function	Туре			LQFP48	HVQFN33	WCSP20
		Port	Glitch filter	Pin	Pin	Ball
$V_{DD(3V3)}$	Supply	-	-	44	29	E2
V_{SS}	Ground	-	-	42	33	E3
V _{SS(IO)}	Ground	-	-	5	33	E3

^[1] Always on.

<u>Table 4</u> shows all pins in order of their port number. The default function after reset is listed first. All port pins PIO0_0 to PIO1_9 have internal pull-up resistors enabled after reset with the exception of the true open-drain pins PIO0_2 and PIO0_3.

Pull-up/pull-down configuration, repeater, and open-drain modes can be programmed through the IOCON registers for each of the port pins.

Table 4. LPC11Axx pin description table

Symbol	Pin	Pin/Ball		Туре	Reset state	Description	
	LQFP48	HVQFN33	WLCSP20				
RESET/PIO0_0	3	2	C1	[2]	I	I; PU	RESET — External reset input with fixed 20 ns glitch filter: A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states and processor execution to begin at address 0.
					I/O	-	PIO0_0 — General purpose digital input/output pin.
PIO0_1/RXD/CLKOUT/ CT32B0_MAT2/SSEL0/	4	3	B2	[3]	I/O	I; PU	PIO0_1 — General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
CLKIN					I	-	RXD — Receiver data input for USART.
					0	-	CLKOUT — Clock output.
					0	-	CT32B0_MAT2 — Match output 2 for 32-bit timer 0.
					I/O	-	SSEL0 — Slave Select for SSP0.
					I	-	CLKIN — External clock input.
PIO0_2/SCL/ACMP_O/ TCK/SWCLK/ CT16B0_CAP0	15	10	0 A1	1 [4][5]	I/O	I; IA	PIO0_2 — General purpose digital input/output pin. High-current sink (20 mA) or standard-current sink (4 mA) programmable; true open-drain for all pin functions. Input glitch filter (50 ns) capable.
					I/O	-	SCL — I ² C-bus clock (true open-drain) input/output. Input glitch filter (50 ns) capable.
					0	-	ACMP_O — Analog comparator output.
					I	-	TCK/SWCLK — Serial Wire Debug Clock (secondary for LQFP and HVQFN packages). Input glitch filter (50 ns) capable. For the WLCSP20 package only, this pin is configured to the SWCLK function by the boot loader after reset.
					I	-	CT16B0_CAP0 — Capture input 0 for 16-bit timer 0. Input glitch filter (50 ns) capable.

^[2] Programmable on/off. By default, the glitch filter is disabled.



Table 4. LPC11Axx pin description table

Symbol	Pin	/Ball			Туре	Reset state	Description
	LQFP48	HVQFN33	WLCSP20				
PIO0_3/SDA/ACMP_O/ SWDIO/CT16B1_CAP0	16	11	B1	[4][6]	I/O	I; IA	PIO0_3 — General purpose digital input/output pin. High-current sink (20 mA) or standard-current sink (4 mA) programmable; true open-drain for all pin functions. Input glitch filter (50 ns) capable.
					I/O	-	SDA — I ² C-bus data (true open-drain) input/output. Input glitch filter (50 ns) capable.
					0	-	ACMP_O — Analog comparator output.
					I/O	-	SWDIO — Serial Wire Debug I/O (secondary for LQFP and HVQFN packages). Input glitch filter (50 ns) capable. For the WLCSP20 package only, this pin is configured to the SWDIO function by the boot loader after reset.
					I	-	CT16B1_CAP0 — Capture input 0 for 16-bit timer 1. Input glitch filter (50 ns) capable.
PIO0_4/R/AOUT/ CT16B0_MAT1/MOSI0		18 A4	3 A4	[7]	I/O	I; PU	PIO0_4 — General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					-	-	R — Reserved.
					0	-	AOUT — D/A converter output.
					0	-	CT16B0_MAT1 — Match output 1 for 16-bit timer 0.
					I/O	-	MOSI0 — Master Out Slave In for SSP0. Input glitch filter (10 ns) capable.
TCK/SWCLK/PIO0_5/ R/CT16B0_MAT2/ SCK0	29	19	-	<u>[9]</u>	I	I; PU	TCK/SWCLK — Test clock TCK for JTAG interface and primary (default) Serial Wire Debug Clock. Input glitch filter (10 ns) capable.
					I/O	-	PIO0_5 — General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					-	-	R — Reserved.
					0	-	CT16B0_MAT2 — Match output 2 for 16-bit timer 0.
					I/O	-	SCK0 — Serial clock for SSP0. Input glitch filter (10 ns) capable.
TCK/SWCLK/PIO0_5/ VDDCMP/ CT16B0_MAT2/ SCK0	-	-	В3	[7][8]	I	I; PU	TCK/SWCLK — Test clock TCK for JTAG interface and secondary Serial Wire Debug ClocK. Use PIO0_2 for the default TCK/SWCLK function. Input glitch filter (10 ns) capable.
					I/O	-	PIO0_5 — General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I	-	VDDCMP — Analog comparator alternate reference voltage.
					0	-	CT16B0_MAT2 — Match output 2 for 16-bit timer 0.
					I/O	-	SCK0 — Serial clock for SSP0. Input glitch filter (10 ns) capable.



Table 4. LPC11Axx pin description table

Symbol	Pin	/Ball			Туре	Reset state	Description
	LQFP48	HVQFN33	WLCSP20				
TDI/PIO0_6/AD0/ CT32B0_MAT3/MISO0	32	21	C3	<u>[9]</u>	I	I; PU	TDI — Test Data In for JTAG interface. Input glitch filter (10 ns) capable.
					I/O	-	PIO0_6 — General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I	-	AD0 — A/D converter input 0.
					0	-	CT32B0_MAT3 — Match output 3 for 32-bit timer 0.
					I/O	-	MISO0 — Master In Slave Out for SSP0. Input glitch filter (10 ns) capable.
TMS/PIO0_7/AD1/ CT32B1_CAP0/	33	22	C4	[9]	I	I; PU	TMS — Test Mode Select for JTAG interface. Input glitch filter (10 ns) capable.
CT16B0_MAT0					I/O	-	PIO0_7 — General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I	-	AD1 — A/D converter input 1.
					I	-	CT32B1_CAP0 — Capture input 0 for 32-bit timer 1. Input glitch filter (10 ns) capable.
					0	-	CT16B0_MAT0 — Match output 2 for 16-bit timer 0.
TDO/PIO0_8/AD2/	34	23	C2	[9]	0	I; PU	TDO — Test Data Out for JTAG interface.
CT32B1_MAT0/SCK1					I/O	-	PIO0_8 — General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I	-	AD2 — A/D converter input 2.
					0	-	CT32B1_MAT0 — Match output 0 for 32-bit timer 1.
					I/O	-	SCK1 — Serial clock for SSP1. Input glitch filter (10 ns) capable.
TRST/PIO0_9/AD3/ CT32B1_MAT1/	35	24	D4	[9]	I	I; PU	TRST — Test Reset for JTAG interface. Input glitch filter (10 ns) capable.
CT16B0_MAT1/CTS					I/O	-	PIO0_9 — General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I	-	AD3 — A/D converter, input 3.
					0	-	CT32B1_MAT1 — Match output 1 for 32-bit timer 1.
					0	-	CT16B0_MAT1 — Match output 1 for 16-bit timer 0.
					I	-	CTS — Clear To Send input for USART. Input glitch filter (10 ns) capable.



Table 4. LPC11Axx pin description table

Symbol	Pin	/Ball			Туре	Reset state	Description	
	LQFP48	HVQFN33	WLCSP20					
SWDIO/PIO0_10/AD4/ CT32B1_MAT2/ CT16B0_MAT2/RTS	38	25	D3	<u>[9]</u>	I/O	I; PU	SWDIO — Primary (default) Serial Wire Debug I/O for the LQFP48 and HVQFN33 packages. For the WLCSP20 package, use PIO0_3. Input glitch filter (10 ns) capable.	
					I/O	-	PIO0_10 — General purpose digital input/output pin. Input glitch filter (10 ns) capable.	
					I	-	AD4 — A/D converter, input 4.	
					0	-	CT32B1_MAT2 — Match output 2 for 32-bit timer 1.	
					0	-	CT16B0_MAT2 — Match output 2 for 16-bit timer 0.	
					Ο	-	RTS — Request To Send output for USART.	
PIO0_11/SCLK/ AD5/CT32B1_MAT3/	39	39	26	D2	<u>[9]</u>	I/O	I; PU	PIO0_11 — General purpose digital input/output pin. Input glitch filter (10 ns) capable.
CT32B0_CAP0					I/O	-	SCLK — Serial clock for USART. Input glitch filter (10 ns) capable.	
					I	-	AD5 — A/D converter, input 5.	
					0	-	CT32B1_MAT3 — Match output 3 for 32-bit timer 1.	
					I	-	CT32B0_CAP0 — Capture input 0 for 32-bit timer 0. Input glitch filter (10 ns) capable.	
PIO0_12/RXD/	46	31	E1	E1 🗓	I/O	I; PU	PIO0_12 — General purpose digital input/output pin.	
ACMP_O/ CT32B0_MAT0/SCL/ CLKIN					I	-	RXD — Receiver data input for USART. This pin is used for ISP communication.	
CLININ					0	-	ACMP_O — Analog comparator output.	
					0	-	CT32B0_MAT0 — Match output 0 for 32-bit timer 0.	
					I/O	-	SCL — I ² C-bus clock input/output. This is not an I ² C-bus open-drain pin ^[10] .	
					I	-	CLKIN — External clock input.	
PIO0_13/TXD/ ACMP_I2/	47	32	D1	[9]	I/O	I; PU	PIO0_13 — General purpose digital input/output pin. Input glitch filter (10 ns) capable.	
CT32B0_MAT1/SDA					0	-	TXD — Transmitter data output for USART. This pin is used for ISP communication.	
					I	-	ACMP_I2 — Analog comparator input 2.	
					0	-	CT32B0_MAT1 — Match output 1 for 32-bit timer 0.	
					I/O	-	SDA — I ² C-bus data input/output. This is not an I ² C-bus open-drain pin ^[10] . Input glitch filter (10 ns) capable.	



Table 4. LPC11Axx pin description table

Symbol	Pin	Pin/Ball			Туре	Reset state	Description
	LQFP48	HVQFN33	WLCSP20				
PIO0_14/MISO1/AD6/ CT32B0_CAP1/	30	20	-	<u>[7]</u>	I/O	I; PU	PIO0_14 — General purpose digital input/output pin. Input glitch filter (10 ns) capable.
CT16B1_MAT1/ VDDCMP					I/O	-	MISO1 — Master In Slave Out for SSP1. Input glitch filter (10 ns) capable.
					I	-	AD6 — A/D converter, input 6.
					I	-	CT32B0_CAP1 — Capture input 1 for 32-bit timer 0. Input glitch filter (10 ns) capable.
					0	-	CT16B1_MAT1 — Match output 1 for 16-bit timer 1.
					I	-	VDDCMP — Analog comparator alternate reference voltage.
PIO0_14/MISO1/AD6/ CT32B0_CAP1/	-	-	В4	[9]	I/O	I; PU	PIO0_14 — General purpose digital input/output pin. Input glitch filter (10 ns) capable.
CT16B1_MAT1					I/O	-	MISO1 — Master In Slave Out for SSP1. Input glitch filter (10 ns) capable.
					I	-	AD6 — A/D converter, input 6.
					I	-	CT32B0_CAP1 — Capture input 1 for 32-bit timer 0. Input glitch filter (10 ns) capable.
					0	-	CT16B1_MAT1 — Match output 1 for 16-bit timer 1.
PIO0_15/TXD/AD7/ CT32B0_CAP2/SDA	41	27	E4	[9]	I/O	I; PU	PIO0_15 — General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					0	-	TXD — Transmitter data output for USART.
					I	-	AD7 — A/D converter, input 7.
					I	-	CT32B0_CAP2 — Capture input 2 for 32-bit timer 0. Input glitch filter (10 ns) capable.
					I/O	-	SDA — I^2 C-bus data input/output. This is not an I^2 C-bus open-drain pin[10]. Input glitch filter (10 ns) capable.
PIO0_16/ ATRG0/ACMP_I3/	18	13	A2	<u>9</u>	I/O	I; PU	PIO0_16 — General purpose digital input/output pin. Input glitch filter (10 ns) capable.
CT16B0_CAP1/SCL					ı	-	ATRG0 — Conversion trigger 0 for ADC or DAC. Input glitch filter (10 ns) capable.
					I	-	ACMP_I3 — Analog comparator input 3.
					I	-	CT16B0_CAP1 — Capture input 1 for 16-bit timer 0. Input glitch filter (10 ns) capable.
					I/O	-	SCL — I ² C-bus clock input/output. This is not an I ² C-bus open-drain pin ^[10] . Input glitch filter (10 ns) capable.



Table 4. LPC11Axx pin description table

Symbol	Pin/Ball					Reset state	Description
	LQFP48	HVQFN33	WLCSP20				
PIO0_17/ ATRG1/ACMP_I4/ CT16B0_CAP2/ CT16B0_MAT0	21	14	АЗ	[9]	I/O	I; PU	PIO0_17 — General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I	-	ATRG1 — Conversion trigger 1 for ADC or DAC. Input glitch filter (10 ns) capable.
					I	-	ACMP_I4 — Analog comparator input 4.
					I	-	CT16B0_CAP2 — Capture input 2 for 16-bit timer 0. Input glitch filter (10 ns) capable.
					0	-	CT16B0_MAT0 — Match output 0 for 16-bit timer 0.
PIO0_18/R/SSEL0/	10	8	-	[3]	I/O	I; PU	PIO0_18 — General purpose digital input/output pin.
CT16B0_CAP0/					-	-	R — Reserved.
CT16B1_CAP1					I/O	-	SSEL0 — Slave Select for SSP0.
					ı	-	CT16B0_CAP0 — Capture input 0 for 16-bit timer 0.
					ı	-	CT16B1_CAP1 — Capture input 1 for 16-bit timer 1.
PIO0_19/CLKIN/	14	9	-	[3]	I/O	I; PU	PIO0_19 — General purpose digital input/output pin.
CLKOUT/ MOSI0/CT16B1_MAT0					ı	-	CLKIN — External clock input.
					0	-	CLKOUT — Clock output.
					I/O	-	MOSI0 — Master Out Slave In for SSP0.
					0	-	CT16B1_MAT0 — Match output 0 for 16-bit timer 1.
PIO0_20/R/SCK0/	22	15	-	[3]	I/O	I; PU	PIO0_20 — General purpose digital input/output pin.
CT32B1_CAP0/ CT16B1_MAT2					-	-	R — Reserved.
					I/O	-	SCK0 — Serial clock for SSP0.
					I	-	CT32B1_CAP0 — Capture input 0 for 32-bit timer 1.
					0	-	CT16B1_MAT2 — Match output 2 for 16-bit timer 1.
PIO0_21/CTS/ ACMP_O/ CT32B1_CAP1/SCLK	23	16	-	[3]	I/O	I; PU	PIO0_21 — General purpose digital input/output pin. If configured as output, this pin is a high-current source output driver (20 mA).
					I	-	CTS — Clear To Send input for USART.
					0	-	ACMP_O — Analog comparator output.
					I	-	CT32B1_CAP1 — Capture input 1 for 32-bit timer 1.
					I/O	-	SCLK — Serial clock for USART.
PIO0_22/MISO0/ ACMP_I5/ CT32B1_MAT2/ CT32B1_CAP2	27	17	7 -	<u>[9]</u>	I/O	I; PU	PIO0_22 — General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I/O	-	MISO0 — Master In Slave Out for SSP0. Input glitch filter (10 ns) capable.
					I	-	ACMP_I5 — Analog comparator input 5.
					0	-	CT32B1_MAT2 — Match output 2 for 32-bit timer 1.
					I	-	CT32B1_CAP2 — Capture input 2 for 32-bit timer 1. Input glitch filter (10 ns) capable.

Table 4. LPC11Axx pin description table

Symbol	Pin	/Ball	I		Type	Reset state	Description
	LQFP48	HVQFN33	WLCSP20				
PIO0_23/RTS/	45	30	-	[3]	I/O	I; PU	PIO0_23 — General purpose digital input/output pin.
ACMP_O/ CT32B0_CAP0/SCLK					0	-	RTS — Request To Send output for USART.
C132D0_CAI 0/3CLK					0	-	ACMP_O — Analog comparator output.
					I	-	CT32B0_CAP0 — Capture input 0 for 32-bit timer 0.
					I/O	-	SCLK — Serial clock for USART.
PIO0_24/SCL/CLKIN/	9	7	-	[3]	I/O	I; PU	PIO0_24 — General purpose digital input/output pin.
CT16B1_CAP0					I/O	-	SCL — I ² C-bus clock input/output. This is not an I ² C-bus open-drain pin[10].
					I	-	CLKIN — External clock input.
					I	-	CT16B1_CAP0 — Capture input 0 for 16-bit timer 1.
PIO0_25/SDA/SSEL1/	17	12	-	<u>[3]</u>	I/O	I; PU	PIO0_25 — General purpose digital input/output pin.
CT16B1_MAT0					I/O	-	SDA — I^2 C-bus data input/output. This is not an I^2 C-bus open-drain pin[10].
					I/O	-	SSEL1 — Slave Select for SSP1.
					0	-	CT16B1_MAT0 — Match output 0 for 16-bit timer 1.
PIO0_26/TXD/MISO1/	1	1	-	[3]	I/O	I; PU	PIO0_26 — General purpose digital input/output pin.
CT16B1_CAP1/ CT32B0_CAP2					0	-	TXD — Transmitter data output for USART.
					I/O	-	MISO1 — Master In Slave Out for SSP1.
					I	-	CT16B1_CAP1 — Capture input 1 for 16-bit timer 1.
					I	-	CT32B0_CAP2 — Capture input 2 for 32-bit timer 0.
PIO0_27/MOSI1/ ACMP_I1/	43	28	-	<u>[9]</u>	I/O	I; PU	PIO0_27 — General purpose digital input/output pin. Input glitch filter (10 ns) capable.
CT32B1_MAT1/ CT16B1_CAP2					I/O	-	MOSI1 — Master Out Slave In for SSP1. Input glitch filter (10 ns) capable.
					I	-	ACMP_I1 — Analog comparator input 1.
					0	-	CT32B1_MAT1 — Match output 1 for 32-bit timer 1.
					I	-	CT16B1_CAP2 — Capture input 2 for 16-bit timer 1. Input glitch filter (10 ns) capable.
PIO0_28/DTR/SSEL1/	2	-	-	[3]	I/O	I; PU	PIO0_28 — General purpose digital input/output pin.
CT32B0_CAP0					0	-	DTR — Data Terminal Ready output for USART.
					I/O	-	SSEL1 — Slave Select for SSP1.
					I	-	CT32B0_CAP0 — Capture input 0 for 32-bit timer 0.
PIO0_29/DSR/SCK1/	13	-	-	[3]	I/O	I; PU	PIO0_29 — General purpose digital input/output pin.
CT32B0_CAP1					I	-	DSR — Data Set Ready input for USART.
					I/O	-	SCK1 — Serial clock for SSP1.
					I	-	CT32B0_CAP1 — Capture input 1 for 32-bit timer 0.



Table 4. LPC11Axx pin description table

Symbol	Pin	/Bal			Type	Reset state	Description
	LQFP48	HVQFN33	WLCSP20				
PIO0_30/RI/MOSI1/ CT32B0_MAT0/ CT16B0_CAP0	40	-	-	[3]	I/O	I; PU	PIO0_30 — General purpose digital input/output pin.
					I	-	RI — Ring Indicator input for USART.
011000_0/110					I/O	-	MOSI1 — Master Out Slave In for SSP1.
					0	-	CT32B0_MAT0 — Match output 0 for 32-bit timer 0.
					I	-	CT16B0_CAP0 — Capture input 0 for 16-bit timer 0.
PIO0_31/RI/MOSI1/	24	-	-	[3]	I/O	I; PU	PIO0_31 — General purpose digital input/output pin.
CT32B1_MAT0/ CT16B1_CAP1					l	-	RI — Ring Indicator input for USART.
011001_0/11					I/O	-	MOSI1 — Master Out Slave In for SSP1.
					0	-	CT32B1_MAT0 — Match output 0 for 32-bit timer 1.
					I	-	CT16B1_CAP1 — Capture input 1 for 16-bit timer 1.
PIO1_0/DCD/SCK0/	31	-	-	[3]	I/O	I; PU	PIO1_0 — General purpose digital input/output pin.
CT32B1_MAT3/ CT16B0_MAT1					I	-	DCD — Data Carrier Detect input for USART.
CTT0B0_WATT					I/O	-	SCK0 — Serial clock for SSP0.
					0	-	CT32B1_MAT3 — Match output 3 for 32-bit timer 1.
					0	-	CT16B0_MAT1 — Match output 1 for 16-bit timer 0.
PIO1_1/DTR/SSEL0/	36	-	-	[3]	I/O	I; PU	PIO1_1 — General purpose digital input/output pin.
CT32B1_MAT3/ CT16B1_MAT0					0	-	DTR — Data Terminal Ready output for USART.
					I/O	-	SSEL0 — Slave Select for SSP0.
					0	-	CT32B1_MAT3 — Match output 3 for 32-bit timer 1.
					0	-	CT16B1_MAT0 — Match output 0 for 16-bit timer 1.
PIO1_2/DSR/MISO0/	37	-	-	[3]	I/O	I; PU	PIO1_2 — General purpose digital input/output pin.
CT16B1_MAT2/ CT16B1_MAT1					I	-	DSR — Data Set Ready input for USART.
CTIODI_WATT					I/O	-	MISO0 — Master In Slave Out for SSP0.
					0	-	CT16B1_MAT2 — Match output 2 for 16-bit timer 1.
					0	-	CT16B1_MAT1 — Match output 1 for 16-bit timer 1.
PIO1_3/RI/MOSI0/	48	-	-	[3]	I/O	I; PU	PIO1_3 — General purpose digital input/output pin.
CT16B1_CAP0					I	-	RI — Ring Indicator input for USART.
					I/O	-	MOSI0 — Master Out Slave In for SSP0.
					I	-	CT16B1_CAP0 — Capture input 0 for 16-bit timer 1.
PIO1_4/RXD/SSEL1/	19	-	-	[3]	I/O	I; PU	PIO1_4 — General purpose digital input/output pin.
CT32B0_MAT1/ CT32B1_CAP0/					I	-	RXD — Receiver data input for USART.
CT32BT_CAP0/ CT16B0_CAP1					I/O	-	SSEL1 — Slave Select for SSP1.
_					0	-	CT32B0_MAT1 — Match output 1 for 32-bit timer 0.
					I	-	CT32B1_CAP0 — Capture input 0 for 32-bit timer 1.
					I	-	CT16B0_CAP1 — Capture input 1 for 16-bit timer 0.



Table 4. LPC11Axx pin description table

Symbol Pin/Ball						Reset state	Description
	LQFP48	HVQFN33	WLCSP20				
PIO1_5/TXD/SCK1/	20	-	-	[3]	I/O	I; PU	PIO1_5 — General purpose digital input/output pin.
CT32B0_MAT2/ CT32B1_CAP1/					0	-	TXD — Transmitter data output for USART.
CT32BT_CAPT/					I/O	-	SCK1 — Serial clock for SSP1.
					0	-	CT32B0_MAT2 — Match output 2 for 32-bit timer 0.
					I	-	CT32B1_CAP1 — Capture input 1 for 32-bit timer 1.
					I	-	CT16B0_CAP2 — Capture input 2 for 16-bit timer 0.
PIO1_6/RTS/MOSI1/	11	-	-	[3]	I/O	I; PU	PIO1_6 — General purpose digital input/output pin.
CT32B0_MAT3/					0	-	RTS — Request To Send output for USART.
CT32B1_CAP2/ CT16B0_MAT0					I/O	-	MOSI1 — Master Out Slave In for SSP1.
					0	-	CT32B0_MAT3 — Match output 3 for 32-bit timer 0.
					I	-	CT32B1_CAP2 — Capture input 2 for 32-bit timer 1.
					0	-	CT16B0_MAT0 — Match output 0 for 16-bit timer 0.
PIO1_7/CTS/MOSI0/ CT32B1_MAT1/ CT16B0_MAT2/ CT16B1_CAP2	25	-	-	[3]	I/O	I; PU	PIO1_7 — General purpose digital input/output pin.
					I	-	CTS — Clear To Send input for USART.
					I/O	-	MOSI0 — Master Out Slave In for SSP0.
					0	-	CT32B1_MAT1 — Match output 1 for 32-bit timer 1.
					0	-	CT16B0_MAT2 — Match output 2 for 16-bit timer 0.
					I	-	CT16B1_CAP2 — Capture input 2 for 16-bit timer 1.
PIO1_8/RXD / MISO1/	26	-	-	[3]	I/O	I; PU	PIO1_8 — General purpose digital input/output pin.
CT32B1_MAT0/ CT16B1_MAT1					I	-	RXD — Receiver data input for USART.
CTTODI_WATT					I/O	-	MISO1 — Master In Slave Out for SSP1.
					0	-	CT32B1_MAT0 — Match output 0 for 32-bit timer 1.
					0	-	CT16B1_MAT1 — Match output 1 for 16-bit timer 1.
PIO1_9/DCD/R/	12	-	-	[3]	I/O	I; PU	PIO1_9 — General purpose digital input/output pin.
CT32B1_MAT2 / CT16B1_MAT2					I	-	DCD — Data Carrier Detect input for USART.
OTTODI_WATE					-	-	R — Reserved.
					0	-	CT32B1_MAT2 — Match output 2 for 32-bit timer 1.
					0	-	CT16B1_MAT2 — Match output 2 for 16-bit timer 1.
XTALIN	6	4	-	[11]	-	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	7	5	-	[11]	-	-	Output from the oscillator amplifier.
V _{DD(IO)}	8	6	E2	[12] [13]	-	-	3.3 V input/output supply voltage.

Table 4. LPC11Axx pin description table

Symbol	Pin/E	Ball		Туре	Reset state	Description
	LQFP48	HVQFN33	WLCSP20			
V _{SS(IO)}	5 3	33	E3 [<u>14</u>]	-	-	Ground.
V _{DD(3V3)}	44 2	29	E2 [12] [13]	-	-	3.3 V supply voltage to the analog blocks, internal regulator, and internal clock generator circuits. Also used as the ADC reference voltage.
V _{SS}	42 3	33	E3 [<u>14</u>]	-	-	Ground.

- [1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled; IA = inactive, no pull-up/down enabled.
- [2] See Figure 32 for the reset configuration.
- [3] 5 V tolerant pin providing standard digital I/O functions with configurable modes and configurable hysteresis (Figure 31).
- [4] I²C-bus pins compliant with the I²C-bus specification for I²C standard mode, I²C Fast-mode, and I²C Fast-mode Plus.
- [5] For the SWD function, a pull-up resistor is recommended for the SWCLK pin (WLCSP20 parts only).
- [6] For the SWD function, a pull-up resistor is recommended for the SWDIO pin (WLCSP20 parts only).
- [7] Not a 5 V tolerant pin due to special analog functionality. Pin provides standard digital I/O functions with configurable modes, configurable hysteresis, and analog I/O. When configured as an analog I/O, the digital section of the pin is disabled (Figure 31).
- [8] If this pin is configured for its VDDCMP function, it cannot be used for SWCLK when the part is on the board. The bypass filter of the power supply filters out the SWCLK clock input signal.
- [9] 5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog I/O. When configured as an analog I/O, digital section of the pin is disabled, and the pin is not 5 V tolerant (Figure 31).
- [10] I²C-bus pins are standard digital I/O pins and have limited performance and electrical characteristics compared to the full I²C-bus specification. Pins can be configured with an on-chip pull-up resistor (pMOS device) and with open-drain mode. In this mode, typical bit rates of up to 100 kbit/s with 20 pF load are supported if the internal pull-ups are enabled. Higher bit rates can be achieved with an external resistor.
- [11] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating. See Section 12.3 if an external clock is connected to the XTALIN pin.
- [12] If separate supplies are used for V_{DD(3V3)} and V_{DD(IO)}, ensure that the power supply pins are filtered for noise with respect to their corresponding grounds V_{SS} and V_{SS(IO)} (LQFP48 package). Using separate filtered supplies reduces the noise to the analog blocks (see also Section 12.1).
- [13] If separate supplies are used for V_{DD(3V3)} and V_{DD(IO)}, ensure that the voltage difference between both supplies is smaller than or equal to 0.5 V.
- [14] Thermal pad (HVQFN33 pin package). Connect to ground.

32-bit ARM Cortex-M0 microcontroller

7. Functional description

7.1 ARM Cortex-M0 processor

The ARM Cortex-M0 is a general purpose, 32-bit microprocessor, which offers high performance and very low power consumption.

7.2 On-chip flash program memory

The LPC11Axx contain up to 32 kB of on-chip flash program memory.

7.3 On-chip EEPROM data memory

The LPC11Axx contain up to 4 kB of on-chip EEPROM data memory.

Remark: The top 64 bytes of the 4 kB EEPROM memory are reserved and cannot be written to. The entire EEPROM is writable for smaller EEPROM sizes.

7.4 On-chip SRAM

The LPC11Axx contain a total of 8 kB, 4 kB, or 2 kB on-chip static RAM data memory.

7.5 On-chip ROM

The on-chip ROM contains the boot loader and the following Application Programming Interfaces (API):

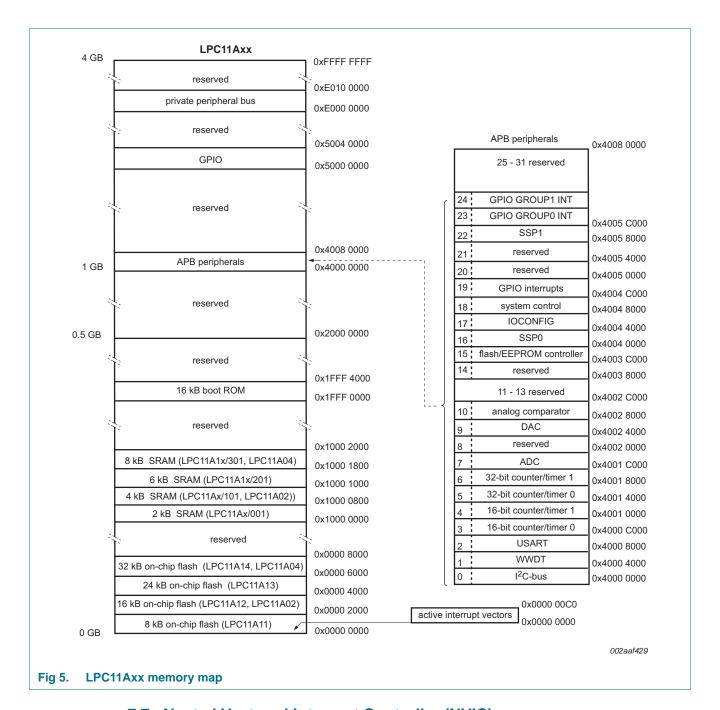
- In-System Programming (ISP) and In-Application Programming (IAP) support for flash programming
- Power profiles for configuring power consumption and PLL settings
- 32-bit integer division routines
- I²C-bus driver routines

7.6 Memory map

The LPC11Axx incorporates several distinct memory regions, shown in the following figures. Figure 5 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The AHB peripheral area is 2 MB in size, and is divided to allow for up to 128 peripherals. The APB peripheral area is 512 kB in size and is divided to allow for up to 32 peripherals. Each peripheral of either type is allocated 16 kB of space. This allows simplifying the address decoding for each peripheral.

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7.7 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is an integral part of the Cortex-M0. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.7.1 Features

- Controls system exceptions and peripheral interrupts.
- In the LPC11Axx, the NVIC supports 32 vectored interrupts including up to 8 inputs to the start logic from the individual GPIO pins.

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- Four programmable interrupt priority levels with hardware priority level masking.
- Software interrupt generation.

7.7.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Up to eight GPIO pins, regardless of the selected function, can be programmed to generate an interrupt on a level, or rising edge or falling edge, or both. The interrupt generating GPIOs can be selected from the GPIO pins with a configurable input glitch filter.

7.8 IOCON block

The IOCON block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Peripherals should be connected to the appropriate pins prior to being activated and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

Up to 16 pins can be configured with a digital input glitch filter for removing voltage glitches with widths of 10 ns or less (see <u>Table 3</u> and <u>Table 4</u>), two pins (PIO0_2 and PIO0_3) can be configured with a 50 ns digital input glitch filter.

7.9 Fast general purpose parallel I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC11Axx use accelerated GPIO functions:

- GPIO registers are a dedicated AHB peripheral so that the fastest possible I/O timing can be achieved.
- An entire port value can be written in one instruction.

Additionally, any GPIO pin (total of up to 42 pins) providing a digital function can be programmed to generate an interrupt on a level, a rising or falling edge, or both.

7.9.1 Features

- Bit level port registers allow a single instruction to set and clear any number of bits in one write operation.
- · Direction control of individual bits.
- All I/O default to inputs with pull-up resistors enabled after reset except for the I²C-bus true open-drain pins PIO0_2 and PIO0_3.
- Pull-up/pull-down configuration, repeater, and open-drain modes can be programmed through the IOCON block for each GPIO pin (see <u>Figure 31</u> and <u>Figure 32</u> for functional diagrams).

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 Control of the digital output slew rate allowing to switch more outputs simultaneously without degrading the power/ground distribution of the device.

7.10 USART

The LPC11Axx contains one USART.

Support for RS-485/9-bit mode allows both software address detection and automatic address detection using 9-bit mode.

The USART includes a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

7.10.1 Features

- Maximum USART data bit rate of 3.125 MBit/s.
- 16-byte Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- FIFO control mechanism that enables software flow control implementation.
- Support for RS-485/9-bit mode.
- Supports a full modem control handshake interface.
- Support for synchronous mode.

7.11 SSP serial I/O controller

The LPC11Axx contain two SSP controllers.

The SSP controller is capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

7.11.1 Features

- Maximum SSP speed of 25 Mbit/s (master) or 4.17 Mbit/s (slave) (in SPI mode)
- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor Microwire buses
- Synchronous serial communication
- Master or slave operation
- 8-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame

7.12 I²C-bus serial I/O controller

The LPC11Axx contains one I²C-bus controller.

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The I²C-bus is bidirectional for inter-IC control using only two wires: a serial clock line (SCL) and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I²C is a multi-master bus and can be controlled by more than one bus master connected to it.

Remark: On the WLCSP package, the bootloader configures the open-drain pins (PIO0_2 and PIO0_3) for the Serial Wire Debug (SWD) function.

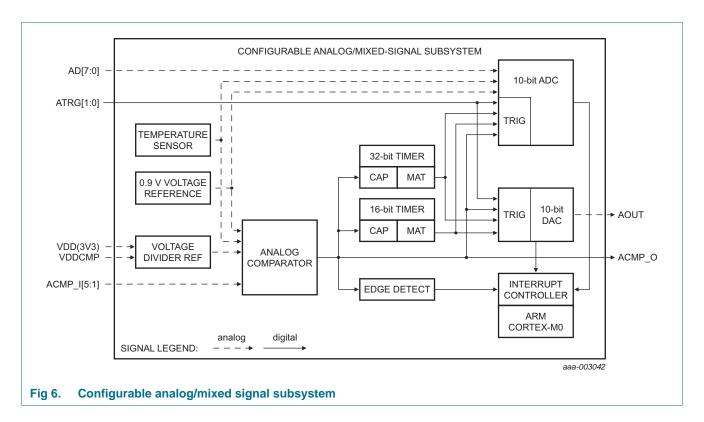
7.12.1 Features

- The I²C-interface is a standard I²C-bus compliant interface with open-drain pins (PIO0_2 and PIO0_3). The I²C-bus interface also supports Fast-mode Plus with bit rates up to 1 Mbit/s.
- The true open-drain pins PIO0_2 and PIO0_3 can be configured with a 50 ns digital input glitch filter.
- If the true open-drain pins are used for other purposes, a limited-performance I²C-bus interface can be configured from a choice of six GPIO pins configured in open-drain mode and with a pull-up resistor. In this mode, typical bit rates of up to 100 kbit/s with 20 pF load are supported if the internal pull-ups are enabled. Higher bit rates can be achieved with an external resistor.
- Easy to configure as master, slave, or master/slave.
- ROM-based I²C-bus driver routines to easily create applications.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I²C-bus can be used for test and diagnostic purposes.
- The I²C-bus controller supports multiple address recognition and a bus monitor mode.

7.13 Configurable analog/mixed-signal subsystems

Multiple analog/mixed-signal subsystems can be configured by software from interconnected digital and analog peripherals. See <u>Figure 6</u>.

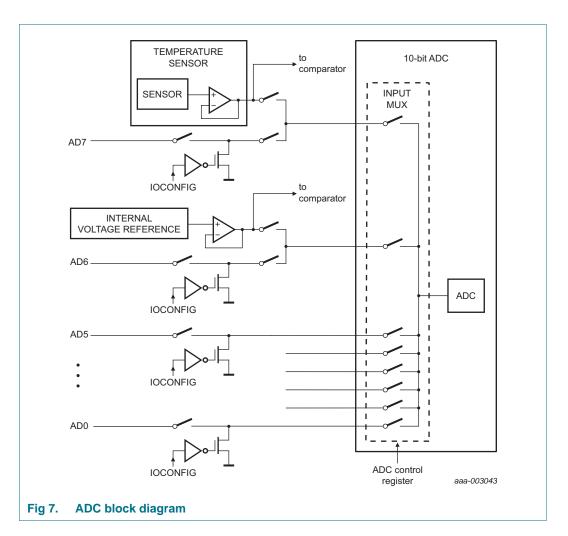
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7.14 10-bit ADC

The LPC11Axx contains one ADC. It is a single 10-bit successive approximation ADC with eight channels.

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7.14.1 Features

- 10-bit successive approximation ADC.
- Input multiplexing among 8 pins.
- Power-down mode.
- Measurement range 0 V to V_{DD(3V3)}.
- 10-bit conversion time ≥ 2.44 µs (up to 400 kSamples/s).
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition of input pins ATRG0 or ATRG1, timer match signal, or comparator output. (Input signals must be held for a minimum of three system clock periods). Also see Section 12.2.
- Individual result registers for each ADC channel to reduce interrupt overhead.

7.15 Internal voltage reference

The internal voltage reference is an accurate 0.9 V and is the output of a low voltage band gap circuit. A typical value at T_{amb} = 25 °C is 0.903 V and varies typically only ± 3 mV over the 0 °C to 85 °C temperature range (see <u>Table 21</u> and <u>Figure 27</u>). The internal voltage reference can be used in the following applications:

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- When the supply voltage V_{DD(3V3)} is known accurately, the internal voltage reference
 can be used to reduce the offset error E_O of the ADC code output. The ADC error
 correction then increases the accuracy of temperature sensor voltage output
 measurements.
- When the ADC is accurately calibrated, the internal voltage reference can be used to measure the power supply voltage. This requires calibration by recording the ADC code of the internal voltage reference at different power supply levels yielding a different ADC code value for each supply voltage level. In a particular application, the internal voltage reference can be measured and the actual power supply voltage can be determined from the stored calibration values. The calibration values can be stored in the EEPROM for easy access.

After power-up and after switching the input channels of the ADC or the comparator, the internal voltage reference must be allowed to settle to its stable value before it can be used as an ADC reference voltage input. Settling times are given in <u>Table 21</u>.

For an accurate measurement of the internal voltage reference by the ADC, the ADC must be configured in single-channel burst mode. The last value of a nine-conversion (or more) burst provides an accurate result.

7.16 Temperature sensor

The temperature sensor transducer uses an intrinsic pn-junction diode reference and outputs a CTAT voltage (Complement To Absolute Temperature). The output voltage varies inversely with device temperature with an absolute accuracy of better than ± 3 °C over the full temperature range (-40 °C to +85 °C). The temperature sensor is only approximately linear with a slight curvature. The output voltage is measured over different ranges of temperatures and fit with linear-least-square lines. See <u>Table 23</u> and <u>Figure 28</u>. For a voltage to temperature conversion, the temperature for a given voltage is calculated using the parameters of the linear-least-square line (see <u>Table 23</u>).

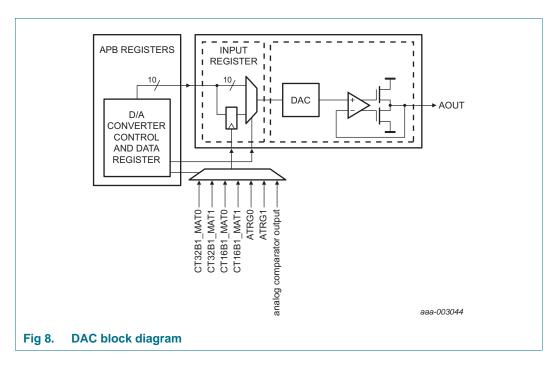
After power-up and after switching the input channels of the ADC or the comparator, the temperature sensor output must be allowed to settle to its stable value before it can be used as an accurate ADC input. Settling times are given in Table 22.

For an accurate measurement of the temperature sensor by the ADC, the ADC must be configured in single-channel burst mode. The last value of a nine-conversion (or more) burst provides an accurate result.

7.17 10-bit DAC

The DAC allows generation of a variable, rail-to-rail analog output.

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7.17.1 Features

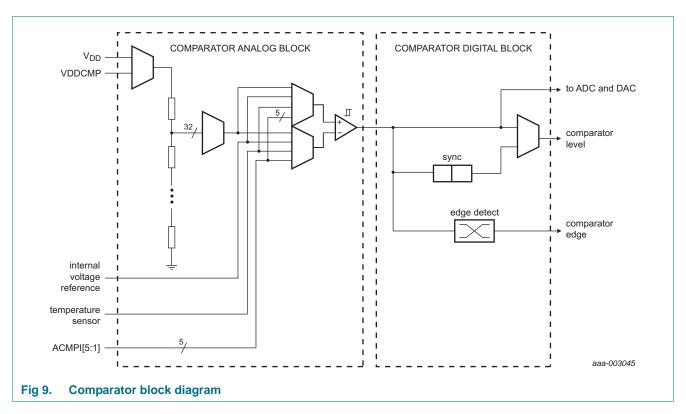
- 10-bit DAC.
- Resistor string architecture.
- Buffered output.
- Power-down mode.
- Conversion speed controlled via a programmable bias current.
- Optional output update modes:
 - write operations to the DAC register.
 - a transition of pins ATRG0 or ATRG1. Input signals must be held for a minimum of three system clock periods.
 - a timer match signal.
 - a comparator output signal held for a minimum of two system clock periods.
- Holds output value during Sleep mode if the DAC is not powered down.

7.18 Analog comparator

The analog comparator with selectable hysteresis can compare voltage levels on external pins and internal voltages. See <u>Table 24</u>.

After power-up and after switching the input channels of the comparator, the output of the voltage ladder must be allowed to settle to its stable value before it can be used as a comparator reference input. Settling times are given in Table 25.

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7.18.1 Features

- Selectable 0 mV, 10 mV (\pm 5 mV), and 20 mV (\pm 10 mV), 40 mV (\pm 20 mV) input hysteresis.
- Five selectable external voltages; fully configurable on either positive or negative input channel.
- Internal voltage reference from band gap and temperature sensor selectable on either positive or negative input channel.
- 32-stage voltage ladder with the internal reference voltage selectable on either the positive or the negative input channel. See <u>Table 24</u> to <u>Table 26</u>.
- Voltage ladder source voltage is selectable from an external pin or the main 3.3 V supply voltage rail.
- Voltage ladder can be separately powered down for applications only requiring the comparator function.
- Interrupt output is connected to NVIC.
- Comparator level output is connected to output pin ACMP_O.
- Comparator output is internally connected to the ADC and DAC and can be used to trigger a conversion.
- The comparator output is also connected internally to capture channel 3 on each of the 32-bit and 16-bit counter/timers.

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7.19 General purpose external event counter/timers

The LPC11Axx includes two 32-bit counter/timers and two 16-bit counter/timers. The counter/timer is designed to count cycles of the system derived clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. Each counter/timer also includes four capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.19.1 Features

- A 32-bit/16-bit timer/counter with a programmable 32-bit/16-bit prescaler.
- Counter or timer operation.
- Four capture channels per timer, that can take a snapshot of the timer value when an
 input signal transitions. A capture event may also generate an interrupt. Up to three
 capture channels are pinned out. One channel is internally connected to the
 comparator output ACMP_O.
- Four match registers per timer that allow:
 - Continuous operation with optional interrupt generation on match.
 - Stop timer on match with optional interrupt generation.
 - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
 - Set LOW on match.
 - Set HIGH on match.
 - Toggle on match.
 - Do nothing on match.

7.20 System tick timer

The ARM Cortex-M0 includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a fixed time interval (typically 10 ms).

7.21 Windowed WatchDog Timer (WWDT)

The purpose of the watchdog is to reset the controller if software fails to periodically service it within a programmable time window.

7.21.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.

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- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from $(T_{cy(WDCLK)} \times 256 \times 4)$ to $(T_{cy(WDCLK)} \times 2^{24} \times 4)$ in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source can be selected from the internal RC oscillator (IRC), or the dedicated watchdog oscillator (WDOsc). This gives a wide range of potential timing choices of watchdog operation under different power conditions.

7.22 Clocking and power control

7.22.1 Crystal and internal oscillators

The LPC11Axx include four independent oscillators.

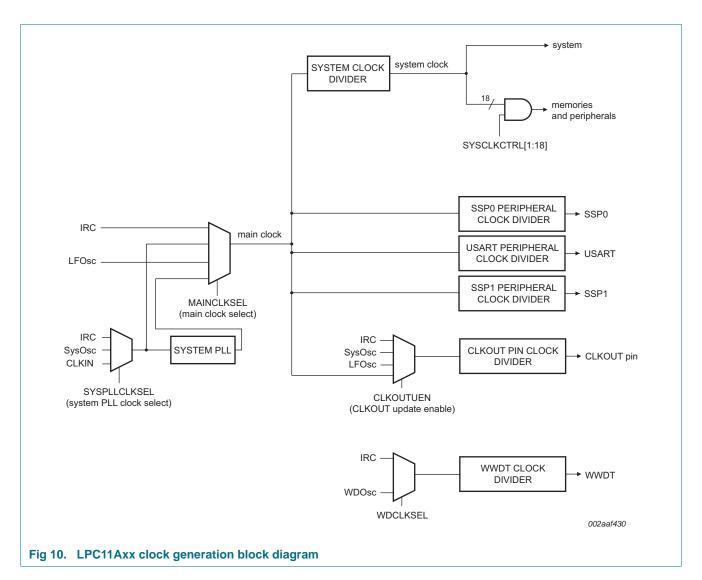
- 1. The crystal oscillator (SysOsc) operating at frequencies between 1 MHz and 25 MHz.
- 2. The internal RC Oscillator (IRC) with a fixed frequency of 12 MHz, trimmed to 1% accuracy.
- 3. The internal low-power, Low-Frequency Oscillator (LFOsc) with a programmable nominal frequency between 9.4 kHz and 2.3 MHz with 40% accuracy.
- 4. The dedicated Watchdog Oscillator (WDOsc) with a programmable nominal frequency between 9.4 kHz and 2.3 MHz with 40% accuracy.

Each oscillator, except the WDOsc, can be used for more than one purpose as required in a particular application.

Following reset, the LPC11Axx will operate from the IRC until switched by software. This allows systems to operate without any external crystal and the bootloader code to operate at a known frequency.

See Figure 10 for an overview of the LPC11Axx clock generation.

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7.22.1.1 Internal RC Oscillator (IRC)

The IRC may be used as the clock source for the WWDT, and/or as the clock that drives the PLL and subsequently the CPU. The nominal IRC frequency is 12 MHz. The IRC is trimmed to 1 % accuracy over the entire voltage and temperature range.

The IRC can be used as a clock source for the CPU with or without using the PLL. The IRC frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

Upon power-up or any chip reset, the LPC11Axx use the IRC as the clock source. Software may later switch to one of the other available clock sources.

7.22.1.2 Crystal Oscillator (SysOsc)

The crystal oscillator can be used as the clock source for the CPU, with or without using the PLL.

The SysOsc operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

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7.22.1.3 Internal Low-Frequency Oscillator (LFOsc) and Watchdog Oscillator (WDOsc)

The LFOsc and the WDOsc are identical internal oscillators. The nominal frequency is programmable between 9.4 kHz and 2.3 MHz. The frequency spread over silicon process variations is \pm 40%.

The WDOsc is a dedicated oscillator for the windowed WWDT.

The LFOsc can be used as a clock source that directly drives the CPU or the CLKOUT pin.

7.22.2 Clock input

A 3.3 V external clock source (25 MHz typical) can be supplied on the selected CLKIN pin or a 1.8 V external clock source can be supplied on the XTALIN pin (see Section 12.3).

7.22.3 System PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100 μ s.

7.22.4 Clock output

The LPC11Axx features a clock output function that routes the IRC, the SysOsc, the LFOsc, or the main clock to an output pin.

7.22.5 Wake-up process

The LPC11Axx begin operation at power-up by using the IRC as the clock source. This allows chip operation to resume quickly. If the SysOsc, the external clock source, or the PLL is needed by the application, software will need to enable these features and wait for them to stabilize before they are used as a clock source.

7.22.6 Power control

The LPC11Axx supports the ARM Cortex-M0 Sleep mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals, allowing fine tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides even better power control.

7.22.6.1 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

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In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

7.22.6.2 Power profiles

The power consumption in Active and Sleep modes can be optimized for the application through simple calls to the power profile. The power configuration routine configures the LPC11Axx for one of the following power modes:

- Default mode corresponding to power configuration after reset.
- CPU performance mode corresponding to optimized processing capability.
- Efficiency mode corresponding to optimized balance of current consumption and CPU performance.
- Low-current mode corresponding to lowest power consumption.

In addition, the power profile includes routines to select the optimal PLL settings for a given system clock and PLL input clock.

7.23 System control

7.23.1 UnderVoltage LockOut (UVLO) protection

The BOD and POR circuits remain enabled at all times to provide UVLO protection from an unexpected power supply droop below a typical threshold level of 2.4 V (see also the *LPC11Axx user manual*). UVLO protection means that the LPC11Axx is held in reset whenever the supply voltage falls below 2.4 V.

See also Section 10.1 "Power supply fluctuations", Section 12.7 "UVLO protection and reset timer circuit", and Section 12.8 "Guidelines for selecting a power supply filter for UVLO protection".

7.23.2 Reset

Reset has several sources on the LPC11Axx: the RESET pin, the Watchdog reset, power-on reset (POR), the ARM SYSRESETREQ software request, and the Brown-Out Detection (BOD) circuit. After the BOD and the POR resets are released, the internal reset timer counts for 100 µs until the internal reset is removed.

Assertion of chip reset by any source (after the operating voltage attains a usable level) starts the IRC and initializes the flash memory controller.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

Writing to a special function register allows the software to reset the following peripherals: the I²C-bus interface, the USART, both SSP controllers, the four counter/timers, the comparator, the ADC, and the DAC.

The RESET pin is a Schmitt trigger input pin and uses a special pad. See Figure 32.

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7.23.3 Brown-out detection

The LPC11Axx include two programmable levels for monitoring the voltage on the $V_{DD(3V3)}$ pin. If this voltage falls below the selected level, the BOD asserts an interrupt signal to the NVIC. This signal can be enabled for interrupt in the Interrupt Enable Register in the NVIC in order to cause a CPU interrupt; alternatively, software can monitor the signal by reading a dedicated status register. In addition, the BOD circuit supports one hardware controlled voltage level for triggering a chip reset.

7.23.4 Code security (Code Read Protection - CRP)

This feature of the LPC11Axx allows user to enable different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System-Programming (ISP) can be restricted. When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by the CRP.

In addition, ISP entry via the PIO0_1 pin can be disabled without enabling CRP. For details see the *LPC11Axx user manual*.

There are three levels of Code Read Protection:

- CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors can not be erased.
- 2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
- 3. Running an application with level CRP3 selected fully disables any access to the chip via the SWD pins and the ISP. This mode effectively disables ISP override using PIO0_1 pin, too. It is up to the user's application to provide (if needed) flash update mechanism using IAP calls or call reinvoke ISP command to enable flash update via the USART.

CAUTION



If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

In addition to the three CRP levels, sampling of pin PIO0_1 for valid user code can be disabled. For details see the *LPC11Axx user manual*.

7.23.5 APB interface

The APB peripherals are located on one APB bus.

7.23.6 AHBLite

The AHBLite connects the CPU bus of the ARM Cortex-M0 to the flash memory, the main static RAM, and the Boot ROM.

7.23.7 External interrupt inputs

All GPIO pins can be level or edge sensitive interrupt inputs.

7.24 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M0. JTAG and Serial Wire Debug (SWD) with four breakpoints and two watchpoints are supported.

The RESET pin selects between the JTAG boundary scan (RESET = LOW) and the ARM SWD debug (RESET = HIGH). The ARM SWD debug port is disabled while the LPC11Axx is in reset.

To perform boundary scan testing, follow these steps:

- 1. Erase any user code residing in flash.
- 2. Power up the part with the RESET pin pulled HIGH externally.
- 3. Wait for at least 250 µs.
- 4. Pull the RESET pin LOW externally.
- 5. Perform boundary scan operations.
- 6. Once the boundary scan operations are completed, assert the TRST pin to enable the SWD debug mode and release the RESET pin (pull HIGH).

Remark: The JTAG interface cannot be used for debug purposes.

On the WLCSP package, the TCK signal is shared with the VDDCMP input on pin PIO0_5. To perform a boundary scan on a blank device, make sure that the PIO0_5 pin is not filtered on the board. The bypass filter usually added to the comparator voltage reference input (VDDCMP) filters out the SWCLK/TCK input signal.

For SWD debug, an alternative TCK/SWCLK clock pin is available on pin PIO0_2. This is the default function after booting for the WLCSP package.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DD(3V3)}	supply voltage (3.3 V)		2.6	3.6	V
$V_{DD(IO)}$	input/output supply voltage		2.6	3.6	V
Vı	input voltage	5 V tolerant I/O pins; only valid when the V _{DD(IO)} supply voltage is present	[2][3] -0.5	+5.5	V
		3 V tolerant I/O pins without over-voltage protection	[4] -0.5	$V_{DD(IO)}$	V
I_{DD}	supply current	per supply pin	-	100	mA
I _{SS}	ground current	per ground pin	-	100	mA
l _{latch}	I/O latch-up current	$-(0.5V_{DD(IO)}) < V_I < (1.5V_{DD(IO)});$ $T_j < 125 ^{\circ}C$	-	100	mA
T _{stg}	storage temperature		[<u>5]</u> –65	+150	°C
T _{j(max)}	maximum junction temperature		-	150	°C
P _{tot(pack)}	total power dissipation (per package)	based on package heat transfer, not device power consumption	-	1.5	W
V _{esd}	electrostatic discharge voltage	human body model; all pins	[6] -6.5	+6.5	kV

- [1] The following applies to the limiting values:
 - a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.
 - b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.
- 2] Applies to all 5 V tolerant I/O pins except true open-drain pins PIO0_2 and PIO0_3 and except the 3 V tolerant pins PIO0_4 and PIO0_14 (LQFP and HVQFN packages) or PIO0_5 (WLCSP package).
- [3] Including voltage on outputs in 3-state mode.
- [4] Applies to 3 V tolerant pins PIO0_4 and PIO0_14 (LQFP and HVQFN packages) or PIO0_5 (WLCSP package).
- [5] Dependent on package type.
- [6] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 k Ω series resistor.

9. Static characteristics

Table 6. Static characteristics

 $T_{amb} = -40$ °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V _{DD(3V3)}	supply voltage (3.3 V)			2.6	3.3	3.6	V
$V_{DD(IO)}$	input/output supply voltage			2.6	3.3	3.6	V
DD	supply current	Active mode; code					
		while(1){}					
		executed from flash; $V_{DD(3V3)} = V_{DD(IO)} = 3.3 \text{ V};$ low-current mode (see Section 7.22.6.2)					
		system clock = 12 MHz; all peripherals disabled	[2][4][5]	-	3	-	mA
		system clock = 48 MHz; all peripherals disabled	[2][6][5]	-	8	-	mA
		Sleep mode; system clock = 12 MHz; $V_{DD(3V3)} = V_{DD(IO)} = 3.3 \text{ V};$ power mode 0 (see Section 7.22.6.2)					
		all peripherals disabled; 12 MHz	[2][4][5]	-	2	-	mA
		all peripherals disabled; 48 MHz	[2][4][5]	-	5	-	mΑ
Standard po	ort pins, RESET						
I _{IL}	LOW-level input current	V _I = 0 V; on-chip pull-up resistor disabled		-	0.5	1000	nA
Іш	HIGH-level input current	V _I = V _{DD(IO)} ; on-chip pull-down resistor disabled		-	0.5	1000	nA
l _{oz}	OFF-state output current	V _O = 0 V; V _O = V _{DD(IO)} ; on-chip pull-up/down resistors disabled		-	0.5	1000	nA
V _I	input voltage	pin configured to provide a digital function	[7][8]	0	-	5.0	V
		5 V tolerant pins					
		3 V tolerant pins: PIO0_4 and PIO0_14 (LQFP and HVQFN packages) or PIO0_5 (HVQFN package)	<u>[7][8]</u>			$V_{DD(IO)}$	
Vo	output voltage	output active		0	-	$V_{DD(IO)}$	V
V _{IH}	HIGH-level input voltage			$0.7V_{DD(IO)}$	-	-	V
				-	-	0.3V _{DD(IO)}	V
V _{IL}	LOW-level input voltage					0.0 (10)	

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 Table 6.
 Static characteristics ...continued

 $T_{amb} = -40$ °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V _{OH}	HIGH-level output voltage	$2.6~V \leq V_{DD(IO)} \leq 3.6~V; \\ I_{OH} = -4~mA$		0.85V _{DD(IO)}	-	-	V
V_{OL}	LOW-level output voltage	$2.6~V \leq V_{DD(IO)} \leq 3.6~V;$ $I_{OL} = 4~mA$		-	-	0.15V _{DD(IO)}	V
I _{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)} - 0.4 \text{ V};$ 2.6 V \le V_{DD(IO)} \le 3.6 V		-4	-	-	mA
I _{OL}	LOW-level output current	$V_{OL} = 0.4 \text{ V}$ 2.6 V \le V_{DD(IO)} \le 3.6 V		4	-	-	mA
I _{OHS}	HIGH-level short-circuit output current	V _{OH} = 0 V	<u>[9]</u>	-	-	-45	mA
I _{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD(IO)}$	<u>[9]</u>	-	-	50	mA
I _{pd}	pull-down current	V _I = 5 V	[10]	10	50	150	μΑ
I _{pu}	pull-up current	$V_I = 0 \text{ V};$ 2.6 V \le V_{DD(IO)} \le 3.6 V		-15	-50	-85	μΑ
		$V_{DD(IO)} < V_I < 5 \text{ V}$		0	0	0	μΑ
High-drive o	utput pin (PIO0_21)	DD(10) 1 -					
I _{IL}		V _I = 0 V; on-chip pull-up resistor disabled		-	0.5	10	nA
I _{IH}	HIGH-level input current	$V_I = V_{DD(IO)}$; on-chip pull-down resistor disabled		-	0.5	10	nA
l _{OZ}	OFF-state output current	V _O = 0 V; V _O = V _{DD(IO)} ; on-chip pull-up/down resistors disabled		-	0.5	10	nA
V _I	input voltage	pin configured to provide a digital function	[7][8]	0	-	5.0	V
Vo	output voltage	output active		0	-	$V_{DD(IO)}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD(IO)}$	-	-	V
V _{IL}	LOW-level input voltage			-	-	$0.3V_{DD(IO)}$	V
V _{hys}	hysteresis voltage			0.4	-	-	V
V _{OH}	HIGH-level output voltage	$2.6 \text{ V} \le \text{V}_{\text{DD(IO)}} \le 3.6 \text{ V};$ $\text{I}_{\text{OH}} = -20 \text{ mA}$		V _{DD(IO)} – 0.4	-	-	V
		$2.6 \text{ V} \leq \text{V}_{\text{DD(IO)}} < 2.5 \text{ V};$ $\text{I}_{\text{OH}} = -12 \text{ mA}$		V _{DD(IO)} – 0.4	-	-	V
V _{OL}	LOW-level output voltage	$ 2.6 \text{ V} \leq \text{V}_{DD(IO)} \leq 3.6 \text{ V}; $ $\text{I}_{OL} = 4 \text{ mA} $		-	-	0.4	V
I _{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)} - 0.4 \text{ V};$ 2.6 V \le V_{DD(IO)} \le 3.6 V		20	-	-	mA
I _{OL}	LOW-level output current	$V_{OL} = 0.4 \text{ V}$ 2.6 V \le V_{DD(IO)} \le 3.6 V		4	-	-	mA

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 Table 6.
 Static characteristics ...continued

 $T_{amb} = -40$ °C to +85 °C, unless otherwise specified.

arrib	,	•					
Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I _{OHS}	HIGH-level short-circuit output current	$V_{OH} = 0 V$	[9]	-	-	-160	mA
I _{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD(IO)}$	[9]	-	-	50	mA
I _{pd}	pull-down current	$V_I = 5 V$		10	50	150	μΑ
I _{pu}	pull-up current	$V_{I} = 0 \text{ V}$ $2.6 \text{ V} \leq V_{DD(IO)} \leq 3.6 \text{ V}$		-15	-50	-85	μА
		$V_{DD(IO)} < V_I < 5 V$		0	0	0	μΑ
I ² C-bus pins (PIO0_2 and PIO0_3)						
V_{IH}	HIGH-level input voltage			$0.7V_{DD(IO)}$	-	-	V
V _{IL}	LOW-level input voltage			-	-	$0.3V_{DD(IO)}$	V
V_{hys}	hysteresis voltage			-	$0.05V_{DD(IO)}$	-	V
l _{OL}	LOW-level output current	V _{OL} = 0.4 V; I ² C-bus pins configured as standard mode pins		4	-	-	mA
		$2.6~V \leq V_{DD(IO)} \leq 3.6~V$					
I _{OL}	LOW-level output current	$V_{OL} = 0.4 \text{ V}$; $I^2\text{C-bus pins}$ configured as high-current sink pins		20	-	-	mA
		$2.6~V \leq V_{DD(IO)} \leq 3.6~V$					
I _{LI}	input leakage current	$V_I = V_{DD(IO)}$	[11]	-	2	4	μΑ
		$V_I = 5 V$		-	10	22	μΑ
Oscillator pin	s						
V _{i(xtal)}	crystal input voltage			-0.5	1.8	1.95	V
V _{o(xtal)}	crystal output voltage			-0.5	1.8	1.95	V

^[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 $^{\circ}$ C), nominal supply voltages.

- [6] IRC disabled; SysOsc enabled; system PLL enabled.
- [7] Including voltage on outputs in 3-state mode.
- [8] All supply voltages must be present.
- [9] Allowed as long as the current limit does not exceed the maximum current allowed by the device.
- [10] Does not apply to 3 V tolerant pins PIO0_4 and PIO0_14 (LQFP and HVQFN packages) or PIO0_5 (HVQFN package).
- [11] To V_{SS} .

^[2] $T_{amb} = 25 \, ^{\circ}C$.

^[3] I_{DD} measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled.

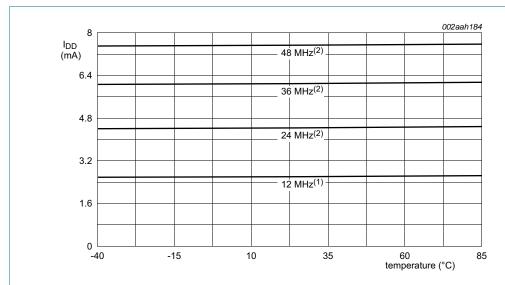
^[4] IRC enabled; SysOsc disabled; system PLL disabled.

^[5] All digital peripherals disabled in the SYSCLKCTRL register except ROM, RAM, and flash. Peripheral clocks to USART and SSP0/1 disabled in system configuration block. Analog peripherals disabled in the PDRUNCFG register except flash memory.

9.1 Power consumption

Power measurements in Active and Sleep modes were performed under the following conditions (see *LPC11Axx user manual*):

- Configure all pins as GPIO with pull-up resistor disabled in the IOCON block.
- · Configure GPIO pins as outputs using the GPIOnDIR registers.
- Write 0 to all GPIO DIR registers to drive the outputs LOW.

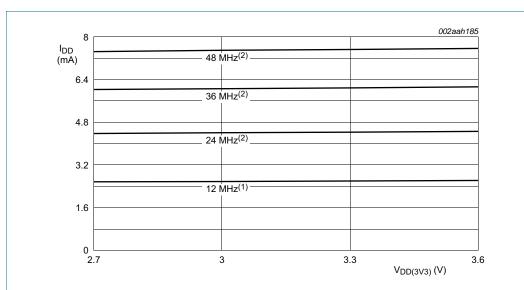


Conditions: $V_{DD(3V3)} = 3.3 \text{ V}$; active mode entered executing code while(1){} from flash; all peripherals disabled in the SYSAHBCLKCTRL register; all peripheral clocks disabled; all analog peripherals disabled in the PDRUNCFG register; low-current mode (see Section 7.22.6.2).

- (1) SysOsc and system PLL disabled; IRC enabled.
- (2) SysOsc and system PLL enabled; IRC disabled.

Fig 11. Active mode: Typical supply current I_{DD} versus temperature for different system clock frequencies (all peripherals disabled)

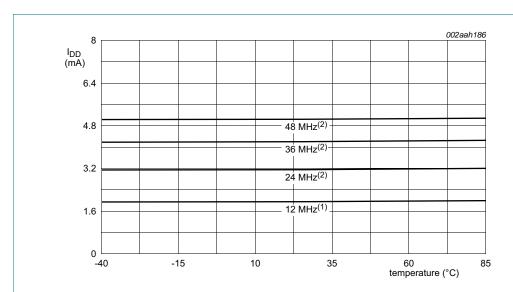
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Conditions: $T_{amb} = 25 \,^{\circ}\text{C}$; active mode entered executing code while(1){} from flash; all peripherals disabled in the SYSAHBCLKCTRL register; all peripheral clocks disabled; all analog peripherals disabled in the PDRUNCFG register; low-current mode (see Section 7.22.6.2).

- (1) SysOsc and system PLL disabled; IRC enabled.
- (2) SysOsc and system PLL enabled; IRC disabled.

Fig 12. Active mode: Typical supply current I_{DD} versus core voltage $V_{DD(3V3)}$ for different system clock frequencies (all peripherals disabled)



Conditions: $V_{DD(3V3)} = 3.3 \text{ V}$; sleep mode entered from flash; all peripherals disabled in the SYSAHBCLKCTRL register and PDRUNCFG register; all peripheral clocks disabled; BOD disabled; low-current mode (see Section 7.22.6.2).

- (1) SysOsc and system PLL disabled; IRC enabled.
- (2) SysOsc and system PLL enabled; IRC disabled.

Fig 13. Sleep mode: Typical supply current I_{DD}versus temperature for different system clock frequencies (all peripherals disabled)

9.2 Peripheral power consumption

The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code is executed. Measured on a typical sample at $T_{amb} = 25\,^{\circ}\text{C}$.

Table 7. Power consumption for individual analog and digital blocks

Peripheral	Typical supply current in mA	
	12 MHz[1]	Average μA/MHz
Analog peripherals		
BOD	0.05	-
BOD, comparator	0.14	-
BOD, comparator, ADC, DAC, temperature sensor	0.40	-
DAC	0.26	-
ADC	0.01	-
Temperature sensor, ADC	0.01	-
Digital peripherals		
USART	0.15	12
I2C	0.02	2
16-bit counter/timer 0/1	0.02	2
32-bit counter/timer 0/1	0.02	2
WWDT	0.02	2

^[1] IRC on; PLL off.

9.3 Electrical pin characteristics

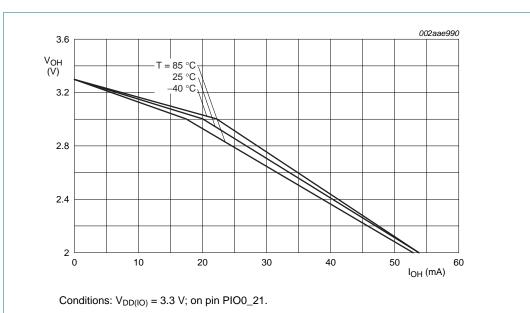


Fig 14. High-current source output driver: Typical HIGH-level output voltage V_{OH} versus HIGH-level output current I_{OH}

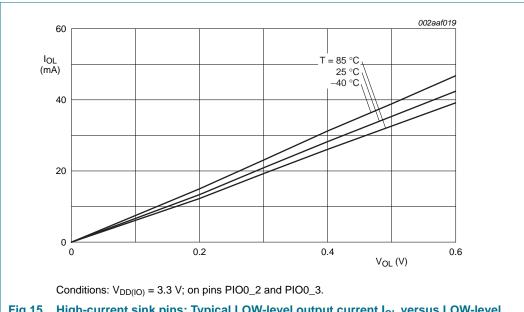
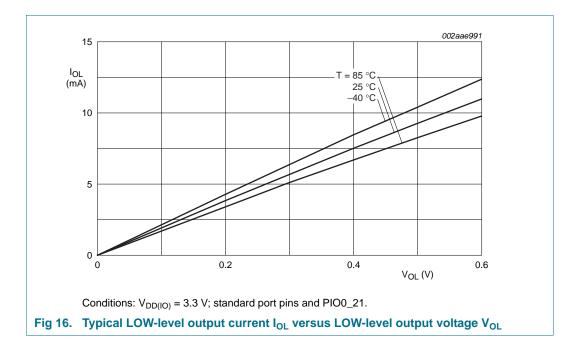
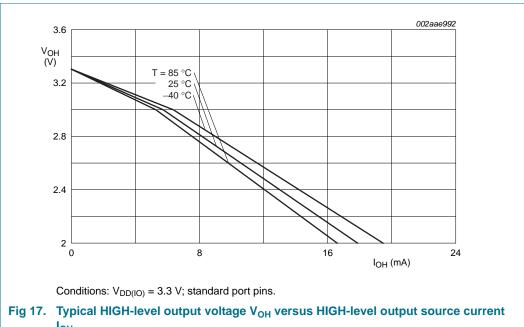
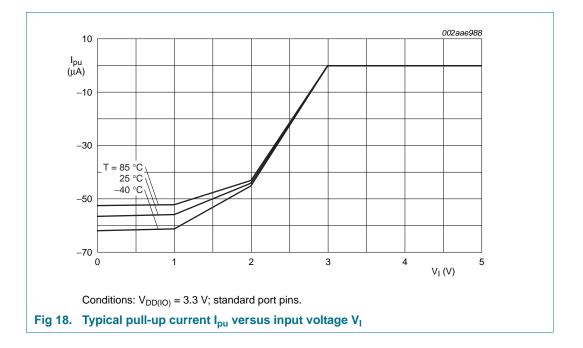


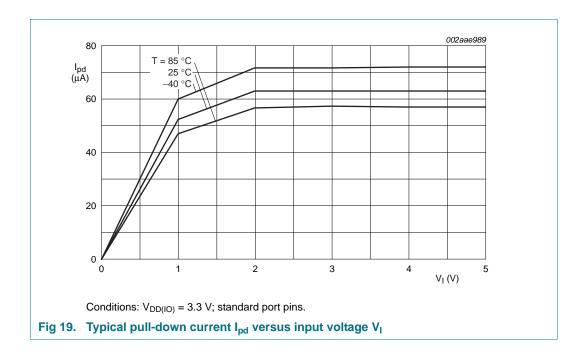
Fig 15. High-current sink pins: Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}





I_{OH}





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10. Dynamic characteristics

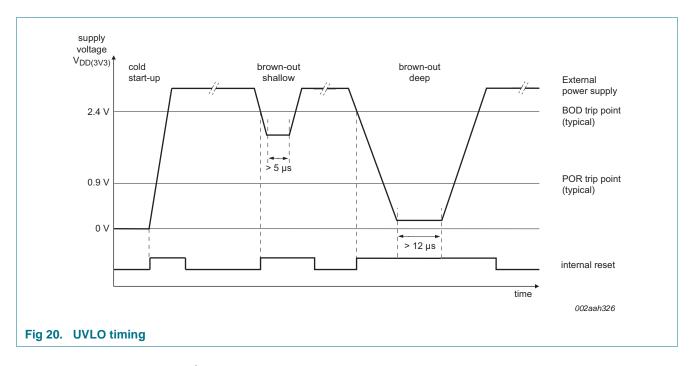
10.1 Power supply fluctuations

If the input voltage $(V_{DD(3V3)})$ to the internal regulator fluctuates, the LPC11Axx is held in reset during a brown-out condition as long as the UVLO circuit is operating. The settling times of the BOD and POR circuits, which constitute the UVLO, determine the minimum time the supply level must remain in the shallow or deep brown-out condition to ensure that the internal reset is asserted properly.

See also Section 7.23.1, Section 12.7, and Section 12.8.

Table 8. UVLO circuits settling characteristics

		_				
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
t _s	settling time	power droop: from active level to shallow brown-out level $(0.9 \ V \le V_{DD(3V3)} \le 2.4 \ V)$	5	-	-	μS
		from active level to deep brown-out level (0 < $V_{DD(3V3)}$ < 0.9 V)	12	-	-	μS



10.2 Flash/EEPROM memory

Table 9. Flash characteristics

 $T_{amb} = -40 \, ^{\circ}\text{C}$ to +85 $^{\circ}\text{C}$. Based on JEDEC NVM qualification. Failure rate < 10 ppm for parts as specified below.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
N_{endu}	endurance		10000	100000	-	cycles

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Table 9. Flash characteristics

 $T_{amb} = -40$ °C to +85 °C. Based on JEDEC NVM qualification. Failure rate < 10 ppm for parts as specified below.

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
t _{ret}	retention time	powered		10	20	-	years
		unpowered		20	40	-	years
t _{er}	erase time	sector or multiple consecutive sectors	[2]	95	100	105	ms
t _{prog}	programming time		<u>[3]</u>	0.95	1	1.05	ms

^[1] Number of program/erase cycles.

Table 10. EEPROM characteristics

 $T_{amb} = -40 \, ^{\circ}\text{C}$ to +85 $^{\circ}\text{C}$; $V_{DD(3V3)} = 2.7 \, \text{V}$ to 3.6 V. Based on JEDEC NVM qualification. Failure rate < 10 ppm for parts as specified below.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
N _{endu}	endurance		100000	1000000	-	cycles
t _{ret}	retention time	powered	100	200	-	years
		unpowered	150	300	-	years
t _{prog}	programming time	64 bytes	-	1.1	-	ms

10.3 External clock for oscillator in slave mode

Remark: The input voltage on the XTALIN/XTALOUT pin must be \leq 1.95 V (see <u>Table 6</u>). For connecting the oscillator to the XTALIN/XTALOUT pins also see <u>Section 12.3</u>.

Table 11. Dynamic characteristic: external clock (XTALIN pin)

 $T_{amb} = -40$ °C to +85 °C; $V_{DD(3V3)}$ over specified ranges.

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
f _{osc}	oscillator frequency		1	-	25	MHz
T _{cy(clk)}	clock cycle time		40	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{\text{cy(clk)}}\times0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{\text{cy(clk)}}\times 0.4$	-	-	ns
t _{CLCH}	clock rise time		-	-	5	ns
t _{CHCL}	clock fall time		-	-	5	ns

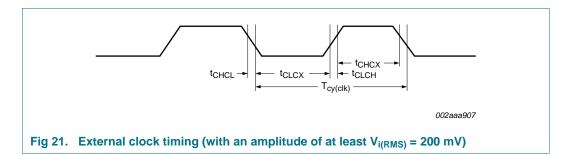
^[1] Parameters are valid over operating temperature range unless otherwise specified.

^[2] Min and max values are valid for T_{amb} = -40 °C to +85 °C only.

^[3] Programming times are given for writing 256 bytes to the flash. Data must be written to the flash in blocks of 256 bytes. Flash programming is accomplished via IAP calls (see *LPC11Axx user manual*). Execution time of IAP calls depends on the system clock and is typically between 1.5 and 2 ms per 256 bytes.

^[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

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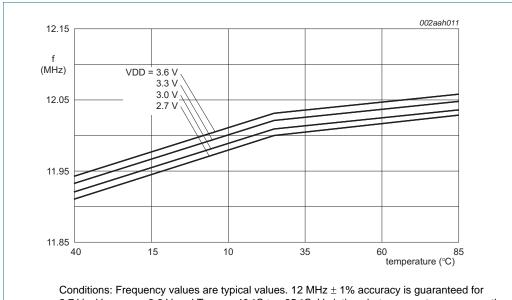
10.4 Internal oscillators

Table 12. Dynamic characteristic: IRC

 $T_{amb} = -40 \text{ °C to } +85 \text{ °C}; 2.7 \text{ V} \le V_{DD(3V3)} \le 3.6 \text{ V.}^{[1]}$

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	-	11.88	12	12.12	MHz

- [1] Parameters are valid over operating temperature range unless otherwise specified.
- [2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.



 $2.7~V \le V_{DD(3V3)} \le 3.6~V$ and $T_{amb} = -40~^{\circ}C$ to +85 $^{\circ}C$. Variations between parts may cause the IRC to fall outside the 12 MHz \pm 1% accuracy specification for voltages below 2.7 V.

Fig 22. Internal IRC frequency vs. temperature

Table 13. Dynamic characteristics: WDOsc and LFOsc

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
f _{osc}	internal oscillator frequency	DIVSEL = 0x1F, FREQSEL = 0x1 in the WDTOSCCTRL register;	[2][3]	-	9.4	-	kHz
		DIVSEL = 0x00, FREQSEL = 0xF in the WDTOSCCTRL register	[2][3]	-	2300	-	kHz

^[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

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- [2] The typical frequency spread over processing and temperature (T_{amb} = -40 °C to +85 °C) is \pm 40%.
- [3] See the LPC11Axx user manual.

10.5 I/O pins

Table 14. Dynamic characteristic: digital I/O pins[1]

 $T_{amb} = -40$ °C to +85 °C; 3.0 V \leq V_{DD(IO)} \leq 3.6 V; load capacitor = 30 pF.

Symbol	Parameter	Conditions	N	Min	Тур	Max	Unit
t _r	rise time	pin configured as output					
		SSO = 1	[2][3] 2	2.5	-	5.0	ns
		SSO = 6	[2][3] 2	2.5	-	4.5	ns
		SSO = 16	<u>[2][4]</u> 3	3.0	-	5.0	ns
t _f	fall time	pin configured as output	[2][3]				
		SSO = 1	2	2.0	-	4.5	ns
		SSO = 6	[2][3] 2	2.0	-	4.5	ns
		SSO = 16	[2][4] 2	2.5	-	5.0	ns

^[1] Applies to standard port pins and RESET pin. Simulated results.

10.6 I²C-bus

Remark: All I²C modes (Standard-mode, Fast-mode, Fast-mode Plus) can be configured for the true open-drain pins PIO0_2 and PIO0_3. If the limited-performance I²C-bus pins are used (I²C-bus functions on standard I/O pins), only Standard-mode with internal pull-up enabled or Fast-mode with external pull-up resistor are supported.

Table 15. Dynamic characteristic: I²C-bus pins[1]

 $T_{amb} = -40 \, ^{\circ}\text{C} \text{ to } +85 \, ^{\circ}\text{C.}$

Symbol	Parameter		Conditions	Min	Max	Unit
f_{SCL}	SCL clock		Standard-mode	0	100	kHz
	frequency		Fast-mode	0	400	kHz
			Fast-mode Plus	0	1	MHz
t _f	fall time	[4][5][6][7]	of both SDA and SCL signals	-	300	ns
			Standard-mode			
			Fast-mode	$20 + 0.1 \times C_b$	300	ns
			Fast-mode Plus	-	120	ns
t_{LOW}	LOW period of		Standard-mode	4.7	-	μS
	the SCL clock		Fast-mode	1.3	-	μS
			Fast-mode Plus	0.5	-	μS

^[2] SSO indicates maximum number of simultaneously switching digital output pins. The pins are optimized for half of the maximum SSO.

^[3] Set SLEW bit in the IOCON register to 1.

^[4] Set SLEW bit in the IOCON register to 0.

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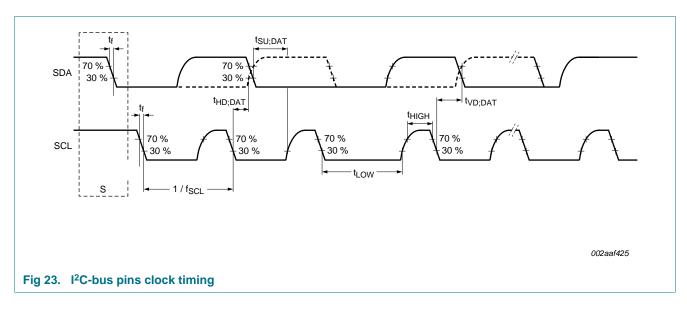
Table 15. Dynamic characteristic: I²C-bus pins[1]

 $T_{amb} = -40 \, ^{\circ}\text{C} \text{ to } +85 \, ^{\circ}\text{C.}$

Symbol	Parameter		Conditions	Min	Max	Unit
t _{HIGH}	HIGH period of	·		4.0	-	μS
	the SCL clock		Fast-mode	0.6	-	μS
		Fast-mode Plus	0.26	-	μS	
t _{HD;DAT}	data hold time	[3][4][8]	Standard-mode	0	-	μS
			Fast-mode	0	-	μS
			Fast-mode Plus	0	-	μS
t _{SU;DAT}	data set-up	[9][10]	Standard-mode	250	-	ns
,	time		Fast-mode	100	-	ns
			Fast-mode Plus	50	-	ns

- [1] See the I²C-bus specification *UM10204* for details.
- [2] Parameters are valid over operating temperature range unless otherwise specified.
- [3] thd: DAT is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.
- [4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- [5] $C_b = \text{total capacitance of one bus line in pF.}$
- [6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.
- [7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.
- [8] The maximum t_{HD;DAT} could be 3.45 μs and 0.9 μs for Standard-mode and Fast-mode but must be less than the maximum of t_{VD;DAT} or t_{VD;ACK} by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.
- [9] tsu;DAT is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.
- [10] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement t_{SU;DAT} = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_{r(max)} + t_{SU;DAT} = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

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10.7 SSP interfaces

Table 16. Dynamic characteristics of SSP pins in SPI mode

 $2.6 \ V \le V_{DD(3V3)} = V_{DD(IO)} \le 3.6 \ V.$

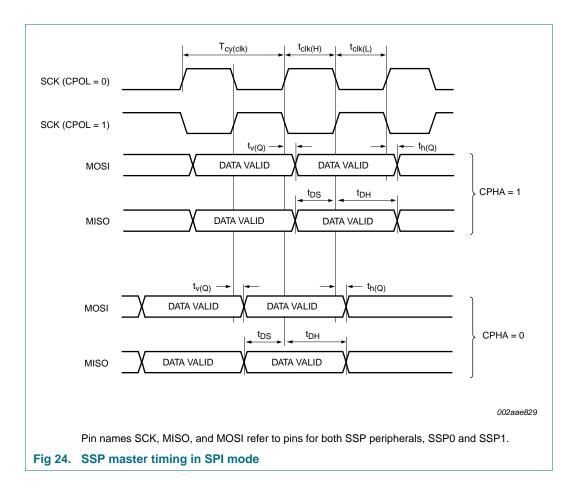
SPI maste T _{cy(clk)}	er (in SPI mode) clock cycle time	full-duplex mode	[1]	50			
T _{cy(clk)}	clock cycle time	·	[1]	50			
		verbana amber tuanamaittina		30	-	-	ns
		when only transmitting	<u>[1]</u>	40			ns
t _{DS}	data set-up time	in SPI mode	[2]	15	-	-	ns
t _{DH}	data hold time	in SPI mode	[2]	0	-	-	ns
$t_{V(Q)}$	data output valid time	in SPI mode	[2]	-	-	10	ns
t _{h(Q)}	data output hold time	in SPI mode	[2]	0	-	-	ns
SPI slave	(in SPI mode)						
T _{cy(PCLK)}	PCLK cycle time			20	-	-	ns
t _{DS}	data set-up time	in SPI mode	[3][4]	0	-	-	ns
t _{DH}	data hold time	in SPI mode	[3][4]	$3 \times T_{cy(PCLK)} + 4$	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[3][4]	-	-	$3 \times T_{cy(PCLK)} + 11$	ns
t _{h(Q)}	data output hold time	in SPI mode	[3][4]	-	-	2 × T _{cy(PCLK)} + 5	ns

^[1] $T_{cy(clk)} = (SSPCLKDIV \times (1 + SCR) \times CPSDVSR) / f_{main}$. The clock cycle time derived from the SPI bit rate $T_{cy(clk)}$ is a function of the main clock frequency f_{main} , the SPI peripheral clock divider (SSPCLKDIV), the SPI SCR parameter (specified in the SSP0CR0 register), and the SPI CPSDVSR parameter (specified in the SPI clock prescale register).

^[2] $T_{amb} = -40 \,^{\circ}\text{C}$ to 85 $^{\circ}\text{C}$.

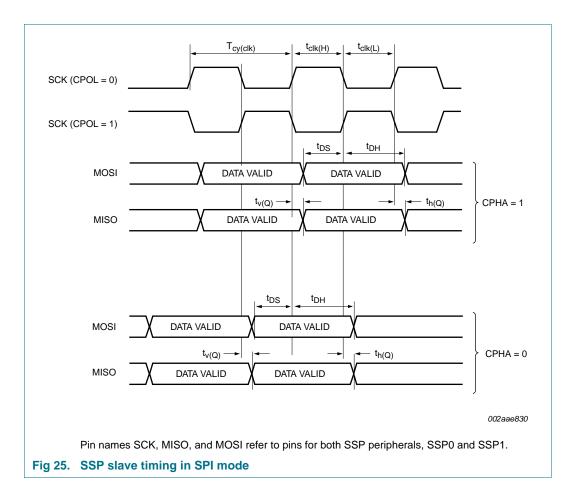
^[3] $T_{cy(clk)} = 12 \times T_{cy(PCLK)}$.

^[4] $T_{amb} = 25$ °C; for normal voltage supply range: $V_{DD(io) = vdd(3v3)} = 3.3$ V.



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11. Characteristics of analog peripherals

Table 17. BOD static characteristics[1]

 $T_{amb} = 25 \, ^{\circ}\text{C}.$

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{th}	threshold voltage					
		interrupt level 2				
		assertion	-	2.52	-	V
		de-assertion	-	2.66	-	V
		interrupt level 3				
		assertion	-	2.80	-	V
		de-assertion	-	2.90	-	V

^[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL, see LPC11Axx user manual.

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Table 18. ADC static characteristics

 T_{amb} = -40 °C to +85 °C unless otherwise specified; ADC frequency 4.5 MHz, $V_{DD(3V3)}$ = 2.7 V to 3.6 V; V_{SS} = 0 V.

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V_{IA}	analog input voltage			0	-	$V_{DD(3V3)}$	V
C _{ia}	analog input capacitance			-	-	4	pF
E _D	differential linearity error		[1][2]	-	-	± 1	LSB
E _{L(adj)}	integral non-linearity		[3]	-	-	± 1.5	LSB
Eo	offset error		<u>[4]</u>	-	-	±20	mV
$V_{err(FS)}$	full-scale error voltage		<u>[5]</u>	-	-	±20	mV
E _T	absolute error		[6]	-	-	± 4	LSB
R _i	input resistance		[7][8]	-	-	2.5	$M\Omega$

- [1] The ADC is monotonic, there are no missing codes.
- [2] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 26.
- [3] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 26.
- [4] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 26.
- [5] The full-scale error voltage or gain error (E_G) is the difference between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 26.
- [6] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 26.
- [7] $T_{amb} = 25$ °C; maximum sampling frequency $f_s = 400$ kSamples/s and analog input capacitance $C_{ia} = 1$ pF.
- [8] Input resistance R_i depends on the sampling frequency f_s : R_i = 1 / ($f_s \times C_{ia}$).

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Table 19. DAC static and dynamic characteristics

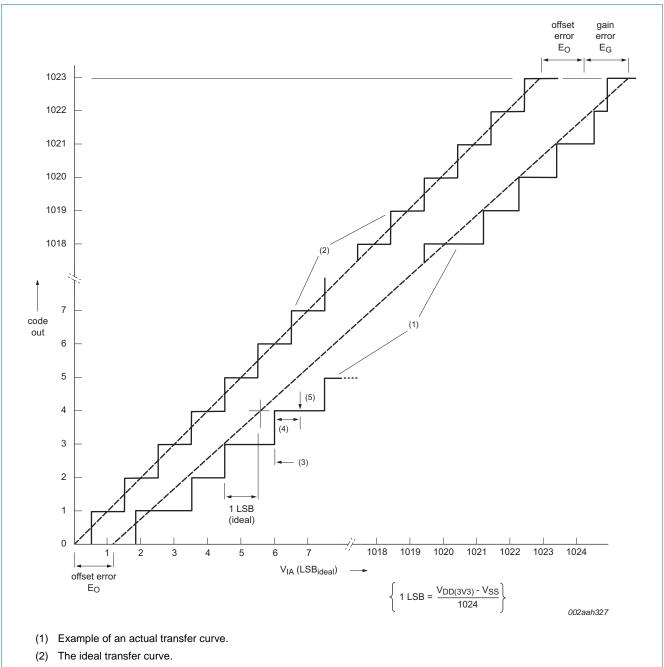
 $V_{DD(3V3)} = 2.7 \text{ V to } 3.6 \text{ V; } T_{amb} = -40 \text{ }^{\circ}\text{C to } +85 \text{ }^{\circ}\text{C unless otherwise specified}$

DD(3V3)							
Symbol	Parameter	Conditions		Min	Тур	Max	Unit
E _D	differential linearity error			-	-	±1	LSB
E _{L(adj)}	integral non-linearity			-	-	±1.5	LSB
Eo	offset error			-	-	0.6	%
E _G	gain error			-	-	0.6	%
C _L	load capacitance			-	-	200	pF
R _L	load resistance			1	-	-	$k\Omega$
R _O	output resistance		[1]	-	< 40		Ω
f _{c(DAC)}	DAC conversion frequency			-	0.4	1	MHz
ts	settling time			-	-	1	μS
Vo	output voltage	Output voltage range with less than 1 LSB deviation; with minimum R _L connected to ground or power supply		0.3	-	V _{DD(3V3)} - 0.3	V
		with minimum R _L connected to ground or power supply		0.175	-	V _{DD(3V3)} - 0.175	V

^[1] Measured on typical samples.

Table 20. DAC sampling frequency range and power consumption

Bias bit	Maximum current	DAC sampling frequency range
0	700 μΑ	0 MHz to 1 MHz
1	350 μΑ	0 MHz to 400 kHz



- (3) Differential linearity error (E_D).
- (4) Integral non-linearity $(E_{L(adj)})$.
- (5) Center of a step of the actual transfer curve.

Fig 26. ADC characteristics

Table 21. Internal voltage reference static and dynamic characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _O output	output voltage	T_{amb} = -40 °C to +85 °C	<u>11</u> 0.855	0.900	0.945	V
		T_{amb} = 70 °C to 85 °C	[2] _	0.906	-	V
		T _{amb} = 50 °C	[2] _	0.905	-	V
		T _{amb} = 25 °C	[<u>3</u>] 0.893	0.903	0.913	V
		T _{amb} = 0 °C	[2] _	0.902	-	V
		$T_{amb} = -20 ^{\circ}C$	[2] _	0.899	-	V
		$T_{amb} = -40 ^{\circ}C$	[2] _	0.896	-	V

- [1] Characterized through simulation.
- [2] Characterized on a typical silicon sample.
- [3] Measured over process variations.

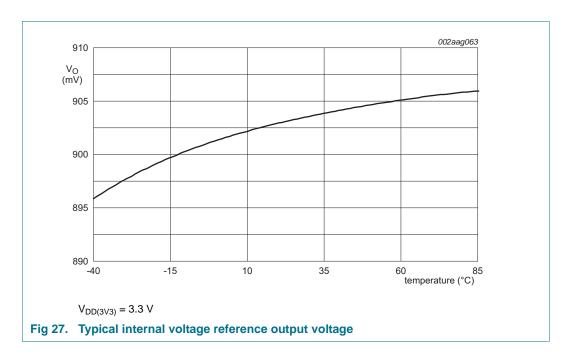


Table 22. Temperature sensor static and dynamic characteristics

 $V_{DD(3V3)} = 2.6 \text{ V to } 3.6 \text{ V}$

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
DT _{sen}	sensor temperature accuracy	$T_{amb} = -40 ^{\circ}\text{C} \text{ to } +85 ^{\circ}\text{C}$	<u>[1]</u> -	-	±3	°C
EL	linearity error	$T_{amb} = -40 ^{\circ}\text{C} \text{ to } +85 ^{\circ}\text{C}$	-	-	±1.1	°C
t _{s(pu)}	power-up settling time	to 99% of temperature sensor output value	[2] _	81	85	μS
t _{s(sw)}	switching settling time	to 99% of temperature sensor output value	[2][3]	1.5	2	μS

^[1] Absolute temperature accuracy.

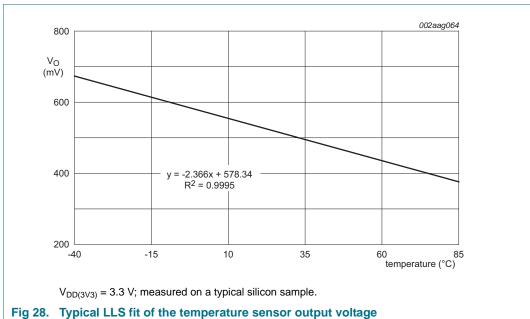
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^[2] Typical values are derived from nominal simulation ($V_{DD(3V3)} = 3.3 \text{ V}$; $T_{amb} = 27 \,^{\circ}\text{C}$; nominal process models). Maximum values are derived from worst case simulation ($V_{DD(3V3)} = 2.6 \text{ V}$; $T_{amb} = 85 \,^{\circ}\text{C}$; slow process models).

[3] Settling time applies to switching between comparator and ADC channels.

Table 23. Temperature sensor Linear-Least-Square (LLS) fit parameters $V_{DD(3V3)} = 2.6 \text{ V to } 3.6 \text{ V}$

Fit parameter	Range	Min	Тур	Max	Unit
LLS slope	$T_{amb} = 0 ^{\circ}C$ to 85 $^{\circ}C$	-	-2.36	-	mV/°C
	$T_{amb} = -40 ^{\circ}\text{C} \text{ to } +85 ^{\circ}\text{C}$	-	-2.36	-	mV/°C
LLS intercept	$T_{amb} = 0 ^{\circ}C$ to 85 $^{\circ}C$	-	577	-	mV
	$T_{amb} = -40 ^{\circ}\text{C} \text{ to } +85 ^{\circ}\text{C}$	-	576	-	mV



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 Table 24.
 Comparator characteristics

 $V_{DD(3V3)}$ = 3.0 V and T_{amb} = 25 °C unless noted otherwise.

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Static cha	aracteristics						
I _{DD}	supply current			-	55	-	μΑ
V_{IC}	common-mode input voltage			0	-	$V_{DD(3V3)}$	V
DV_O	output voltage variation			0	-	$V_{DD(3V3)}$	V
V _{offset}	offset voltage	V _{IC} = 0.1 V		-	-4 to +4.2	-	mV
		V _{IC} = 1.5 V		-	±2	-	mV
		V _{IC} = 2.8 V		-	±2.5		mV
Dynamic	characteristics						
t _{startup}	start-up time	nominal process		-	4	-	μS
t _{PD}	propagation delay	HIGH to LOW; $V_{DD(3V3)} = 3.3 \text{ V}$;					
		V_{IC} = 0.1 V; 50 mV overdrive input	<u>[1]</u>	122	130	142	ns
		V _{IC} = 0.1 V; rail-to-rail input	<u>[1]</u>	173	189	233	ns
		V _{IC} = 1.5 V; 50 mV overdrive input	<u>[1]</u>	101	108	119	ns
		V _{IC} = 1.5 V; rail-to-rail input	<u>[1]</u>	114	127	162	ns
		V _{IC} = 2.9 V; 50 mV overdrive input	<u>[1]</u>	123	134	143	ns
		V _{IC} = 2.9 V; rail-to-rail input	<u>[1]</u>	79	91	120	ns
t _{PD}	propagation delay	LOW to HIGH; $V_{DD(3V3)} = 3.3 \text{ V}$;					
		V_{IC} = 0.1 V; 50 mV overdrive input	[1]	221	232	254	ns
		V _{IC} = 0.1 V; rail-to-rail input	[1]	59	63	68	ns
		V _{IC} = 1.5 V; 50 mV overdrive input	[1]	183	229	249	ns
		V _{IC} = 1.5 V; rail-to-rail input	<u>[1]</u>	147	174	213	ns
		V _{IC} = 2.9 V; 50 mV overdrive input	<u>[1]</u>	171	192	216	ns
		V _{IC} = 2.9 V; rail-to-rail input	<u>[1]</u>	235	305	450	ns
V_{hys}	hysteresis voltage	positive hysteresis; $V_{DD(3V3)} = 3.0 \text{ V}$; $V_{IC} = 1.5 \text{ V}$	[2]	-	5, 10, 20	-	mV
V _{hys}	hysteresis voltage	negative hysteresis; $V_{DD(3V3)} = 3.0 \text{ V}$; $V_{IC} = 1.5 \text{ V}$	[2]	-	5, 10, 20	-	mV
R _{lad}	ladder resistance	-		-	1.034	-	$M\Omega$

^[1] $C_L = 10 \text{ pF}$; results from measurements on silicon samples over process corners and over the full temperature range $T_{amb} = -40 \, ^{\circ}\text{C}$ to +85 $^{\circ}\text{C}$.

^[2] Input hysteresis is relative to the reference input channel and is software programmable.

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Table 25. Comparator voltage ladder dynamic characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
t _{s(pu)}	power-up settling time	to 99% of voltage ladder output value	[1] -	-	30	μS
t _{s(sw)}	switching settling time	to 99% of voltage ladder output value	[1] - [2]	-	15	μS

^[1] Maximum values are derived from worst case simulation (V_{DD(3V3)} = 2.6 V; T_{amb} = 85 °C; slow process models).

Table 26. Comparator voltage ladder reference static characteristics

 $V_{DD(3V3)} = 3.3 \text{ V; } T_{amb} = -40 \text{ °C to} + 85 \text{ °C}.$

DD(3V3)	anib					
Symbol	Parameter	Conditions	Min	Тур	Max[1]	Unit
E _{V(O)}	output voltage error	Internal V _{DD(3V3)} supply				
		decimal code = 00	0	0	0	%
		decimal code = 08	-0.45	-0.5	-0.55	%
		decimal code = 16	-0.99	-1.1	-1.21	%
		decimal code = 24	-1.26	-1.4	-1.54	%
		decimal code = 30	-1.35	-1.5	-1.65	%
		decimal code = 31	-1.35	-1.5	-1.65	%
$E_{V(O)}$	output voltage error	External VDDCMP supply				
		decimal code = 00	0	0	0	%
		decimal code = 08	0.44	0.4	0.36	%
		decimal code = 16	-0.18	-0.2	-0.22	%
		decimal code = 24	-0.45	-0.5	-0.55	%
		decimal code = 30	-0.54	-0.6	-0.66	%
		decimal code = 31	-0.45	-0.5	-0.55	%

^[1] Measured on typical silicon samples with a 2 kHz input signal and overdrive < 100 μ V. Power switched off to all analog peripherals except the comparator.

^[2] Settling time applies to switching between comparator and ADC channels.

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12. Application information

12.1 ADC usage notes

The following guidelines show how to increase the performance of the ADC in a noisy environment beyond the ADC specifications listed in <u>Table 18</u>:

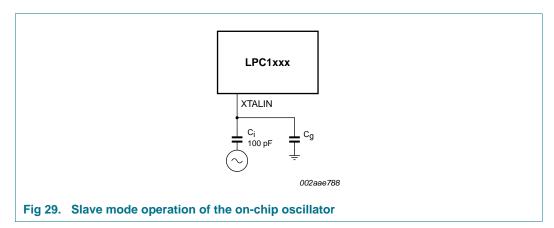
- The ADC input trace must be short and as close as possible to the LPC11Axx chip.
- The ADC input traces must be shielded from fast switching digital signals and noisy power supply lines.
- Because the ADC and the digital core share the same power supply, the power supply line must be adequately filtered.
- To improve the ADC performance in a very noisy environment, put the device in Sleep mode during the ADC conversion.

12.2 Use of ADC input trigger signals

For applications that use trigger signals to start conversions and require a precise sample frequency, ensure that the period of the trigger signal is an integral multiple of the period of the ADC clock.

12.3 XTAL input

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with $C_i = 100$ pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV(RMS) is needed.



In slave mode the input clock signal should be coupled by means of a capacitor of 100 pF (Figure 29), with an amplitude between 200 mV (RMS) and 1000 mV (RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTALOUT pin in this configuration can be left unconnected.

External components and models used in oscillation mode are shown in <u>Figure 30</u> and in <u>Table 27</u> and <u>Table 28</u>. Since the feedback resistance is integrated on chip, only a crystal and the capacitances C_{X1} and C_{X2} need to be connected externally in case of fundamental mode oscillation (the fundamental frequency is represented by L, C_L and

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 R_S). Capacitance C_P in <u>Figure 30</u> represents the parallel package capacitance and should not be larger than 7 pF. Parameters F_{OSC} , C_L , R_S and C_P are supplied by the crystal manufacturer (see <u>Table 27</u>).

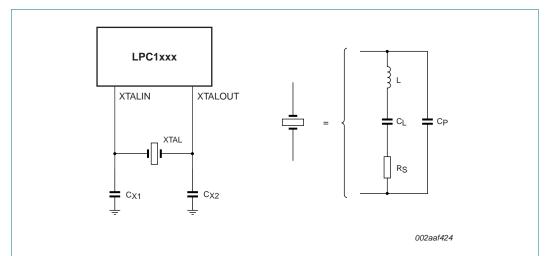


Fig 30. Oscillator modes and models: oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

Table 27. Recommended values for C_{χ_1}/C_{χ_2} in oscillation mode (crystal and external components parameters) low frequency mode

Fundamental oscillation frequency Fosc	Crystal load capacitance C _L	Maximum crystal series resistance R _S	External load capacitors C _{X1} , C _{X2}
1 MHz - 5 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 300 Ω	39 pF, 39 pF
	30 pF	< 300 Ω	57 pF, 57 pF
5 MHz - 10 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 200 Ω	39 pF, 39 pF
	30 pF	< 100 Ω	57 pF, 57 pF
10 MHz - 15 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 60 Ω	39 pF, 39 pF
15 MHz - 20 MHz	10 pF	< 80 Ω	18 pF, 18 pF

Table 28. Recommended values for C_{χ_1}/C_{χ_2} in oscillation mode (crystal and external components parameters) high frequency mode

Fundamental oscillation frequency F _{OSC}	Crystal load capacitance C _L	Maximum crystal series resistance R _S	External load capacitors C _{X1} , C _{X2}
15 MHz - 20 MHz	10 pF	< 180 Ω	18 pF, 18 pF
	20 pF	< 100 Ω	39 pF, 39 pF
20 MHz - 25 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 80 Ω	39 pF, 39 pF

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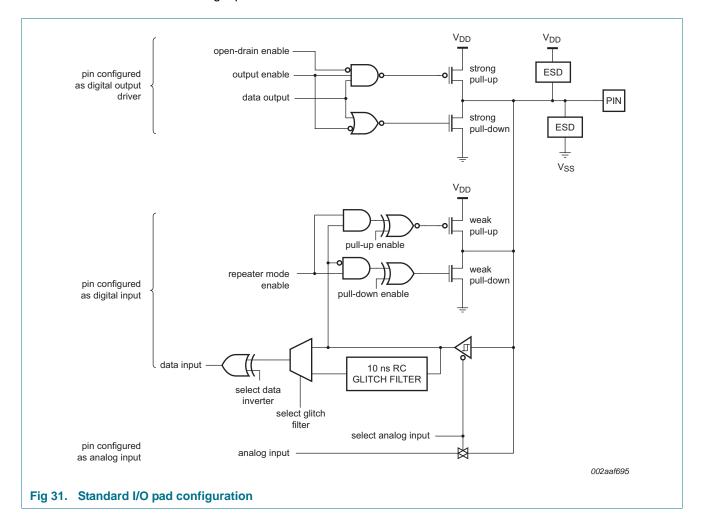
12.4 XTAL Printed Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{x1} , C_{x2} , and C_{x3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plain. Loops must be made as small as possible in order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Values of C_{x1} and C_{x2} should be chosen smaller accordingly to the increase in parasitics of the PCB layout.

12.5 Standard I/O pad configuration

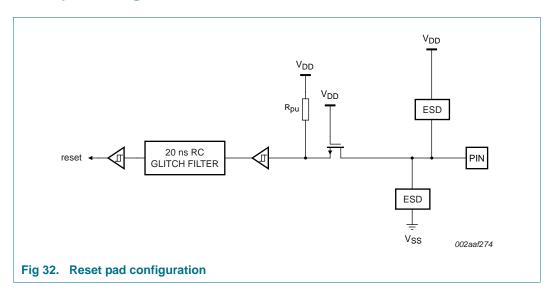
Figure 31 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver with configurable open-drain output
- · Digital input: Pull-up enabled/disabled
- · Digital input: Pull-down enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Digital input: Input glitch filter selectable on 17 pins.
- Analog input

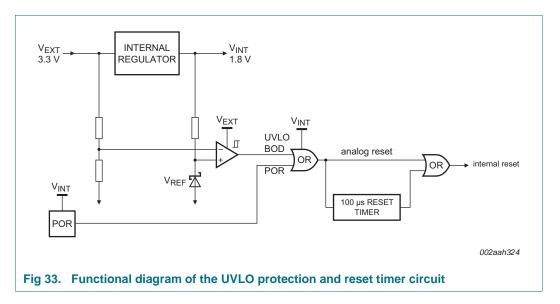


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12.6 Reset pad configuration



12.7 UVLO protection and reset timer circuit



12.8 Guidelines for selecting a power supply filter for UVLO protection

For the UVLO circuits to hold the part in reset during shallow and deep brown-out conditions, you must filter the power supply line to allow for the BOD and POR circuits to settle when short voltage drops occur (see <u>Section 10.1 "Power supply fluctuations"</u>).

Select the capacitance of the decoupling/bypass capacitor according to the following guidelines:

 $C >> I_{DD} \times t_s \! / \! \Delta V_{DD(3V3)}$ with

- $\Delta V_{DD(3V3)} \approx 100$ mV for the voltage drop below the BOD or POR trip points.
- $I_{DD} \approx 3$ mA with the IRC running and PLL/SysOsc off (see Figure 12).

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- $t_s = 5 \mu s$ for shallow brown-out (see <u>Table 8</u>).
- $t_s = 12 \mu s$ for deep brown-out (see <u>Table 8</u>).

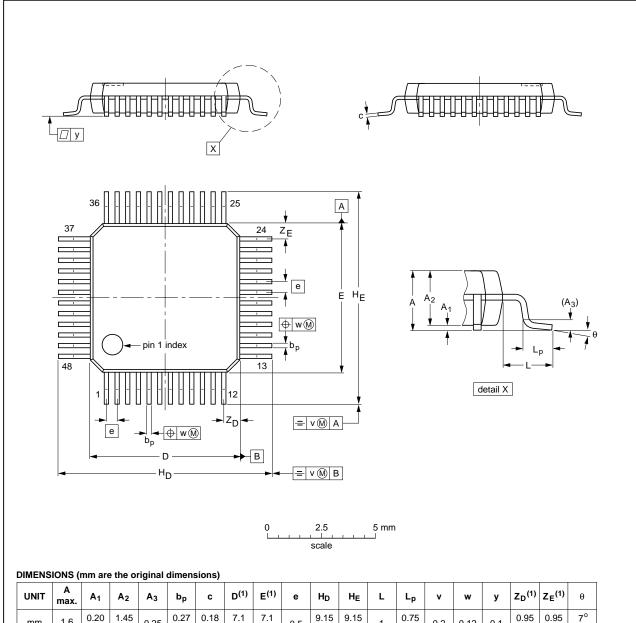
With these parameters, the decoupling/bypass capacitor to add to the supply line is:

- $C >> 0.15 \mu F$ for shallow brown-out
- C >> 0.36 μ F for deep brown-out

13. Package outline

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm

SOT313-2



UNIT	A max.	A ₁	A ₂	А3	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	H _D	HE	L	Lp	v	w	у	Z _D ⁽¹⁾	Z _E ⁽¹⁾	θ	
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7° 0°	

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

	REFER	EUROPEAN	ISSUE DATE			
IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
136E05	MS-026				00-01-19 03-02-25	
		IEC JEDEC		IEC JEDEC JEITA	IEC JEDEC JEITA PROJECTION	

Fig 34. Package outline LQFP48

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HVQFN33: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 x 7 x 0.85 mm

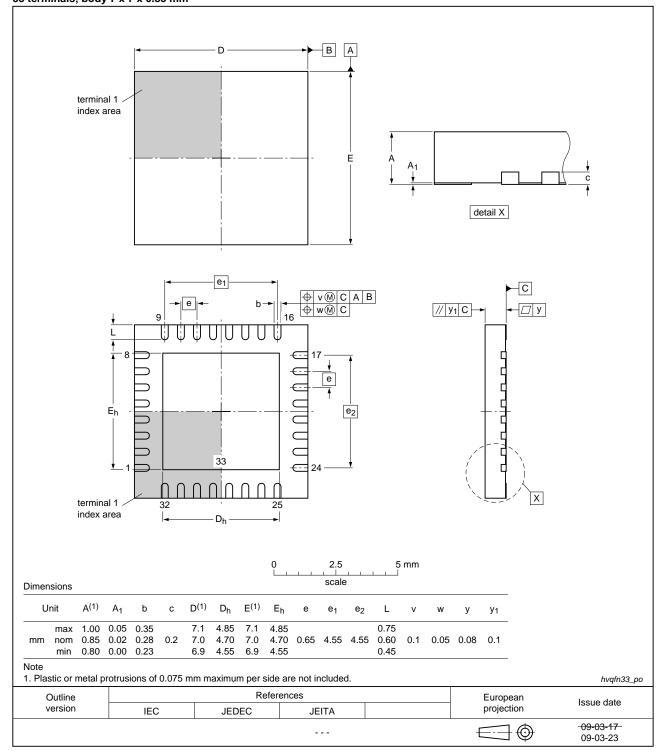


Fig 35. Package outline HVQFN33 (7x7)

HVQFN33: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm

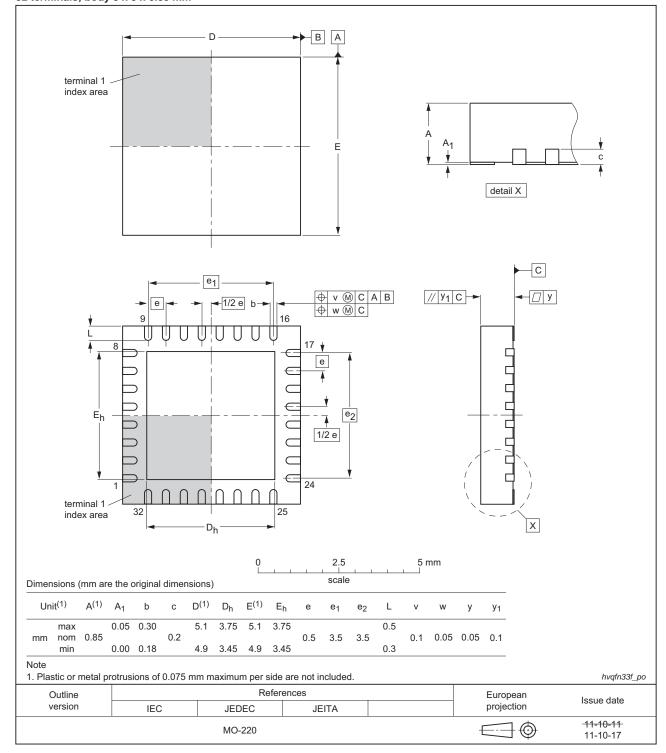


Fig 36. Package outline HVQFN33 (5x5)

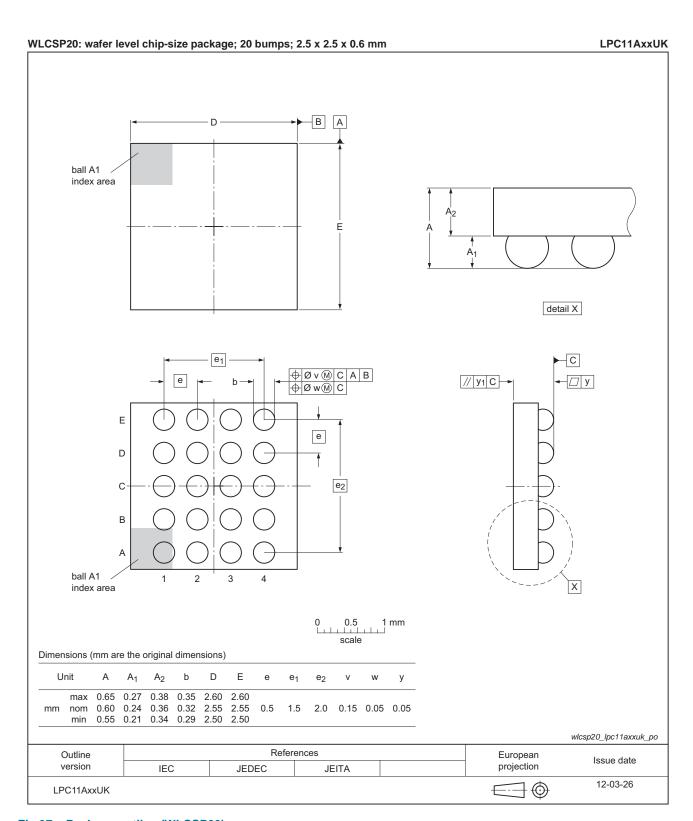
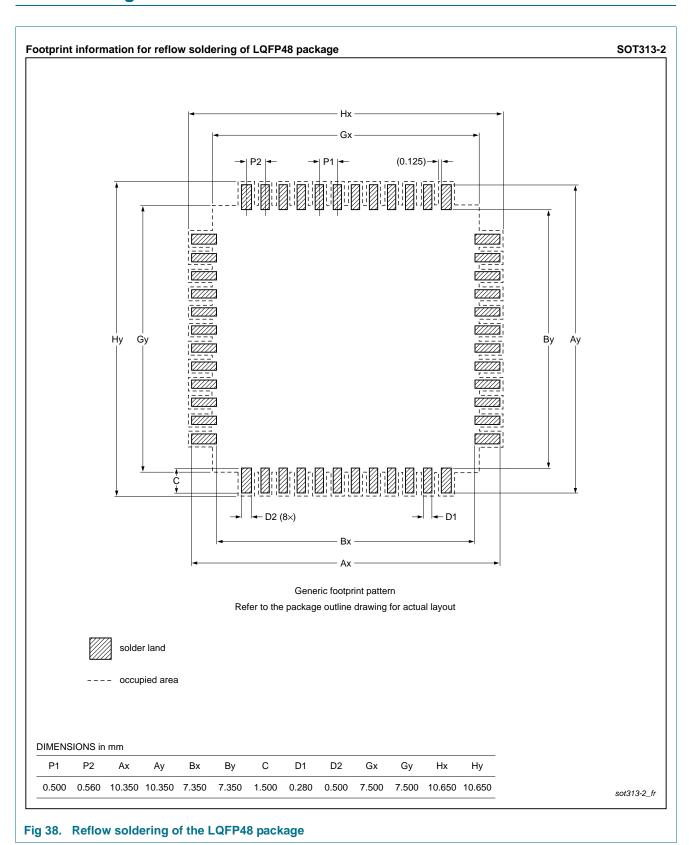
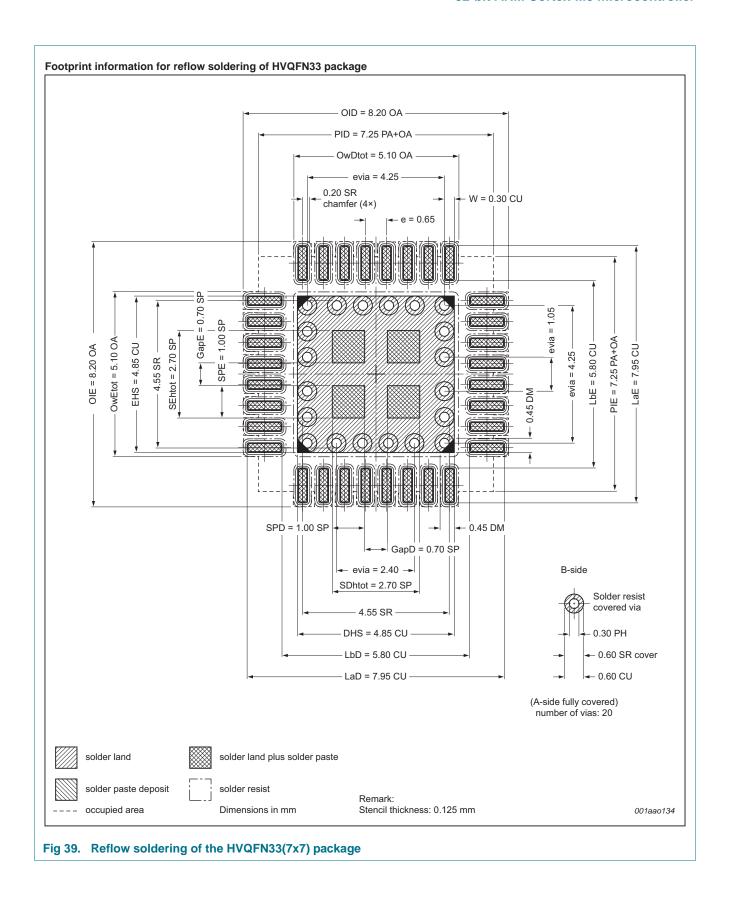


Fig 37. Package outline (WLCSP20)

14. Soldering





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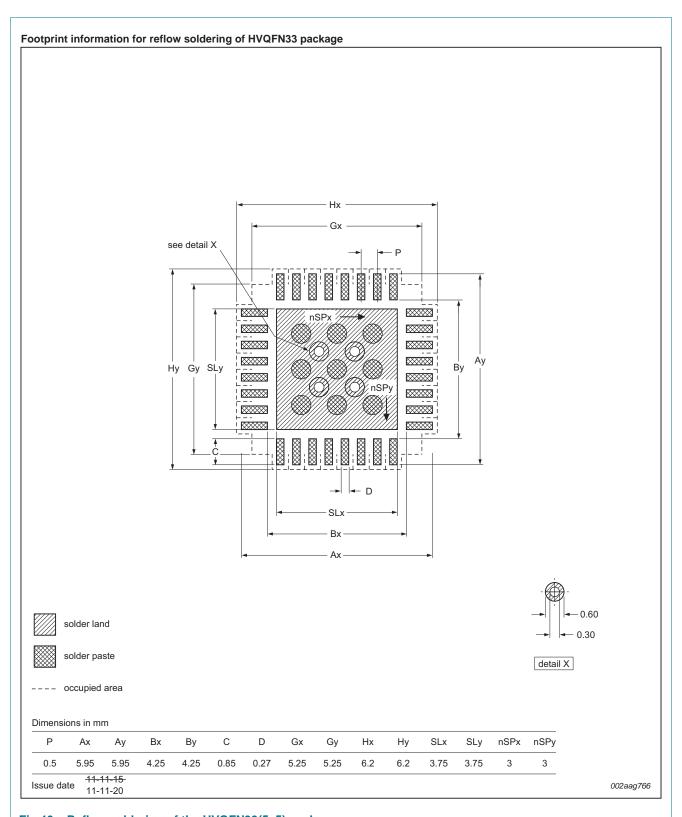


Fig 40. Reflow soldering of the HVQFN33(5x5) package

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15. Abbreviations

Table 29. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
BOD	Brown-Out Detection
GPIO	General Purpose Input/Output
PLL	Phase-Locked Loop
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
TTL	Transistor-Transistor Logic
USART	Universal Synchronous/Asynchronous Receiver/Transmitter
UVLO	Under-Voltage LockOut

16. Revision history

Table 30. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC11AXX v.3	20120907	Product data sheet	-	LPC11AXX v.2.1
	Section 10.	1 abbreviated for clarity.		
		cription including descript	tion of cold start-up	behavior moved to the
	_	user manual.		
				n ground" removed. This in the <i>LPC11Axx user manual</i> .
	 Details regard 	arding boundary scan ad	ded to Section 7.24	#Emulation and debugging".
		Functional diagram of the ne reset timer circuit.	e UVLO protection a	and reset timer circuit" updated
			ng a nawar supply f	ilter for LIVI O protection"
	added.	o Guidelines for selectin	ig a power suppry i	ilter for UVLO protection"
	 Section 7.2 	3.2 updated to include in	nternal reset timer.	
	 Parameter 	t _{PD} corrected in Table 24		
	 Parameter 	E _{V(O)} corrected in <u>Table</u>	<u>26</u> .	
LPC11AXX v.2.1	20120704	Product data sheet	-	LPC11AXX v.2
	 Data sheet 	status changed to Produ	ıct.	
	 Changed T 	able note [2] in Table 24.		
	 Changed T 	able note [1] in Table 8.		
	 Added Table 	e note [1] in Table 9.		
	 Moved DT_s 	$_{ m en}$ and ${ m E_L}$ values from ty	p to max in Table 2	2.
	 Corrected \ 	/ _{esd} in Table 5.		
	Added Table	e note [5] and Table note	e [6] to Table 4.	
LPC11AXX v.2	20120625	Preliminary data shee	et -	LPC11AXX v.1
		status changed to Prelin	-	
		f _{clk} removed from Table	11.	
	 t_{er} removed 			
		EPROM size specified in		
		3 "UVLO reset behavior"		
	 Power cons Figure 13). 	sumption data updated fo	or active mode and	sleep mode (see Figure 11 to
		sumption data for active a Table 6 and Section 9.1		ith all peripherals enabled
	 Parameters 	s t _{s(pu)} and t _{s(sw)} removed	from Section 7.15.	
	 Parameter 	t _{PD} updated in Table 25.		
	 SSP dynan 	nic characteristics added	in Table 17.	
	 WDOsc and 	d LFOsc max and min fre	equency values upd	ated throughout the data sheet.
	 Section 12. 	7 "UVLO protection circu	uit" added.	
		ues for parameters E _D , E aracteristics" changed to		C _L in Table 20 "DAC static and
		V _O corrected for condition		+85 °C in Table 22.
	20120322	Objective data sheet		

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17. Legal information

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