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CY24488

Quad-PLL Clock Generator with Two-Wire Serial Interface

Features

- Three output frequencies plus reference out
- Programmable output frequencies through two-wire serial interface
- Output frequencies from 4.9152 to 148.5 MHz
- Uses an external 27 MHz crystal or 27 MHz input clock
- Optional analog VCXO
- Programmable output drive strength to minimize EMI
- The equivalent without a serial port is the CY22388/89/91
- 16-pin TSSOP package
- 3.3 V operation with 2.5 V output buffer option

Benefits

- Meets most Digital Set Top Box, DVD Recorder, and DTV application requirements
- Multiple high performance PLLs allow synthesis of unrelated frequencies
- Integration eliminates the need for external loop filter components
- Complete VCXO solution with ± 120 ppm (typical pull range)

Functional Description

The CY24488 generates up to three independent clock frequencies, and a buffered copy of the reference crystal frequency, from a single crystal or reference input. Five clock output pins are available, which allows some frequencies to be driven on two or more output pins. Outputs can also be individually enabled or disabled. When a CLK output is individually disabled, it drives low.

The analog voltage controlled crystal oscillator (VCXO) allows you to “pull” the reference crystal to a frequency that is slightly higher or lower than nominal. This causes all output clocks to shift by an equivalent parts-per-million (PPM). The VCXO is controlled by the analog control voltage applied to the V_{IN} pin. For applications that do not require the VCXO functionality, it can be disabled.

A serial programming interface (SPI) permits in-system configuration of the device by writing to internal registers. It is used to set the output frequencies, enable and disable outputs, enable and disable the VCXO feature, and more. The SPI provides volatile programming. When powered down, the device reverts to its preSPI state. When the system is powered back up, the SPI registers need to be configured again. Specific configuration details are given in the following sections of this data sheet.

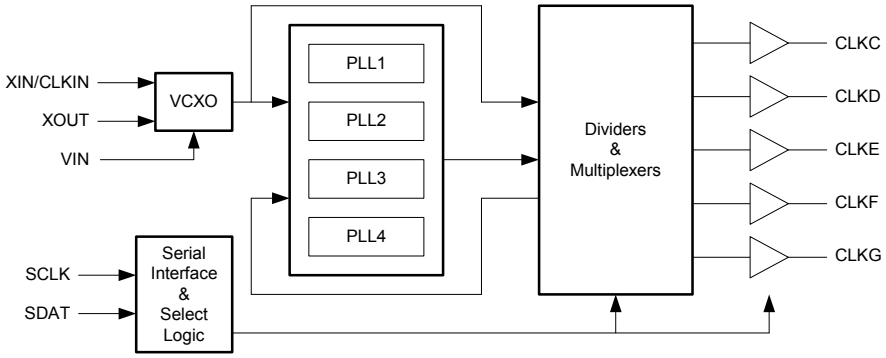
Customers may contact their Cypress FAE or salesperson for any frequency that is not listed in this data sheet. The data sheet can be updated with a new hex code for the requested frequency.

For a complete list of related documentation, click here.

Applications and Frequencies

Output Clock	Application	Frequencies (MHz)
CLKC	Audio	6.144, 8.192, 11.2896, 12.288, 16.384, 16.9344, 18.432, 22.5792, 24.576, 33.8688, 36.864
	iLink	24.576
	HDMI	25.175, 28.322
CLKD	Video	27, 27.027, 54, 54.054, 81
	USB	12, 24, 48
	Video-Pixel Frequency	74.25/1.001, 74.25, 148.5/1.001, 148.5
	Modem	4.9152, 11.0592
	iLink	24.576
CLKE	Video	13.5, 27, 54, 81, 108
	Ethernet	25
	PCI	33.3333, 66.6666
	Processor	20, 30, 40, 50, 60, 80, 100
CLKF	See CLKC/D/E	REFOUT or Copy of CLKC, CLKD or CLKE
CLKG	See CLKC/D/E	REFOUT or Copy of CLKC, CLKD or CLKE

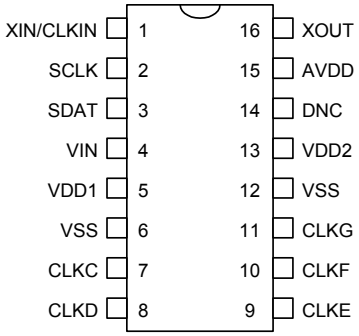
Logic Block Diagram



Contents

Pinouts

Figure 1. 16-pin TSSOP pinout



Pin Definitions

Pin Name	Pin Number	Description
XIN/CLKIN	1	Crystal Input (27 MHz) or External Input Clock (27 MHz)
XOUT	16	Crystal Output
CLKC	7	Clock Output
CLKD	8	Clock Output
CLKE	9	Clock Output
CLKF	10	Clock Output
CLKG	11	Clock Output
SCLK	2	Serial Interface Clock Input
SDAT	3	Serial Interface Data
V_{IN}	4	Analog Control Input for VCXO
DNC	14	Do Not Connect. This pin must be left floating.
AVDD	15	Core and input Voltage Supply
V_{DD1}	5	Voltage Supply for Outputs CLKC
V_{DD2}	13	Voltage Supply for Outputs CLKD, CLKE, CLKF, CLKG
V_{SS}	6, 12	Ground

Functional Overview

Default Startup Configuration

The default state of the device refers to its state at power on. All output clocks are off except CLKG, which outputs a copy of the 27 MHz reference clock. The serial programming interface must be used to configure the device for the desired output frequencies. Because the serial programming memory is volatile, the device reverts to its default configuration when power is cycled.

Reference Input

There are three programmable reference operating modes for the CY24488 family of devices. Table 1 shows the data values that must be programmed into the device for each of the reference operating modes. The correct values are required to ensure frequency accuracy and VCXO pullability.

The first mode uses an external 27 MHz pullable crystal and incorporates the internal analog VCXO. The crystal is connected between the XIN/CLKIN and XOUT pins. Refer the section Crystal Requirements for further details.

The second mode disables the VCXO input control and uses a standard 27 MHz crystal. Crystal requirements are relaxed relative to the VCXO mode. The crystal is connected between the XIN/CLKIN and XOUT pins. Refer the section Crystal Requirements. In this mode, tie the V_{IN} pin to AVDD.

The third mode accepts an external 27 MHz reference clock, applied to the XIN/CLKIN pin. In this configuration, the XOUT pin must be unconnected. The VCXO feature is not available; tie the V_{IN} pin to AVDD.

Table 1. Register Settings for VCXO and Reference

Reference Clock and VCXO	Crystal			Address	
	Manufacturer Part Number	Package	Specified C_L	16H	17H
CLKIN (external reference), VCXO off	–	–	–	89	3A
Crystal, VCXO off	any	any	10.7 pF	88	4F
Crystal, VCXO off	any	any	12 pF	88	5F
Crystal, VCXO off (default)	any	any	12.6 pF	88	67
Crystal, VCXO off	any	any	14 pF	88	77
Crystal, VCXO on	KDS DSX530GA	5 × 3.2 mm	12.6 pF	88	3A
Crystal, VCXO on	KDS DSX530GA	5 × 3.2 mm	10.7 pF	88	2A
Crystal, VCXO on	RIVER FCX-03	5 × 3.2 mm	12 pF	88	41
Crystal, VCXO on	KDK	5 × 3.2 mm	12 pF	88	3A
Crystal, VCXO on	KDS	SMD-49	12 pF	88	39
Crystal, VCXO on	Ecliptek ECX-6277	SMD-49	12 pF	88	41

Analog VCXO

The VCXO feature allows you to fine tune the output frequency through a control voltage applied to the V_{IN} pin. A special pullable crystal must be used to have adequate VCXO pull range. This data sheet lists specific crystals that are qualified for use with the CY24488. Specific serial programming values are also given for each crystal.

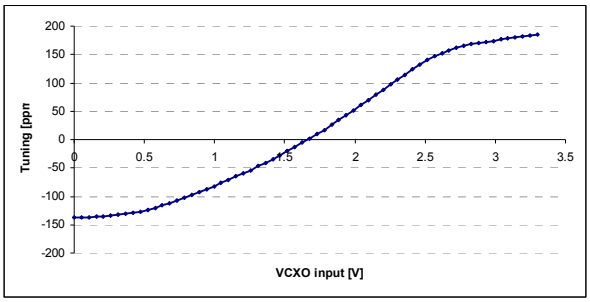
The special crystal requirements are eliminated if the VCXO feature is not needed. To disable the VCXO, the V_{IN} pin must be tied high, and the appropriate register values given in the programming table must be programmed into the device.

The VCXO is completely analog, so there is infinite resolution on the VCXO pull curve. The analog-to-digital converter steps that are normally associated with a digital VCXO input are not present in this device.

VCXO Profile

Figure 2 shows an example of a VCXO profile. The analog voltage input is on the X-axis and the PPM range is on the Y-axis. An increase in the VCXO input voltage results in a corresponding increase in the output frequency. This has the effect of moving the PPM from a negative to positive offset.

Figure 2. VCXO Profile



Crystal Requirements

The crystal requirements for the CY24488 differ for the VCXO and non-VCXO modes. In all cases, the device must be programmed correctly for the specific crystal used, as indicated in Table 1 on page 5.

Crystals for Non-VCXO Mode

When not using the VCXO, the V_{IN} pin must be tied high. The CY24488 uses a standard AT-cut parallel resonant crystal, which is available in a variety of packages. The key crystal parameter is load capacitance (C_L). The CY24488 has programmable load capacitance to match a range of crystal C_L values. The specific configurations are shown in Table 1 on page 5. Crystals with C_L values outside this range are not recommended.

Pullable Crystals for VCXO Mode

When the VCXO mode is used, the crystal requirements increase considerably to ensure the pullable range and glitch free pulling. Table 1 on page 5 lists the crystals that Cypress has qualified for use with the CY24488, and the corresponding programming configurations. Customers wishing to use non-qualified crystals must first contact Cypress technical support.

Output Configurations

CLKC, CLKD, and CLKE are the three primary synthesized output clocks. For each one, you can select from several clock frequencies, as shown in the following tables. To do this, find the desired frequency from the appropriate table, then use the serial programming interface to write the specified hexadecimal data into the specified memory addresses.

In some cases, the data at a particular memory address controls multiple functions, so only some of the bit values are specified. Since a byte is the smallest unit of data that can be written, it is necessary to construct the full data byte before writing it. To do this, look in the other tables to find the correct values for the other bits in that byte.

Any of the remaining output clocks (CLKF and CLKG) can be configured to generate duplicate copies of any the three primary clocks. Any of these clocks can also drive a buffered version of the reference crystal frequency.

Table 2. CLKC Output Frequencies (Audio, iLink, or HDMI)

Frequency (MHz)	Application	Frequency Error	Register Address						
			0AH	0BH	0CH	0DH	0EH	0FH	48H[1]
CLKC off and PLL off (default)	–	–	–	–	88	–	–	44	8D
CLKC off	–	–	–	–	–	–	–	–	8D
25.175	HDMI	0 ppm	01	07	D2	26	18	72	AD
28.322	HDMI	0 ppm	10	39	E2	94	39	6A	91
6.144 (48 K × 128)	Audio	0 ppm	17	3E	D0	1C	06	64	A5
12.288 (32 K × 384)	Audio	0 ppm	17	3E	D0	1C	06	64	A9
16.384 (32 K × 512)	Audio	0 ppm	17	3E	D0	19	0E	64	81
18.432 (48 K × 384)	Audio	0 ppm	17	3E	D0	1C	06	64	89
24.576 (48 K × 512)	Audio, iLink	0 ppm	17	3E	D0	1C	06	64	B5
36.864 (48 K × 768)	Audio	0 ppm	17	3E	D0	1C	06	64	95
11.2896 (44.1 K × 256)	Audio	0 ppm	17	3E	D0	30	16	66	A5
16.9344 (44.1 K × 384)	Audio	0 ppm	17	3E	D0	30	16	66	85
22.5792 (44.1 K × 512)	Audio	0 ppm	17	3E	D0	30	16	66	A9
33.8688 (44.1 K × 768)	Audio	0 ppm	17	3E	D0	30	16	66	89

Note
1. Bits [7:6] control CLKC drive strength. The values given in this table correspond to a drive strength setting of '10'. See Table 8 and Table 7 on page 8.

Table 3. CLKD Output Frequencies (Video, Pixel rate, USB, modem or iLink)

Frequency (MHz)	Application	Frequency Error	Register Address			
			10H	11H	12H	50H
CLKD off and PLL off (default)	–	–	–	–	00	8E
CLKD off	–	–	–	–	–	8E
12	USB	0 ppm	01	08	30	A2
24	USB	0 ppm	07	1E	30	86
48	USB	0 ppm	07	1E	30	8A
4.9152	Modem	+38 ppm	18	21	26	A2
11.0592	Modem	+11 ppm	39	8F	28	A6
24.576	iLink	6 ppm	56	8E	33	82
27 (reference)	Video	0 ppm	–	–	02	9A
27.027	Video	0 ppm	7B	F2	33	86
54 (ref * 2)	Video	0 ppm	02	0E	30	8A
54.054	Video	0 ppm	7B	F2	33	8A
74.25/1.001	Video pixel rate	0 ppm	59	F8	2C	96
74.25	Video pixel rate	0 ppm	00	03	22	96
81 (ref * 3)	Video	0 ppm	00	07	30	B6
148.5/1.001	Video pixel rate	0 ppm	59	F8	2C	B2
148.5	Video pixel rate	0 ppm	00	03	22	B2

Table 4. CLKE Output Frequencies (Ethernet, Video, PCI, Processor)

Frequency (MHz)	Application	Frequency Error	Register Address			
			13H	14H	15H	53H[2]
CLKE off and PLL off (default)	–	–	–	–	00	3E
CLKE off	–	–	–	–	–	3E
13.5	Video	0 ppm	00	05	26	8E
27 (reference)	Video	0 ppm	–	–	02	6E
54	Video	0 ppm	00	06	24	2E
81	Video	0 ppm	00	07	24	DE
108	Video	0 ppm	00	06	24	5E
20	Processor	0 ppm	07	26	24	9E
25	Ethernet	0 ppm	07	17	30	AE
30	Processor	0 ppm	01	08	28	AE
33.333333	PCI	0 ppm	19	62	30	AE
40	Processor	0 ppm	07	26	30	AE
50	Processor	0 ppm	19	62	30	2E
60	Processor	0 ppm	01	08	28	DE
66.666666	PCI	0 ppm	19	62	30	DE
80	Processor	0 ppm	07	26	30	DE
100	Processor	0 ppm	19	62	30	5E

Note
2. Bits [1:0] control CLKD drive strength. The values given in this table correspond to a drive strength setting of '10'. See Table 8 and Table 7 on page 8.

Table 5. CLKF Output Clock

Frequency (MHz)	Address 55H, Data value (hex)
CLKF off (default)	0C
27 MHz reference	18
Copy of CLKC	copy of data from Table 2 on page 6 address 48H
Copy of CLKD	copy of data from Table 3 on page 7 address 50H
Copy of CLKE	copy of data from Table 4 on page 7 address 53H, divided by 4 [3]

Table 6. CLKG Output Clock (Default = Reference out)

Frequency (MHz)	Address 57H	
	bits [7:6]	bits [5:0]
CLKG off	10	001100
27 MHz reference (default)	drive strength (default=10). Refer Table 7	011000
Copy of CLKC	drive strength (default=10). Refer Table 7	bits[5:0] of address 48H. Refer Table 2 on page 6
Copy of CLKD	drive strength (default=10). Refer Table 7	bits[5:0] of address 50H. Refer Table 3 on page 7
Copy of CLKE	drive strength (default=10). Refer Table 7	bits[7:2] of address 53H. Refer Table 4 on page 7

Enabling and Disabling Output Clocks

All output clocks can be individually enabled or disabled. Only CLKG is on at power on. All other clocks are off (driven low), and their respective PLLs are off. When using the serial programming interface to set an output to a desired frequency, the PLL Lock Time (AC Parameters Table) applies.

When turning off an output, the output buffer and associated PLL are turned off by different register addresses. As a result, it is possible to turn off an output by programming just one byte, but the PLL continues to run and consume some power. So, the PLL Lock Time does not apply when turning the output back on.

The clock configuration tables also show a second off state that also turns off the PLL, saving additional power. This requires programming one or two additional bytes, and the PLL Lock Time applies.

Output Drive Strength

Output drive strength is configurable, with 2 bits available to set the drive strength for each output. The default value is ‘10’, which is medium high. This is the recommended setting for outputs operating at 3.3 V. The recommended setting for 2.5 V outputs is ‘11’, which must be programmed by you. Table 7 shows which bits must be changed, and how to integrate these bits with other control bits to create valid bytes for shifting in.

You may program any output to a lower drive strength if EMI is a problem. ‘00’ is the lowest drive strength, while ‘11’ is the highest. Note that the lowest setting is very weak and is not suitable for most applications.

Table 7. Drive Strength (DS) Values [4]

DS Value	Drive Strength	3.3 V Output	2.5 V Output
00	Very low	EMI Adjustment	EMI Adjustment
01	Medium low	EMI Adjustment	EMI Adjustment
10 (default)	Medium high	Standard	EMI Adjustment
11	High	Extra Drive	Standard

Notes
3. Bits [7:6] of address 55H are don’t care. Dividing by 4 is equivalent to right shifting by 2 bits.
4. The default drive strength (DS) setting for all clocks is ‘10’. All output specifications for 3.3 V outputs are given for this value. Output specifications for 2.5 V outputs are given for a setting of ‘11’. To change the DS settings, the serial programming interface must be used to program in the desired values. You may program in any 2-bit value, but certain output specifications are not valid for settings other than ‘10’ (3.3 V) or ‘11’ (2.5 V). See the DC Parameters and AC Parameters tables for further details.

Table 8. Register Settings for Output Drive Strength [5]

Output Clock	Drive strength bits	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CLKC	bits[7:6] of 48H	DS		see address 48H in Table 2 on page 6					
CLKD	bits[1:0] of 53H	see address 53H in Table 4 on page 7						DS	
CLKE	bits[7:6] of 54H	DS		0	0	0	0	0	0
CLKF	bits[5:4] of 56H	1	1	DS		0	0	0	0
CLKG	bits[7:6] of 57H	DS		see address 57H in Table 6 on page 8					

Output Supply Voltage

The clock outputs may be operated at either 3.3 V or 2.5 V. CLKC has its own power pin (V_{DD1}), while all other clocks are powered by V_{DD2}. V_{DD1} and V_{DD2} may be operated at different voltages if desired. AVDD must always be 3.3 V.

The CY24488 also has internal register settings that must be configured for the actual output supply voltage. The default settings are optimized for $V_{DD1} = V_{DD2} = 3.3$ V. Table 9 and Table 7 on page 8 show the values that need to be programmed for 2.5 V supply voltage.

Table 9. Register Settings for Output Supply Voltages

Output	Output Supply Voltages	Address	
		41H	43H
CLKC	$V_{DD1} = 3.3$ V	BF (default)	–
	$V_{DD1} = 2.5$ V	7F	–
CLKD, CLKE, CLKF, CLKG	$V_{DD2} = 3.3$ V	–	A0 (default)
	$V_{DD2} = 2.5$ V	–	90

Programming Flow

The device registers may be programmed in any sequence, but for convenience, a suggested programming flow is shown in Figure 3.

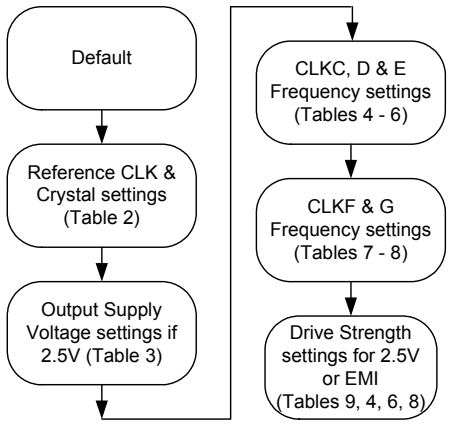
Any step in this programming sequence may be skipped if the default value is the desired value.

When programming an output frequency, the new frequency is valid on that output after all of the specified data values are written to all of the specified addresses. When changing an output frequency, the output may transition through one or more indeterminate frequencies between the writing of the first byte and the last byte.

Note that some of the programming steps are not as independent as they appear in the flow diagram. In particular, addresses 48H, 53H, and 57H control both output frequencies and drive strength. Because a byte is the smallest unit that may be programmed through the serial interface, you must consider both the frequency setting and the output drive strength when constructing the byte value to be written into these particular address. It is not necessary to write more than once to any address, but that one write must have all of the bits set correctly.

Example: configure CLKC for 33.8688 MHz and 2.5 V output. For address 48H, start with the value in Table 2 on page 6: 89H (binary 10001001). Table 8 shows that bits 7 and 6 control the drive strength, which must be '11' (from Table 7 on page 8). Therefore, the final value is 11001001, which is C9H. This value is written once.

Figure 3. Programming Flow



Note

5. The default drive strength (DS) setting for all clocks is '10'. All output specifications for 3.3 V outputs are given for this value. Output specifications for 2.5 V outputs are given for a setting of '11'. To change the DS settings, the serial programming interface must be used to program in the desired values. You may program in any 2-bit value, but certain output specifications are not valid for settings other than '10' (3.3 V) or '11' (2.5 V). See the DC Parameters and AC Parameters tables for further details.

Serial Programming Interface Protocol and Timing

The CY24488 uses pins SDAT and SCLK for a 2-wire serial interface that operates up to 400 kbit/s in Read or Write mode. Except for the data hold time (t_{DH}), it is compliant to the I^2C bus standard. The basic Write protocol is:

Start Bit; 7-bit Device Address (DA); R/$\overline{W}$ Bit; Slave Clock Acknowledge (ACK); 8-bit Memory Address (MA); ACK; 8-bit Data; ACK; 8-bit Data in MA+1 if desired; ACK; 8-bit Data in MA+2; ACK; and more until STOP Bit. The basic serial format is shown in Figure 5.

Figure 4. Data Transfer Sequence on the Serial Bus

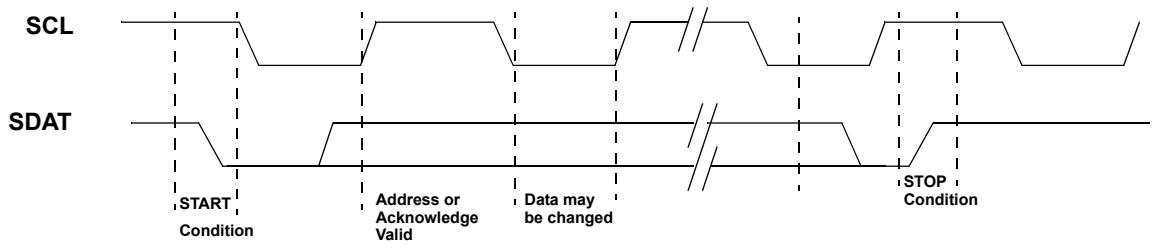
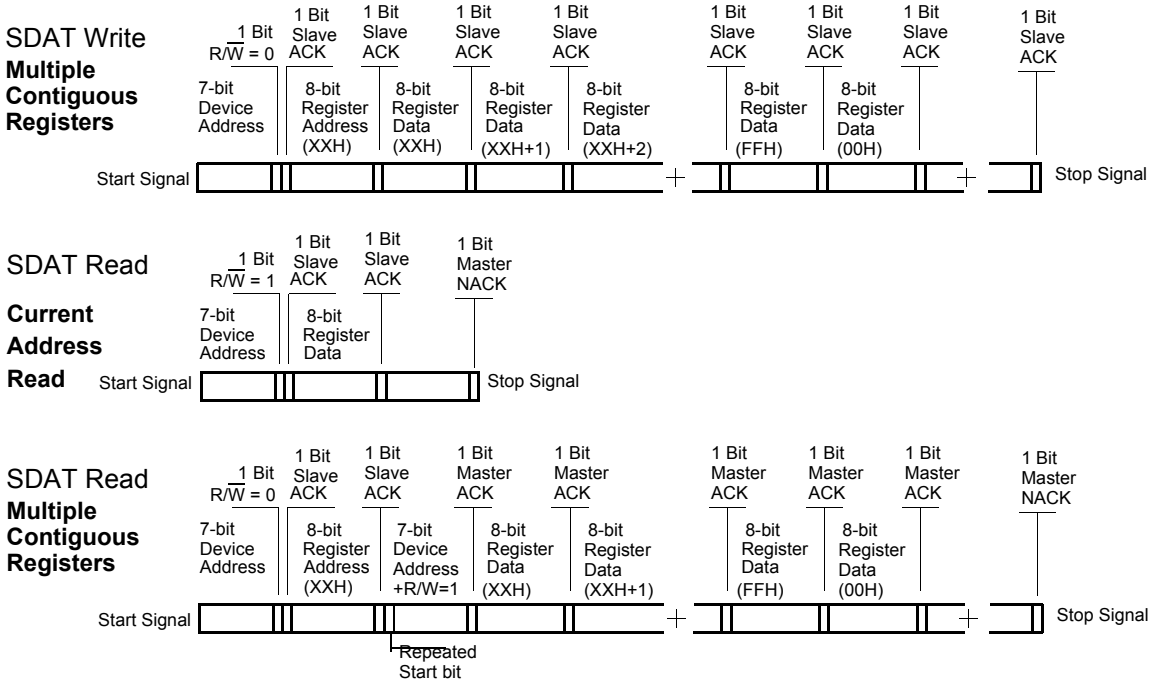


Figure 5. Data Frame Architecture



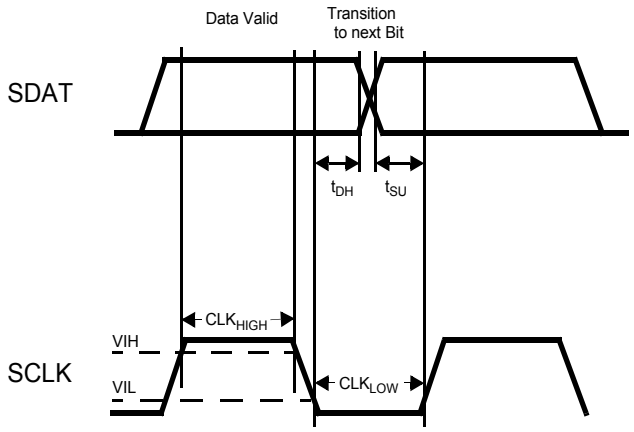
Device Address

The device address is a 7-bit value. The default serial interface address is 47H.

Data Valid

Data is valid when the clock is HIGH, and can be transitioned only when the clock is LOW, as shown in Figure 6.

Figure 6. Data Valid and Data Transition Periods



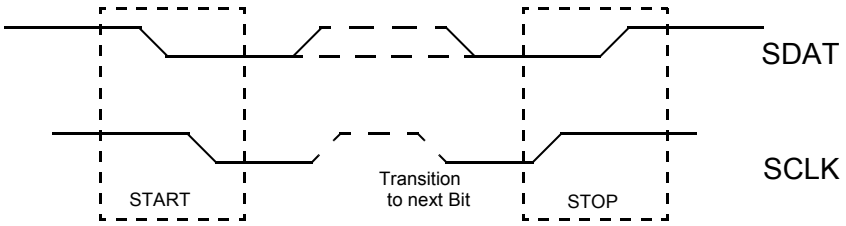
Data Frame

Every new data frame is indicated by a start and stop sequence, as shown in Figure 7.

START Sequence: Start Frame is indicated by SDAT going LOW when SCLK is HIGH. Every time a start signal is given, the next 8-bit data must be the device address (seven bits) and a R/$\overline{W}$ bit, followed by register address (eight bits) and register data (eight bits).

STOP Sequence: Stop Frame is indicated by SDAT going HIGH when SCLK is HIGH. A Stop Frame frees the bus to write to another part on the same bus or writing to another random register address.

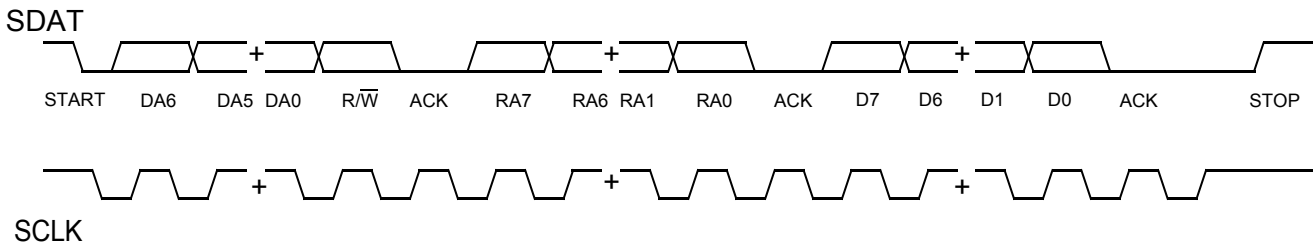
Figure 7. Start and Stop Frame



Acknowledge Pulse

During Write Mode the CY24488 responds with an Acknowledge (ACK) pulse after every eight bits. This is accomplished by pulling the SDAT line LOW during the N*9th clock cycle, as shown in Figure 8 (N = the number of bytes transmitted). During Read Mode the acknowledge pulse after the data packet is sent is generated by the master.

Figure 8. Frame Format (Device Address, R/$\overline{W}$, Register Address, Register Data)



Write Operations

Writing Individual Bytes

A valid write operation must have a full 8-bit register address after the device address word from the master, which is followed by an acknowledge bit from the slave (SDAT = 0/LOW). The next eight bits must contain the data word intended for storage. After the data word is received, the slave responds with another acknowledge bit (SDAT = 0/LOW), and the master must end the write sequence with a STOP condition.

Writing Multiple Bytes

To write more than one byte at a time, the master does not end the write sequence with a STOP condition. Instead, the master can send multiple contiguous bytes of data to be stored. After each byte, the slave responds with an acknowledge bit, the same as after the first byte, and accepts data until the acknowledge bit is responded to by the STOP condition. When receiving multiple bytes, the CY24488 internally increments the register address.

Read Operations

Read operations are initiated the same way as Write operations except that the R/W bit of the slave address is set to '1' (HIGH). There are three basic read operations: current address read, random read, and sequential read.

Current Address Read

The CY24488 has an onboard address counter that retains one more than the address of the last word access. If the last word written or read was word 'n', then a current address read operation returns the value stored in location 'n+1'. When the CY24488 receives the slave address with the R/W bit set to a '1', the CY24488 issues an acknowledge and transmits the 8-bit word. The master device does not acknowledge the transfer, but does generate a STOP condition, which causes the CY24488 to stop transmission.

Random Read

Through random read operations, the master may access any memory location. To perform this type of read operation, first set the word address. Send the address to the CY24488 as part of a write operation. After the word address is sent, the master generates a START condition following the acknowledge. This terminates the write operation before any data is stored in the address, but not before the internal address pointer is set. Next, the master reissues the control byte with the R/W byte set to '1'. The CY24488 then issues an acknowledge and transmits the 8-bit word. The master device does not acknowledge the transfer, but does generate a STOP condition, which causes the CY24488 to stop transmission.

Sequential Read

Sequential read operations follow the same process as random reads except that the master issues an acknowledge instead of a STOP condition after transmission of the first 8-bit data word. This action results in an incrementing of the internal address pointer, and subsequently output of the next 8-bit data word. By continuing to issue acknowledges instead of STOP conditions, the master may serially read the entire contents of the slave device memory. Note that register addresses outside of 0AH to 17H and 40H to 57H can be read from but are not real registers and do not contain configuration information. When the internal address pointer points to the FFH register, after the next increment, the pointer points to the 00H register.

Serial Programming Interface Timing

Table 10. Serial Programming Interface Timing Specifications

Parameter	Description	Min	Max	Unit
f_{SCLK}	Frequency of SCLK	–	400	kHz
	Start Mode Time from SDA LOW to SCL LOW	0.6	–	µs
CLK_{LOW}	SCLK LOW Period	1.3	–	µs
CLK_{HIGH}	SCLK HIGH Period	0.6	–	µs
t_{SU}	Data Transition to SCLK HIGH	100	–	ns
t_{DH}	Data Hold (SCLK LOW to data transition)	100	–	ns
	Rise Time of SCLK and SDAT	–	300	ns
	Fall Time of SCLK and SDAT	–	300	ns
	Stop Mode Time from SCLK HIGH to SDAT HIGH	0.6	–	µs
	Stop Mode to Start Mode	1.3	–	µs

Absolute Maximum Conditions

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 11. Absolute Maximum Conditions

Parameter	Description	Condition	Min	Max	Unit
$AV_{DD}/V_{DD1}/V_{DD2}$	Core Supply Voltage		–0.5	4.6	V
V_{IN}	Input Voltage	Relative to V_{SS}	–0.5	V_{DD} + 0.5	VDC
T_S	Temperature, Storage	Non-functional	–65	+125	°C
ESD_{HBM}	ESD Protection (Human Body Model)	MIL-STD-883, Method 3015	2000	–	Volts
UL-94	Flammability Rating	V-0 at 1/8 in.	–	10	ppm
MSL	Moisture Sensitivity Level	16-pin TSSOP	1		

Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
AV_{DD}	Core Operating Voltage	3.0	3.3	3.6	V
V_{DD1}/V_{DD2}	Output Operating Voltage	3.0	3.3	3.6	V
		2.3	2.5	2.7	V
T_A	Ambient Temperature	–10	–	70	°C
C_{LOAD}	Maximum Load Capacitance	–	–	15	pF
t_{PU}	Power-up time for all V_{DD}s reach minimum specified voltage (power ramps must be monotonic)	0.05	–	500	ms

Pullable Crystal Specifications (For VCXO Applications)

Pullable Crystal Specifications for part CY2448 are as follows [6]

Parameter	Description	Condition	Min	Typ	Max	Unit
F_{NOM}	AT-cut Crystal	Parallel resonance, Fundamental mode	–	27	–	MHz
C_{LNOM}	Nominal Load Capacitance	Order crystal at one specific C_{LNOM} 0 ppm	11.4	12	12.6	pF
R_1	Equivalent Series Resistance (ESR)	Fundamental mode (CL = Series)	–	–	40	Ω
DL	Crystal Drive Level	Nominal V_{DD} at 25°C over ±120 ppm Pull Range	–	–	300	µW
F_{3SEPHI}[7]	Third Overtone Separation from 3 × F_{NOM}	Mechanical Third (High side of 3 × F_{NOM})	240	–	–	ppm
F_{3SEPLO}[7]	Third Overtone Separation from 3 × F_{NOM}	Mechanical Third (Low side of 3 × F_{NOM})	–	–	–120	ppm

Non-pullable Crystal Specifications (For non-VCXO Applications)

Non-pullable Crystal Specifications for part CY2448 are as follows [6]

Parameter	Description	Condition	Min	Typ	Max	Unit
F_{NOM}	AT-cut Crystal	Parallel resonance, Fundamental mode	–	27	–	MHz
C_{LNOM}	Nominal Load Capacitance	Order crystal at one specific C_{LNOM} 0 ppm	10.7	12	14.0	pF
R_1	Equivalent Series Resistance (ESR)	Fundamental mode (CL = Series)	–	–	40	Ω
DL	Crystal Drive Level	Nominal V_{DD} at 25°C	–	–	300	µW

Notes
6. Device operates to following specs which are guaranteed by design.
7. Increased tolerance available from pull range less than ±120 PPM.

DC Parameters

The DC Parameters for part CY24488 are as follows [8]

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{OH}[9]	Output High Current	$V_{OH} = V_{DD} – 0.5$, $V_{DD} = 3.3$ V	12	–	–	mA
I_{OL}[9]	Output Low Current	$V_{OL} = 0.5$, $V_{DD} = 3.3$ V	12	–	–	mA
I_{IH}	Input High Current	$V_{IH} = V_{DD}$, excluding V_{IN}, XIN/CLKIN	–	5	10	µA
I_{IL}	Input Low Current	$V_{IL} = 0$ V, excluding V_{IN}, XIN/CLKIN	–	5	10	µA
V_{IH}	Input High Voltage	XIN/CLKIN input CMOS levels	0.7 × AV_{DD}	–	–	V
V_{IL}	Input Low Voltage	XIN/CLKIN input CMOS levels	–	–	0.3 × AV_{DD}	V
V_{VCXO}	V_{IN} Input Range		0	–	AV_{DD}	V
I_{VDD}	Supply Current	V_{DD} Current	–	60	–	mA
C_{INXIN}	Input Capacitance at XIN/CLKIN	VCXO Disabled External Reference	–	15	–	pF
C_{INXTAL}	Input Capacitance at Crystal	VCXO Disabled Fixed Freq. Oscillator	–	12	–	pF

Notes
8. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with fully loaded outputs.
9. Drive strength settings: ‘10’ for 3.3 V outputs; ‘11’ for 2.5 V outputs.

AC Parameters

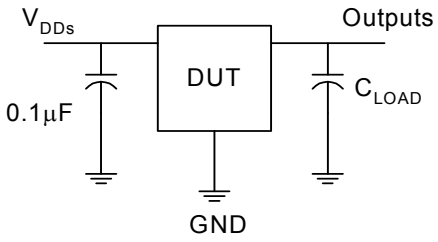
The AC Parameters for part CY24488 are as follows [10]

Parameter	Description	Conditions	Min	Typ	Max	Units
1/t1	Output Frequency		4.9152	–	148.5	MHz
DC1[11, 12]	Output Duty Cycle (excluding REFOUT)	Duty Cycle is defined in Figure 10 on page 17. t_2/t_1, 50% of V_{DD} External reference duty cycle between 40% and 60% measured at $V_{DD}/2$ (Clock output is ≤ 125 MHz)	45	50	55	%
DC2[11, 12]	Output Duty Cycle (excluding REFOUT)	Duty Cycle is defined in Figure 10. t_2/t_1, 50% of V_{DD} External reference duty cycle between 40% and 60% measured at $V_{DD}/2$ (Clock output is > 125 MHz)	40	50	60	%
DC_{REFOUT}[11, 12]	Output Duty Cycle	Duty Cycle is defined in Figure 10. t_2/t_1, 50% of V_{DD} (XIN/CLKIN Duty Cycle = 45/55%)	40	50	60	%
ER[11]	Rising Edge Rate	Output Clock Edge Rate. Measured from 20% to 80% of V_{DD}. C_{LOAD} = 15 pF. See Figure 11 on page 17.	0.75	1.2	–	V/ns
EF[11]	Falling Edge Rate	Output Clock Edge Rate. Measured from 80% to 20% of V_{DD}. C_{LOAD} = 15 pF. See Figure 11.	0.75	1.2	–	V/ns
T_9	Clock Jitter	Period Jitter; V_{DD1} = V_{DD2} = 3.3 V drive strength = '10'	–	250	–	ps
T_{10}	PLL Lock Time	From end of serial programming sequence to correct output frequency	–	1	5	ms
$f_{\Delta XO}$	VCXO Crystal Pull Range	Using non-SMD-49 crystal specified in Table 1 on page 5. Nominal Crystal Frequency Input assumed (0 ppm) at 25 °C and 3.3 V	±110	±120	–	ppm
		Using SMD-49 crystal specified in Table 1 on page 5. Nominal Crystal Frequency Input assumed (0 ppm) at 25 °C and 3.3 V.	±105	±120	–	ppm

Notes
10. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with fully loaded outputs.
11. Drive strength settings: '10' for 3.3 V outputs; '11' for 2.5 V outputs.
12. Guaranteed when values in Table 9 on page 9 and Table 8 on page 9 are programmed to match the output supply voltage.

Test and Measurement Setup

Figure 9. Test and Measurement Diagram



Voltage and Timing Definitions

Figure 10. Duty Cycle Definition

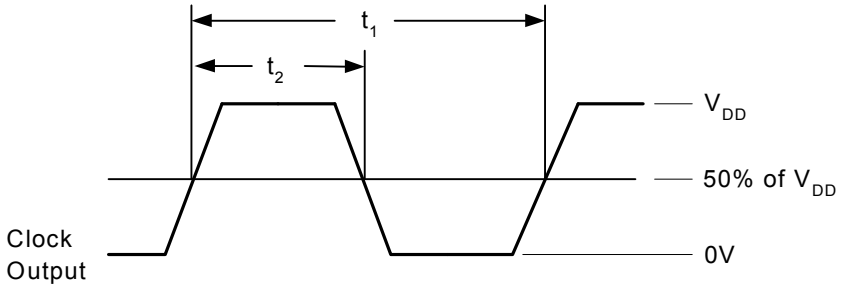
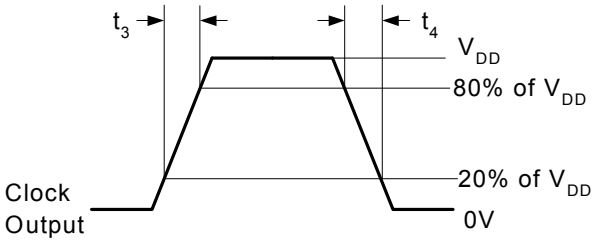


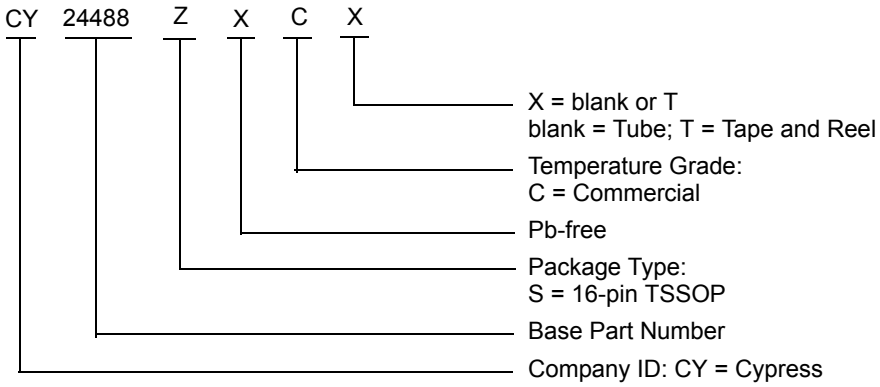
Figure 11. ER = (0.6 × V_{DD})/t_3, EF = (0.6 × V_{DD})/t_4



Ordering Information

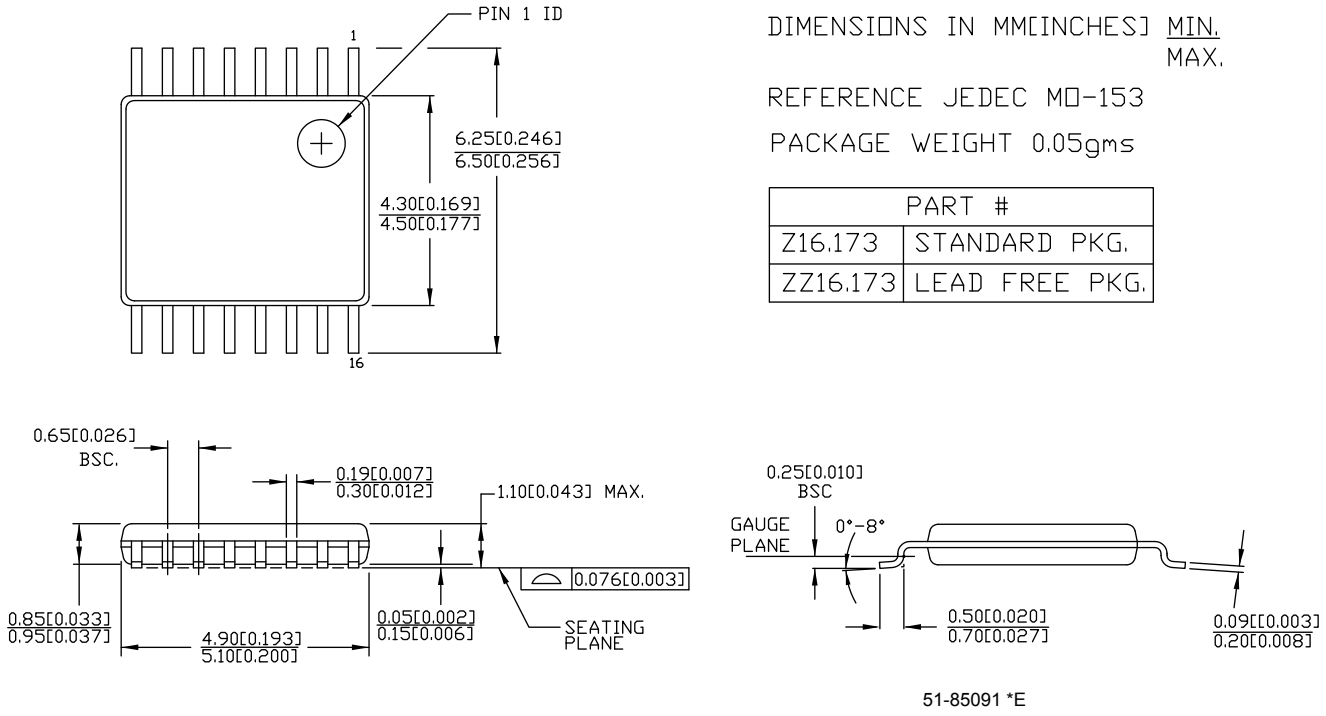
Part Number	Type	Production Flow
Pb-free		
CY24488ZXC	16-pin TSSOP	Commercial, 0 °C to +70 °C
CY24488ZXCT	16-pin TSSOP – Tape and Reel	Commercial, 0 °C to +70 °C

Ordering Code Definitions



Package Drawing and Dimensions

Figure 12. 16-pin TSSOP (4.40 mm Body) Z16.173/ZZ16.173 Package Outline, 51-85091



Acronyms

Acronym	Description
ACK	Acknowledge
DTV	Digital Television
DVD	Digital Video Disc or Digital Versatile Disc
ESR	Equivalent Series Resistance
FAE	Field Application Engineer
HDMI	High-Definition Multimedia Interface
I^2C	Inter IC Communications Interface
PCI	Peripheral Component Interconnect
PLL	Phase-Locked Loop
SPI	Serial Peripheral Interface
TSSOP	Thin-Shrink Small Outline Package
USB	Universal Serial Bus
VCXO	Voltage Controlled Crystal Oscillator

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
mm	millimeter
ns	nanosecond
ppm	parts-per-million
%	percentage
pF	picofarad
V	volt

Document History Page

Document Title: CY24488, Quad-PLL Clock Generator with Two-Wire Serial Interface Document Number: 001-09608				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	497098	RGL	See ECN	New data sheet.
*A	504259	RGL	See ECN	Change status from Advance Information to Final. Minor text additions across the document.
*B	2621905	KVM / AESA	12/15/08	Updated Document Title to read as “CY24488 Quad PLL Clock Generator with 2-Wire Serial Interface”. Replaced “I^2C” with “2-wire” in all instances across the document. Updated Serial Programming Interface Timing: Updated Table 10: Changed minimum value of t_{DH} parameter from 0 ns to 100 ns corresponding to “Data Hold (SCLK LOW to data transition)”. Updated to new template.
*C	2761988	KVM	09/10/09	Updated AC Parameters: Updated minimum and maximum values of “Output Frequency” parameter.
*D	3083299	CXQ	11/10/10	Added Contents. Updated DC Parameters: Removed C_{IN} parameter and its details. Updated AC Parameters: Updated typical value of T_9 parameter (Removed “±”). Updated Ordering Information: No change in part numbers. Added Ordering Code Definitions. Updated Package Drawing and Dimensions: spec 51-85091 – Changed revision from *A to *C. Added Acronyms and Units of Measure. Minor text edits. Updated to new template.
*E	4202940	CINM	11/26/2013	Updated Package Drawing and Dimensions: spec 51-85091 – Changed revision from *C to *D. Updated to new template. Completing Sunset Review.
*F	4581659	XHT	11/28/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end. Updated Package Drawing and Dimensions: spec 51-85091 – Changed revision from *D to *E.
*G	5529250	XHT	11/22/2016	Updated Functional Overview: Updated Serial Programming Interface Protocol and Timing: Updated Figure 5 (Replaced ACK with NACK for the last transactions in SDAT Read). Updated to new template. Completing Sunset Review.
*H	5993954	AESATMP8	12/14/2017	Updated logo and Copyright.

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