Product Specification

PE42420

UltraCMOS® SPDT RF Switch
100 – 6000 MHz

Features

- HaRP™ technology enhanced
  - No gate and phase lag
  - No drift in insertion loss and phase
- Supports +1.8V control logic
- High linearity
  - IIP3 of 65 dBm
- High isolation
  - 69 dB @ 1 GHz
  - 62 dB @ 3 GHz
  - 50 dB @ 6 GHz
- High ESD tolerance
  - 4kV HBM on RFC
  - 2kV HBM on all other pins

Product Description

The PE42420 is a HaRP™ technology-enhanced absorptive 50Ω SPDT RF switch developed on the UltraCMOS® process technology.

This general purpose switch is comprised of two RF ports and has very high isolation performance. It is ideal for RF and IF transceiver signal switching (signal amplitude adjust), discrete DSA stages, and filter bank switching applications. No blocking capacitors are required if DC voltage is not present on the RF ports.

Peregrine's HaRP™ technology enhancements deliver high linearity and excellent harmonics performance with the economy and integration of conventional CMOS.

Figure 1. Functional Diagram

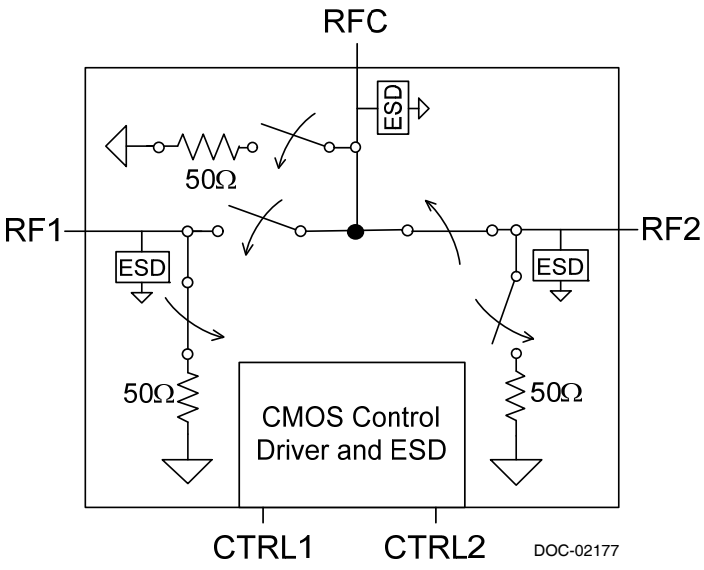


Figure 2. Package Type
20-lead 4x4 mm LGA

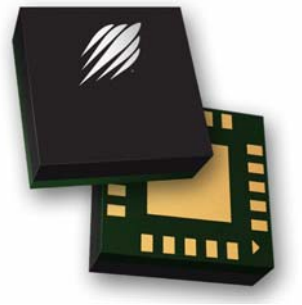


Table 1. Electrical Specifications Typical @ 25°C, V_{DD} = 3.0V ($Z_S = Z_L = 50\Omega$)

Parameter	Path	Condition	Min	Typ	Max	Unit
Operating frequency			100		6000	MHz
Insertion loss	RFC–RFX	100–1000 MHz 1000–2000 MHz 2000–3000 MHz 3000–4000 MHz 4000–5000 MHz[1] 5000–6000 MHz[1]		0.95 0.95 1.00 1.15 1.25 1.60	1.15 1.15 1.2 1.35 1.55 1.9	dB dB dB dB dB dB
Isolation	RFX–RFX	100–1000 MHz 1000–2000 MHz 2000–3000 MHz 3000–4000 MHz 4000–5000 MHz 5000–6000 MHz	67 63 59 60 54 44	69 64 62 64 60 50		dB dB dB dB dB dB
Isolation	RFC–RFX	100–1000 MHz 1000–2000 MHz 2000–3000 MHz 3000–4000 MHz 4000–5000 MHz 5000–6000 MHz	69 65 63 62 52 44	71 67 68 67 57 48		dB dB dB dB dB dB
Return loss	All ports	100–4000 MHz 4000–5000 MHz[1] 5000–6000 MHz[1]		20 15 13		dB dB dB
Input 1 dB compression point[2]	RFC–RFX	100–6000 MHz	33			dBm
Input IP2	RFC–RFX	100–6000 MHz		110		dBm
Input IP3	RFC–RFX	100–6000 MHz	60	65		dBm
Switching time		50% CTRL to 90% or 10% RF		300	400	ns

Notes: 1. Insertion loss and return loss can be improved by external matching
2. The input 1dB compression point is a linearity figure of merit. Refer to *Table 3* for the maximum operating power P_{IN} (50Ω)

Figure 3. Pin Configuration (Top View)

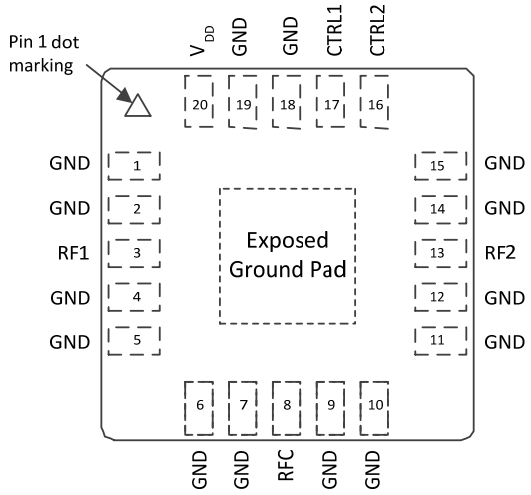


Table 2. Pin Descriptions

Pin #	Pin Name	Description
1, 2, 4-7, 9, 10-12, 14, 15, 18, 19	GND	Ground
3	RF1[1]	RF port
8	RFC[1]	RF common
13	RF2[1]	RF port
16	CTRL2	Digital control logic input 2
17	CTRL1	Digital control logic input 1
20	V_{DD}	Supply voltage
Pad	GND	Exposed pad: ground for proper operation

Note 1: RF pins 3, 8 and 13 must be at 0V DC. The RF pins do not require DC blocking capacitors for proper operation if the 0V DC requirement is met

Table 3. Operating Ranges

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	2.7		5.5	V
Supply current V_{DD} = 2.7 to 5.5V	I_{DD}		120	200	µA
Digital input high (CTRL1, CTRL2)	V_{IH}	1.17		3.6	V
Digital input low (CTRL1, CTRL2)	V_{IL}	-0.3		0.6	V
Digital input current	I_{CTRL}		9	12	µA
Maximum operating power (RFC-RFX)[1]	P_{IN}			30	dBm
Maximum power into termination (RFX)[1]	P_{MAX}			20	dBm
Operating temperature range	T_{OP}	-40		+85	°C

Notes: 1. 100% duty cycle, all bands, 50Ω

Table 4. Absolute Maximum Ratings

Parameter/Condition	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	-0.3	5.5	V
Digital input voltage (CTRL1, CTRL2)	V_{CTRL}	-0.3	3.6	V
Operating power (RFC-RFX)[1]	P_{IN}		30	dBm
Power into termination (RFX)[1]	P_{MAX}		20	dBm
Storage temperature range	T_{ST}	-65	+150	°C
Maximum die junction temperature	T_{Jmax}		+125	°C
ESD voltage HBM[2] RFC All other pins	V_{ESD}		 4000 2000	 V V
ESD voltage MM[3], all pins	V_{ESD}		100	V

Notes: 1. 100% duty cycle, all bands, 50Ω
2. Human Body Model (MIL-STD 883 Method 3015)
3. Machine Model (JEDEC JESD22-A115)

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS® device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS® devices are immune to latch-up.

Switching Frequency

The PE42420 has a maximum 25 kHz switching frequency.

Switching frequency describes the time duration between switching events. Switching time is the time duration between the point the control signal reaches 50% of the final value and the point the output signal reaches within 10% or 90% of its target value. Switching time is provided in *Table 1*.

Table 5. Truth Table

CTRL1	CTRL2	RFC – RF1	RFC – RF2
Low	Low	OFF	OFF
Low	High	OFF	ON
High	Low	ON	OFF
High	High	N/A[1]	N/A[1]

Note 1: CTRL1 = High and CTRL2 = High are not supported

Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE42420 in the 20-lead 4x4 mm LGA package is MSL3.

Spurious Performance

The typical spurious performance of the PE42420 is –155 dBm.

Typical Performance Data @ 25°C and V_{DD} = 3.0V unless otherwise specified

Figure 4. Insertion Loss (RFC-RFX)

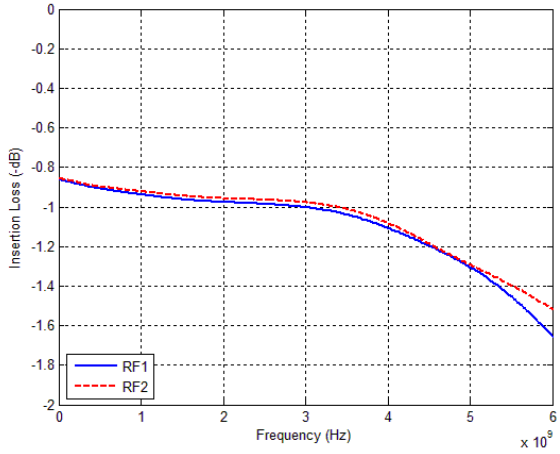


Figure 5. Insertion Loss vs Temp (RFX-RFC)

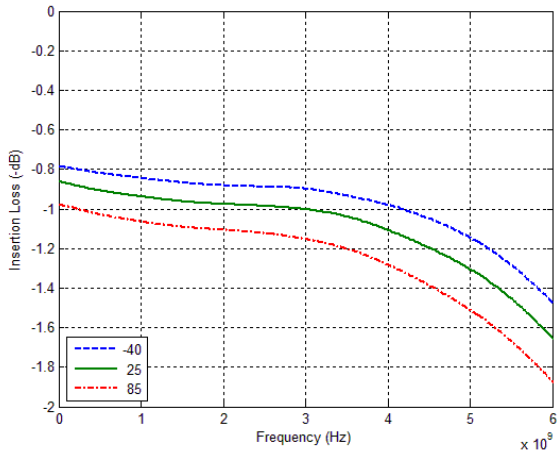


Figure 6. Insertion Loss vs V_{DD} (RFX-RFC)

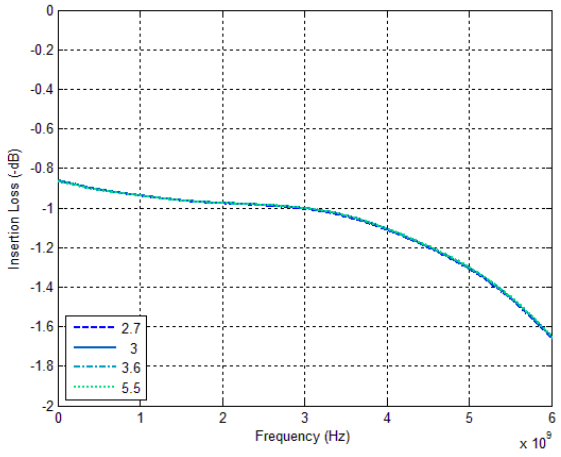


Figure 7. RFC Port Return Loss vs Temp (RF1 Active)

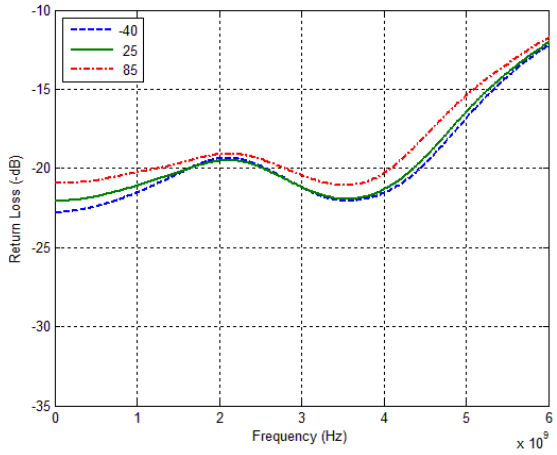
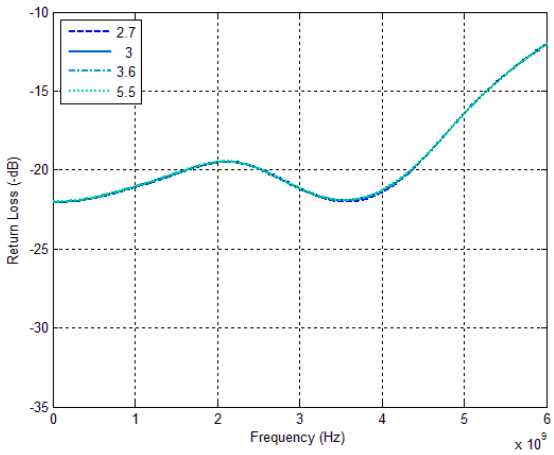


Figure 8. RFC Port Return Loss vs V_{DD} (RF1 Active)



Typical Performance Data@ 25°C and V_{DD} = 3.0V unless otherwise specified

Figure 9. RFC Port Return Loss vs Temp (RF2 Active)

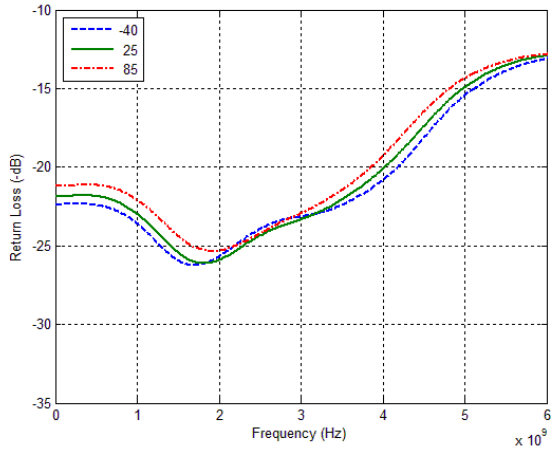


Figure 10. RFC Port Return Loss vs V_{DD} (RF2 Active)

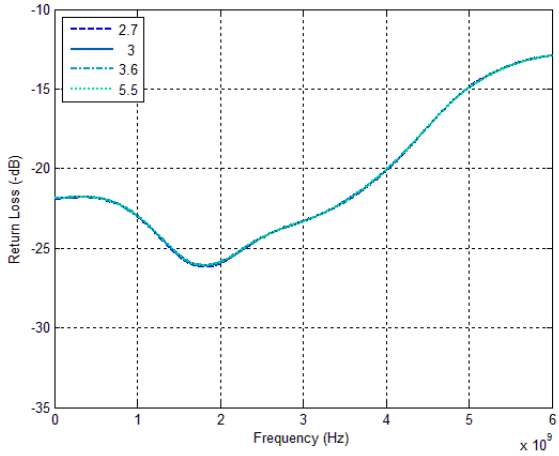


Figure 11. Active Port Return Loss vs Temp (RF1 Active)

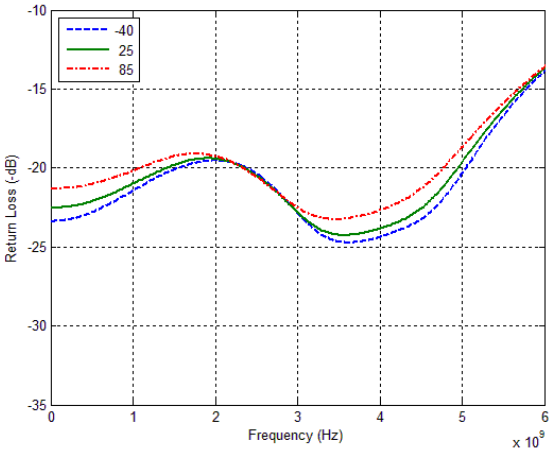


Figure 12. Active Port Return Loss vs V_{DD} (RF1 Active)

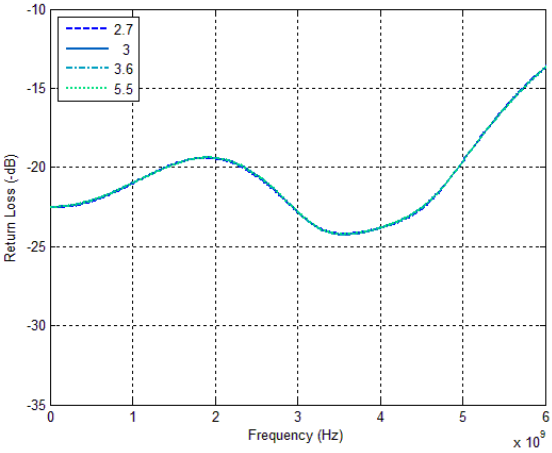


Figure 13. Terminated Port Return Loss vs Temp (RF1 Active)

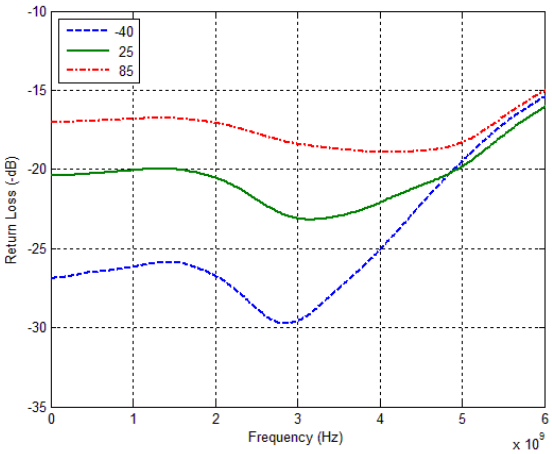
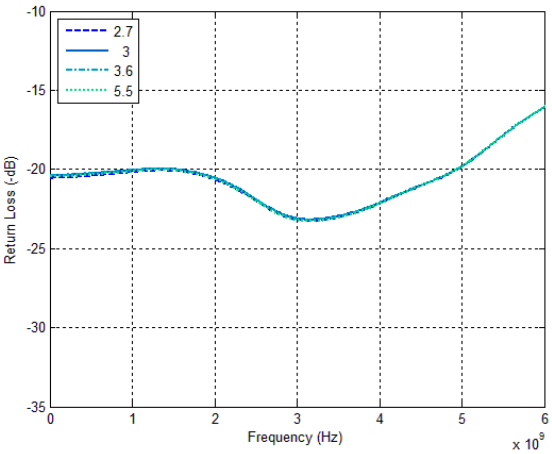


Figure 14. Terminated Port Return Loss vs V_{DD} (RF1 Active)



Typical Performance Data@ 25°C and V_{DD} = 3.0V unless otherwise specified

Figure 15. Isolation vs Temp (RFX-RFX)

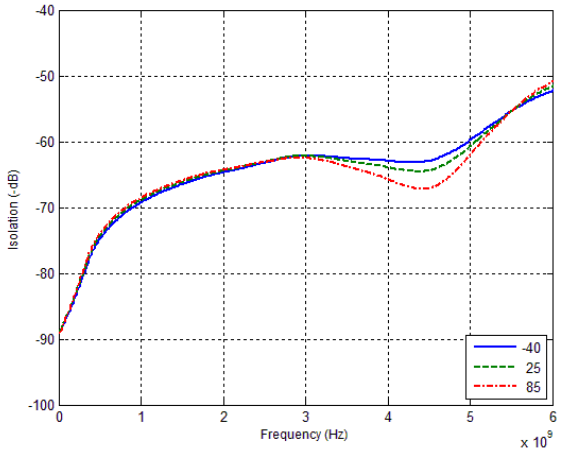


Figure 16. Isolation vs V_{DD} (RFX-RFX)

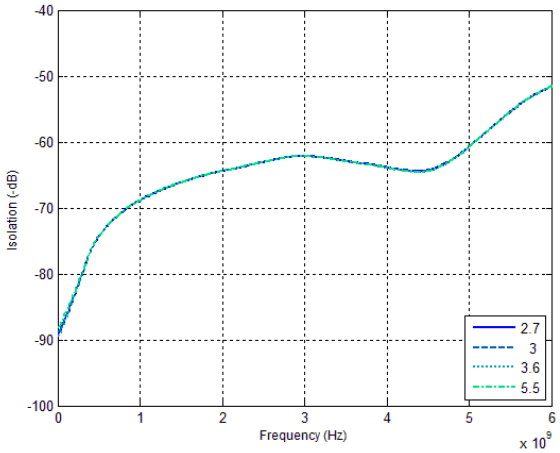


Figure 17. Isolation vs Temp (RFC-RFX)

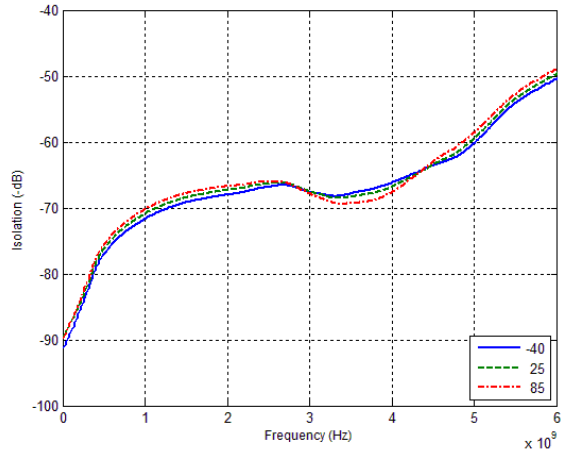
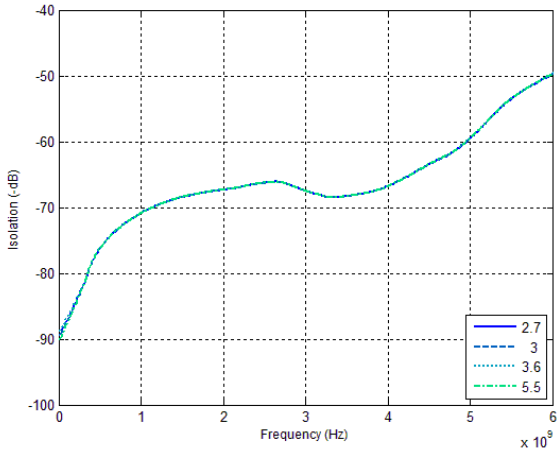


Figure 18. Isolation vs V_{DD} (RFC-RFX)



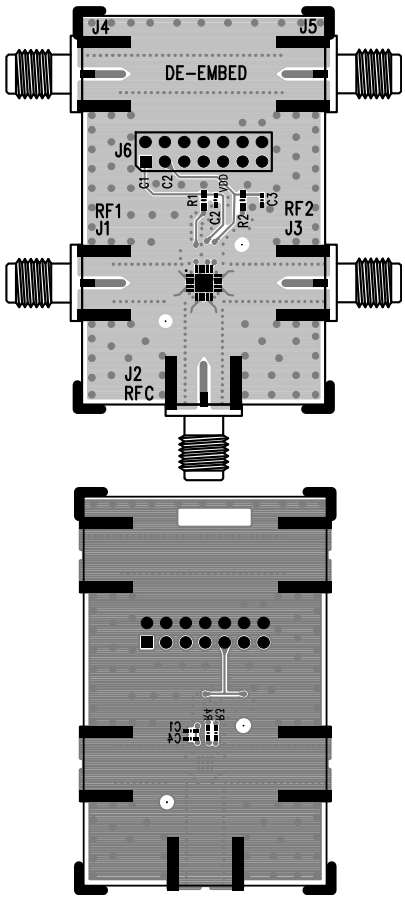
Evaluation Kit

The SPDT switch evaluation board was designed to ease customer evaluation of Peregrine's PE42420. The RF common port is connected through a 50Ω transmission line via the top SMA connector, J2. RF1 and RF2 ports are connected through 50Ω transmission lines via SMA connectors J1 and J3, respectively. A 50Ω through transmission line is available via SMA connectors J4 and J5, which can be used to calculate the loss of the PCB. J6 provides DC and digital inputs to the device.

The board is constructed of a four metal layer material with a total thickness of 36 mils. To achieve high isolation, the 50Ω transmission lines are designed in layer 2 using a stripline waveguide design. The board stack up for 50Ω transmission lines has 10 mil thickness of Rogers 4350 between layer 1 and layer 2, and 10 mil thickness of Rogers 4350 between layer 2 and layer 3.

For the true performance of the PE42420 to be realized, the PCB should be designed in such a way that RF transmission lines and sensitive DC I/O traces are heavily isolated from one another.

Figure 19. Evaluation Board Layouts



101-0551

Figure 20. Evaluation Board Schematic

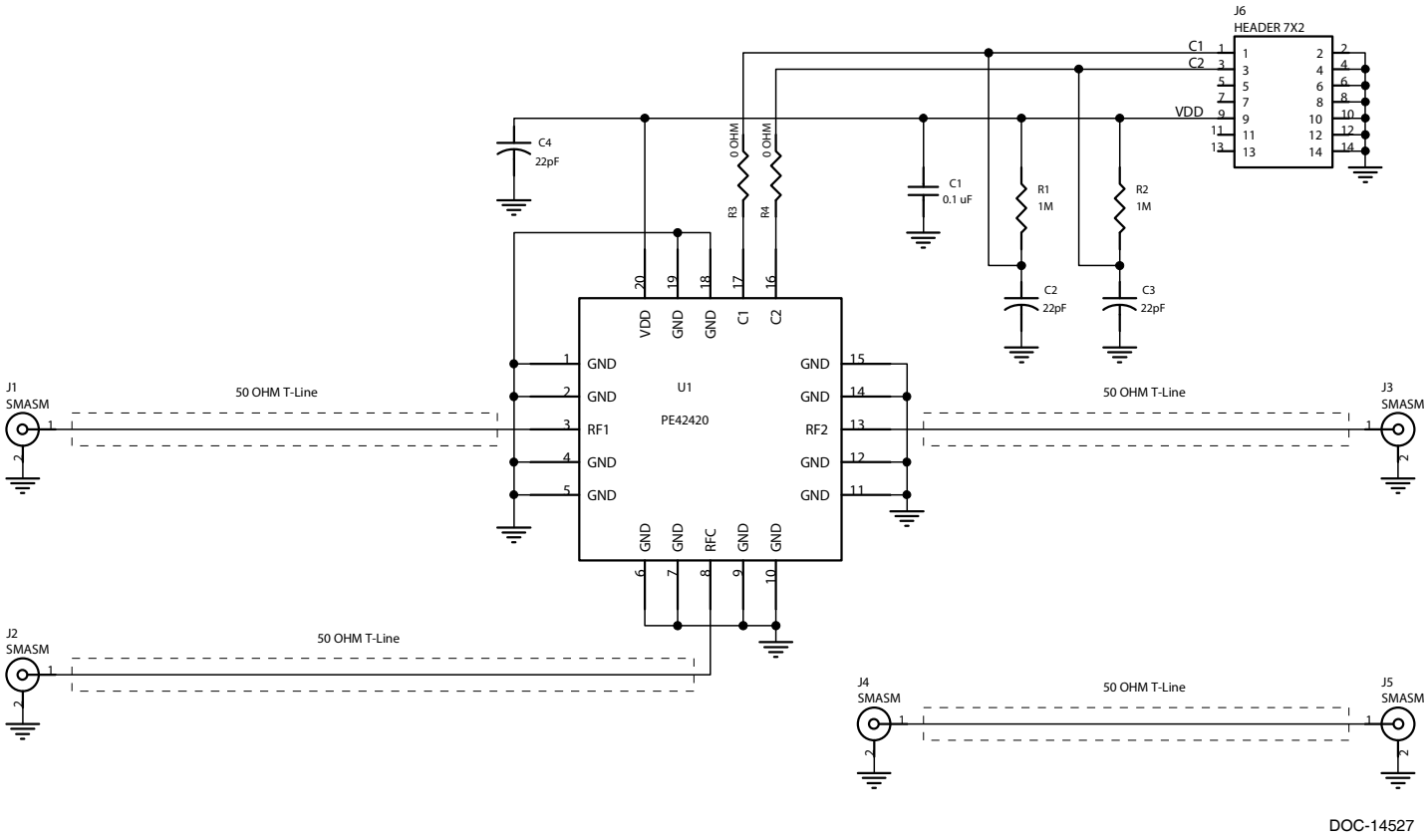


Figure 21. Package Drawing
20-lead 4x4 mm LGA

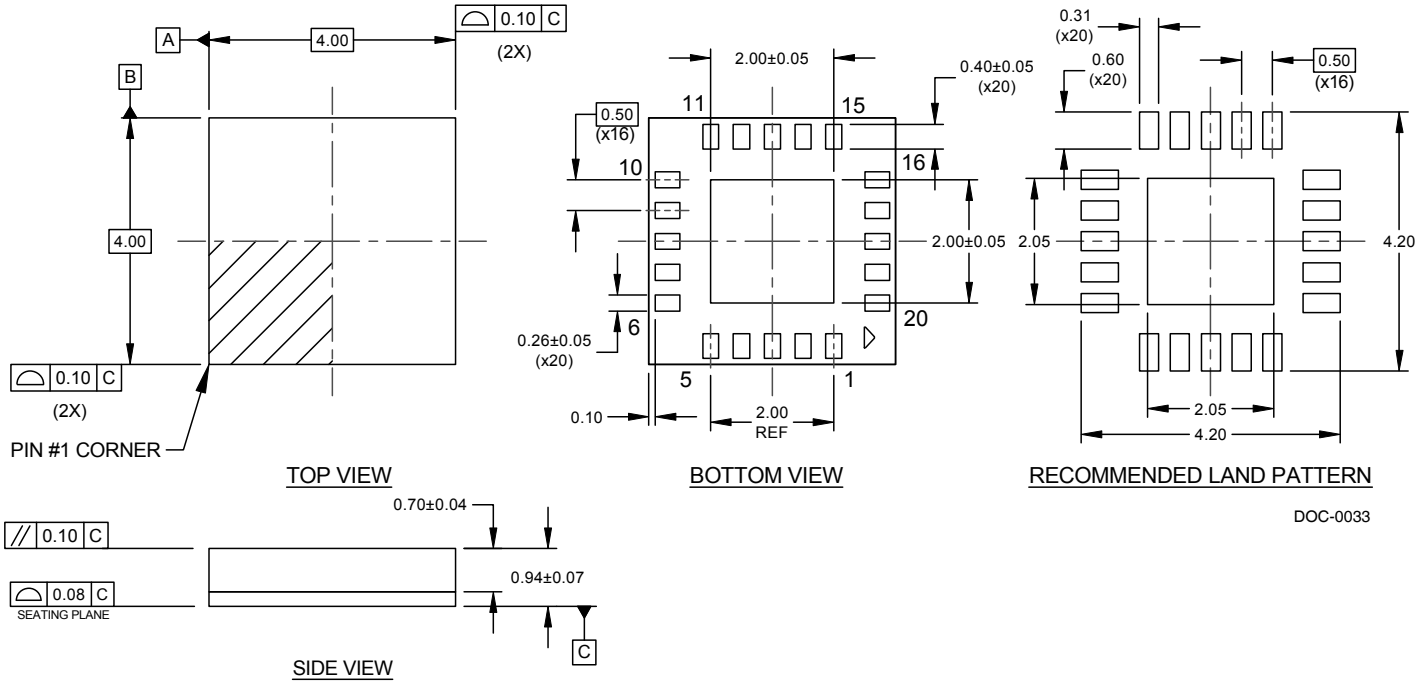
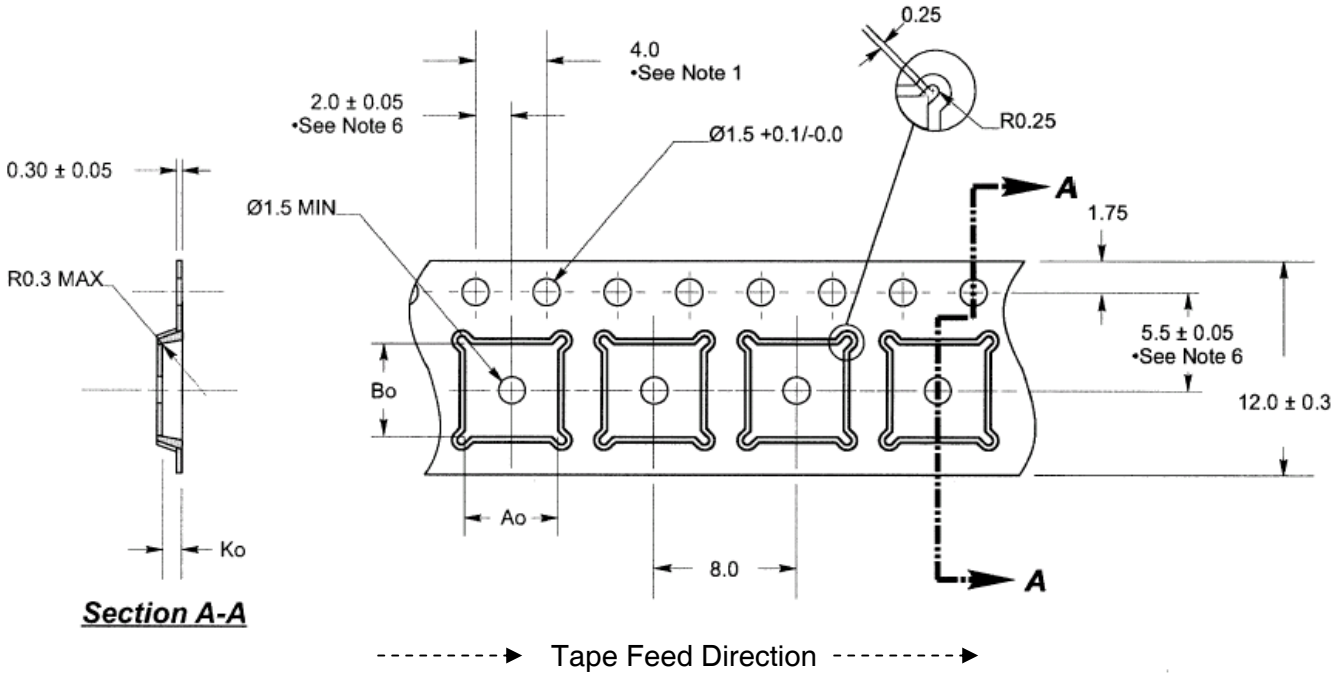


Figure 22. Top Marking Specifications

DOC-01641

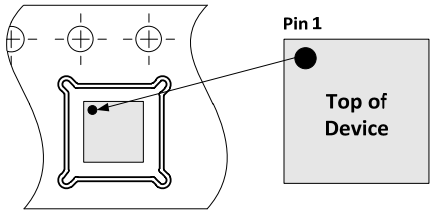
● = Pin 1 designator
YYWW = Date Code
ZZZZZ = Last five digits of Lot Number

Figure 23. Tape and Reel Drawing



Notes:
1. 10 sprocket hole pitch cumulative tolerance ±0.02
2. Camber not to exceed 1 mm in 100 mm
3. Material: PS + C
4. Ao and Bo measured as indicated
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole

Ao = 4.35 mm
Bo = 4.35 mm
Ko = 1.1 mm



Device Orientation in Tape

Table 6. Ordering Information

Order Code	Description	Package	Shipping Method
PE42420LGBB-Z	PE42420 SPDT RF switch	Green 20-lead 4x4 mm LGA	3000 units / T&R
EK42420-02	PE42420 Evaluation kit	Evaluation kit	1 / Box

Sales Contact and Information

For sales and contact information please visit www.psemi.com.

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