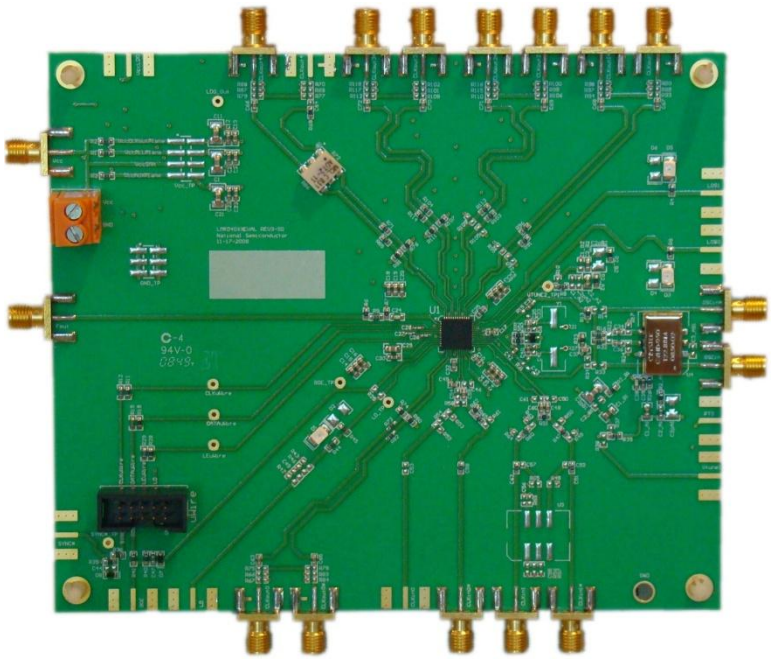
LMK041xx Family
Precision Clock Conditioner with Dual PLLs and Integrated VCO
Evaluation Board Operating Instructions

2012-01-16



LMK04100EVAL
LMK04131EVAL
LMK04102EVAL
LMK04133EVAL

Texas Instruments
Precision Timing Devices

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Quick Start

Full evaluation board instructions with data are downloadable from the product folder of the device at National Semiconductor's website, www.ti.com.

1. Connect a voltage of 3.3 volts to either the Vcc SMA connector or the alternate connector.
2. Connect a reference clock from a signal generator or other source. Exact frequency depends on programming. Default modes use a 122.88 MHz reference.
3. Connect the uWire header to a computer parallel port with the CodeLoader cable. A USB communication option is available, search at www.ti.com for: USB2UWIRE-IFACE.
4. Program the device with CodeLoader. Ctrl-L must be pressed at least once to load all registers once after CodeLoader is started or after restoring a Mode. CodeLoader is available for download at www.ti.com/tool/codeloader .
5. Measurements may be made at any clock output or Fout if enabled by programming.

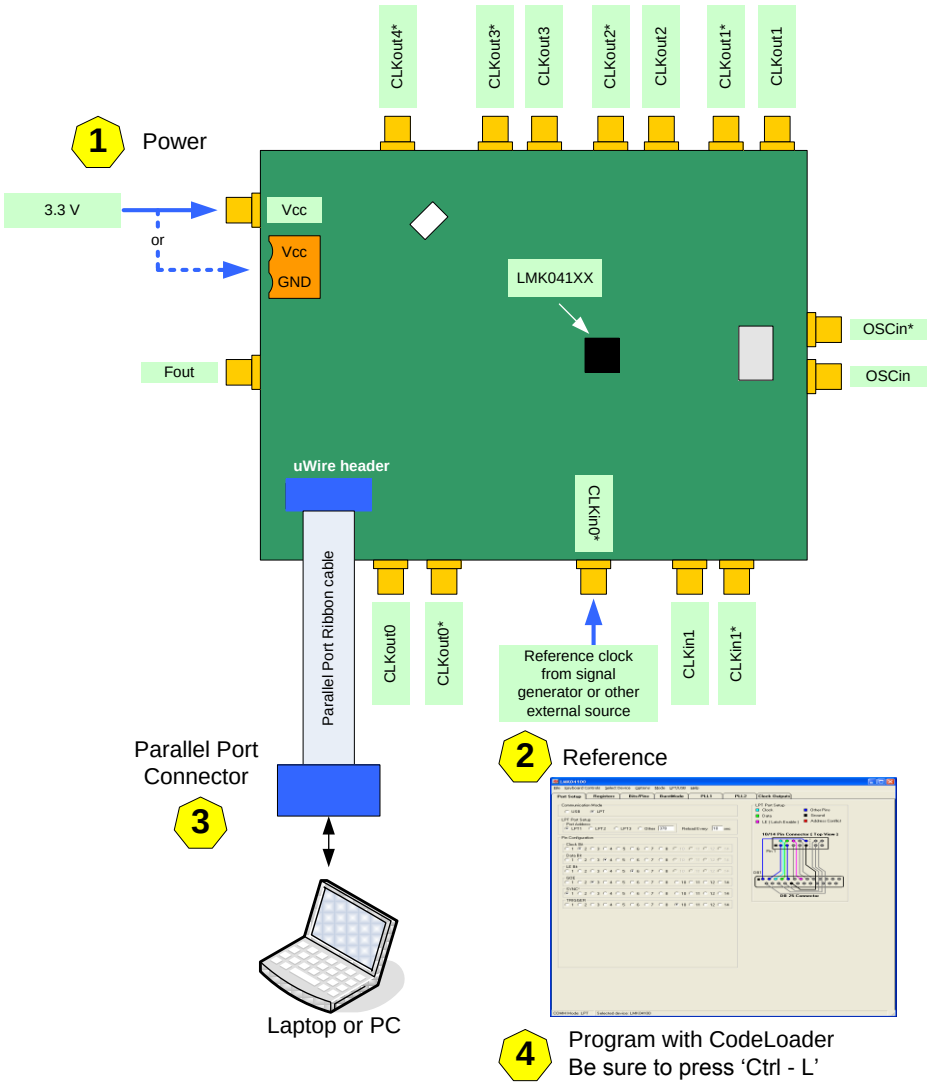


Figure 1 - Quick Start Diagram

PLL Loop Filters and Loop Parameters

The loop filters on the LMK041xx evaluation board are setup using the approach above. The loop filter for PLL1 has been configured for a narrow loop bandwidth (< 100 Hz), while the loop filter of PLL2 has been configured for a wide loop bandwidth (> 100 kHz). The specific loop bandwidth values depend on the phase noise performance of the oscillator mounted on the board. The following tables contain the parameters for PLL1 and PLL2 for each oscillator option.

National's Clock Design Tool can be used to optimize PLL phase noise/jitter for given specifications. See: http://www.ti.com/tool/clockdesigntool

PLL 1 Loop Filter

Table 1. PLL1 Loop Filter Parameters for Crystek 122.88 MHz VCXO and 12.288 MHz Vectron Crystal

Phase Margin	50º	Kφ (Charge Pump)	100 uA
Loop Bandwidth	12 Hz	Phase Detector Freq	1.024 MHz
		VCO Gain	2.5 kHz/Volt
Reference Clock Frequency	122.88 MHz	Output Frequency	122.88 MHz (To PLL 2)
Loop Filter Components	C1 = 100 nF	C2 = 680 nF	R2 = 39 kΩ

PLL2 Loop Filter

122.88 MHz VCXO (Reference Input)					
	LMK041x0B	**LMK041x1B**	**LMK041x2B**	**LMK041x3B**	**Units**
C1	Open				
C2	12				nF
C3	0				nF
C4	0.01				nF
R2	1.8				kΩ
R3	0.6				kΩ
R4	0.2				kΩ
Charge Pump Current, Kϕ	3.2				mA
Phase Detector Frequency	61.44				MHz
Frequency	1228.8	1474.56	1720.32	1966.08	MHz
Kvco	8	9	13	19	MHz/V
N	20	24	28	32	
Phase Margin	85.5	85.5	85.0	84.0	degrees
Loop Bandwidth	366	343	424	542	kHz

Note: PLL Loop Bandwidth is a function of Kϕ, Kvco, N as well as loop components. Changing Kϕ and N will change the loop bandwidth.

Evaluation Board Inputs/Outputs

The following table contains descriptions of the various inputs and outputs for the evaluation board.

Table 2. LMK041xx Evaluation Board I/O

Connector Name	Input/Output	Description
CLKout0 / CLKout0*, CLKout1 / CLKout1*, CLKout2 / CLKout2*, CLKout3 / CLKout3*, CLKout4 / CLKout4*	Output	Populated connectors. Differential clock output pairs. See **Error! Reference source not found.** for format of the output depending on part number. If an LVCMOS output, each output can be independently configured (non-inverted, inverted, tri-state, and LOW). On the evaluation board, all clock outputs are AC-coupled to allow safe testing with RF test equipment. • All LVPECL/2VPECL clock outputs are terminated to GND with a 120 ohm resistor, one on each output pin of the pair. CLKout4 is configured with an on board balun. Part number is Mini-circuits' ADT2-1T. According to the ADT2-1T datasheet the 3 dB frequency range is 0.4 to 450 MHz. See Appendix F: Balun Information for more detail.
Fout	Output	Populated connector. When enabled, buffered VCO output. AC-coupled. The default configuration on the board contains a 3-dB attenuator on the Fout signal.
Vcc	Input	Populated connector. DC power supply for the PCB. Removing R1, R2, or R3 allow for splitting the power to various devices on the board. For example, the VCXO is powered from the VccAUXPlane connected via R3. Note: The LMK04100 Family contains internal voltage regulators for the VCO, PLL and related circuitry. The clock outputs do not have an internal regulator. A clean power supply is required for best performance.
VccLDO	Input	Unpopulated connector. Vcc input for LDOs on bottom of PCB. Refer to schematics for more information.

<table>
<tr><th>Connector Name</th><th>Input/Output</th><th>Description</th></tr>
<tr><td>CLKin0/CLKin0*,
CLKin1/CLKin1*</td><td>Input</td><td>Populated connectors.

Reference clock inputs for PLL1. The default board configuration is setup for a single-ended reference source at CLKin0* (CLKin0 pin is AC-coupled to ground). The mode of the clock input buffer is programmable in CodeLoader on the Bits/Pins tab, and may be either bi-polar junction mode or MOS mode.

The input level for the various modes is as in the datasheet:
<table>
<tr><th colspan="5">AC Coupled Input Clock Voltage Levels</th></tr>
<tr><th>Input</th><th>Mode</th><th>Min</th><th>Max</th><th>Units</th></tr>
<tr><td>Differential</td><td>Bipolar</td><td>0.25</td><td>2.0</td><td>Vpp</td></tr>
<tr><td>Differential</td><td>MOS</td><td>0.25</td><td>2.0</td><td>Vpp</td></tr>
<tr><td>Single Ended</td><td>Bipolar</td><td>0.5</td><td>3.1</td><td>Vpp</td></tr>
<tr><td>Single Ended</td><td>MOS</td><td>0.5</td><td>3.1</td><td>Vpp</td></tr>
</table>
If a DC-coupled clock is used to drive either of the inputs, the high voltage level must be at least 2 volts and the low voltage no greater than 0.4 volts.

By default CLKin0 is the active input in either of the auto-switching modes (CLKin0 non-revertive, CLKin0 revertive). When loss of CLKin0 is detected, the device automatically switches to CLKin1 if an active reference clock is attached. See datasheet for further explanation.</td></tr>
<tr><td>LOS0, LOS1</td><td>Output</td><td>Unpopulated connectors.

Loss-of-Signal indicator (when LOS_TYPE = Active CMOS, default) for CLKin0/0* and CLKin1/1*. The LEDs D5 and D3 are light red when no signal is detected according to the datasheet specification for LOS pins. Bits/Pins, LOS_TYPE = Active CMOS for default operation.</td></tr>
<tr><td>OSCin/OSCin*</td><td>Input</td><td>Populated connectors.

By altering the PCB an external VCXO may be attached to the OSCin/OSCin* SMA connectors. Either a differential or single-ended device may be used. If a single-end device is used, OSCin* should be tied to GND through a capacitor that matches the AC-coupling capacitor value used for the OSCin pin. See datasheet for OSCin port signal specifications.</td></tr>
</table>

Connector Name	Input/Output	Description
Vtune1	Output	Unpopulated connector. Tuning voltage output from the loop filter for PLL1. If an external VCXO is used, this tuning voltage should be connected to the voltage control pin of the external VCXO. Note: Resistor R38 must be populated with a zero ohm resistor to control an off-board VCXO.
uWire	Input/Output	Populated connector. 10-pin header programming interface for the board. Of Most important are the CLKuWire, DATAuWire, and LEuWire programming lines from this header. Each of these signals, GEO, and SYNC* can be monitored through test points on the board.
LD	Output	Unpopulated connector. The LD pin is attached to a multiplexer inside the device and may be programmed with a variety of internal signals for monitoring internal device functions and troubleshooting. See datasheet for further explanation. The *lock detect* signal is accessible through this pin.
LD_TP	Output	Test point attached to the LD pin of the device. See LD above for more information.
GOE	Input	Unpopulated connector. Access to GOE of device.
SYNC*	Input	Unpopulated connector. Access to SYNC* of device.
PTO	Output	Unpopulated connector. Vcc SMA located close to OSCin SMAs for powering external oscillator boards.

Appendix A: CodeLoader Usage

Code Loader is used to program the evaluation board with either an LPT port using the included CodeLoader cable or with a USB port using the optional USB <--> uWire cable available from http://www.ti.com/tool/usb2uwire-iface. The part number is USB2UWIRE-IFACE.

Port Setup Tab

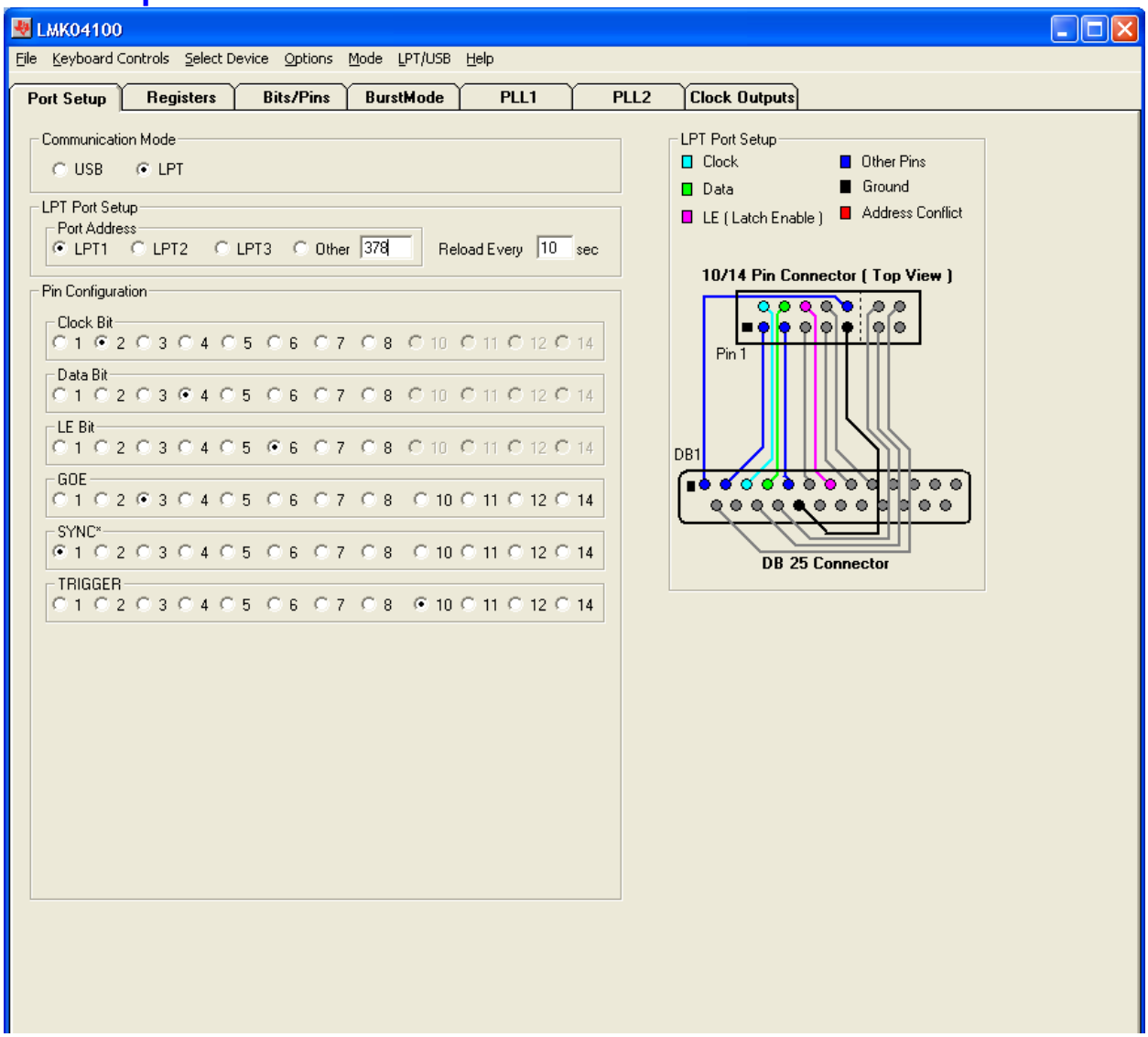


Figure 2 - Port Setup tab

On the Port Setup tab, the user may select the type of communication port (USB or Parallel) that will be used to program the device on the evaluation board. If parallel port is selected, the user should ensure that the correct port address is entered.

The Pin Configuration field is hardware dependent and normally SHOULD NOT be changed by the user. Figure 2 shows the default settings.

Clock Outputs Tab

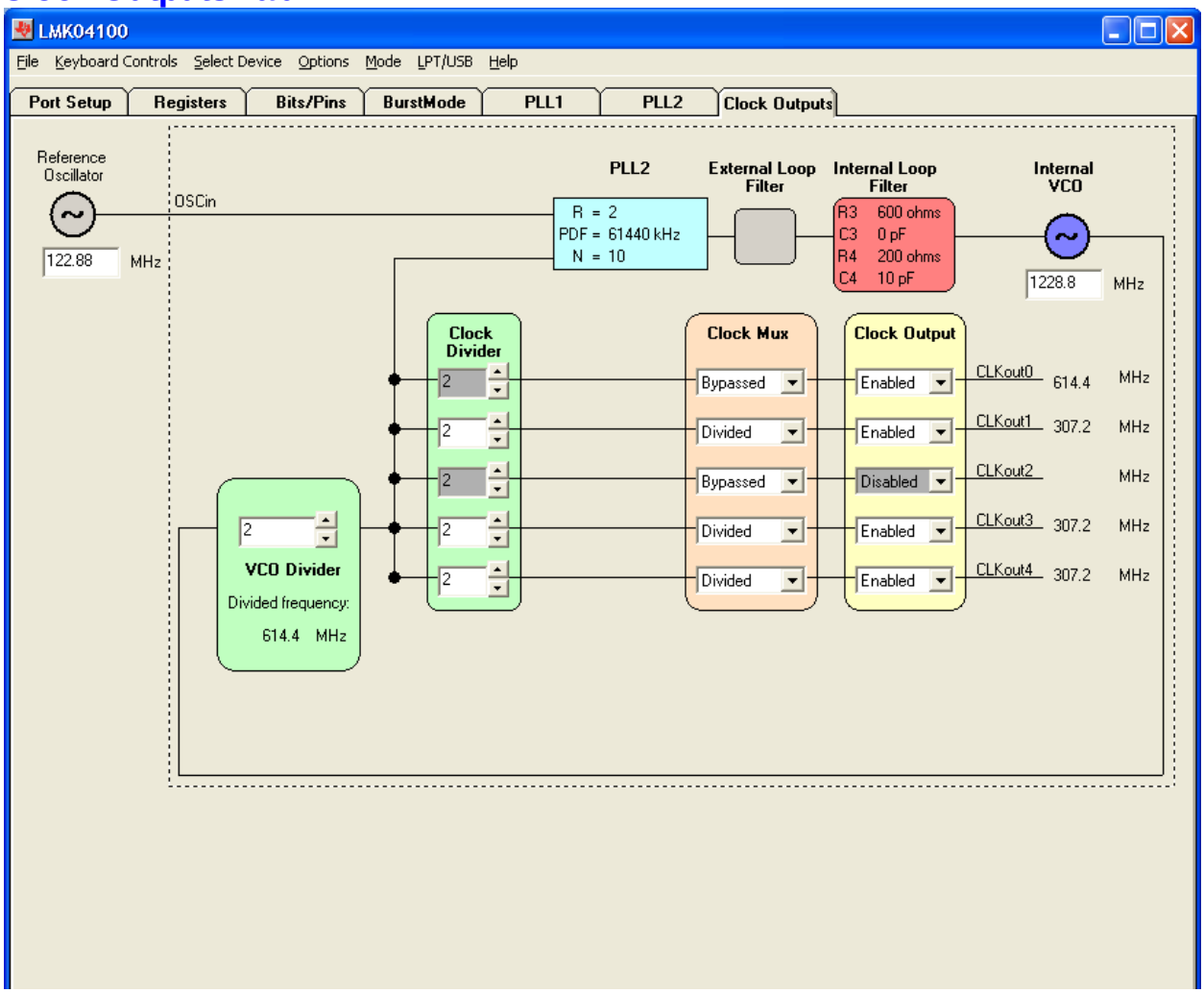


Figure 3 - Clock Outputs tab

The clock outputs tab allows the user to Enable/Disable individual clock outputs, select the clock mode (Bypass/Divided/Delayed/Divided & Delayed), set the clock output delay value (if delay is enabled), and the clock output divider value (2, 4, 6, …, 510).

This tab also allows the user to select the VCO Divider value (2, 3, …, 8). Note that the total PLL2 N divider value is composed of both the VCO Divider value and the N value shown in the blue box in the image, and is given by: N_TOTAL = VCO Divider * N.

Clicking on the blue box that contains R, PDF and N values takes the user to the PLL2 tab where these values may be changed.

Clicking on the components in the box containing the Internal Loop Filter values allows the user to change these component values.

The Reference Oscillator value field may be changed in either the Clock Outputs tab or the PLL2 tab. Note this value should match the value of the on-board VCXO or Crystal. **When using the EN_PLL2_REF2X = 1**, then Reference Oscillator field should be twice the VCXO or Crystal frequency.

PLL1 Tab

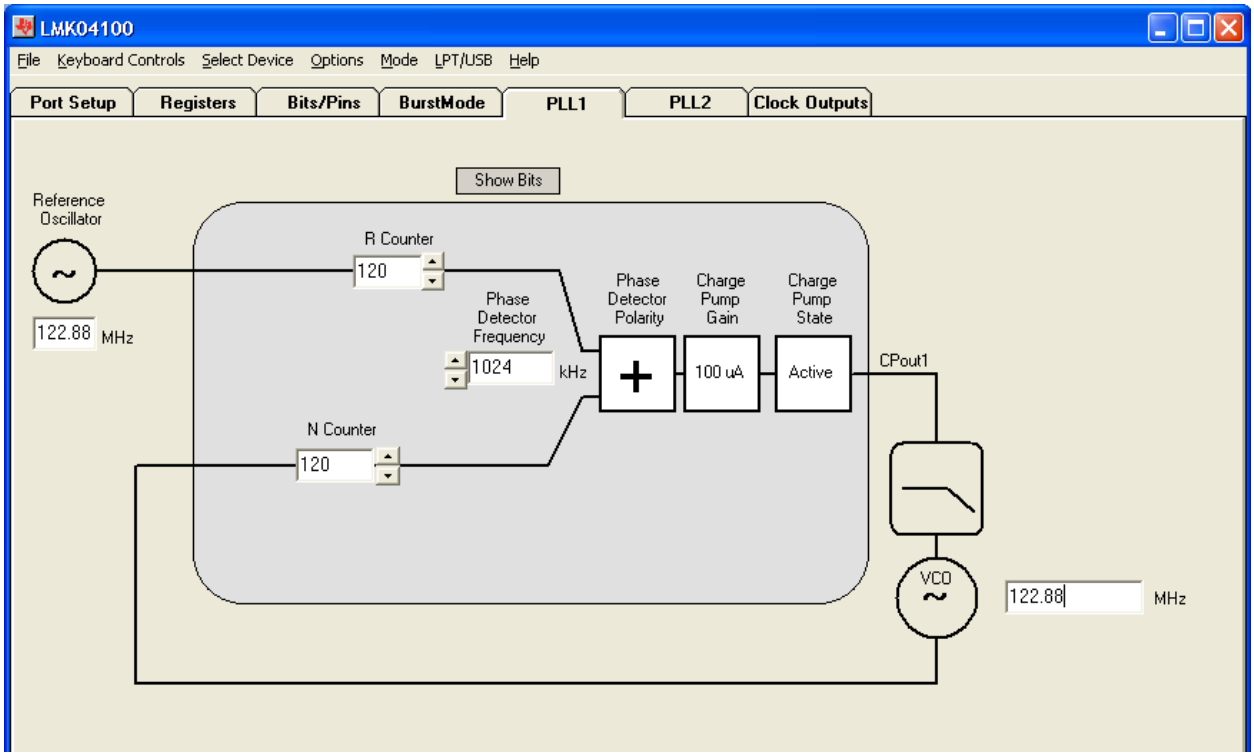


Figure 4 - PLL1 tab.

The PLL1 tab allows the user to change:

- External VCXO (or Crystal oscillator) frequency. ***Note: This value must be entered in both the PLL1 and PLL2 tabs.***
- PLL1 Phase detector frequency
- PLL1 R-counter value
- PLL1 N-counter value
- CLKin (Reference) oscillator frequency
- PLL1 Phase Detector polarity (for external VCXO tuning slope, click on the polarity value)
- PLL1 Charge pump gain (left click and right click on the charge pump current value)
- PLL1 Charge pump state (click on the charge pump state value)

Note that the value entered in the **VCO** frequency field on the PLL1 tab must match the **Reference Oscillator** frequency entered on the PLL2 tab and the OSCin_FREQ on the Bits/Pins tab. Updating the PLL2 tab Reference Oscillator frequency will automatically update the value of OSCin_FREQ on the Bits/Pins tab. The only time that the Reference Oscillator frequency of PLL2 tab will be different from the VCO frequency of PLL1 is when the EN_PLL2_REF2X mode is enabled.

PLL2 Tab

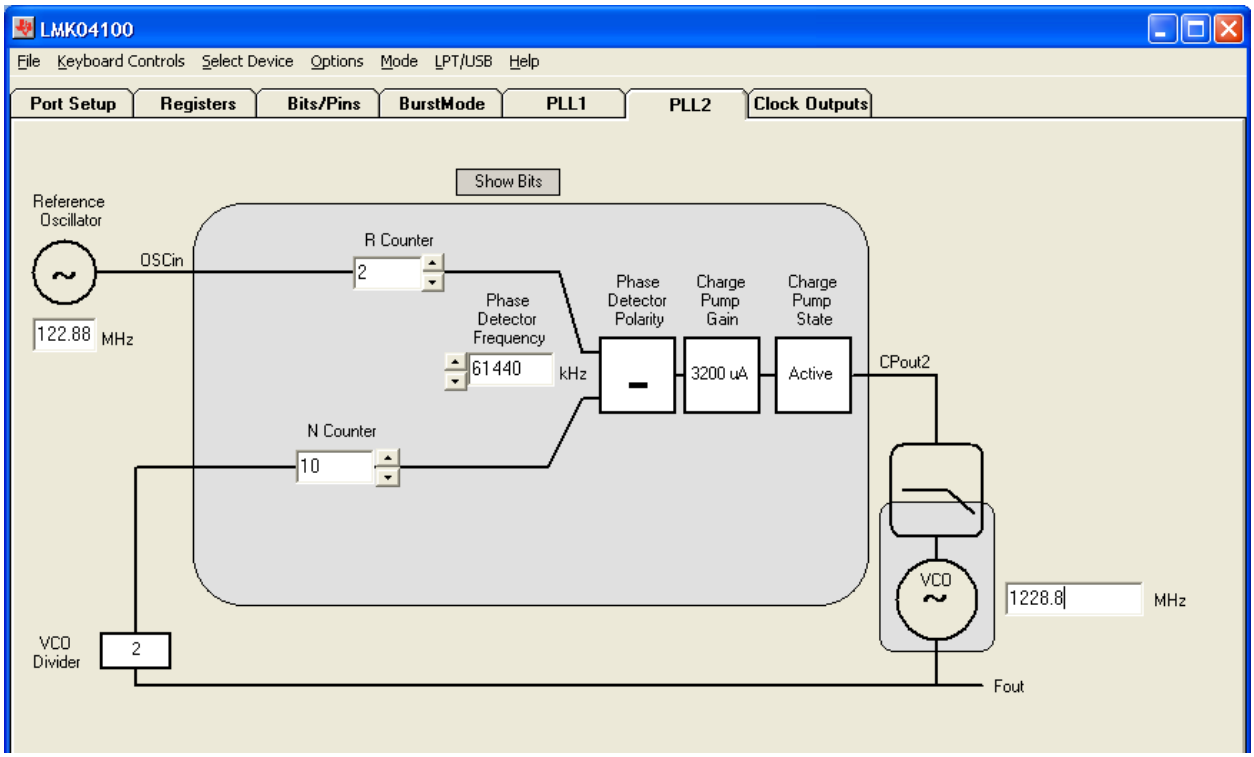


Figure 5 - PLL2 tab.

The PLL2 tab allows the user to change:

- VCO frequency
- PLL2 Phase detector frequency
- PLL2 R-counter value
- PLL2 N-counter value
- The frequency of the external VCXO (or XTAL oscillator). ***Note: This value must be entered in both the PLL1 and PLL2 tabs.***
- PLL2 Charge pump gain
- PLL2 Charge pump state

Any changes made on this tab are reflected in the Clock Outputs tab. Note that the PLL2 Phase Detector polarity is fixed and cannot be changed by the user. Also note that the VCO frequency should conform to the specified frequency range for the device.

Note that the value entered in the **VCO** frequency field on the PLL1 tab must match the **Reference Oscillator** frequency entered on the PLL2 tab and the OSCin_FREQ on the Bits/Pins tab. Updating the PLL2 tab Reference Oscillator frequency will automatically update the value of OSCin_FREQ on the Bits/Pins tab. The only time that the Reference Oscillator frequency of PLL2 tab will be different from the VCO frequency of PLL1 is when the EN_PLL2_REF2X mode is enabled.

Bits/Pins Tab

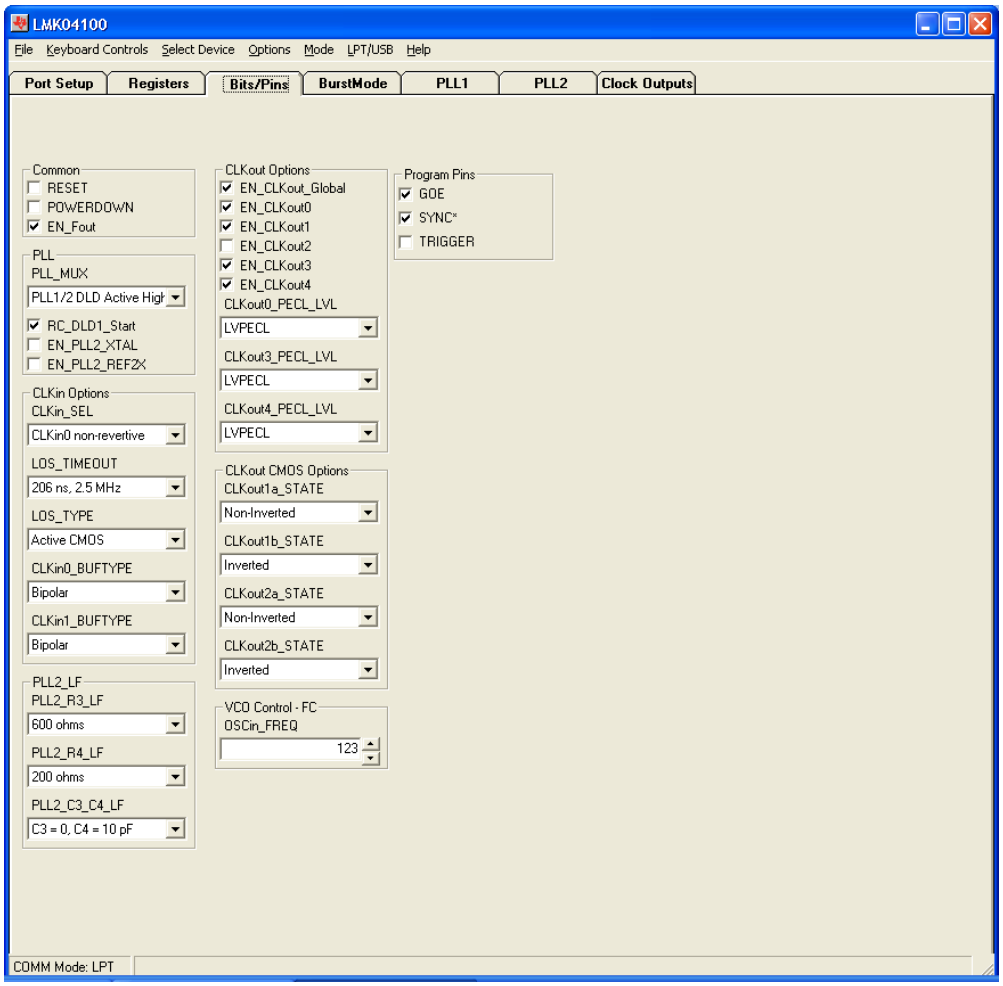


Figure 6 - Bits/Pins tab.

The Bits/Pins tab allows the user to program bits directly. Many of which are not available on other tabs. Refer to the datasheet for more detailed information. The bits available are:

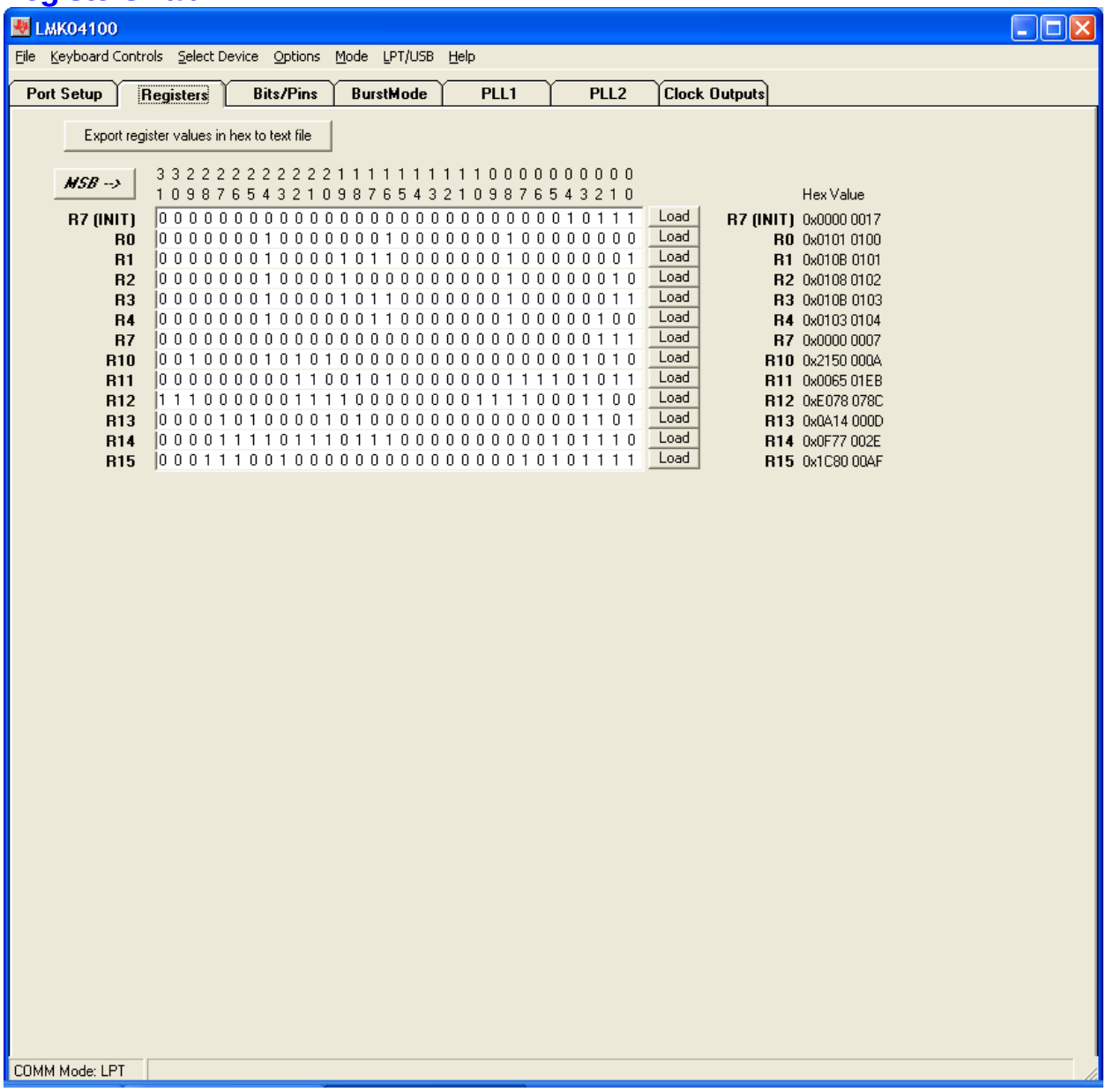
- Common Box
  - RESET - Set the reset bit. This will reset the device. In a normal application it is not necessary to program this bit clear since it is auto-clearing. However in the CodeLoader software, RESET must be clicked again (cleared) to not cause a reset every time R7 is programmed.
  - POWERDOWN - Place the device in powerdown mode.
  - EN_Fout – Enable the Fout port.
- PLL Box
  - PLL_MUX – Set the function of the LD pin.
  - RC_DLD1_Start – Prevent PLL2 from locking until digital lock detect from PLL1 is achieved.

  - EN_PLL2_XTAL – Enables Crystal mode for PLL2. For use with Crystals as opposed to a VCXO.
  - EN_PLL2_REF2X – Doubles the reference frequency of PLL2. Note with this is enabled, the PLL_R value is invalid. Program the Reference Oscillator on PLL2 Tab to be twice the VCO frequency on PLL1 tab. This adjustment must be done manually.

- CLKin Options Box
  - CLKin_SEL – Sets manual or automatic switching modes for selecting a reference oscillator for PLL1.
  - LOS_TIMEOUT – The timeout value before a loss of signal on a clock input is registered on the LOS pins.
  - LOS_TYPE – Set the type of output for the LOS pins.
  - CLKin0_BUFTYPE & CLKin1_BUFTYPE – Select the input buffer used for the respective clock input.
- PLL2_LF Box
  - Set the integrated loop filter values for PLL2 including,
    - PLL2_R3_LF – R3 value
    - PLL2_R4_LF – R4 value
    - PLL2_C3_C4_LF – C3 and C4 value at the same time
  - It is also possible to set these values by clicking on the loop filter values on the Clock Outputs tab.
- CLKout Options Box
  - EN_CLKout_Global – A global enable for clocks, **if unchecked no outputs will be observed!**
  - EN_CLKout0 through EN_CLKout4 – Individual clock output enables. These can also be set on the Clock Outputs tab.
  - The number of options vary depending on the option of the LMK device selected.
    - CLKout#_PECL_LVL – Set the level of an LVPECL output to LVPECL or 2VPECL. The 2VPECL a higher output level than LVPECL.
- CLKout CMOS Options Box
  - The presence of this box and the number of options on this tab depends upon the option of the LMK device.
    - CLKout##_STATE – Set the state of the individual LVCMOS output.
- VCO Control – FC Box
  - OSCin_FREQ – Must be set to the reference frequency of PLL2 in MHz, which should normally be the VCO frequency of PLL1. **NOTE: It is important to enter the correct frequency value in this field, as it is used by the internal state machine of the LMK041xx to execute its calibration routine for the internal VCO.** An incorrect value may result in an unlocked condition for the synthesizer.
    - Entering a reference oscillator frequency on PLL2 tab will automatically update this register with the frequency to the nearest MHz.
- Program Pins Box
  - GOE – Set high or low voltage on GOE pin. Checked is high voltage.
    - If GOE is low, then no clock outputs will be observed!

- SYNC* – Set high or low voltage on SYNC* pin. Checked is high voltage.
  - If SYNC* is low, then no clock outputs will be observed on divided clock outputs!
- TRIGGER – Set high or low voltage on pin 10 of uWire header.

Registers Tab



The registers tab shows the value of each register. This is convenient for programming the device to the desired settings, then recording the hex values for programming in your own application. By clicking in the "bit field" it is possible to manually change the value of registers by typing '1' and '0.'

Appendix B: Typical Phase Noise Performance Plots

PLL1

The LMK041xx's two stage jitter cleaning process involves masking the reference noise with a VCXO or Crystal. Therefore the phase noise performance of the VCXO or Crystal of PLL1 is a very important contributor to the final phase noise of the system.

Crystek 122.88 MHz VCXO

The phase noise of the reference is masked by the phase noise of this VCXO by using a narrow loop bandwidth. This VCXO sets the reference noise to PLL2. Figure 7 shows the open loop typical phase noise performance of the CVHD-950-122.88 Crystek VCXO.

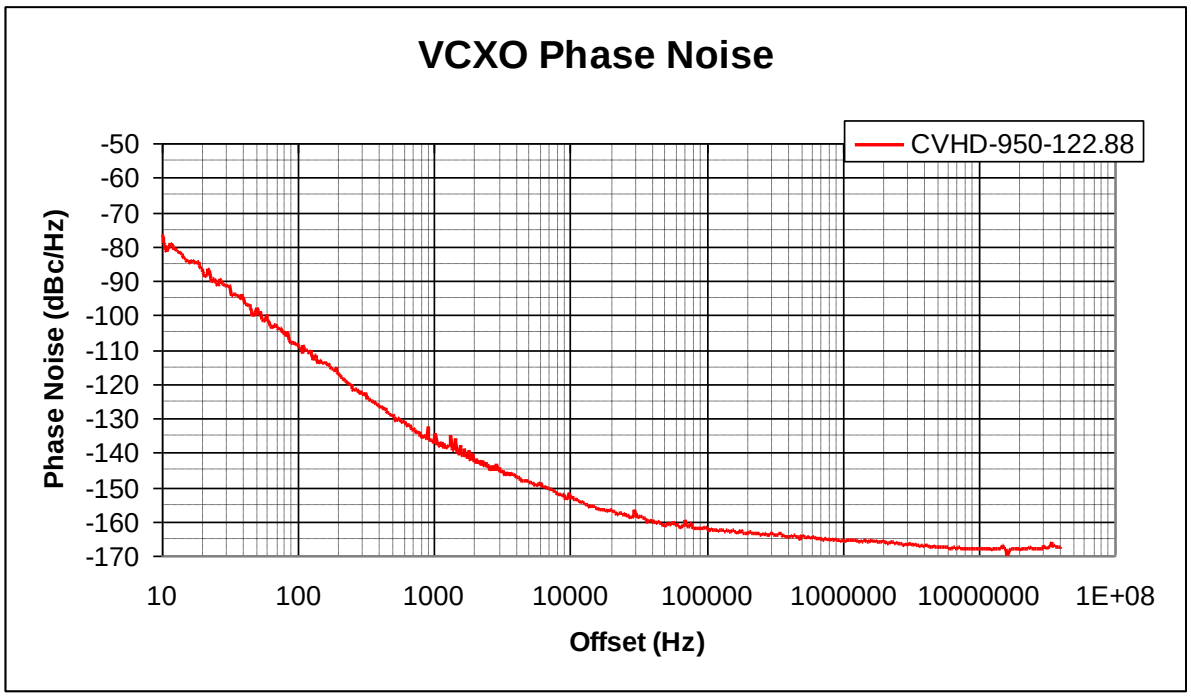


Figure 7 - CVHD-950-122.88 MHz VCXO Phase Noise at 122.88 MHz

Table 3 - VCXO Phase Noise at 122.88 MHz (dBc/Hz)

Offset	Phase Noise
10 Hz	-76.6
100 Hz	-108.9
1 kHz	-137.4
10 kHz	-153.3
100 kHz	-162.0
1 MHz	-165.7
10 MHz	-168.1
40 MHz	-168.1

Table 4 - VCXO RMS Jitter to high offset of 20 MHz at 122.88 MHz (rms fs)

Low Offset	Jitter
10 Hz	515.4
100 Hz	60.5
1 kHz	36.2
10 kHz	35.0
100 kHz	34.5
1 MHz	32.9
10 MHz	22.7

PLL2

The closed loop performance of the system as measured at the VCO output Fout. Fout phase noise performance of the various LMK options is plotted in Figure 8. Table 5 and Table 6 summarize the phase noise and jitter of Fout.

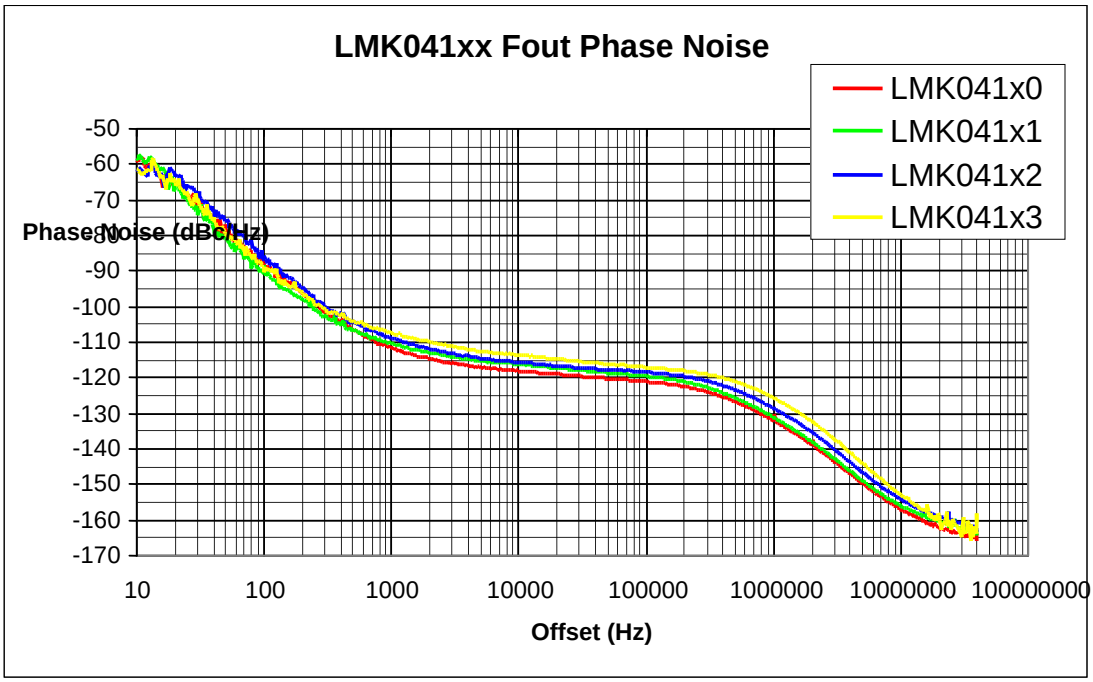


Figure 8 - LMK041xx PLL2 Phase Noise (Fout)

Table 5 - LMK041x0 Phase Noise (dBc/Hz)

Offset	LMK041x0	LMK041x1	LMK041x2	LMK041x3
10 Hz	-58.7	-58.3	-61.3	-61.1
100 Hz	-88.0	-88.3	-85.7	-90.4
1 kHz	-111.6	-110.2	-108.9	-107.5
10 kHz	-118.2	-116.3	-115.7	-113.5
100 kHz	-121.1	-119.5	-118.4	-117.0
1 MHz	-132.0	-131.1	-128.6	-125.6
10 MHz	-157.1	-155.8	-154.0	-152.7
40 MHz	-165.9	-164.2	-162.3	-160.8

Table 6 - LMK041x0 RMS Jitter; Integrated to from low limit to 20 MHz (rms fs)

Low Offset	LMK041x0	LMK041x1	LMK041x2	LMK041x3
10 Hz	580.0	506.6	443.4	356.0
100 Hz	127.2	117.5	124.5	132.8
1 kHz	114.8	111.3	114.9	128.1
10 kHz	111.7	108.0	112.0	125.0
100 kHz	97.3	92.7	99.2	112.2
1 MHz	39.7	36.2	41.6	50.9
10 MHz	6.0	5.9	6.0	5.5

Clock Outputs

The LMK04100 Family features LVDS, LVPECL, 2VPECL, and LVCMOS types of outputs. Included below are various phase noise measurements for each output.

Device	LVDS	LVPECL/2VPECL	LVCMOS	VCO Frequency
LMK041x0 (LMK04100)		X	X	1185 to 1296 MHz
LMK041x1 (LMK04131)	X	X	X	1430 to 1570 MHz
LMK041x2 (LMK04102)		X	X	1566 to 1724 MHz
LMK041x3 (LMK04133)	X	X	X	1840 to 2160 MHz

Note: The device in parenthesis is the device used for the measurement in these evaluation board instructions.

Clock Output Measurement Technique

The measurement technique for each output type varies.

LVDS – measured with an ADT2-1T balun to test equipment.
LVPECL/2VPECL – Measured by terminating complementary output with 50 ohm load, then taking output to test equipment.
LVCMOS – Measured by enabling only one side of the LVCMOS output and taking the operating output to test equipment.

The following table lists the test conditions used for the phase noise measurements for the VCXO option:

Table 7 . LMK041xx test conditions

Parameter	Value
PLL1 Reference clock input	CLKin0* single-ended input, CLKin0 AC-coupled to GND
PLL1 Reference Clock frequency	122.88 MHz
PLL1 Phase detector frequency	1024 kHz
PLL1 Charge Pump Gain	100 uA
VCXO frequency	122.88 MHz
PLL2 phase detector frequency	61.44 MHz
PLL2 Charge Pump Gain	3200 uA
PLL2 REF2X mode	Disabled

LMK041x0 Phase Noise

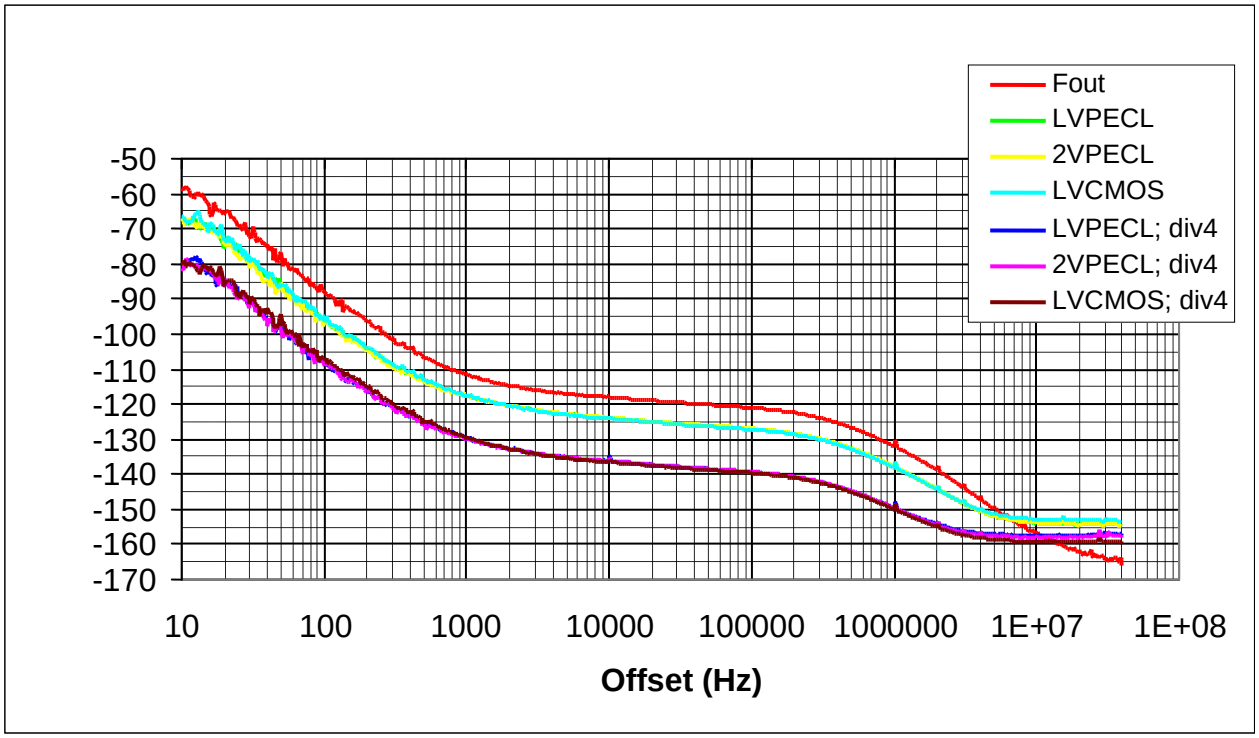


Figure 9 - LMK041x0B Phase Noise

The Fout frequency is 1228.8 MHz. The clock out frequency is 614.4 MHz, and the clock out div 4 frequency is 153.6 MHz.

Table 8 - LMK041x0 Phase Noise (dBc/Hz)

Offset	Fout	LVPECL	2VPECL	LVCMOS	LVPECL div4	2VPECL div4	LVCMOS div4
10 Hz	-58.7	-67.1	-67.1	-66.3	-79.8	-81.5	-79.7
100 Hz	-88.0	-95.8	-96.8	-94.8	-107.5	-109.1	-106.6
1 kHz	-111.6	-117.6	-117.7	-117.9	-129.5	-130.2	-129.4
10 kHz	-118.2	-123.8	-123.8	-124.2	-134.8	-135.2	-136.0
100 kHz	-121.1	-127.0	-127.0	-127.3	-139.4	-139.3	-139.6
1 MHz	-132.0	-137.9	-137.8	-138.1	-149.5	-149.6	-150.0
10 MHz	-157.1	-153.8	-153.8	-152.8	-157.4	-158.1	-159.2
40 MHz	-165.9	-154.8	-154.8	-153.6	-157.3	-158.0	-159.7

Table 9 - LMK041x0 RMS Jitter; Integrated to from low limit to 20 MHz (rms fs)

Low Limit	Fout	LVPECL	2VPECL	LVCMOS	LVPECL div4	2VPECL div4	LVCMOS div4
10 Hz	580.0	474.7	449.2	522.4	493.9	466.5	493.5
100 Hz	127.2	128.3	127.9	127.1	148.9	145.6	139.4
1 kHz	114.8	119.9	120.4	117.9	141.8	138.7	129.9
10 kHz	111.7	116.8	117.3	114.9	139.3	136.2	127.3
100 kHz	97.3	102.9	103.3	101.6	128.8	125.3	116.3
1 MHz	39.7	50.5	50.6	52.4	94.3	89.5	79.5

LMK041x1 Phase Noise

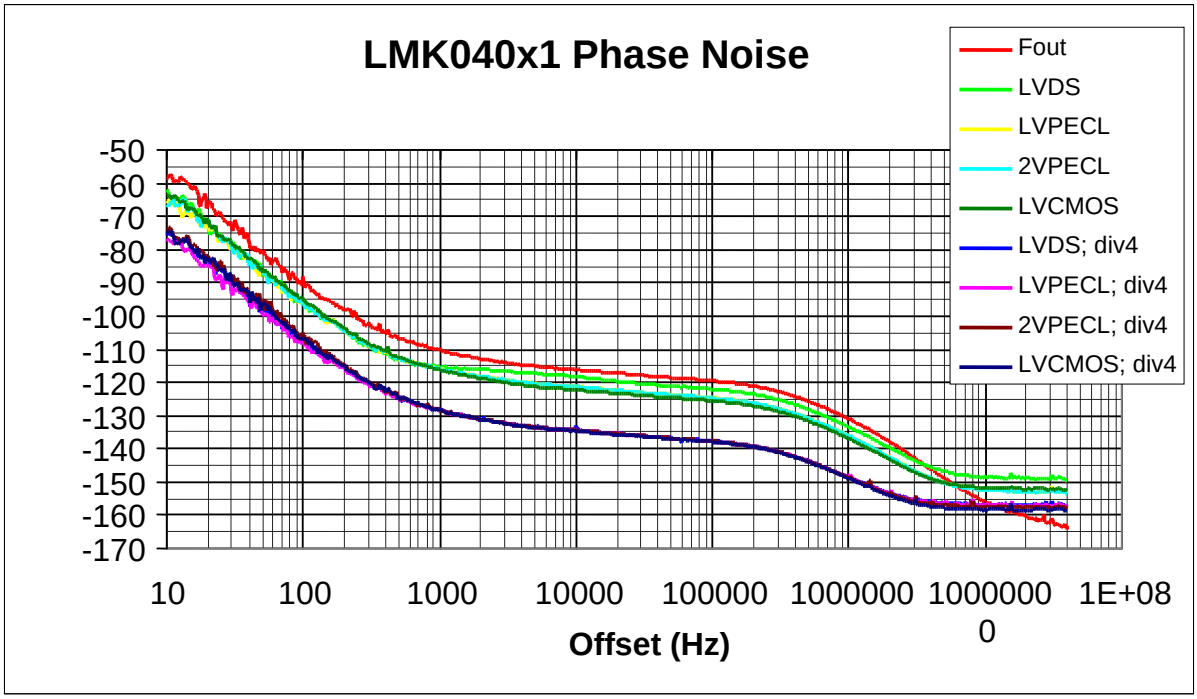


Figure 10 - LMK041x1 Phase Noise

The Fout frequency is 1474.56 MHz. The clock out frequency is 737.28 MHz, and the clock out div 4 frequency is 184.32 MHz. Note that the LVDS performance at 737.28 MHz is degraded because it is outside of the balun's operational bandwidth.

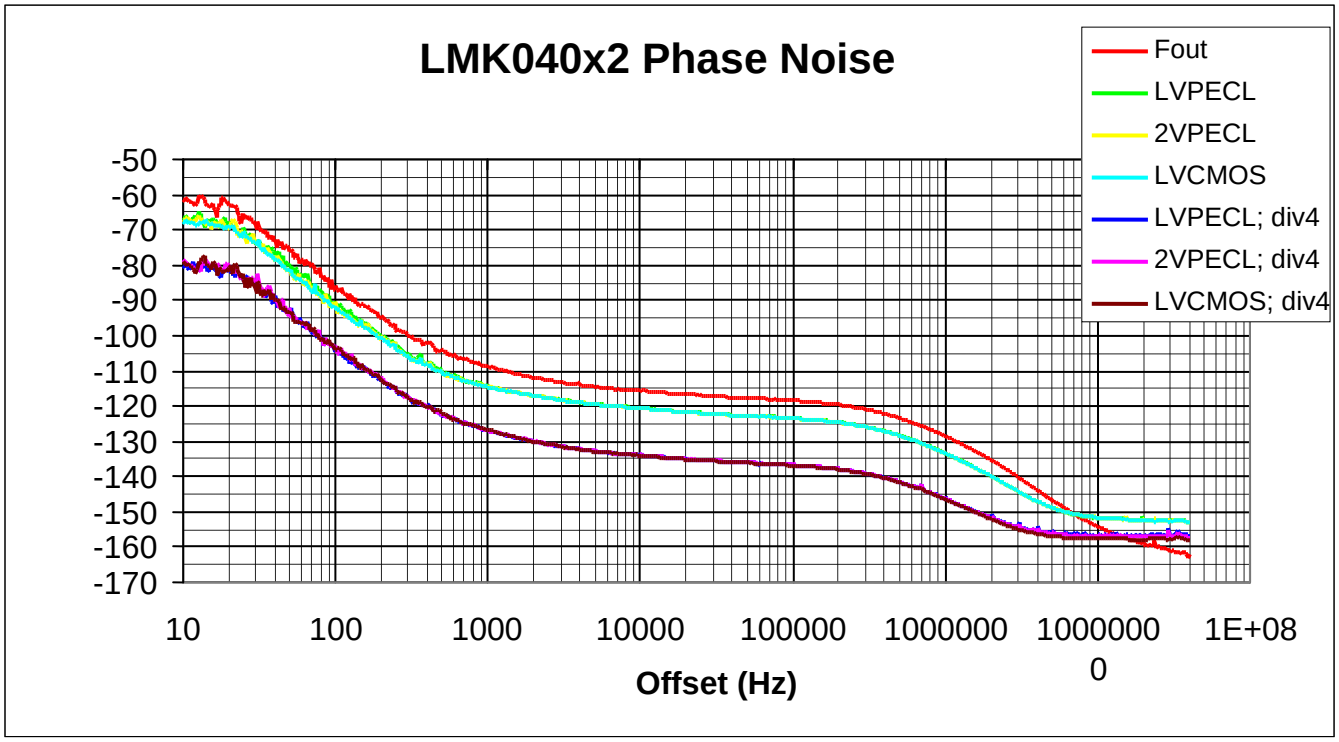
Table 10 - LMK041x1 Phase Noise (dBc/Hz)

Offset	Fout	LVDS	LVPECL	2VPECL	LVCMOS	LVDS div4	LVPECL div4	2VPECL div4	LVCMOS div4
10 Hz	-58.3	-62.0	-65.4	-66.4	-63.4	-74.8	-76.7	-73.8	-74.6
100 Hz	-88.3	-96.4	-95.9	-96.0	-94.8	-106.7	-107.7	-105.3	-106.7
1 kHz	-110.2	-115.3	-115.7	-115.8	-116.2	-128.3	-128.3	-128.1	-128.3
10 kHz	-116.3	-118.1	-121.2	-121.3	-122.0	-132.8	-134.0	-134.3	-134.7
100 kHz	-119.5	-122.0	-124.7	-124.7	-125.5	-137.7	-137.7	-137.8	-137.9
1 MHz	-131.1	-133.5	-136.2	-136.2	-137.0	-148.5	-148.7	-148.7	-148.9
10 MHz	-155.8	-148.2	-152.3	-152.3	-151.7	-156.9	-157.1	-157.5	-158.3
40 MHz	-164.2	-149.5	-153.5	-153.6	-152.5	-157.5	-157.3	-158.0	-158.8

Table 11 - LMK041x1 RMS Jitter; Integrated to from low limit to 20 MHz (rms fs)

Low Limit	Fout	LVDS	LVPECL	2VPECL	LVCMOS	LVDS div4	LVPECL div4	2VPECL div4	LVCMOS div4
10 Hz	506.6	538.4	425.5	458.5	501.9	532.2	445.6	591.0	544.1
100 Hz	117.5	178.3	132.4	131.8	123.1	141.0	138.6	139.1	132.5
1 kHz	111.3	174.2	127.0	126.4	116.2	135.1	133.3	131.4	125.5
10 kHz	108.0	169.5	123.4	122.8	113.0	132.4	130.7	128.7	122.8
100 kHz	92.7	147.7	107.2	106.7	98.7	120.7	119.0	116.8	110.8
1 MHz	36.2	72.9	50.4	50.1	49.1	85.2	83.4	80.3	73.4

LMK041x2 Phase Noise



The Fout frequency is 1720.32 MHz. The clock out frequency is 860.16 MHz, and the clock out div 4 frequency is 215.04 MHz.

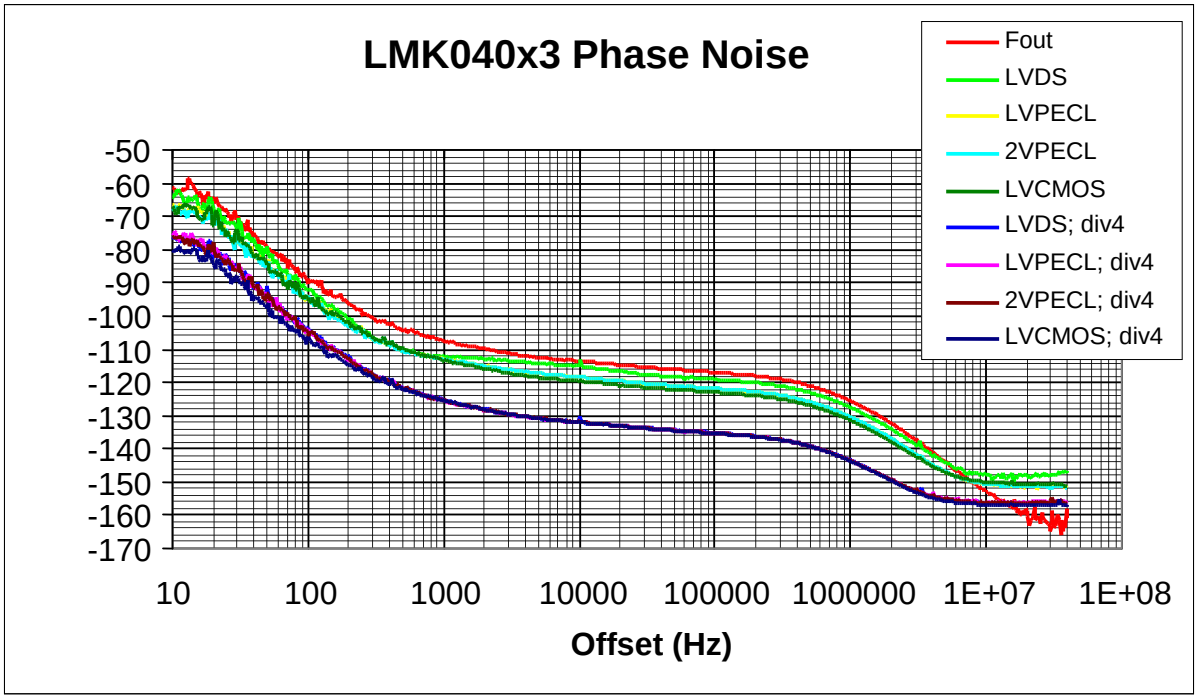
Table 12 - LMK041x2 Phase Noise (dBc/Hz)

Offset	Fout	LVPECL	2VPECL	LVCMOS	LVPECL div4	2VPECL div4	LVCMOS div4
10 Hz	-61.3	-66.6	-67.3	-67.7	-80.1	-78.7	-78.9
100 Hz	-85.7	-91.5	-90.4	-91.9	-103.3	-103.2	-103.8
1 kHz	-108.9	-114.3	-114.2	-114.6	-126.7	-127.2	-126.5
10 kHz	-115.7	-120.7	-120.7	-120.6	-133.5	-133.7	-134.1
100 kHz	-118.4	-123.5	-123.5	-123.5	-136.7	-136.7	-136.8
1 MHz	-128.6	-133.4	-133.4	-133.4	-146.2	-146.3	-146.5
10 MHz	-154.0	-151.5	-151.5	-151.6	-156.7	-157.0	-157.7
40 MHz	-162.3	-153.0	-153.2	-153.2	-157.0	-157.3	-158.2

Table 13 - LMK041x2 RMS Jitter; Integrated to from low limit to 20 MHz (rms fs)

Low Limit	Fout	LVPECL	2VPECL	LVCMOS	LVPECL div4	2VPECL div4	LVCMOS div4
10 Hz	443.4	498.1	477.3	450.5	439.3	473.4	458.5
100 Hz	124.5	143.1	140.8	140.4	141.0	140.7	136.6
1 kHz	114.9	132.7	132.1	132.0	132.3	131.1	126.6
10 kHz	112.0	129.6	129.0	129.0	130.0	128.7	124.2
100 kHz	99.2	115.7	115.2	115.2	119.7	118.3	113.7
1 MHz	41.6	54.9	54.8	54.7	79.2	77.1	71.8

LMK041x3 Phase Noise



The Fout frequency is 1966.08 MHz. The clock out frequency is 983.04 MHz, and the clock out div 4 frequency is 245.76 MHz. Note that the LVDS performance at 737.28 MHz is degraded because it is outside of the balun's operational bandwidth.

Table 14 - LMK041x3 Phase Noise (dBc/Hz)

Offset	Fout	LVDS	LVPECL	2VPECL	LVCMOS	LVDS div4	LVPECL div4	2VPECL div4	LVCMOS div4
10 Hz	-61.1	-63.9	-66.2	-67.6	-67.0	-76.1	-75.2	-75.9	-80.1
100 Hz	-90.4	-92.1	-94.6	-93.9	-94.3	-103.5	-103.7	-104.4	-106.3
1 kHz	-107.5	-112.2	-112.8	-112.8	-113.6	-125.5	-125.8	-125.5	-125.4
10 kHz	-113.5	-115.1	-118.1	-118.2	-119.7	-130.3	-131.4	-131.5	-132.0
100 kHz	-117.0	-119.1	-121.8	-121.9	-123.0	-135.2	-135.3	-135.3	-135.3
1 MHz	-125.6	-127.6	-130.4	-130.4	-131.5	-143.5	-143.6	-143.6	-143.7
10 MHz	-152.7	-148.0	-150.6	-150.6	-150.0	-156.3	-156.1	-156.3	-156.8
40 MHz	-160.8	-147.2	-151.9	-151.9	-151.2	-156.8	-156.4	-156.6	-157.3

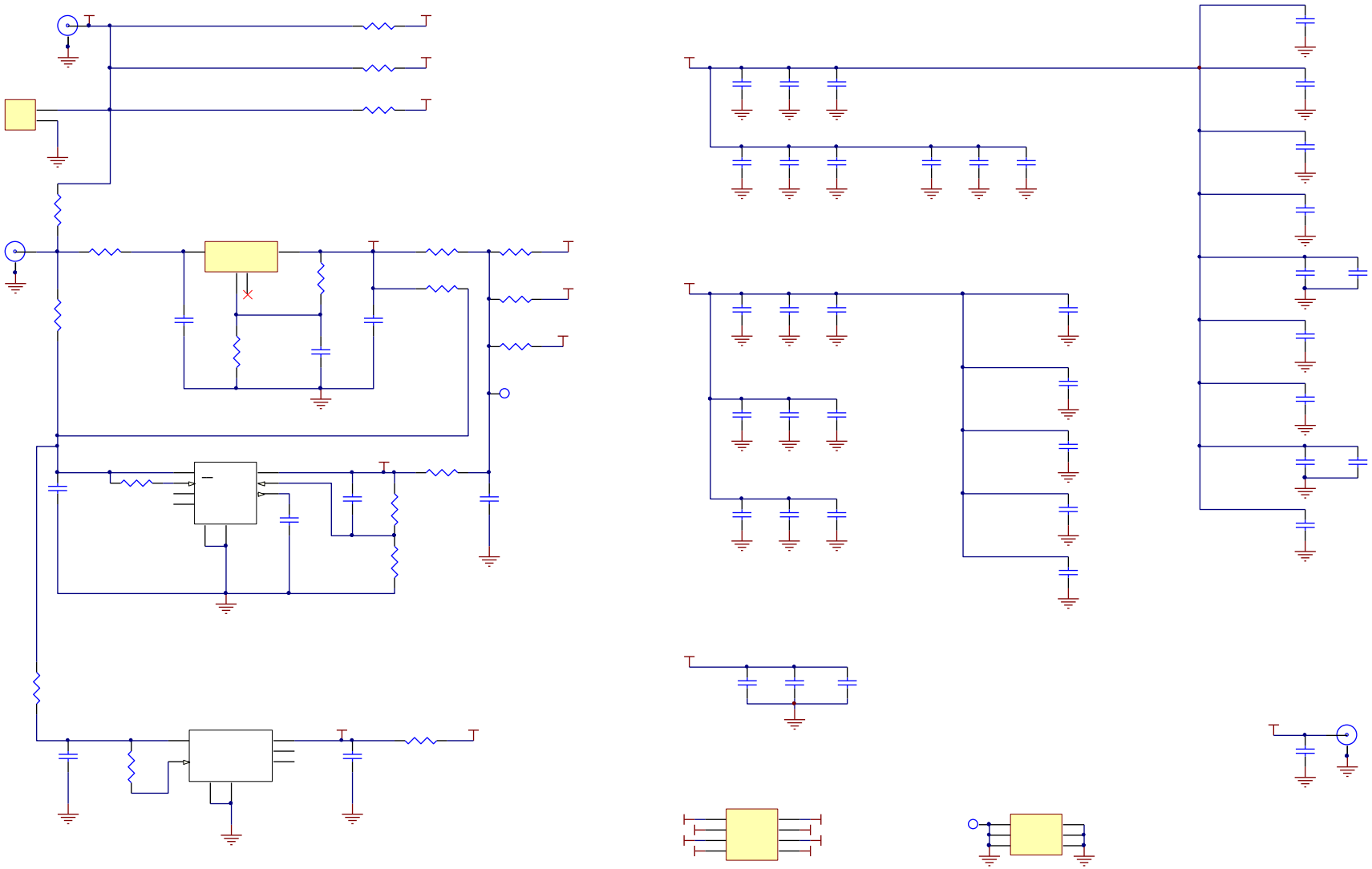
Table 15 - LMK041x3 RMS Jitter; Integrated to from low limit to 20 MHz (rms fs)

Low Limit	Fout	LVDS	LVPECL	2VPECL	LVCMOS	LVDS div4	LVPECL div4	2VPECL div4	LVCMOS div4
10 Hz	356.0	531.5	367.7	339.0	367.6	471.8	499.6	464.0	338.9
100 Hz	132.8	210.0	153.3	153.4	137.4	147.1	146.5	146.2	141.5
1 kHz	128.1	205.5	149.2	149.5	132.6	140.7	140.5	140.2	137.1
10 kHz	125.0	200.9	145.8	146.1	129.6	138.1	137.9	137.6	134.4
100 kHz	112.2	181.2	131.6	131.9	117.3	127.2	127.1	126.7	123.5
1 MHz	50.9	88.9	64.4	64.5	59.5	79.6	80.6	79.7	75.8

LMK04100BEVAL schematic.
Refer to BOM for differences.

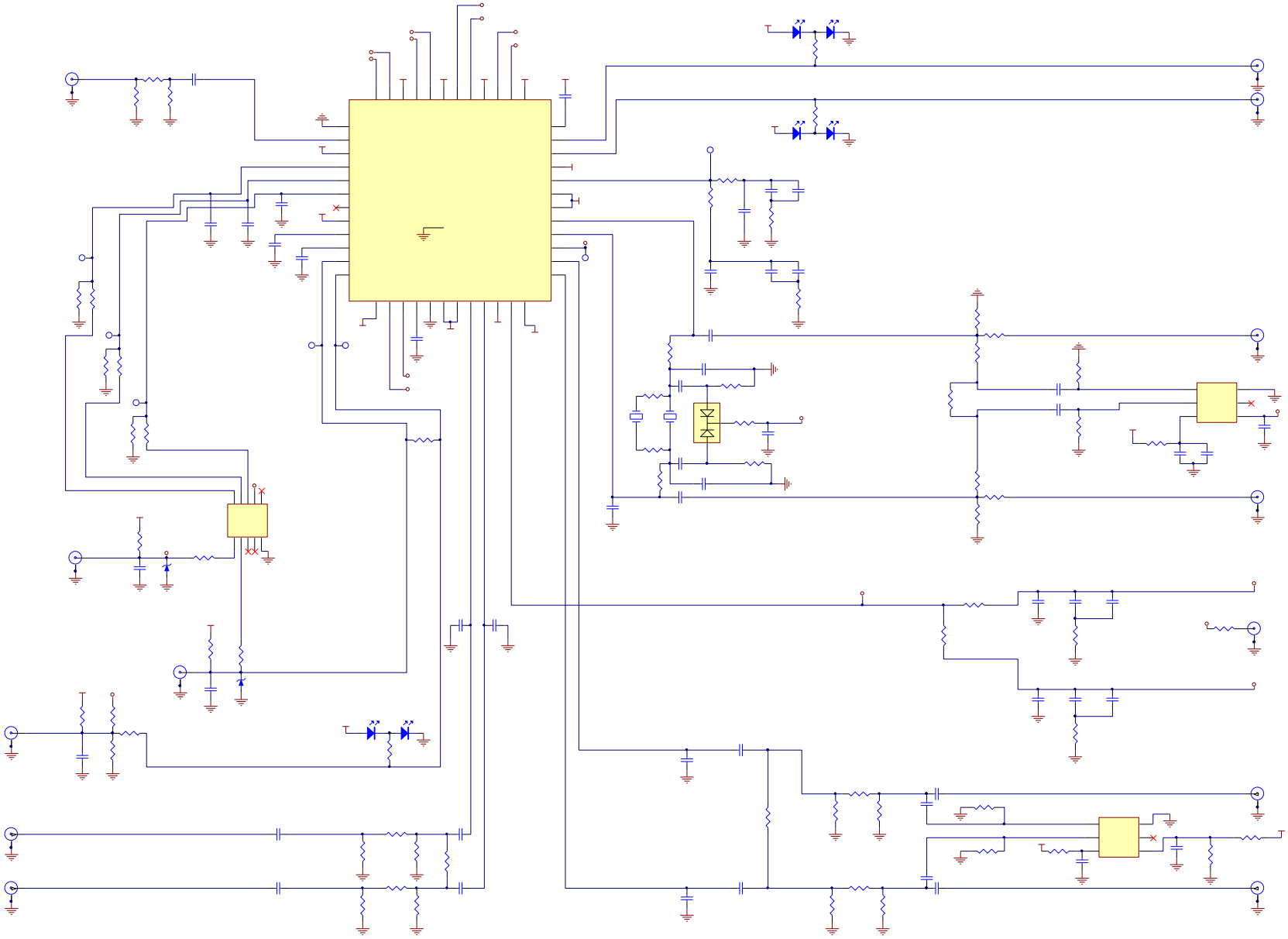
Appendix C: Schematics

Power



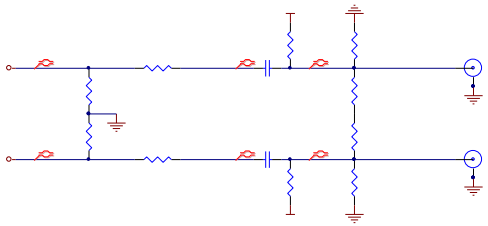
LMK04100BEVAL schematic.
Refer to BOM for differences.

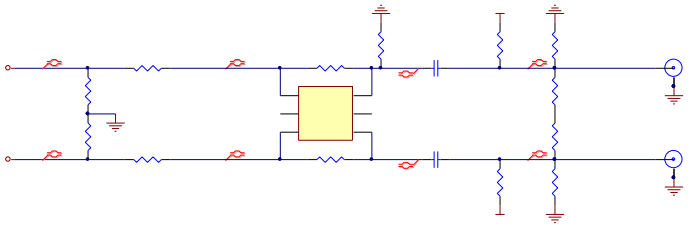
Main

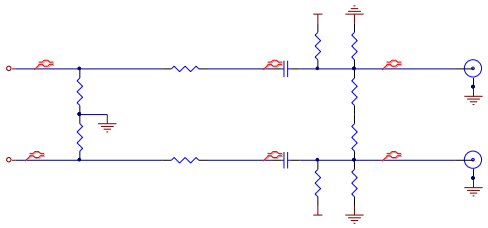


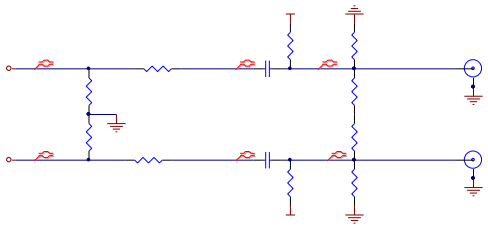
LMK04100BEVAL schematic.
Refer to BOM for differences.

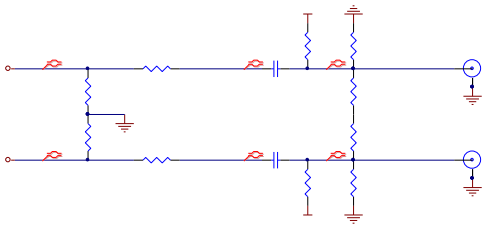
Clock Outputs











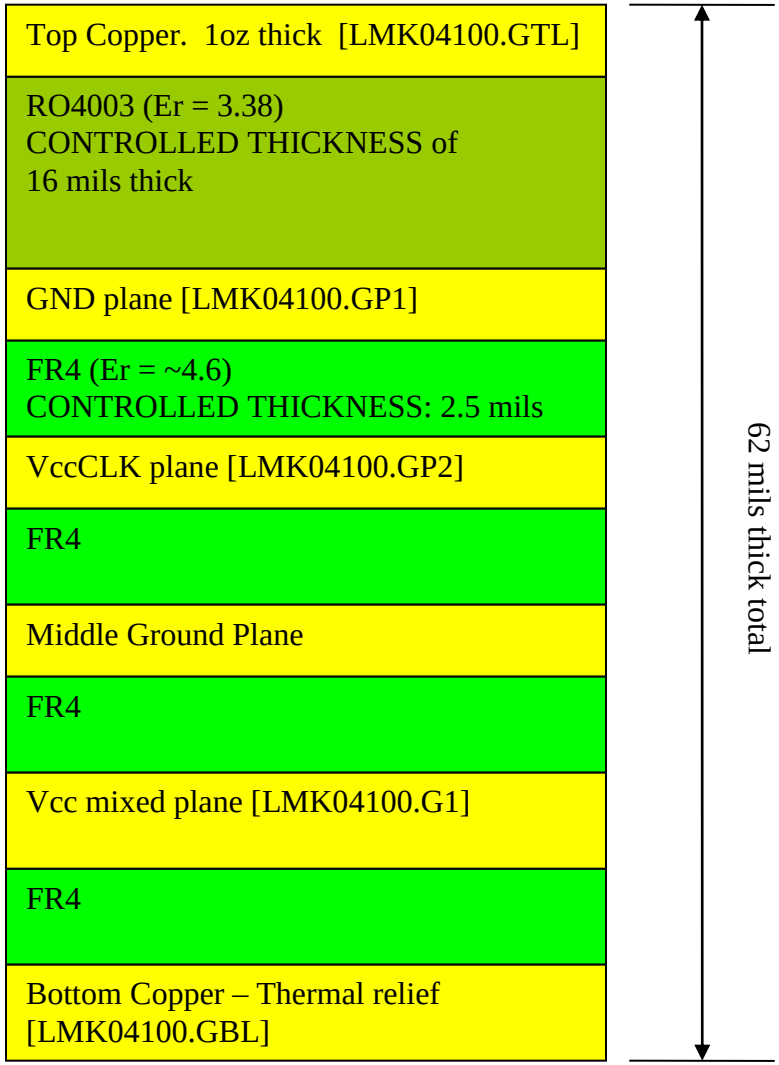
Appendix D: Board Layers Stackup

Layers of the 6 layer evaluation board include:
Blue is dielectrics

- Top layer for high priority high frequency signals
  - 1 oz CU
- RO4003 Dielectric, 16 mils
- Ground plane
- FR4, 2.5 mils thick.
- Power plane #1 – VccCLK
- FR4, xx mils
- middle ground plane
- FR4, xx mils
- VccPLL, VccAux
- FR4, xx mils
- Bottom layer copper clad for thermal relief

Top to bottom layer order:

LMK04100.GTL	(1) top copper
LMK04100.GP1	(2) gnd
LMK04100.GP2	(3) vcc
LMK04100.GP3	(4) gnd
LMK04100.G1	(5) vcc
LMK04100.GBL	(6) bottom copper



Appendix E: Bill of Materials

Common Bill of Materials for Evaluation Boards (page 1/3)

Part	Manufacturer	Part Number	Qnt	Identifier
Capacitors				
2.0 pF	Kemet	C0603C209C5GAC	2	C33, C41
33 pF	Kemet	C0402C330J5GAC	3	C26, C27, C28
100 pF	Kemet	C0603C101J5GAC	2	C24, C38
1 nF	Kemet	C0603C102J5GAC	1	C37
2.2 nF	Kemet	C0603C222K5RAC	2	C35, C40
6.8 nF	Kemet	C0603C682K1RACTU	1	C2_B2
10 nF	Kemet	C0603C103K1RACTU	4	C6, C9, C16, C20
12 nF	Panasonic	ECH-U01123JX5	1	C2_A2
0.1 uF	Kemet	C0603C104J3RAC	25	C3, C5, C8, C10, C13, C15, C17, C19, C23, C30, C34, C36, C45, C48, C59, C60, C63, C65, C66, C67, C68, C69, C70, C71, C72
100 nF	Kemet	C0603C104J3RAC	1	C1_A1
330 nF	Kemet	C0603C334K4RACTU	1	C1_B1
0.47 uF	Kemet	C0603C474K8PACTU	1	C32
680 nF	Kemet	C0603C684K8PAC	1	C2_A1
1 uF	Kemet	C0603C105K8PAC	10	C2, C4, C7, C12, C14, C18, C22, C25, C39, C47
10 uF	Kemet	C0805C106K9PAC	5	C1, C2pB1, C11, C21, C29

Common Bill of Materials for Evaluation Boards (continued, 2/3)

Resistors				
0 ohm	Vishay/Dale	CRCW06030000Z0EA	23	C51, C58, C62, R1, R2, R3, R26, R32, R44, R47, R60, R65, R68, R71, R73, R82, R85, R91, R96, R103, R104, R113, R114
18 ohm	Vishay/Dale	CRCW060318R0JNEA	1	R5
51 ohm	Vishay/Dale	CRCW060351R0JNEA	2	R13, R62
100 ohm	Vishay/Dale	CRCW0603100RJNEA	2	R16, R51
120 ohm	Vishay/Dale	CRCW0603120RJNEA	2	R107, R111
180 ohm	Vishay/Dale	CRCW0603180RJNEA	2	R36, R41
270 ohm	Vishay/Dale	CRCW0603270RJNEA	5	R4, R6, R7, R8, R45
1.8 k	Vishay/Dale	CRCW06031K80JNEA	1	R2_A2
2.2 k	Vishay/Dale	CRCW06032K20JNEA	2	R35, R40
2.7 k	Vishay/Dale	CRCW06032K70JNEA	1	R2_B2
3.9 k	Vishay/Dale	CRCW06033K90JNEA	1	R2_B1
4.7 k	Vishay/Dale	CRCW06034K70JNEA	2	R20, R30
10 k	Vishay/Dale	CRCW060310K0JNEA	1	R23
15 k	Vishay/Dale	CRCW060315K0JNEA	3	R12, R19, R29
27 k	Vishay/Dale	CRCW060327K0JNEA	3	R11, R18, R28
39 k	Vishay/Dale	CRCW060339K0JNEA	1	R2_A1
Other				
POWER_SMALL	Weidmuller	1594540000	1	J1
SMA	Johnson Components	142-0701-851	14	CLKin0*, CLKin1, CLKin1*, CLKout0*, CLKout0, CLKout1*, CLKout1, CLKout2*, CLKout2, CLKout3*, CLKout3, CLKout4*, Fout, Vcc
SMA_FRAME	Printed Circuits Corp.	PCB	1	F1
Red LED	Lumex	SML-LX2832IC-TR	2	D3, D5
Green LED	Lumex	SML-LX2832GC-TR	1	D1
0.875" Standoff	SPC Technology	SPCS-14	4	S1, S2, S3, S4
ADT2-1T	Minicircuits	ADT2-1T+	1	B1
HEADER_2X5(POLARIZED)	FCI Electronics	52601-S10-8	1	uWire
3.3 V zener	Comchip	CZRU52C3V3	2	D7, D8
SMV-1249-074	Skyworks	SMV1249-074LF	1	D9

Common Bill of Materials for Evaluation Boards (continued, 3/3)

Open				
Open	R		78	R14, R17, R21, R22, R24, R25, R27, R33, R34, R38, R42, R43, R46, R48, R49, R50, R52, R53, R54, R55, R56, R57, R58, R59, R61, R63, R64, R66, R67, R69, R70, R72, R75, R77, R78, R79, R83, R84, R86, R87, R88, R89, R90, R93, R94, R97, R98, R99, R100, R101, R102, R105, R106, R108, R109, R110, R112, R115, R116, R117, R118, R200, R201, R202, R203, R204, R205, R206, R207, R208, R209, R210, R211, R212, R213, R214, R215, R216
Open	C		44	C1_A2, C1_B2, C2pB2, C2pA2, C2pA1, C2_B1, C3_AB1, C43, C44, C46, C49, C50, C52, C53, C54, C55, C56, C57, C61, C64, C200, C201, C202, C203, C204, C205, C206, C207, C208, C209, C210, C211, C212, C213, C214, C215, C216, C217, C218, C219, C220, C221, C222, C223
Open	U		4	U3, U200, U201, U202
Open	SMA		12	OSCin*, OSCin, LOS0, LOS1, VccLDO, LD, PTO, GOE, SYNC*, CLKout4, Vtune1, CLKin0
Open	Y		1	Y200
Open	D		3	D2, D4, D6

Bill of Material Custom to LMK04100BEVAL

Part	Manufacturer	Part Number	Qnt	Identifier
Capacitors				
0.1 uF	Kemet	C0603C104J3RAC	2	C31, C42
Resistors				
0 ohm	Vishay/Dale	CRCW06030000Z0EA	2	R9, R39
120 ohm	Vishay/Dale	CRCW0603120RJNEA	4	R74, R76, R80, R81
Other				
LMK04100B	National Semiconductor	LMK04100B	1	U1
CVHD-950-122.88	Crystek	CVHD-950-122.88	1	U4
Open				
Open			6	R10, R15, R31, R37, R92, R95
Open			1	Y1

Bill of Material Custom to LMK04100BEVAL-XO

Part	Manufacturer	Part Number	Qnt	Identifier
Capacitors				
Resistors				
0 ohm	Vishay/Dale	CRCW06030000Z0EA	4	R10, R15, R31, R37
120 ohm	Vishay/Dale	CRCW0603120RJNEA	4	R74, R76, R80, R81
Other				
LMK04100B	National Semiconductor	LMK04100B	1	U1
12.288 MHz XTAL	Vectron	VXB1-1127-12M288	1	Y1
Open				
Open			2	C31, C42
Open			4	R9, R39, R92, R95
Open			1	U4

Bill of Material Custom to LMK04131BEVAL

Part	Manufacturer	Part Number	Qnt	Identifier
Capacitors				
0.1 uF	Kemet	C0603C104J3RAC	2	C31, C43
Resistors				
0 ohm	Vishay/Dale	CRCW06030000Z0EA	2	R9, R39
120 ohm	Vishay/Dale	CRCW0603120RJNEA	2	R92, R95
Other				
LMK04131B	National Semiconductor	LMK04131B	1	U1
CVHD-950-122.88	Crystek	CVHD-950-122.88	1	U4
Open				
Open			8	R10, R15, R31, R37, R74, R76, R80, R81
Open			1	Y1

Bill of Material Custom to LMK04131BEVAL-XO

Part	Manufacturer	Part Number	Qnt	Identifier
Capacitors				
Resistors				
0 ohm	Vishay/Dale	CRCW06030000Z0EA	4	R10, R15, R31, R37
120 ohm	Vishay/Dale	CRCW0603120RJNEA	2	R92, R95
Other				
LMK04131B	National Semiconductor	LMK04131B	1	U1
12.288 MHz XTAL	Vectron	VXB1-1127-12M288	1	Y1
Open				
Open			2	C31, C42
Open			6	R9, R39, R74, R76, R80, R81
Open			1	U4

Bill of Material Custom to LMK04102BEVAL

Part	Manufacturer	Part Number	Qnt	Identifier
Capacitors				
0.1 uF	Kemet	C0603C104J3RAC	2	C31, C42
Resistors				
0 ohm	Vishay/Dale	CRCW06030000Z0EA	2	R9, R39
120 ohm	Vishay/Dale	CRCW0603120RJNEA	4	R74, R76, R80, R81
Other				
LMK04102B	National Semiconductor	LMK04102B	1	U1
CVHD-950-122.88	Crystek	CVHD-950-122.88	1	U4
Open				
Open			6	R10, R15, R31, R37, R92, R95
Open			1	Y1

Bill of Material Custom to LMK04133BEVAL

Part	Manufacturer	Part Number	Qnt	Identifier
Capacitors				
0.1 uF	Kemet	C0603C104J3RAC	2	C31, C42
Resistors				
0 ohm	Vishay/Dale	CRCW06030000Z0EA	2	R9, R39
120 ohm	Vishay/Dale	CRCW0603120RJNEA	2	R92, R95
Other				
LMK04133B	National Semiconductor	LMK04133B	1	U1
CVHD-950-122.88	Crystek	CVHD-950-122.88	1	U4
Open				
Open			8	R10, R15, R31, R37, R74, R76, R80, R81
Open			1	Y1

Appendix F: Balun Information

Typical Balun Frequency Response

The following figure illustrates the typical frequency response of the Mini-circuit's ADT2-1T balun.

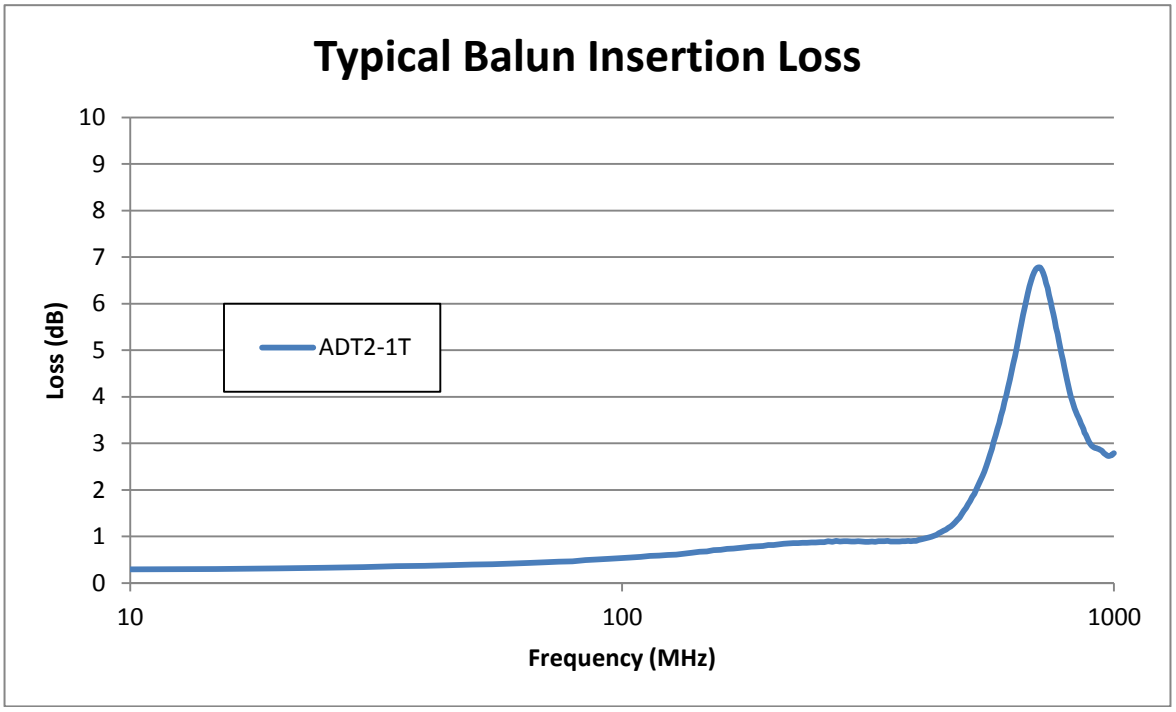


Figure 11 - Typical Balun Frequency Response

Appendix G: VCXO/Crystal changes

This appendix contains instructions for changing the active on-board oscillator for PLL1.

Changing from Crystal Resonator to VCXO

If the board has been setup to use the crystal-based oscillator with PLL1, the crystal may be disabled and the VCXO enabled as described on the following pages:

Summary

1. Connect power to VCXO
2. Disconnect Crystal RF path and connect VCXO RF path
3. Connect charge pump output from PLL1 to VCXO Loop Filter (A1) and VCXO.
4. Connect charge pump output from PLL2 to VCXO Loop filter (A2).

Procedures

1. Connect power to VCXO
    a. Install a 0 ohm resistor in R26 (near the VCXO)

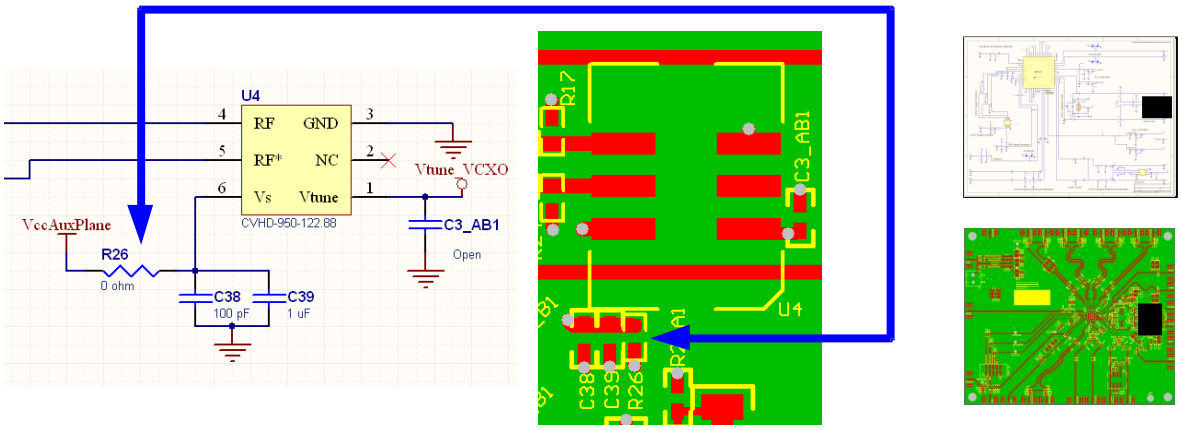


Figure 12

2. Disconnect Crystal RF path and connect VCXO RF path
    a. Remove resistors R15 and R31.
    b. Install 0.1 uF capacitors in C31 and C43.

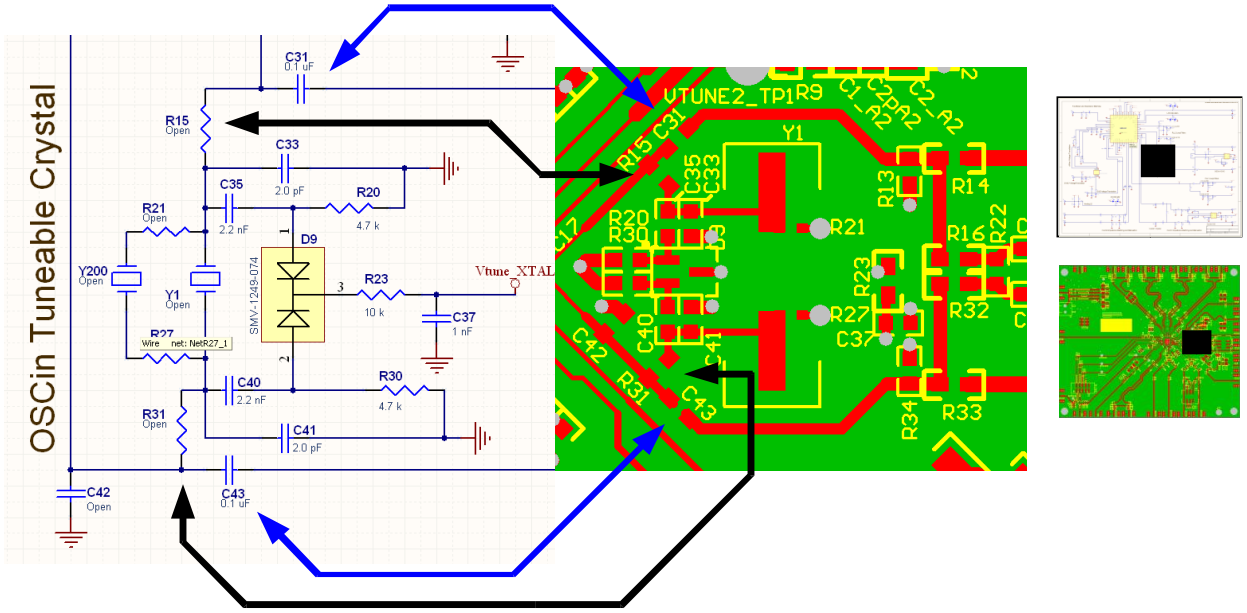


Figure 13

3. Connect charge pump output from PLL1 to VCXO Loop Filter (A1) and VCXO.
    a. Remove R37 and install a 0 ohm resistor in R39. This resistor can be "switched" between the two footprints.

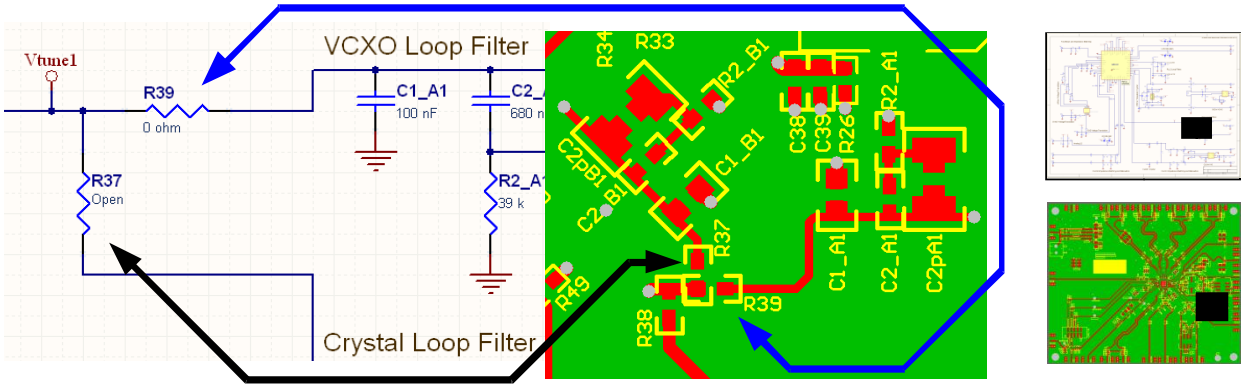


Figure 14

4. Connect charge pump output from PLL2 to VCXO Loop filter (A2).
    a. Remove R10 and install a 0 ohm resistor in R9. This resistor can be "switched" between the two footprints.

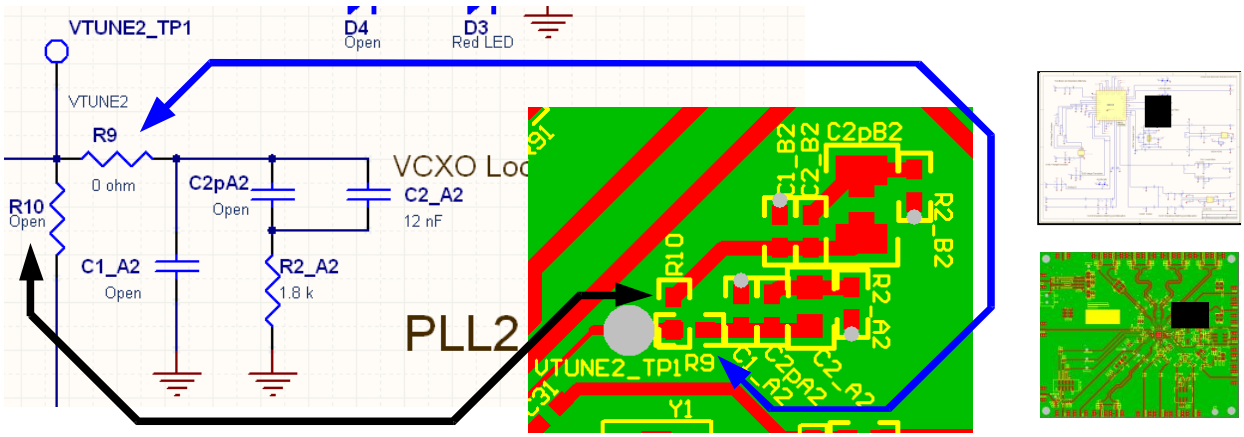


Figure 15

Changing from VCXO to Crystal Resonator

If the board has been setup to use the VCXO for PLL1, the VCXO may be disabled and the crystal enabled as described on the following pages:

Summary

1. Remove power from VCXO
2. Disconnect VCXO RF path and connect Crystal RF path
3. Connect charge pump output from PLL1 to Crystal Loop Filter (B1) and Crystal
4. Connect charge pump output from PLL2 to Crystal Loop filter (B2)

Procedures

1. Remove power from VCXO
    a. Remove 0 ohm resistor in R26 (near the VCXO)

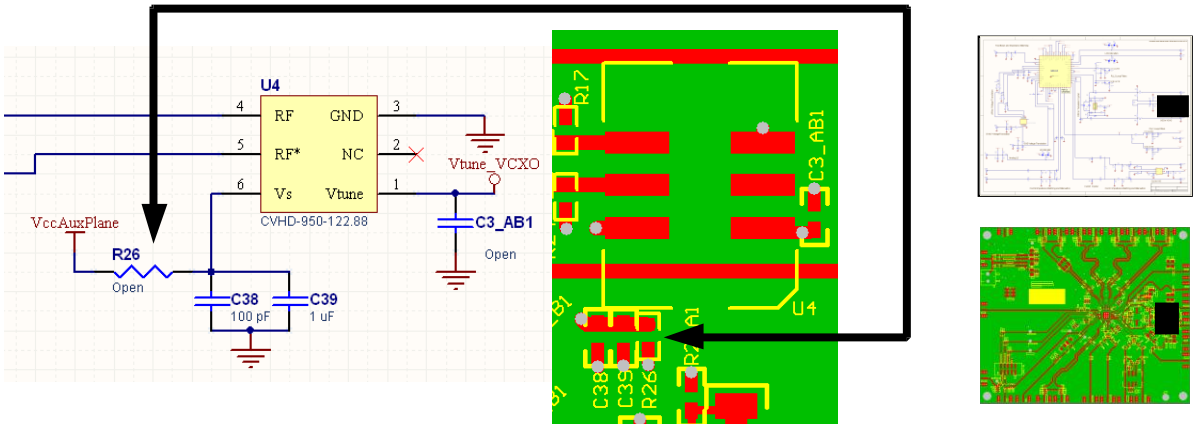


Figure 16

2. Disconnect VCXO RF path and connect Crystal RF path
    a. Install 0 ohm resistors R15 and R31.
    b. Remove 0.1 uF capacitors in C31 and C43.

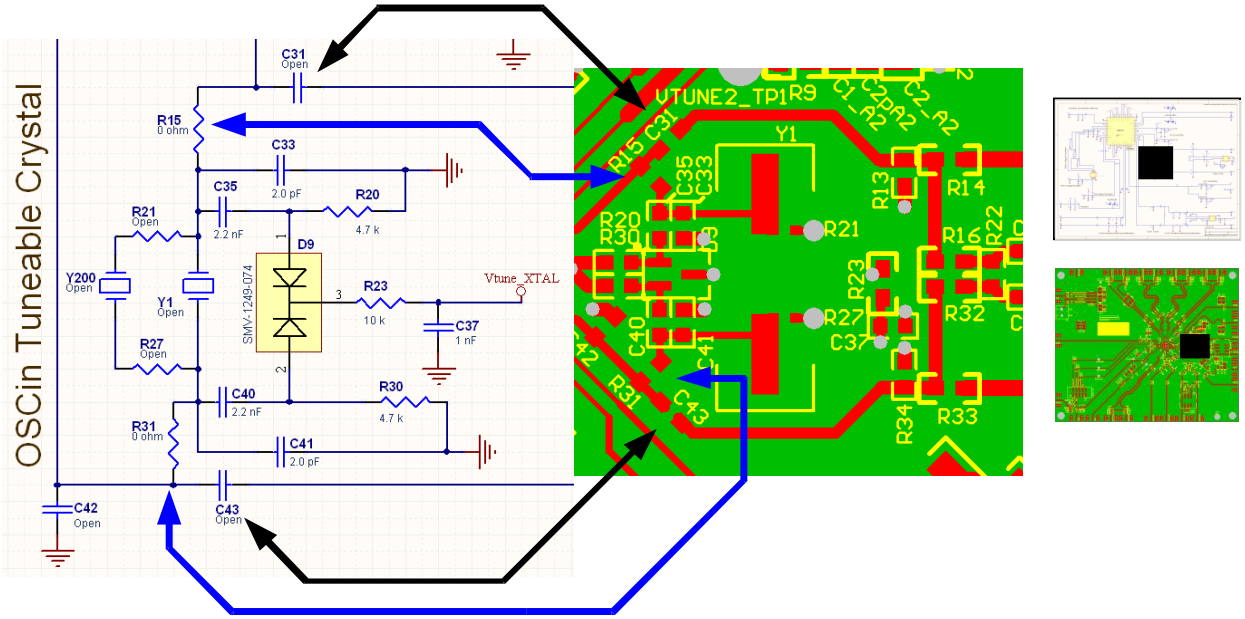


Figure 17

3. Connect charge pump output from PLL1 to Crystal Loop Filter (B1) and Crystal
    a. Remove R39 and install a 0 ohm resistor in R37. This resistor can be "switched" between the two footprints.

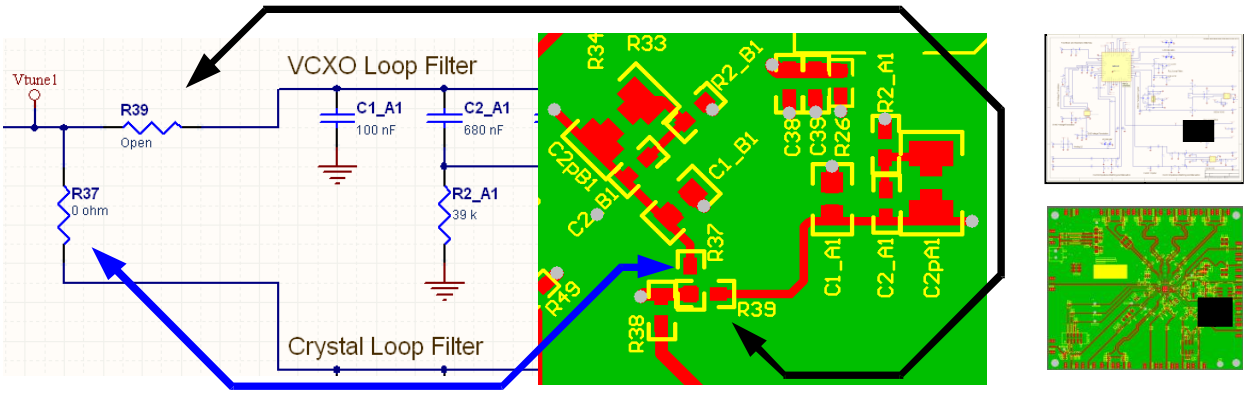


Figure 18

4. Connect charge pump output from PLL2 to Crystal Loop filter (B2)
    a. Remove R9 and install a 0 ohm resistor in R10. This resistor can be "switched" between the two footprints.

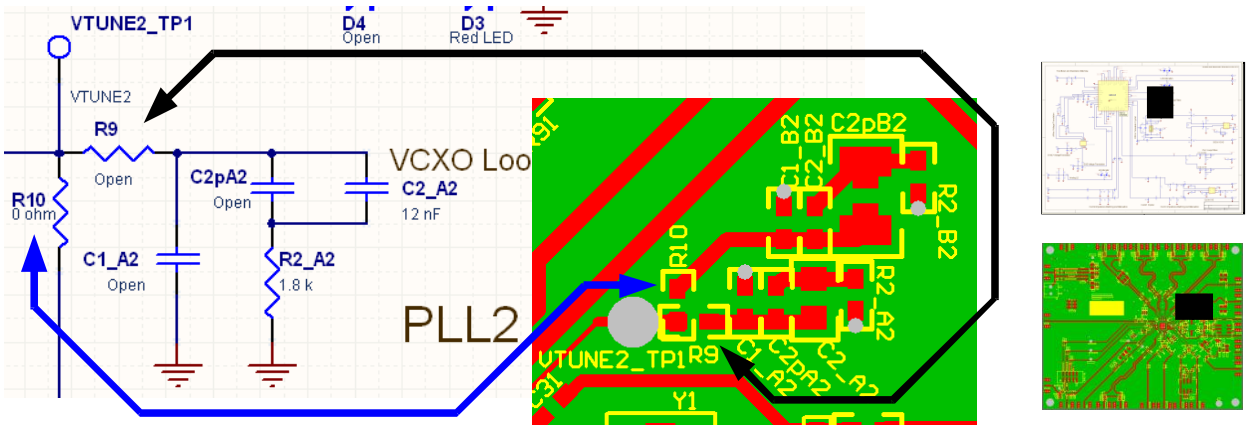


Figure 19

Appendix H: LMK04100

The block diagram in Figure 20 illustrates the functional architecture of the LMK041xx clock conditioner. It features a cascaded, dual PLL arrangement, available internal loop filter components for PLL2, internal VCO with PLL2 for frequency synthesis, and clock distribution section with individual clock output dividers and delay adjustment blocks. The dual reference clock input to PLL1 provides fail-safe redundancy for phase locked loop operation. The cascaded PLL architecture allows PLL1 to be used as a jitter cleaner for an incoming reference clock that contains excessive phase noise. This requires the user to select an external oscillator (VCXO or crystal) that provides the desired phase noise performance at the clock output. This external oscillator becomes the reference clock for PLL2 and along with the phase noise characteristics of PLL2 and the internal VCO, determines the final phase noise performance at FOUT and the output of the clock distribution section.

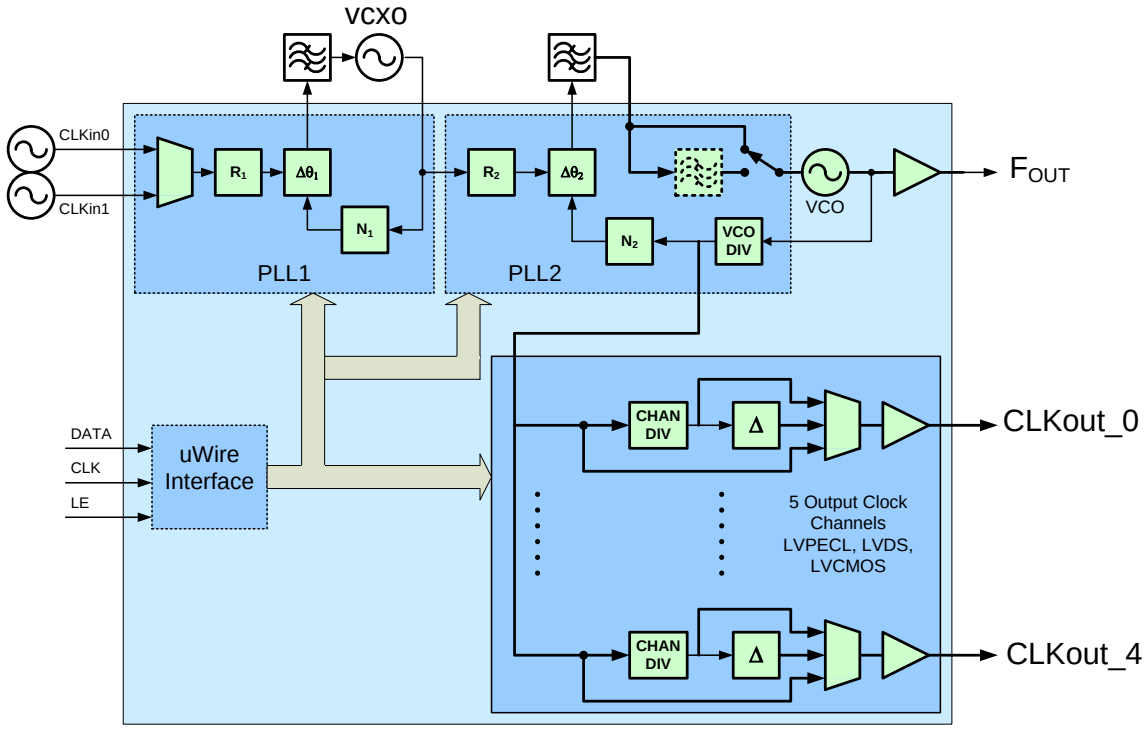


Figure 20 - Functional Block Diagram of the LMK041xx Dual PLL Precision Clock Conditioner with External VCXO module.

PLL1 has been designed to work with either an off-the-shelf VCXO package or with a user-designed discrete implementation that employs a crystal resonator and associated tuning components. The Figure 21 shows an example of a discretely implemented VCXO using a crystal resonator.

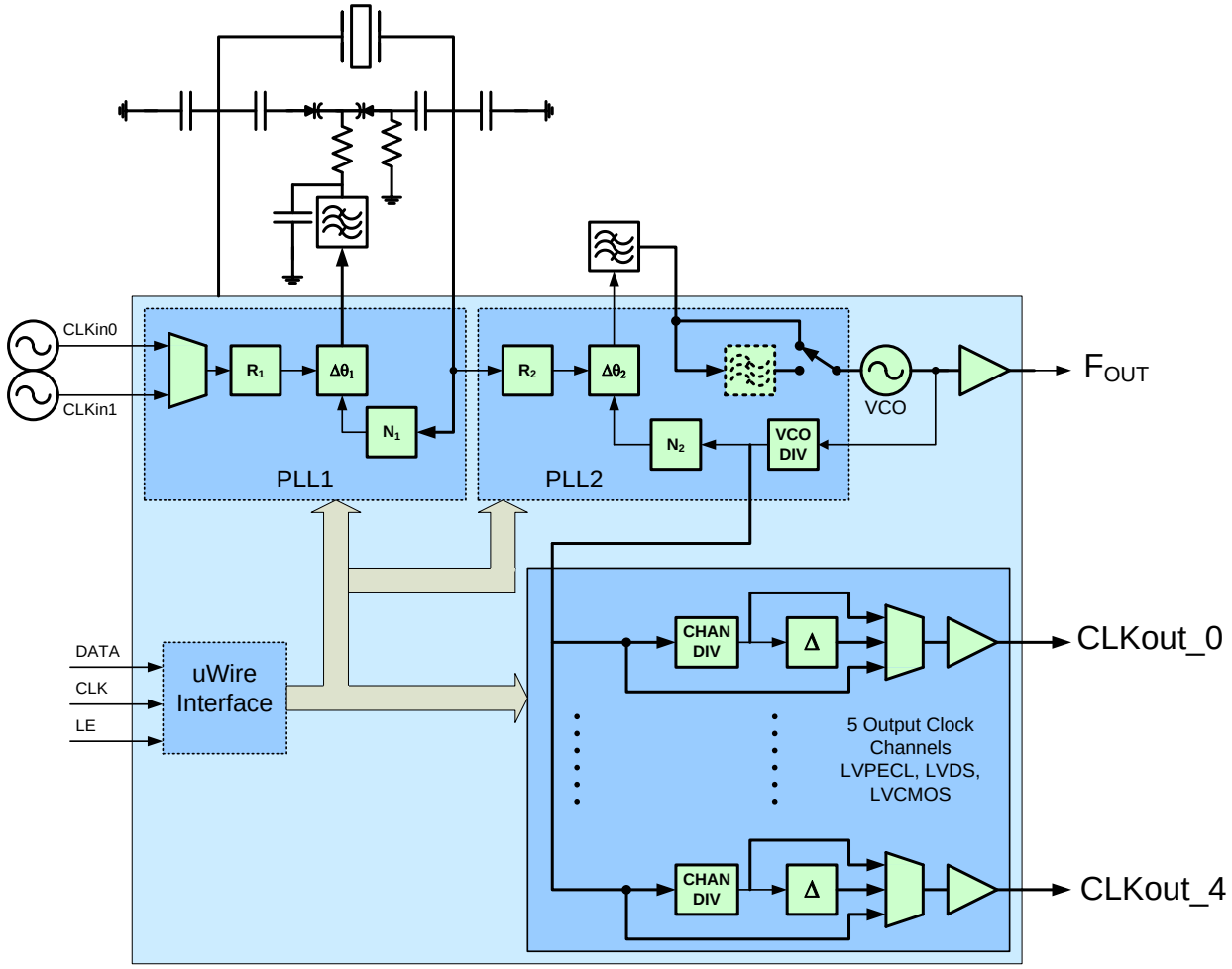


Figure 21 - LMK041xx with the XTAL Resonator option and Tuning Circuit

LMK04100 Family evaluation boards are configured with either a VCXO or Crystal (-XO) on board. It is possible to place a VCXO on a Crystal board or a Crystal on a VCXO board by removing and replacing certain components on the board. Instructions for modifying the board are presented in Appendix G: VCXO/Crystal changes.

Figure 22 below shows the crystal oscillator circuit diagram.

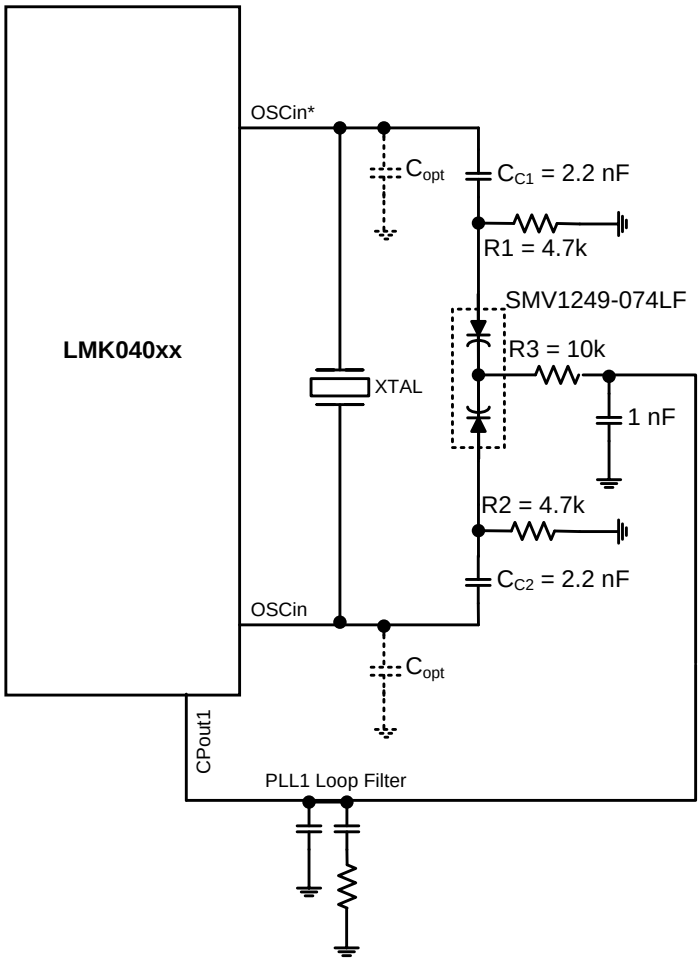


Figure 22 - Crystal Oscillator Circuit diagram

Appendix I: Properly Configuring LPT Port

When trying to solve any communications issue, it is convenient to program the POWERDOWN bit to confirm high/low current draw of the evaluation board or the PLL_MUX between "Logic Low" and "Logic High" LD output to confirm successful communications.

LPT Driver Loading

The parallel port must be configured for proper operation. To confirm that the LPT port driver is successfully loading click "LPT/USB" → "Check LPT Port." If the driver properly loads then the following message is displayed:

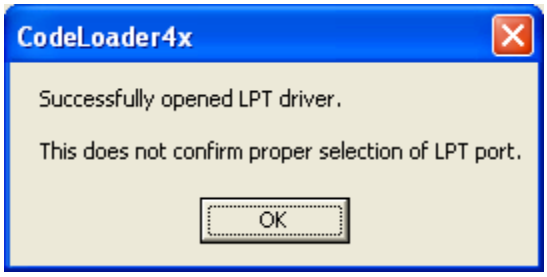


Figure 23 - Successfully Opened LPT Driver

Successful loading of LPT driver does not mean LPT communications in CodeLoader are setup properly. The proper LPT port must be selected and the LPT port must not be in an improper mode.

The PC must be rebooted after install for LPT support to work properly.

Correct LPT Port/Address

To determine the correct LPT port in Windows, open the device manager (On Windows XP, Start → Settings → Control Panel → System → Hardware Tab → Device Manager) and check the LPT port under the Ports (COM & LPT) node of the tree. It can be helpful to confirm that the LPT port is mapped to the expected port address, for instance to confirm that LPT1 is really mapped to address 0x378. This can be checked by viewing the properties of the LPT1 port and viewing resources tab to verify that the I/O Range starts at 0x378. CodeLoader expects the a traditional port mapping:

Port	Address
LPT1	0x378
LPT2	0x278
LPT3	0x3BC

If a non-standard address is used, use the "Other" port address in CodeLoader and type in the port address in hexadecimal. It is possible to change the port address in the computer's BIOS settings. The port address is set in CodeLoader at the Port Setup tab as shown in Figure 24.

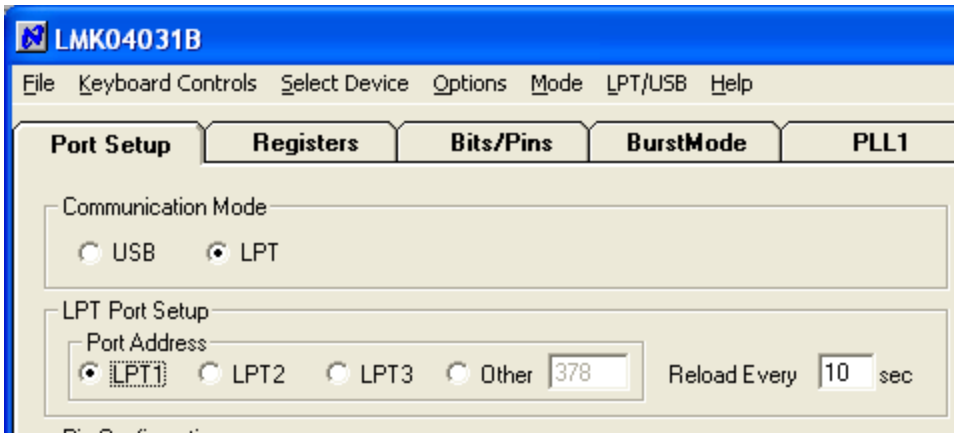


Figure 24 - Selecting the LPT Port

Correct LPT Mode

If communications are not working, then it is possible the LPT port mode is set improperly. It is recommended to use the simple, Output-only mode of the LPT port. This can be set in the BIOS of the computer. Common terms for this desired parallel port mode are "Normal," "Output," or "AT." It is possible to enter BIOS setup during the initial boot up sequence of the computer.

Appendix J: Troubleshooting Information

If the evaluation board is not behaving as expected, the most likely issues are…

1) Board communication issue
2) Incorrect Programming of the device
3) Setup Error

Refer to this checklist for a practical guide on identifying/exposing possible issues.

1) Confirm Communications

Refer to Appendix I: Properly Configuring LPT Port to trouble shoot this item.

Remember to load device with Ctrl-L!

2) Confirm PLL1 operation/locking

1) Program PLL_MUX = "PLL 1 R Divider /2"
2) Confirm that LD pin output is half the expected phase detector frequency of PLL1.
    i. If not, examine CLKin_SEL programming.
    ii. If not, examine CLKin0_BUFTYPE / CLKin1_BUFTYPE.
    iii. If not, examine PLL1 register R programming.
    iv. If not, examine physical CLKin input.

3) Program PLL_MUX = "PLL 1 N Divider /2"
4) Confirm that LD pin output is half the expected phase detector frequency of PLL1.
    i. If not, examine PLL1 register N programming.
    ii. If not, examine physical OSCin input.

Naturally, the output frequency of the above two items, PLL 1 R Divider/2 and PLL 1 N Divider /2, on LD pin should be the same frequency.

5) Program PLL_MUX = "PLL1 DLD Active High"
6) Confirm the LD pin output is high.
    i. If high, then PLL1 is locked, continue to PLL2 operation/locking.

(continued on next page)

7) If LD pin output is low, but the frequencies are the same, it is possible that excessive leakage on Vtune pin is causing the digital lock detect to not activate. By default PLL2 waits for the digital lock detect to go high before allowing PLL2 and the integrated VCO to lock. Different VCXO models have different input leakage specifications. High leakage, low PLL1 phase detector frequencies, and low PLL1 charge pump current settings can cause the PLL1 charge pump to operate longer than the digital lock detect timeout which allows the device to lock, but prevents the digital lock detect from activating.
    i. Redesign PLL1 loop filter with higher phase detector frequency
    ii. Redesign PLL1 loop filter with higher charge pump current
    iii. Isolate VCXO tuning input from PLL1 charge pump with an op amp.
    iv. Program RC_DLD1_Start = 0, this will allow PLL2 to starting lock even if the digital lock detect on PLL1 is not high.

3) Confirm PLL2 operation/locking

1) Program PLL_MUX = “PLL 2 R Divider /2”
2) Confirm that LD pin output is half the expected phase detector frequency of PLL2.
    i. If not, examine PLL2 register R programming.
    ii. If not, examine physical OSCin input.

3) Program PLL_MUX = “PLL 2 N Divider /2”
4) Confirm that LD pin output is half the expected phase detector frequency of PLL2.
    i. If not, confirm OSCin_FREQ is programmed to OSCin frequency.
    ii. If not, examine PLL2 register N programming.

Naturally, the output frequency of the above two items should be the same frequency.

5) Program PLL_MUX = “PLL2 DLD Active High”
6) Confirm the LD pin output is high.

7) Program PLL_MUX = “PLL1/2 DLD Active High”
8) Confirm the LD pin output is high.

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