SY89537L

3.3V Precision LVPECL and LVDS Programmable Multiple Output Bank Clock Synthesizer and Fanout Buffer

General Description

The SY89537L integrated programmable clock synthesizer and fanout is part of a precision PLL-based clock generation family optimized for enterprise switch, router, and multiprocessor server applications. This family is ideal for generating internal system timing requirements up to 700MHz for multiple ASICs, FPGAs, and NPUs. These devices integrate the following blocks into a single monolithic IC:

- PLL (Phase-Lock-Loop) based synthesizer
- Fanout buffers
- Clock generator (dividers)
- Logic translation (LVPECL, LVDS)
- Five independently programmable output banks

This level of integration minimizes additive jitter and part-to-part skew associated with discrete alternatives, resulting in superior system-level timing with reduced board space and power. For applications that require a zero-delay function, see the SY89538L.

All support documentation can be found on Micrel's web site at: www.micrel.com.

Applications

- Enterprise routers, switches, servers and workstations
- Parallel processor-based systems
- Internal system clock generation for ASICs, NPUs, FPGAs

Markets

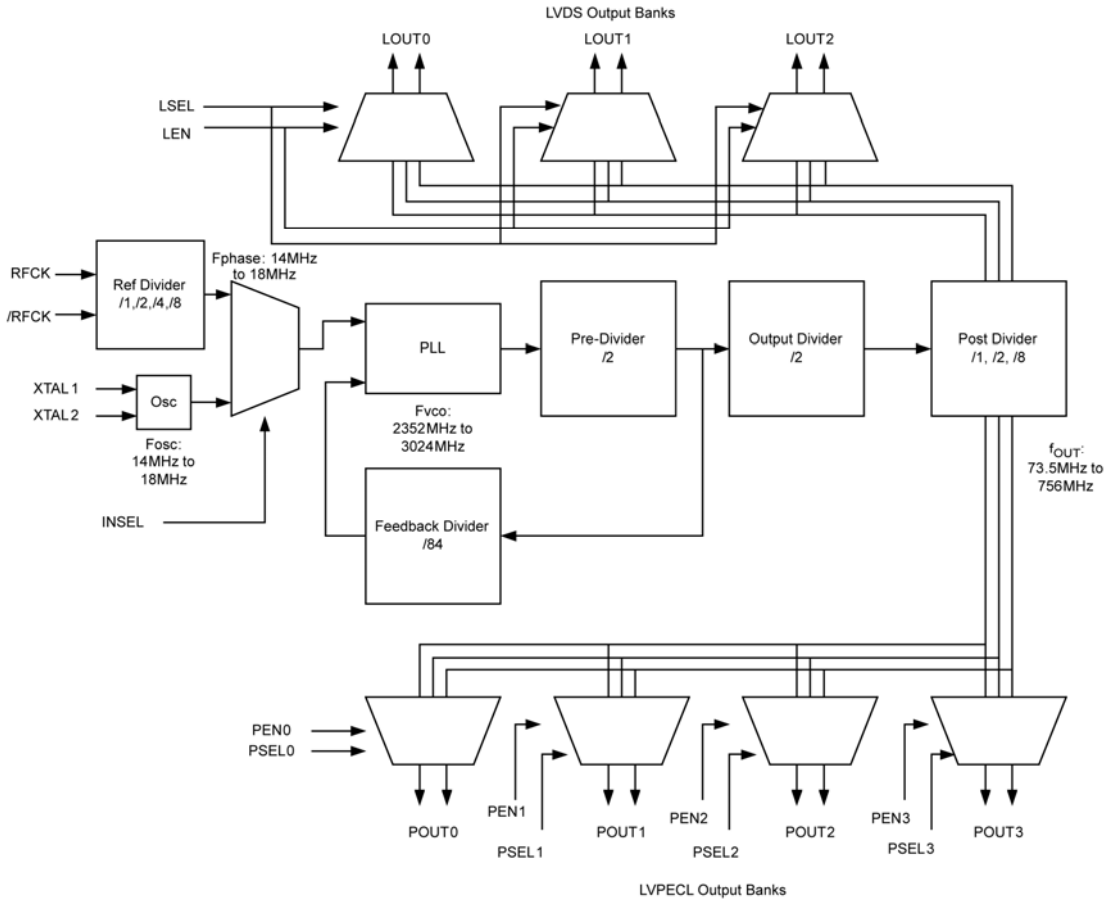
- LAN/WAN
- Enterprise servers
- Test and measurement

Precision Edge®

Features

- Integrated programmable synthesizer with multiple output dividers, fanout buffers, and clock drivers
- Direct interface to crystal: 14MHz to 18MHz
- Input MUX accepts a reference and a crystal (XTAL) source
  - Ideal for reference backup clock source or system test frequency source
  - Patent-pending unique input MUX isolates XTAL and reference inputs minimizes crosstalk
- Guaranteed AC performance:
  - 87.15MHz to 700MHz output frequency range (with RFCK at 16.6MHz)
  - <100ps$_{PP}$ total jitter
  - <7ps$_{RMS}$ cycle-to-cycle jitter
  - <8ps$_{PP}$ deterministic jitter
  - <0.7ps$_{RMS}$ crosstalk induced jitter
  - <50ps bank-to-bank skew
- Output bank synchronization control pin
- LVPECL and LVDS outputs
- TTL/CMOS compatible control logic
- Five independently programmable output frequency banks:
  - Four differential LVPECL output banks
  - One differential LVDS output bank with 3 output pairs
- Separate output enable for each bank
- 3.3V ±10% power supply (2.5V output capable)
- Guaranteed over the commercial and industrial temperature range (-40C to +85C)
- Available in 44-pin (7mm x 7mm) QFN package

Functional Block Diagram



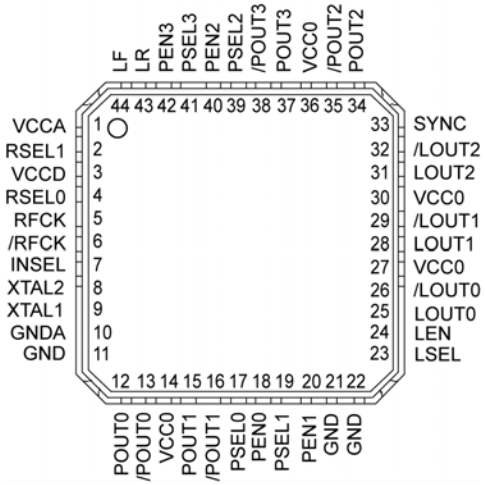
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89537LMY	QFN-44	Industrial	SY89537LMY with Pb-Free bar-line indicator	Matte-Sn Pb-Free
SY89537LMYTR[2]	QFN-44	Industrial	SY89537LMY with Pb-Free bar-line indicator	Matte-Sn Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.

Pin Configuration



44-Pin QFN

Pin Description

Power

Pin Number	Pin Name	Pin Function
1	VCCA	Analog PLL Power Pin: Connects to "quiet" 3.3V supply. 3.3V power pins are not internally connected on the die, and must be connected together on the PCB. Bypass with 0.1µF//0.01µF low ESR capacitors and place as close to the VCCA pin as possible.
3	VCCD	Digital Logic Core Power Pin: VCCD connects to a 3.3V supply. Power pins are not internally connected on the die, and must be connected together on the PCB. Bypass with 0.1µF//0.01µF low ESR capacitors and place bypass capacitors as close to the VCCD pin as possible.
14, 27, 30, 36	VCCO	LVDS and LVPECL Output Driver Power Pins: The outputs can be powered from a 2.5V supply or 3.3V supply. Connect all VCCO pins to the same power supply: 3.3V ±10% or 2.5V ±5%. Power pins are not internally connected on the die, and must be connected together on the PCB. Bypass with 0.1µF//0.01µF low ESR capacitor and place as close to the VCCO pin as possible.
10	GNDA	PLL Ground: Connect to "quiet" ground. GNDA and GND are not internally connected on the die, and must be connected on the PCB.
11, 21, 22	GND, Exposed Pad	Ground: GND pins and exposed pad must both be connected to the most negative potential of the chip ground.

Control and Configuration

Pin Number	Pin Name	Pin Function
43	LR	Analog Input/Output: Provides the reference voltage for the PLL loop filter and is used with the LF pin. See "External Loop Filter Considerations" for recommended loop filter values.
44	LF	Analog Input/Output: Provides the loop filter node for the PLL. See "External Loop Filter Considerations" for loop filter values.
2, 4	RSEL1, RSEL0	TTL/CMOS Reference Input Pre-scaler. The two-bit input pre-scaler divides the input reference frequency by /1, /2, /4, or /8. RSEL0 is the LSB bit. See "Reference Input Divider Select Table," for proper decoding. The threshold voltage $V_{TH} = V_{CC}/2$. Internal 25kΩ pull-up.
7	INSEL	TTL/CMOS Input Select Control. Selects either XTAL or Reference (RFCK) input. Internal 25kΩ pull-up. The default is logic HIGH, and selects the XTAL input. The threshold voltage $V_{TH} = V_{CC}/2$. Logic HIGH: XTAL Select Logic LOW: Reference Input Select
23	LSEL	TTL/CMOS input select control signal for the LVDS LOUT0-LOUT2 outputs. LSEL and LEN are used to decode the selection and the post divider of the LVDS output bank. LSEL includes an internal 25kΩ pull-up. See "LVDS Output and Frequency Select Table" for proper decoding. The threshold voltage $V_{TH} = V_{CC}/2$.
24	LEN	TTL/CMOS Input Enable Pin. Used to control the LOUT0-LOUT2 outputs and acts as a frequency select pin. LEN and LSEL are used to decode the selection and the post divider of the LVDS output bank. See the "LVDS Output and Frequency Select Table" for proper decoding. LEN includes an internal 25kΩ pull-up. When disabled, LOUT0-LOUT2 outputs are LOW, and the complimentary outputs are HIGH. The threshold voltage $V_{TH} = V_{CC}/2$.
17 19 39 41	PSEL0 PSEL1 PSEL2 PSEL3	TTL/CMOS input select control signals for the PECL POUT0-POUT3 outputs. PSELx and PENx are used together to decode the selection and post divider of the PECL outputs. PSELx pins include an internal 25kΩ pull-up. The threshold voltage $V_{TH} = V_{CC}/2$. See "PECL Output Frequency and Select Table" for proper decoding.
18 20 40 42	PEN0 PEN1 PEN2 PEN3	TTL/CMOS input enable pin. Used to control the POUT0-PECL2 outputs and acts as a frequency select pins. PENx and PSELx are used together; see the "PECL Output and Frequency Select Table" for proper decoding. PENx includes an internal 25kΩ pull-up. When disabled, PECL0-PECL2 outputs are LOW. The threshold voltage $V_{TH} = V_{CC}/2$.
33	SYNC	TTL/CMOS output bank synchronization control. Internal 25kΩ pull-up. The default state is HIGH. After any bank has been programmed, all PECL and LVDS outputs are synchronized when the SYNC control pin is toggled with a HIGH-LOW-HIGH transition. See "Synchronization" section for details. The threshold voltage $V_{TH} = V_{CC}/2$.

Pin Description (continued)

Input/Output

Pin Number	Pin Name	Pin Function
5, 6	RFCK, /RFCK	Reference Clock Differential Input. Input accepts any input, single-ended or differential: TTL/CMOS, LVPECL, LVDS, HSTL, and SSTL. RFCK requires external termination. See "Input Interface" section for details.
8, 9	XTAL2, XTAL1	Crystal Input. Directly connect a series resonant crystal across inputs. See "Quartz Crystal Oscillator Specification" table. Place crystal as close to the input as possible, keep XTAL and traces away from adjacent noisy traces to minimize noise coupling, and place the XTAL on the same side as the SY89537L (component side).
12, 13 15, 16 34, 35 37, 38	POUT0, /POUT0 POUT1, /POUT1 POUT2, /POUT2 POUT3, /POUT3	100K LVPECL Output Drivers. Terminate all PECL outputs with 50Ω to V_{CCO}-2V. Each output pair has respective output frequency control (PSELx, PENx) pins. See "PECL Output and Frequency Select Table" for proper coding. For low jitter applications, unused PECL output pairs should be terminated with pull-down resistors. See "Output Termination Recommendations" section for termination detail.
25, 26 28, 29 31, 32	LOUT0, /LOUT0 LOUT1, /LOUT1 LOUT2, /LOUT2	Differential LVDS Compatible Output Drivers. Output termination is 100Ω across the pair. For low-jitter applications, unused LVDS output pairs should be terminated with 100Ω across the pair. See "Output Termination Recommendations" section for details.

Reference Input Driver Select Table

RSEL1	RSEL0	Internal Reference Clock
0	0	RFCK / 8
0	1	RFCK / 4
1	0	RFCK / 2
1	1	RFCK / 1

Table 1. Reference Input Divider Select Table

Output and Frequency Select Tables

PSELx	PENx	POUTx
0	0	Disable Output
0	1	(VCO/4) / 2
1	0	(VCO/4) / 8
1	1	(VCO/4) / 1

Table 2. PECL Output and Frequency Select Table

LSEL	LEN	LOUTx
0	0	Disable Output
0	1	(VCO/4) / 2
1	0	(VCO/4) / 8
1	1	(VCO/4) / 1

Table 3. LVDS Output and Frequency Select Table

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
XTAL Input Voltage ($V_{XTAL1, 2}$) ..... V_{CC} –1.9V to V_{CC}
Output Current (I_{OUT})
  LVPECL Outputs ..... ±50mA
  LVDS Outputs ..... ±10mA
Lead Temperature (soldering, 20 sec.) ..... +260°C
Storage Temperature (T_s) ..... –65°C to 150°C

Operating Ratings[2]

Supply Voltage ($V_{CCD,}$ V_{CCA}) ..... +3.0V to +3.6V
Supply Voltage (V_{CCO}) ..... +2.375V to +3.6V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance[3]
  QFN (θ_{JA})
    Still-Air ..... 24°C/W
  QFN (ψ_{JB})
    Junction-to-Board ..... 8°C/W

DC Electrical Characteristics[4]

Power Supply

T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CCA}	PLL Power Supply	Note 5	3.0	3.3	3.6	V
V_{CCD}	Control Logic Supply Voltage	Note 5	3.0	3.3	3.6	V
V_{CCO}	Output Supply Voltage		2.375	2.5	2.625	V
			3.0	3.3	3.6	V
I_{CC}	Total Power Supply Current	No load, max. V_{CC}, Note 6		240	300	mA
I_{CCA}	Analog Supply Current	Max. V_{CC}		10		mA
I_{CCO}	Output Supply Current	No load, max. V_{CC}		55		mA
I_{CCD}	Digital Supply Current	Max. V_{CC}		175		mA

LVCMOS/LVTTL Input Control Logic

V_{CCA} = V_{CCD} +3.3V ±10%, V_{CCO} = +2.5V ±5% or +3.3V ±10%; T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
I_{IH}	Input High Current	V_{IN} = V_{CC}	–125		150	µA
I_{IL}	Input Low Current	V_{IN} = 0.5V	–300			µA

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB. θ_{JA} and Ψ_{JB} values are determined for a 4-layer board in still-air, unless otherwise stated.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
5. V_{CCA} and V_{CCD} are not internally connected. They must be connected together on the PCB.
6. I_{CC} = I_{CCA} + I_{CCO} + I_{CCD}.

Reference Clock Input

V_{CCA} = V_{CCD} +3.3V ±10%, V_{CCO} = +2.5V ±5% or +3.3V ±10%; T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage	RFCK, /RFCK			V_{CCD} + 0.3	V
V_{IL}	Input LOW Voltage	RFCK, /RFCK	–0.3			V
V_{IN}	Input Voltage Swing	RFCK, /RFCK, See Figure 1a.	100			mV
$V_{DIFF-IN}$	Differential Input Voltage Swing	RFCK, /RFCK, See Figure 1b.	200			mV

LVPECL Output DC Electrical Characteristics

V_{CCA} = V_{CCD} +3.3V ±10%, V_{CCO} = +2.5V ±5% or +3.3V ±10%, R_L = 50Ω into V_{CCO}–2V; T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage		V_{CCO}–1.075		V_{CCO}–0.830	V
V_{OL}	Output LOW Voltage		V_{CCO}–1.860		V_{CCO}–1.570	V
V_{OUT}	Output Voltage Swing	See Figure 1a.	550	800		mV
$V_{DIFF-OUT}$	Differential Output Voltage Swing	See Figure 1b.	1100	1600		mV

LVDS Output DC Electrical Characteristics

V_{CCA} = V_{CCD} +3.3V ±10%, V_{CCO} = +2.5V ±5% or +3.3V ±10%, R_L = 100Ω across the pair; T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OUT}	Output Voltage Swing	See Figure 1a.	250	325		mV
$V_{DIFF-OUT}$	Differential Output Voltage Swing	See Figure 1b.	500	650		mV
V_{OCM}	Output Common Mode Voltage		1.125		1.275	V
ΔV_{OCM}	Change in Common Mode Voltage				25	mV

AC Electrical Characteristics

V_{CCA} = V_{CCD} = +3.3V ±10%; V_{CCO} = +2.5V ±5% or +3.3V ±10%, R_L (LVDS) = 100Ω across the output, R_L (LVPECL) = 50Ω into V_{CCO}–2V; T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{IN}	XTAL Input Frequency Range	Note 7	14		18	MHz
	Reference Input Frequency Range		14		144	MHz
f_{PHASE}	Phase Detector Operating Frequency Range		14		18	MHz
f_{OUT}	Output Frequency Range		73.5		756	MHz
f_{VCO}	Internal VCO Frequency Range		2352		3024	MHz
t_{SKEW}	LVPECL Output Banks (0–3), Bank-to-Bank	Note 8		15	50	ps
	LVDS Output Banks (0–2), Bank-to-Bank			15	50	ps
	Part-to-Part Skew	Note 9			200	ps
t_{LOCK}	PLL Lock Time				10	ms
t_{JITTER}	Loop Filter Optimized for Cycle-to-Cycle Jitter • R = 130Ω • C1 = 0.47µF • C2 = 100pF					
	1-Sigma Cycle-to-Cycle Jitter (XTAL Reference)	Note 10		4	6	ps_{RMS}
	1-Sigma Cycle-to-Cycle Jitter (RFCK Reference)	Note 10		5	7	ps_{RMS}
	Deterministic Jitter	Note 11		5.5	8	ps_{PP}
	Total Jitter	Note 12		80	100	ps_{PP}
	Spur			-35		dBc@ fphase
	XTAL/RFCK Crosstalk-Induced Jitter	Note 13			0.7	ps_{RMS}
BW	PLL Bandwidth	See “PLL Stability” Table	28.8		99.8	kHz
t_{DC}	F_{OUT} Duty Cycle		43	50	57	%
t_r, t_f	Output Rise/Fall Time (20% to 80%) LVPECL		100	250	400	ps
	Output Rise/Fall Time (20% to 80%) LVDS		80	150	300	ps
$t_{PW\_SYNC\_MIN}$		See “Synchronization”	8			Internal clock cycle
t_{PD_SYNC}		See “Synchronization”		8		Internal clock cycle

Notes:

7. Fundamental mode, series resonant crystal.
8. The bank-to-bank skew is defined as the worst-case difference between any two similar delay paths within a single device operating at the same voltage and temperature.
9. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.
10. Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles, $T_n - T_{n-1}$ where T is the time between rising edges of the output signal.
11. Deterministic jitter is measured at 2.5Gbps with both K28.5 and 2^{23}-1 PRBS pattern.
12. Total jitter definition: with an ideal clock input of frequency <f_{MAX}, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.
13. Crosstalk is measured at the output while applying two similar differential clock frequencies that are asynchronous with respect to each other at the inputs.

Single-Ended and Differential Swings

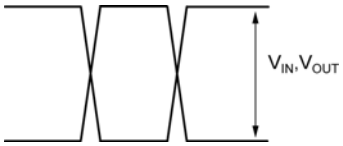


Figure 1a. Single-Ended Voltage Swing

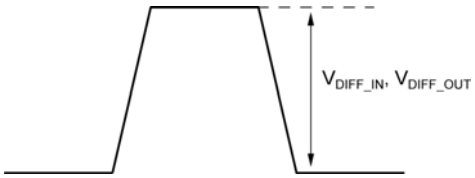


Figure 1b. Differential Voltage Swing

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Functional Description

Overall Function

The SY89537L integrated programmable clock synthesizer and fanout buffer is part of a precision PLL-based clock generation family optimized for internal system clock generation for (FPGAs, ASICs, NPU) applications.

Input MUX

The device's input patent-pending MUX accepts both a single-ended or differential reference clock; and a 14MHz to 18MHz series resonant crystal (XTAL). The input MUX has built-in isolation, which minimizes crosstalk between the two inputs. The input MUX drives the PLLs phase detector, which expects a frequency between 14MHz and 18MHz, therefore, the reference clock can be a maximum frequency of 144MHz when the reference divider is set to: divide-by-8. The minimum frequency that the reference accepts is 14MHz when the reference divider is set at: divide-by-1.

PLL VCO

The VCOs range of operation is from 2.352GHz to 3.024GHz, and the output frequency range is from 73.5MHz to 756MHz. The minimum output frequency is calculated according to the following equation:

$$f_{OUT} = \frac{fphase \times PreDivider \times FeedbackDivider}{PreDivider \times OutoutDivider \times PostDivider}$$

$$f_{OUT}(min) = \frac{14MHz \times 2 \times 84}{2 \times 2 \times 8}$$

$$f_{OUT}(min) = 73.5MHz$$

The maximum output frequency is calculated according to the following equation:

$$f_{OUT}(max) = \frac{18MHz \times 2 \times 84}{2 \times 2 \times 1}$$

$$f_{OUT}(max) = 756MHz$$

Crystal Input and Oscillator Interface

The SY89537L features a fully integrated on-board oscillator, which minimizes system implementation cost. The oscillator is a series resonant, multi-vibrator type crystal driver.

Oscillator Tips

1. Mount the crystal as close to the SY89537L as possible to minimize parasitic effects.
2. Mount on the same plane as the SY89537 to minimize on via hole inductance.
3. To minimize noise pick up on the loop filter pins, cut the ground plane directly underneath the loop filter component pads and traces.
4. Keep the crystal and its traces away from adjacent noisy traces to minimize on noise coupling.

Table 4 illustrates the crystal specifications. Figure 2 below illustrates how to interface the crystal with the SY89537L.

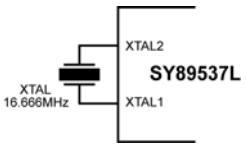

Figure 2. Crystal Interface

Quartz Crystal Selection:

Note: Raltron Series Resonant: AS-16.666-S-SMD-T-MI (2) Raltron

External Loop Filter Considerations

The SY89537L features an external PLL loop filter that allows the users to tailor the PLLs behavior. It is recommended that ceramic capacitors with NPO or X7R dielectric be used, since they have very low effective series resistance. For applications that require ultra-low, cycle-to-cycle jitter, use the components shown in Figure 3a. For best total jitter and best spur reduction, use the components shown in Figure 3b. Larger values of the pole capacitor (C2) results in less total jitter; however, the loop stability decreases. Loop stability decreases since the pole capacitor begins to dominate over the zero capacitor (C1). The external loop filter allows the user to change the loop filter values for specific jitter requirements. Using a smaller resistor in the loop filter decreases the PLLs loop bandwidth. This results in less noise from the PLL input, but potentially more noise from the VCO.

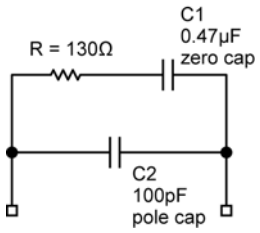

Figure 3a. Loop Filter for Lowest Cycle-to-Cycle Jitter

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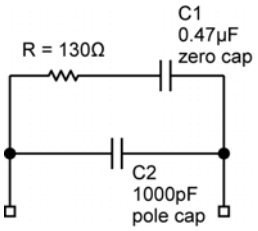

Figure 3b. Loop Filter for Lowest Total Jitter and Best Reference Spur Reduction

The reference spur is located at the phase detector frequency away from the carrier frequency. The attenuation of the reference spur is a function of the loop filter. Figure 4a shows the attenuation of the reference spur with the loop filter shown in Figure 3a. Figure 4b shows the attenuation of the reference spur with the loop filter shown in Figure 3b.

Crystal Frequency: 14MHz to 18MHz

Mode of Oscillation: Fundamental

	Min.	Typ.	Max.	Unit
Frequency Tolerance @25°C		±30	±50	ppm
Frequency Stability over 0*C to 70°C		±50	±100	ppm
Operating Temperature Range	–20		+70	°C
Storage Temperature Range	–55		+125	°C
Aging (per yr/1st 3yrs)			±5	ppm
Equivalent Series Resistance (ESR)			50	Ω
Drive Level		100		µW

Table 4. Quartz Crystal Oscillator Specifications

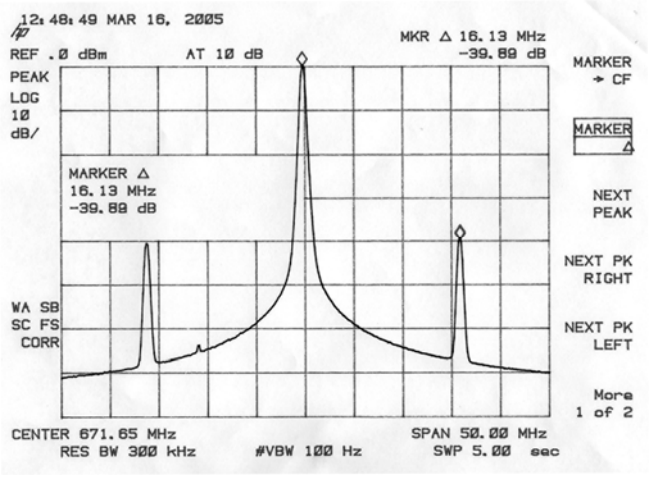

Figure 4a. Reference Spur at -39dB at 16MHz (R = 130Ω, C1 = 0.47µF, C2 = 100pF)

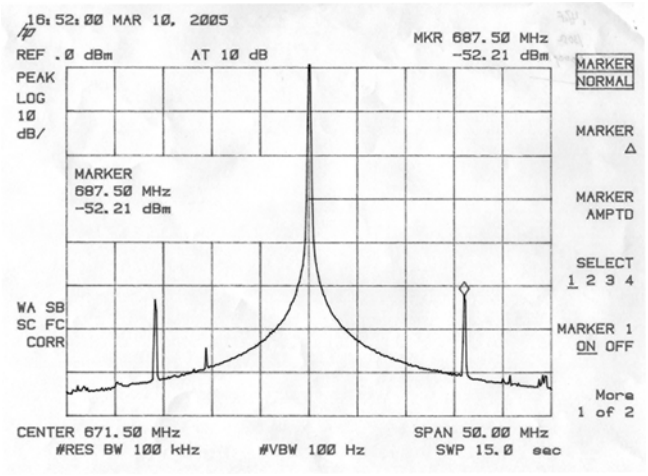

Figure 4b. Reference Spur at -52dB at 16MHz (R = 130Ω, C1 = 0.47µF, C2 = 1000pF)

Power Supply Filtering Techniques

As with any high-speed integrated circuit, power supply filtering is very important. At a minimum, VCCA, VCCD, and all VCCO pins should be individually connected using a via to the power supply plane, and separate bypass capacitors should be used for each pin. To achieve optimal jitter performance, each power supply pin should use separate instances of the circuit shown in Figure 5.

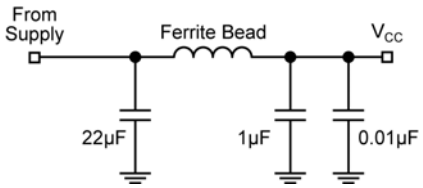

Figure 5. SY89537L Recommended Power Supply De-Coupling

Note:

For V_{CCA} and V_{CCD} use ferrite bead, Murata P/N BLM21A1025.

For V_{CCO} use ferrite bead, Murata, P/N BLM31P005.

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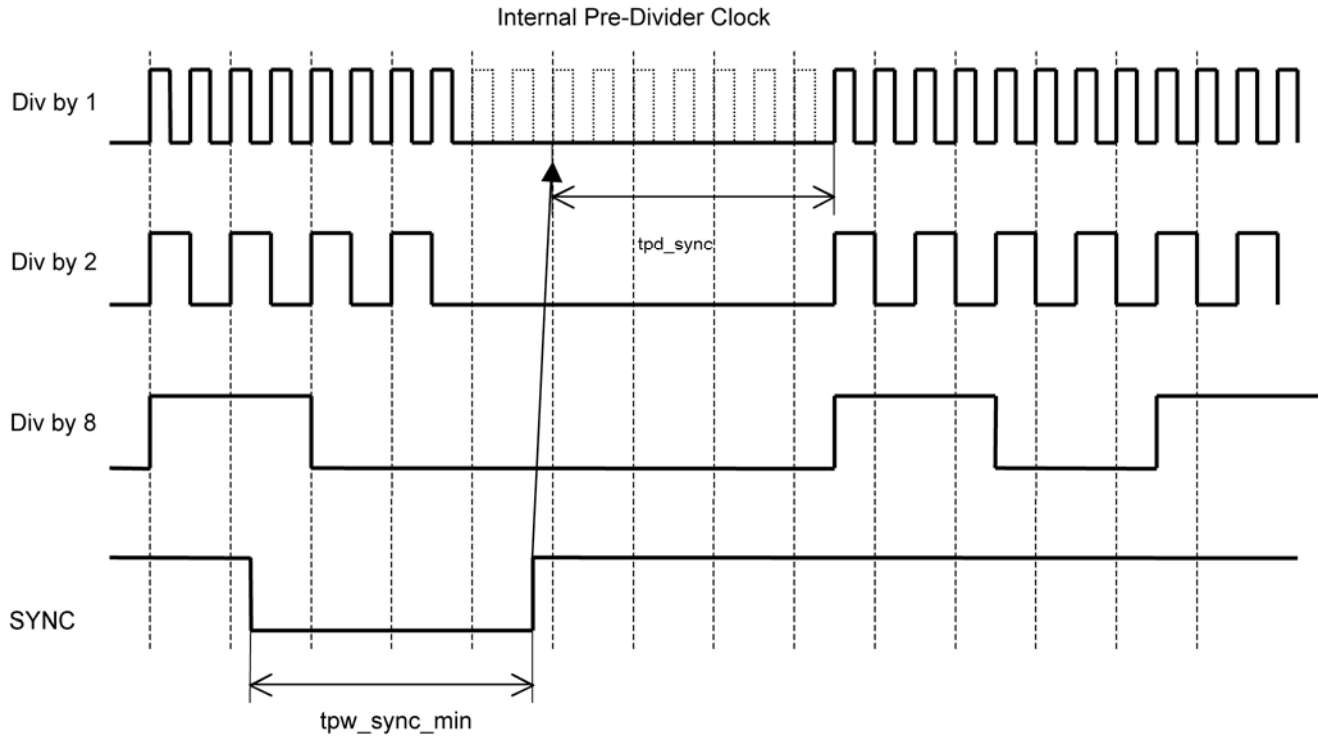
Synchronization



Output Synchronization Controlled by SYNC Timing Diagram

The SYNC control input is used to synchronize all divider outputs of the post divider. When a HIGH-LOW transition is applied to the SYNC control input the outputs are disabled when all post-divider outputs are LOW, see “Output Synchronization Controlled by SYNC Timing Diagram” for details. Once SYNC is asserted with a rising edge, the outputs are enabled when all internal divider stages are reaching their LOW state. This ensures a simultaneous switching of all outputs with the next LOW-HIGH transition of the pre-divider clock.

PLL Stability

For the loop filter configurations shown in Figure 3a and 3b, Table 5a and 5b below summarizes the PLLs loop stability in terms of damping factor, natural frequency, and bandwidth, and illustrates the pole and zero cutoff frequencies determined by the loop filter

Parameter										Units
V_{CC}	3	3	3	3.3	3.3	3.3	3.6	3.6	3.6	V
Temperature	–40	-40	-40	25	25	25	85	85	85	C
VCO Frequency	2352	2800	3024	2352	2800	3024	2352	2800	3024	MHz
Charge Pump Current	1.80E-04	1.80E-04	1.80E-04	1.80E-04	1.80E-04	1.80E-04	1.80E-04	1.80E-04	1.80E-04	A
Loop Filter Resistor	130	130	130	130	130	130	130	130	130	Ω
Zero Capacitor	4.70E-07	4.70E-07	4.70E-07	4.70E-07	4.70E-07	4.70E-07	4.70E-07	4.70E-07	4.70E-07	F
Pole Capacitor	1.00E-09	1.00E-09	1.00E-09	1.00E-09	1.00E-09	1.00E-09	1.00E-09	1.00E-09	1.00E-09	F
VCO Gain (KVCO)	3.20E+09	4.50E+09	4.50E+09	2.80E+09	3.30E+09	3.10E+09	2.30E+09	1.70E+09	1.30E+09	Hz/V
Feedback Divider	168	168	168	168	168	168	168	168	168	Integer
Phase Detector Frequency	14	16	18	14	16	18	14	16	18	MHz
Damping Factor	2.6	3.1	3.1	2.4	2.6	2.6	2.2	1.7	1.9	
Natural Frequency	13600.29	16127.95	16127.95	12721.90	13811.16	13386.09	11530.20	9912.83	8668.52	Hz
Ratio=Phase Detector Freq/BW	197	160	180	225	219	262	274	424	624	
Zero Frequency	2.61E+03	2.61E+03	2.61E+03	2.61E+03	2.61E+03	2.61E+03	2.61E+03	2.61E+03	2.61E+03	Hz
Loop Bandwidth (BN)	7.1E+04	9.98E+04	9.98+04	6.21E+04	7.32E+04	6.88E+04	5.1E+04	3.77E+04	2.88E+04	Hz
Pole Frequency	1.22E+07	1.22E+07	1.22E+07	1.22E+07	1.22E+07	1.22E+07	1.22E+07	1.22E+07	1.22E+07	Hz

Table 5a. Optimized for Lowest Cycle-to-Cycle Jitter
(R = 130Ω, C1 = 0.47µF, C2 = 100pF)

Parameter										Units
V_{CC}	3	3	3	3.3	3.3	3.3	3.6	3.6	3.6	V
Temperature	–40	-40	-40	25	25	25	85	85	85	C
VCO Frequency	2352	2800	3024	2352	2800	3024	2352	2800	3024	MHz
Charge Pump Current	1.80E-04	1.80E-04	1.80E-04	1.80E-04	1.80E-04	1.80E-04	1.80E-04	1.80E-04	1.80E-04	A
Loop Filter Resistor	130	130	130	130	130	130	130	130	130	Ω
Zero Capacitor	4.70E-07	4.70E-07	4.70E-07	4.70E-07	4.70E-07	4.70E-07	4.70E-07	4.70E-07	4.70E-07	F
Pole Capacitor	1.00E-09	1.00E-09	1.00E-09	1.00E-09	1.00E-09	1.00E-09	1.00E-09	1.00E-09	1.00E-09	F
VCO Gain (KVCO)	3.20E+09	4.50E+09	4.50E+09	2.80E+09	3.30E+09	3.10E+09	2.30E+09	1.70E+09	1.30E+09	Hz/V
Feedback Divider	168	168	168	168	168	168	168	168	168	Integer
Phase Detector Frequency	14	16	18	14	16	18	14	16	18	MHz
Damping Factor	2.6	3.1	3.1	2.4	2.6	2.6	2.2	1.7	1.9	
Natural Frequency	13600.29	16127.95	16127.95	12721.90	13811.16	13386.09	11530.20	9912.83	8668.52	Hz
Ratio=Phase Detector Freq/BW	197	160	180	225	219	262	274	424	624	
Zero Frequency	2.61E+03	2.61E+03	2.61E+03	2.61E+03	2.61E+03	2.61E+03	2.61E+03	2.61E+03	2.61E+03	Hz
Loop Bandwidth (BN)	7.1E+04	9.98E+04	9.98+04	6.21E+04	7.32E+04	6.88E+04	5.1E+04	3.77E+04	2.88E+04	Hz
Pole Frequency	1.22E+06	1.22E+06	1.22E+06	1.22E+06	1.22E+06	1.22E+06	1.22E+06	1.22E+06	1.22E+06	Hz

Table 5b. Optimized for Total Jitter
(R = 130Ω, C1 = 0.47µF, C2 = 1000pF)

Figure 6 shows the open and closed loop gain of the SY89537L. The closed loop-gain plot shows that the SY89537L when configured with the recommended loop filter values has essentially no jitter peaking near the -3dB point. In addition, the open loop curve shows the frequency at which unity gain occurs for a typical case of the SY89537L with V_{CC} = 3.3V at T_A = 25°C. At unity gain, Figure 7 can be used to determine the phase margin or stability of the SY89537L.

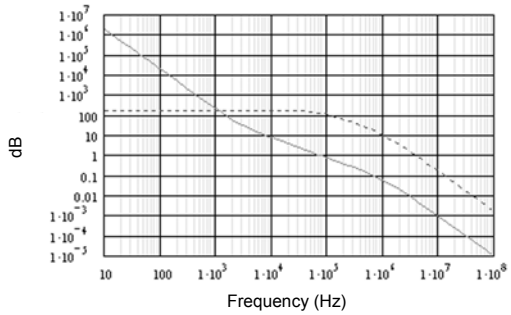


Figure 6. Open and Closed Loop Gain at V_{CC} = 3.3V, T_A = 25°C

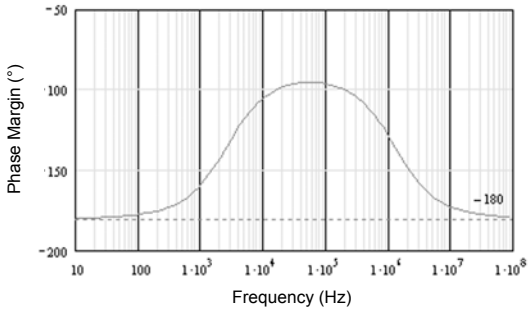


Figure 7. Phase Margin Plot at V_{CC} = 3.3V, T_A = 25°C

Figure 8 illustrates the VCO frequency versus the loop filter control voltage at 3.3V, T_A = 25°C. The normal loop filter control voltage is -300mV to +300mV. Figure 9 illustrates the VCO gain curve at V_{CC} = 3.3V, T_A = 25°C. With this set of information, determining the loop stability with other sets of loop filter configurations are possible.

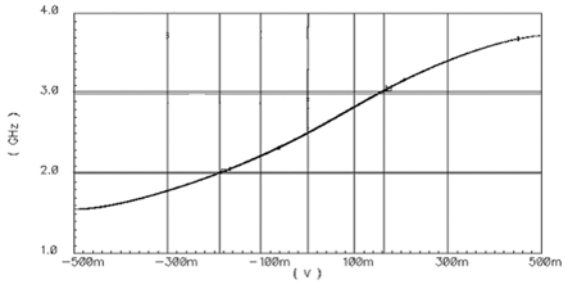


Figure 8. VCO Frequency vs. Loop Filter Control Voltage at 3.3V, T_A = 25°C

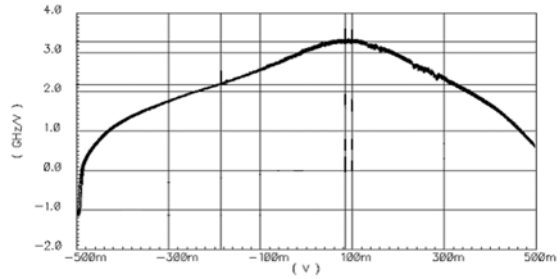


Figure 9. VCO Gain vs. Loop Filter Control Voltage at 3.3V, T_A = 25°C

Input Interface

RFCK is designed to accept any differential or single-ended input signal 300mV above V_{CC} or 300mV below GND. RFCK should not be left floating. Tie either the true or complement input to GND, but not both. A logic zero is achieved by connecting the complement input to GND with the true input floating. For TTL input, tie a 2.5kΩ resistor between the complement input and GND. LVDS, CML and HSTL differential signals may be connected directly to the reference inputs.

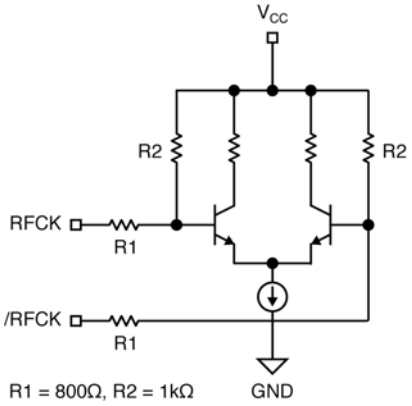


Figure 10. Simplified Input Structure

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Input Termination

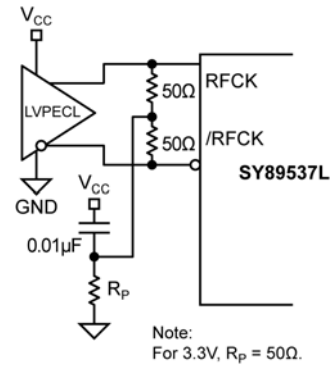

Figure 11a. LVPECL Interface (DC-Coupled)

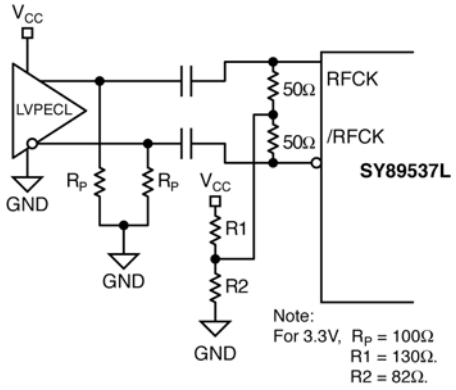

Figure 11b. LVPECL Interface (AC-Coupled)

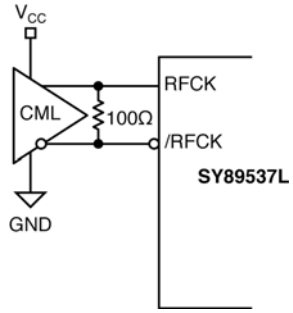

Figure 11c. CML Interface (DC-Coupled)

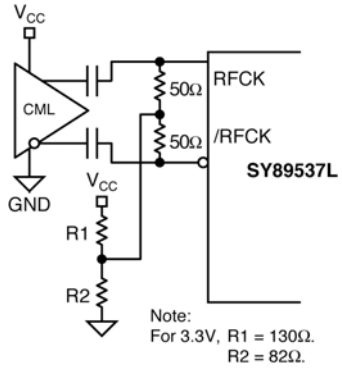

Figure 11d. CML Interface (AC-Coupled)

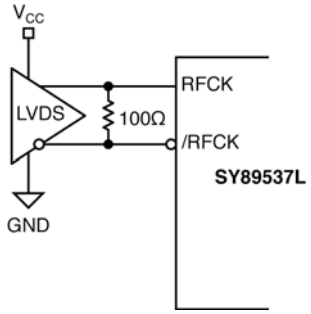

Figure 11e. LVDS (DC-Coupled)

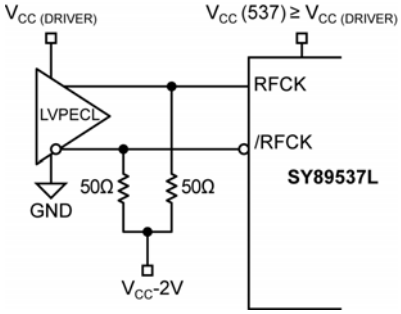

Figure 11f. 2.5V LVPECL (DC-Coupled)

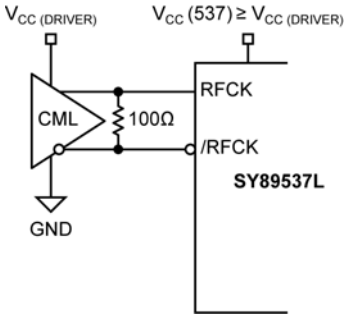

Figure 11g. 2.5V CML (DC-Coupled)

Output Bank and Frequency Control

There are five independently programmable output frequency banks, four differential LVPECL output banks and one differential LVDS output bank with three output pairs. Each bank has frequency control SELx and Enx to generate different divider ratios (see "PECL and LVDS Output and Frequency Select" Tables). It can be programmed for pass-through, internal divided VCO clock divide-by- /2, /8 or disable state. When disabled, the non-inverted output goes to static LOW and the inverted output goes to static HIGH.

Output Logic Characteristics

See "Output Termination Recommendations" for proper termination. When LVPECL single-ended output is desired, the unused complimentary output should be terminated. Unused LVPECL output pairs can be left floating. LVDS output pairs should be terminated with 100Ω across the pair. In order to minimize jitter and skew, unused LVDS output banks and unused LVDS output pairs should be terminated with 100Ω across each pair.

LVPECL Outputs:

- Typical voltage swing is 800mV into 50Ω.
- Common mode voltage is V_{CCO}–1.3V.

LVDS Outputs:

- Typical voltage swing is 325mV into 100Ω.
- Common mode voltage is 1.2V.

Output Termination Recommendations

LVPECL

LVPECL has high input impedance, very low output (open emitter) impedance, and small signal swing which results in low EMI. LVPECL is ideal for driving 50Ω-and-100Ω-controlled impedance transmission lines. There are several techniques for terminating the LVPECL output: Parallel Termination Thevenin-Equivalent, Parallel Termination (3-resistor), and AC-coupled termination. Unused output pairs may be left floating. However, single-ended outputs must be terminated, or balanced.

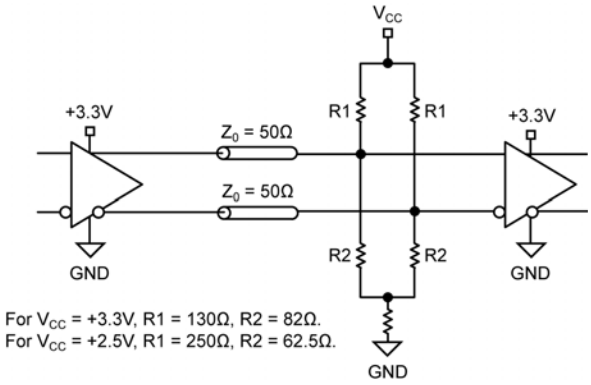

Figure 12a. Parallel Thevenin-Equivalent

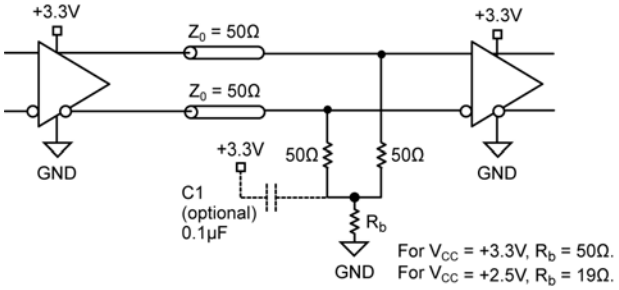

Figure 12b. Parallel Termination

LVDS

LVDS specifies a small swing of 325mV typical, on a nominal 1.2V common mode above ground. The common mode voltage has tight limits to permit large variations in ground between an LVDS driver and receiver. Also, change in common mode voltage, as a function of data input, is kept to a minimum, to keep EMI low.

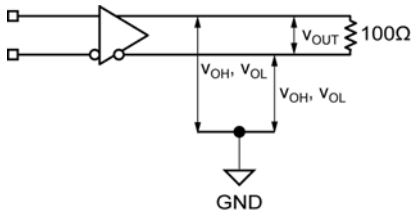

Figure 13a. LVDS Differential Measurement

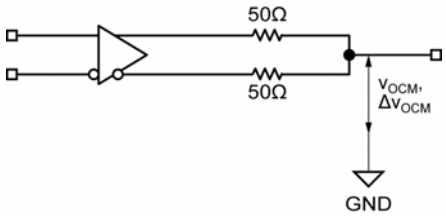

Figure 13b. LVDS Common Mode Measurement

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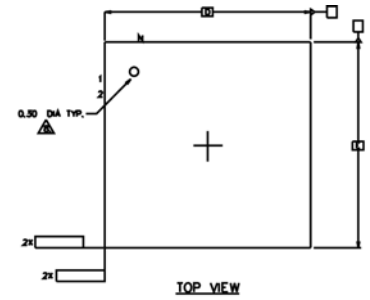
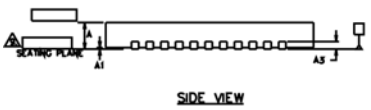
Related Product and Support Documentation

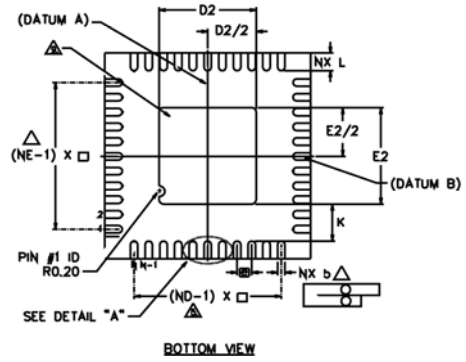
Part Number	Function	Data Sheet Link
SY89538L	3.3V, Precision LVPECL and LVDS Programmable, Multiple Output Bank Clock Synthesizer and Fanout Buffer with Zero Delay	http://www.micrel.com/product-info/products/sy89538l.shtml
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml

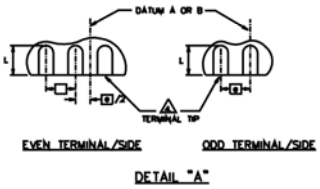
Package Information



NOTES :
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M. – 1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. θ IS IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
6. MAX. PACKAGE WARPAGE IS 0.05 mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LASER MARKED.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
10. THIS DRAWING CONFORMES TO JEDEC REGISTERED OUTLINE MO-220







SYMBOL	DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		44		3
ND		11		4
NE		11		
L	0.55	0.60	0.65	
b	0.18	0.25	0.30	4
D2	3.20	3.30	3.40	
E2	3.20	3.30	3.40	
D		7.00 BSC		
E		7.00 BSC		
A	0.80	0.85	1.00	
A1	0.00	0.02	0.05	
K		0.20 MIN.		
θ	0	——	12	2

44-Pin QFN

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