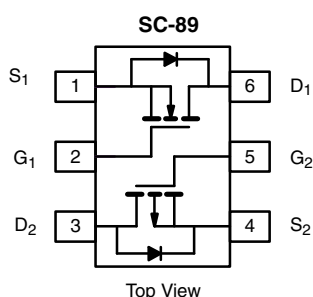


Complementary N- and P-Channel 60 V (D-S) MOSFET

PRODUCT SUMMARY

	V _{DS} (V)	R _{DS(on)} (Ω)	I _D (mA)
N-Channel	60	1.40 at V _{GS} = 10 V	500
		3 at V _{GS} = 4.5 V	200
P-Channel	- 60	4 at V _{GS} = - 10 V	- 500
		8 at V _{GS} = - 4.5 V	- 25



Marking Code: H

Ordering Information: Si1029X-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

- **Halogen-free According to IEC 61249-2-21 Definition**
- TrenchFET® Power MOSFETs
- Very Small Footprint
- High-Side Switching
- Low On-Resistance:
N-Channel, 1.40 Ω
P-Channel, 4 Ω
- Low Threshold: ± 2 V (typ.)
- Fast Switching Speed: 15 ns (typ.)
- Gate-Source ESD Protected: 2000 V
- Compliant to RoHS Directive 2002/95/EC


RoHS
COMPLIANT
HALOGEN
FREE

BENEFITS

- Ease in Driving Switches
- Low Offset (Error) Voltage
- Low-Voltage Operation
- High-Speed Circuits

APPLICATIONS

- Replace Digital Transistor, Level-Shifter
- Battery Operated Systems
- Power Supply Converter Circuits

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

Parameter		Symbol	N-Channel		P-Channel		Unit
			5 s	Steady State	5 s	Steady State	
Drain-Source Voltage		V _{DS}	60		- 60		V
Gate-Source Voltage		V _{GS}	± 20				
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 25 °C	I _D	320	305	- 200	- 190	mA
	T _A = 85 °C		230	220	- 145	- 135	
Pulsed Drain Current ^b		I _{DM}	650		- 650		
Continuous Source Current (Diode Conduction) ^a		I _S	450	380	- 450	- 380	
Maximum Power Dissipation ^a	T _A = 25 °C	P _D	280	250	280	250	mW
	T _A = 85 °C		145	130	145	130	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150				°C
Gate-Source ESD Rating (HBM, Method 3015)		ESD	2000				V

Notes:

a. Surface mounted on FR4 board.

b. Pulse width limited by maximum junction temperature.

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)									
Parameter	Symbol	Test Conditions		Min.	Typ.	Max.	Unit		
Static									
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 10 μA	N-Ch	60			V		
		V _{GS} = 0 V, I _D = - 10 μA	P-Ch	- 60					
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	1		2.5			
		V _{DS} = V _{GS} , I _D = - 250 μA	P-Ch	- 1		- 3.0			
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 5 V	N-Ch			± 50	nA		
			P-Ch			± 100			
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 0 V, V _{GS} = ± 10 V	N-Ch			± 150			
			P-Ch			± 200			
		V _{DS} = 50 V, V _{GS} = 0 V	N-Ch			10			
		V _{DS} = - 50 V, V _{GS} = 0 V	P-Ch			- 25			
On-State Drain Current ^a	I _{D(on)}	V _{DS} = 50 V, V _{GS} = 0 V, T _J = 85 °C	N-Ch			100	mA		
		V _{DS} = - 50 V, V _{GS} = 0 V, T _J = 85 °C	P-Ch			- 250			
V _{DS} = 10 V, V _{GS} = 4.5 V		N-Ch	500						
V _{DS} = - 10 V, V _{GS} = - 4.5 V		P-Ch	- 50						
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{DS} = 7.5 V, V _{GS} = - 4.5 V	N-Ch	800					
		V _{DS} = - 10 V, V _{GS} = - 10 V	P-Ch	- 600					
		V _{GS} = 4.5 V, I _D = 200 mA	N-Ch			3	Ω		
		V _{GS} = - 4.5 V, I _D = - 25 mA	P-Ch			8			
		V _{GS} = 10 V, I _D = 500 mA	N-Ch			1.40			
		V _{GS} = - 10 V, I _D = - 500 mA	P-Ch			4			
V _{GS} = 10 V, I _D = 500 mA, T _J = 125 °C	N-Ch			2.50					
V _{GS} = - 10 V, I _D = - 500 mA, T _J = 125 °C	P-Ch			6					
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 200 mA	N-Ch		200		ms		
		V _{DS} = - 10 V, I _D = - 100 mA	P-Ch		100				
Diode Forward Voltage ^a	V _{SD}	I _S = 200 mA, V _{GS} = 0 V	N-Ch			1.4	V		
		I _S = - 200 mA, V _{GS} = 0 V	P-Ch			- 1.4			
Dynamic ^b									
Total Gate Charge	Q _g	N-Channel V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 250 mA	N-Ch		750		pC		
Gate-Source Charge	Q _{gs}		P-Ch		1700				
Gate-Drain Charge	Q _{gd}	P-Channel V _{DS} = - 30 V, V _{GS} = - 15 V, I _D = - 500 mA	N-Ch		75				
			P-Ch		260				
Input Capacitance	C _{iss}	N-Channel V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz	N-Ch		225		pF		
			P-Ch		460				
Output Capacitance	C _{oss}	P-Channel V _{DS} = - 25 V, V _{GS} = 0 V, f = 1 MHz	N-Ch		30			ns	
			P-Ch		23				
Reverse Transfer Capacitance	C _{rss}		N-Ch		6				
			P-Ch		10				
Turn-On Time ^c	t _{ON}		N-Ch		3				
			P-Ch		5				
Turn-Off Time ^c	t _{OFF}		N-Ch		15				
			P-Ch		20				
			N-Ch		20				
			P-Ch		35				

Notes:

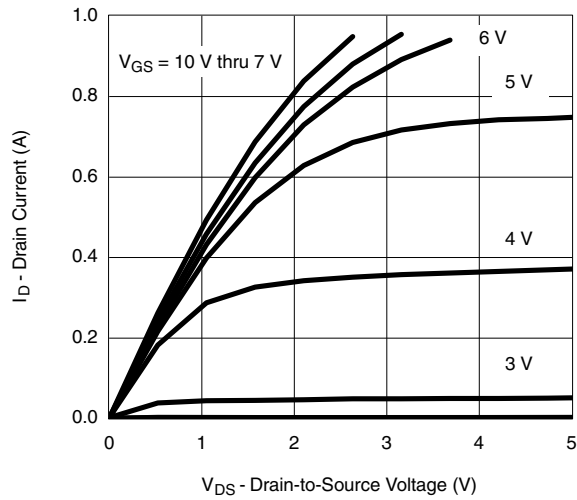
a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

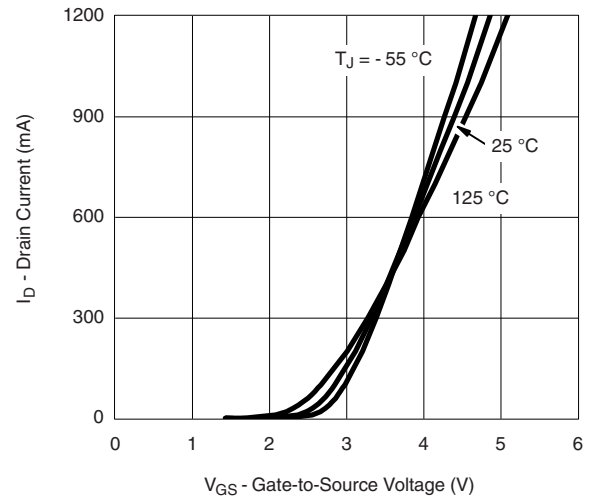
c. Switching time is essentially independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

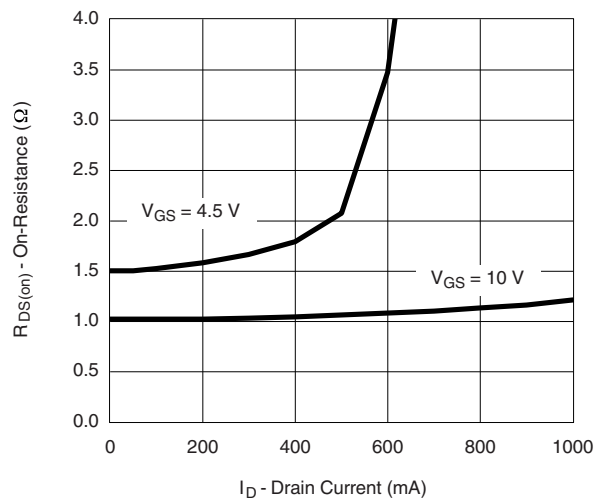
N-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)



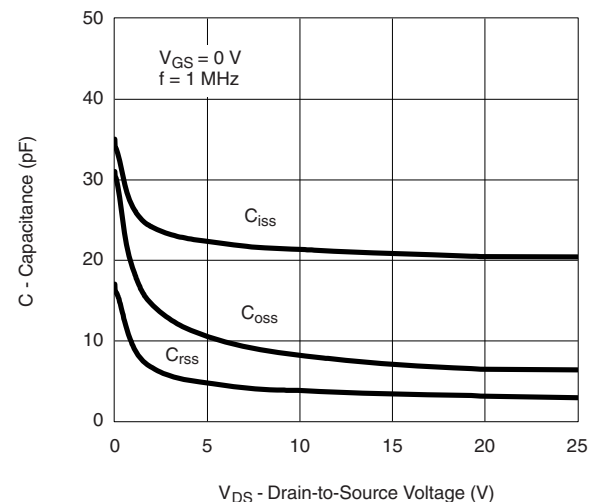
Output Characteristics



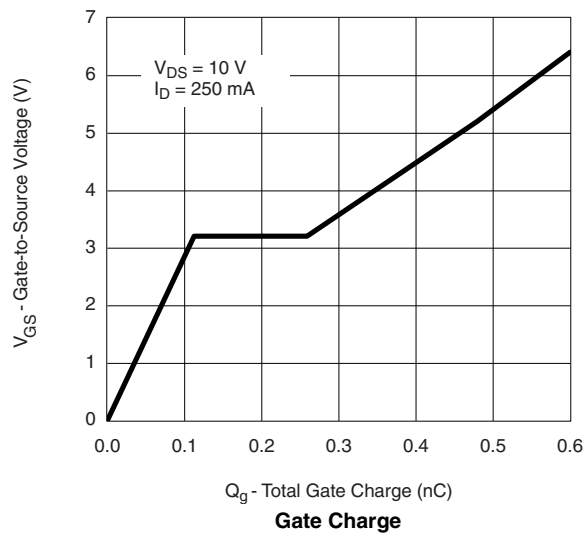
Transfer Characteristics



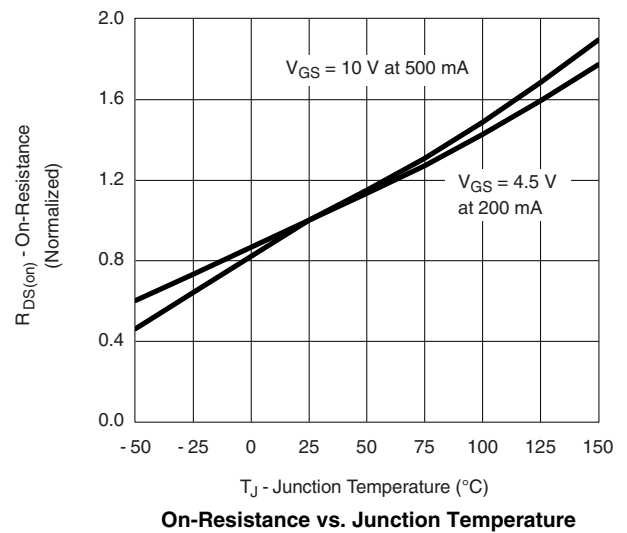
On-Resistance vs. Drain Current



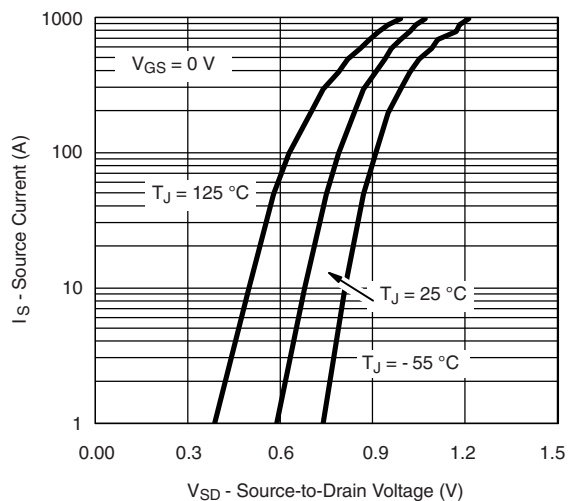
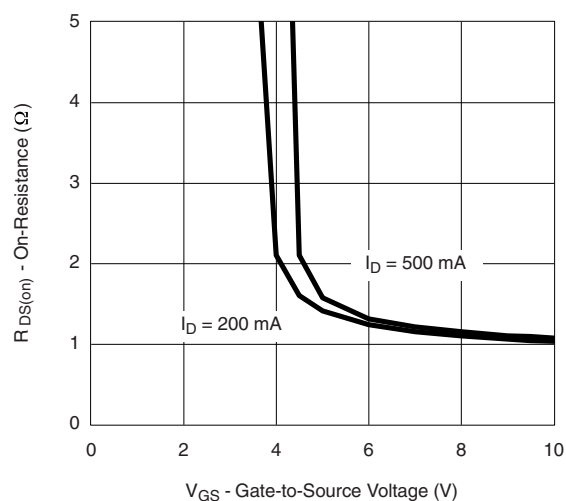
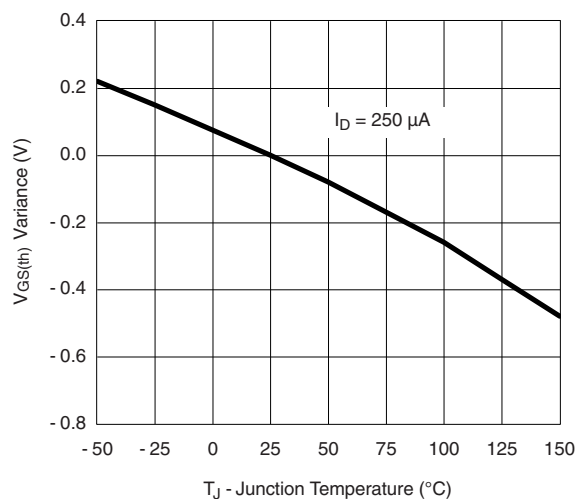
Capacitance



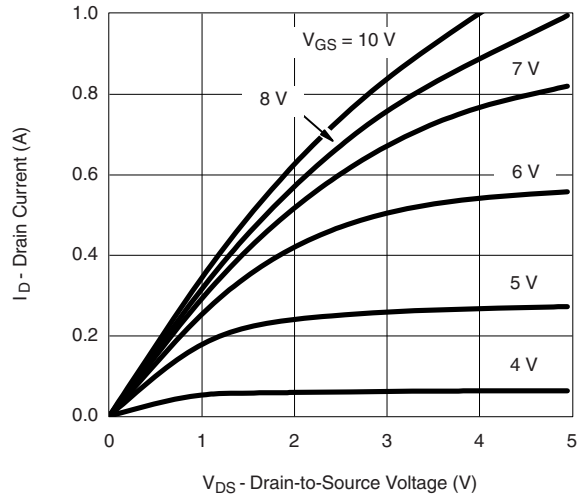
Gate Charge



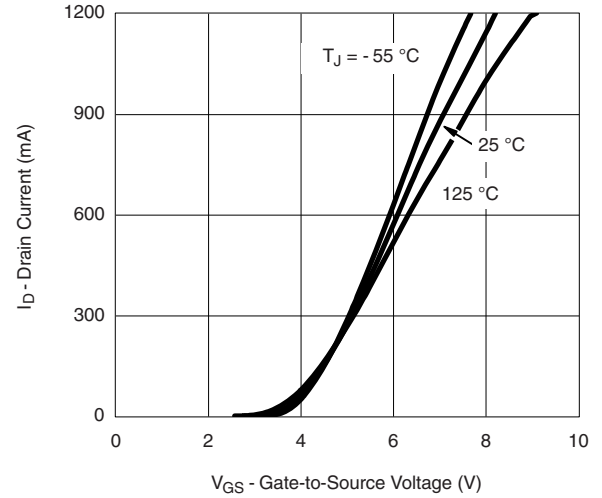
On-Resistance vs. Junction Temperature

N-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Source-Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage Variance Over Temperature

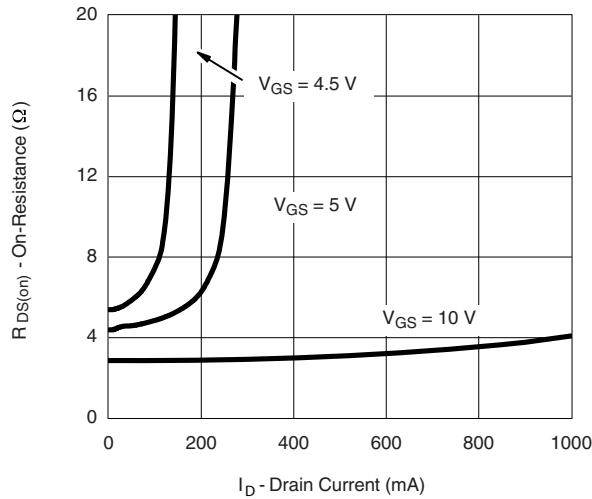
P-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)



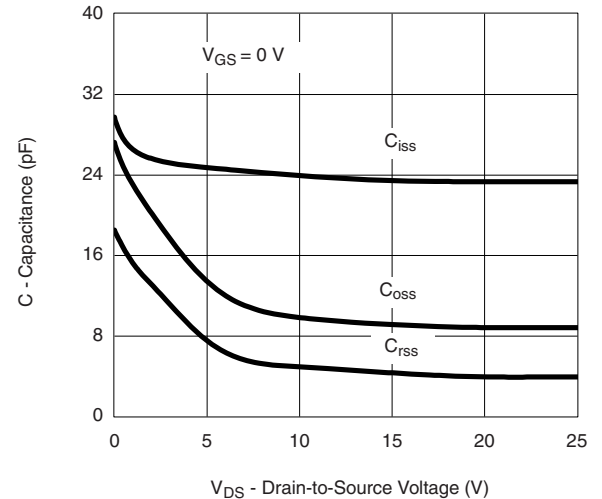
Output Characteristics



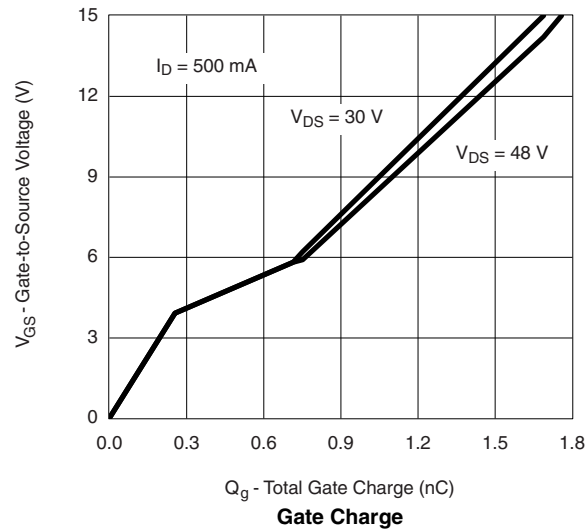
Transfer Characteristics



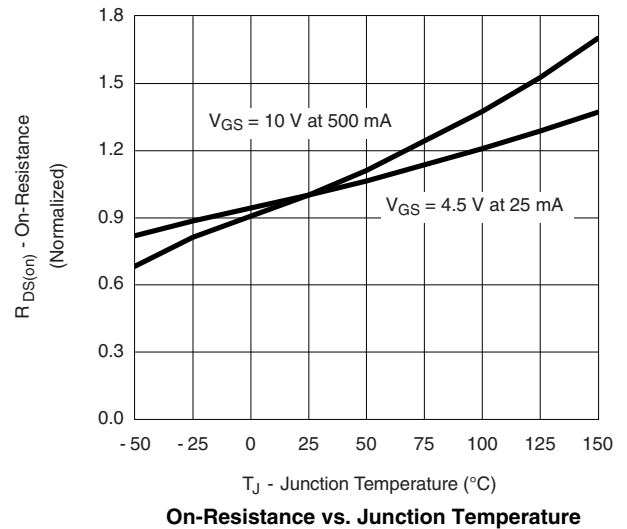
On-Resistance vs. Drain Current



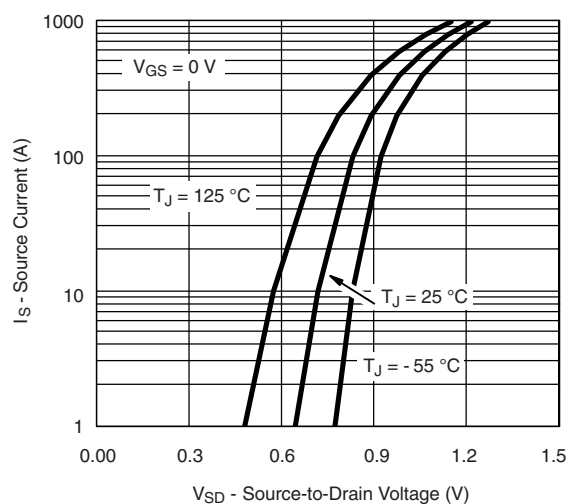
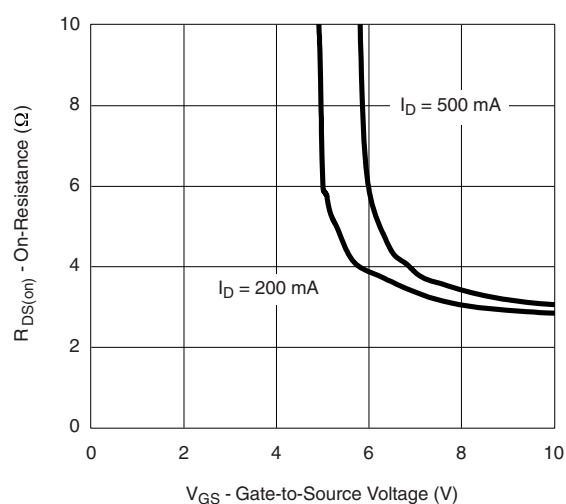
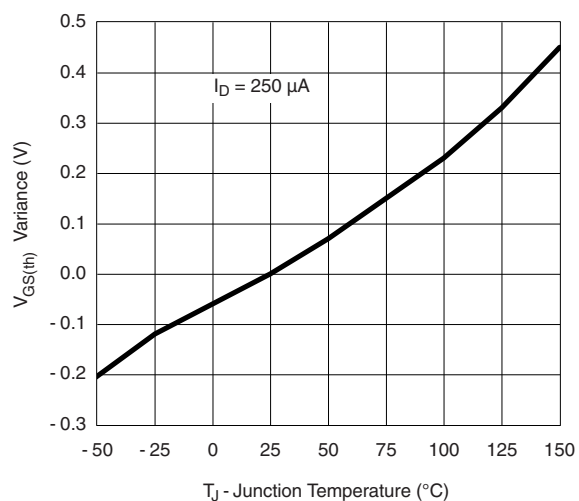
Capacitance



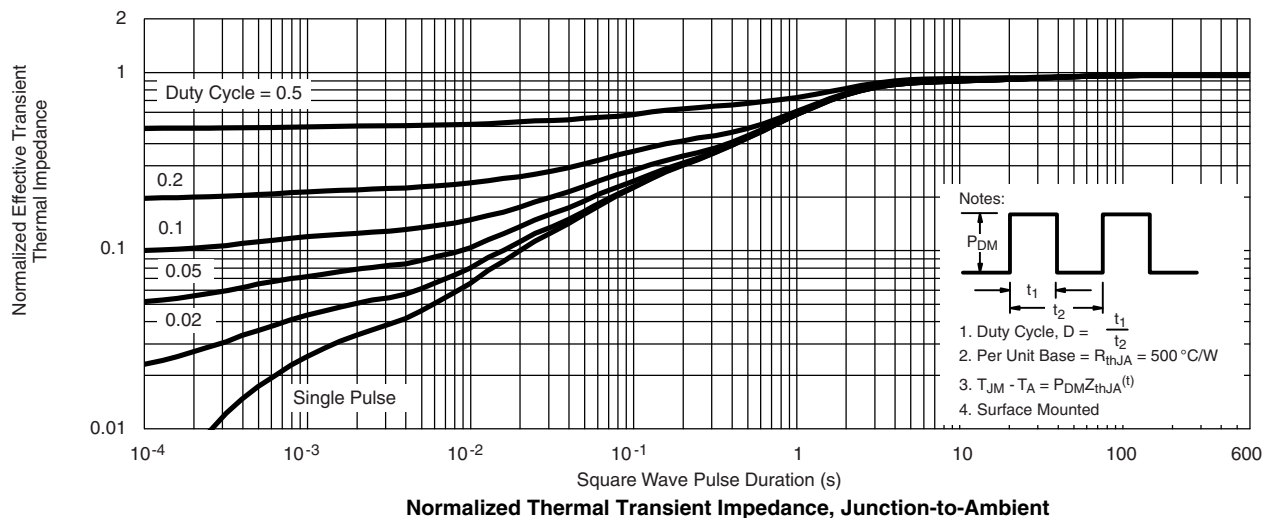
Gate Charge



On-Resistance vs. Junction Temperature

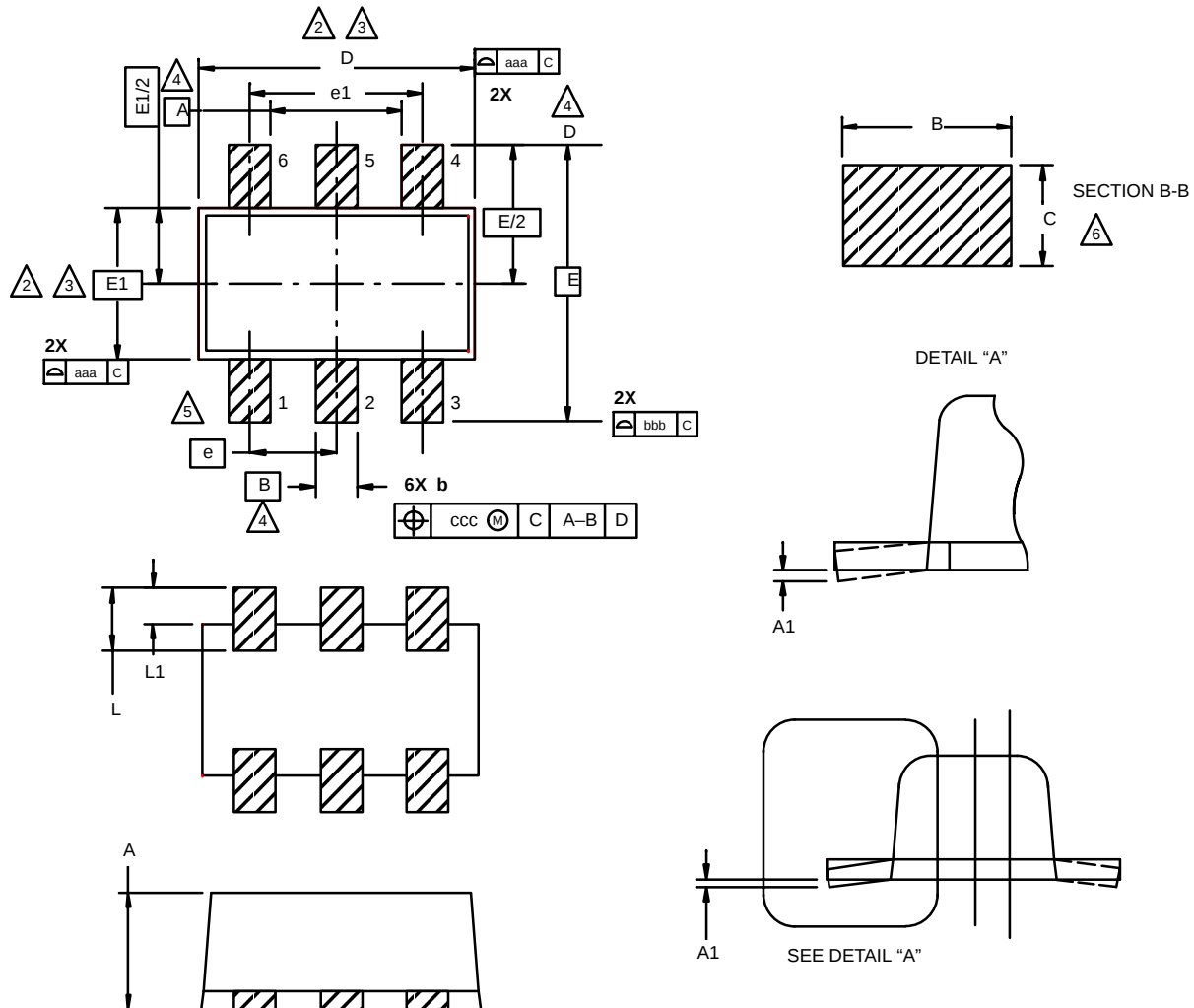
P-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Source-Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage Variance Over Temperature

N- OR P-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)



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SC89: 6- LEADS (SOT-563F)



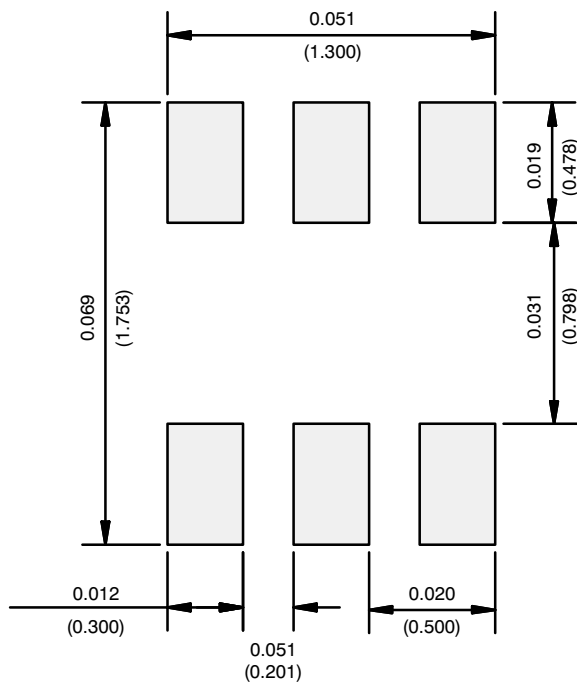
NOTES:

1. Dimensions in millimeters.

- △2 Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per dimension E1 does not include interlead flash or protrusion, interlead flash or protrusion shall not exceed 0.15 mm per side.
- △3 Dimensions D and E1 are determined at the outmost extremes of the plastic body exclusive of mold flash, the bar burrs, gate burrs and interlead flash, but including any mismatch between the top and the bottom of the plastic body.
- △4 Datums A, B and D to be determined 0.10 mm from the lead tip.
- △5 Terminal numbers are shown for reference only.
- △6 These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.

	MILLIMETERS		Note	Symbol	Tolerances Of Form And Position
Dim	Min	Max			
A	0.56	0.60		aaa	0.10
A1	0.00	0.10		bbb	0.10
b	0.15	0.30		ccc	0.10
c	0.10	0.18			
D	1.50	1.70	2, 3		
E	1.55	1.70			
E1	1.20 BSC		2, 3		
e	0.50 BSC				
e1	1.00 BSC				
L	0.35 BSC				
L1	0.20 BSC				
ECN: E-00499—Rev. B, 02-Jul-01 DWG: 5880					

RECOMMENDED MINIMUM PADS FOR SC-89: 6-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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