

## 1:4 Clock Driver for Intel PCI Express Chipsets

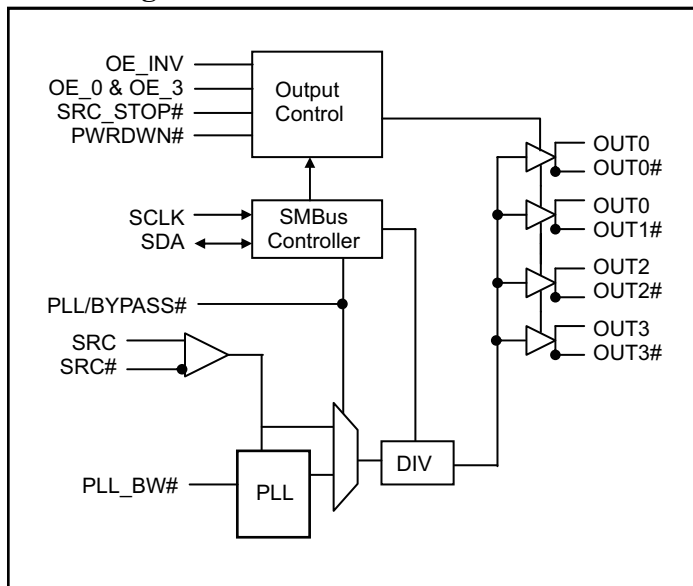
### Features

- Four Pairs of Differential Clocks
- Low skew < 50ps
- Low jitter < 50ps
- Output Enable for all outputs
- Outputs tristate control via SMBus
- Power Management Control
- Programmable PLL Bandwidth
- PLL or Fanout operation
- 3.3V Operation
- Packaging (Pb-free and Green):
  - 28-Pin SSOP (H28) & 28-Pin TSSOP (L28)

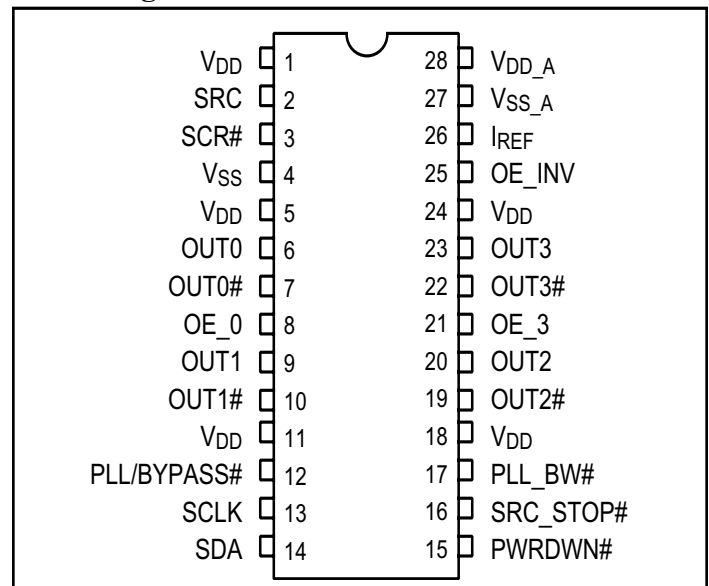
### Description

Pericom Semiconductor's PI6C20400 is a high-speed, low-noise differential clock buffer designed to be companion to PI6C410B. The device distributes the differential SRC clock from PI6C410B to four differential pairs of clock outputs either with or without PLL. The clock outputs are controlled by input selection of SRC\_STOP#, PWRDWN# and SMBus, SCLK and SDA. When input of either SRC\_STOP# or PWRDWN# is low, the output clocks are Tristated. When PWRDWN# is low, the SDA and SCLK inputs must be Tri-stated.

### Block Diagram



### Pin Configuration



### Pin Descriptions

Pin Name	Type	Pin No	Description
SRC & SRC#	Input	2, 3	0.7V Differential SRC input from PI6C410 clock synthesizer
OE_0 & OE_3	Input	8, 21	3.3V LVTTTL input for enabling outputs, active high. OE_0 for OUT0 / OUT0# OE_3 for OUT3 / OUT3#
OE_INV	Input	25	3.3V LVTTTL input for inverting the OE, SRC_STOP# and PWRDWN# pins. When 0 = same stage When 1 = OE_0, OE_3, SRC_STOP#, PWRDWN# inverted.
OUT[0:3] & OUT[0:3]#	Output	6, 7, 9, 10, 19, 20, 22, 23	0.7V Differential outputs
PLL/BYPASS#	Input	12	3.3V LVTTTL input for selecting fan-out of PLL operation.
SCLK	Input	13	SMBus compatible SCLOCK input
SDA	I/O	14	SMBus compatible SDATA
IREF	Input	26	External resistor connection to set the differential output current
SRC_STOP#	Input	16	3.3V LVTTTL input for SRC stop, active low
PLL_BW#	Input	17	3.3V LVTTTL input for selecting the PLL bandwidth
PWRDWN#	Input	15	3.3V LVTTTL input for Power Down operation, active low
VDD	Power	1, 5, 11, 18, 24	3.3V Power Supply for Outputs
VSS	Ground	4	Ground for Outputs
VSS_A	Ground	27	Ground for PLL
VDD_A	Power	28	3.3V Power Supply for PLL

### Serial Data Interface (SMBus)

This part is a slave only SMBus device that supports indexed block read and indexed block write protocol using a single 7-bit address and read/write bit as shown below.

### Address assignment

A6	A5	A4	A3	A2	A1	A0	W/R
1	1	0	1	1	1	0	0/1

### Data Protocol

1 bit	7 bits	1	1	8 bits	1	8 bits	1	8 bits	1		8 bits	1	1 bit
Start bit	Slave Addr	R/W	Ack	Register offset	Ack	Byte Count = N	Ack	Data Byte 0	Ack	...	Data Byte N - 1	Ack	Stop bit

#### Notes:

- Register offset for indicating the starting register for indexed block write and indexed block read. Byte Count in write mode cannot be 0.

**Data Byte 0: Control Register**

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Source Pin
0	Outputs Mode 0 = Divide by 2 1 = Normal	RW	1 = Normal	OUT[0:3], OUT[0:3]#	NA
1	PLL/BYPASS# 0 = Fanout 1 = PLL	RW	1 = PLL	OUT[0:3], OUT[0:3]#	NA
2	PLL Bandwidth 0 = High Bandwidth, 1 = Low Bandwidth	RW	1 = Low	OUT[0:3], OUT[0:3]#	NA
3	TBD				NA
4	TBD				NA
5	TBD				NA
6	SRC_STOP# 0 = Driven when stopped 1 = Tristate	RW	0 = Driven when stopped	OUT[0:3], OUT[0:3]#	
7	PWRDWN# 0 = Driven when stopped 1 = Tristate	RW	0 = Driven when stopped	OUT[0:3], OUT[0:3]#	NA

**Data Byte 1: Control Register**

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Source Pin
0					
1	OUTPUTS enable 1 = Enabled 0 = Disabled	RW	1 = Enabled	OUT0, OUT0#	NA
2		RW	1 = Enabled	OUT1, OUT1#	NA
3					
4					
5	OUTPUTS enable 1 = Enabled 0 = Disabled	RW	1 = Enabled	OUT2, OUT2#	NA
6		RW	1 = Enabled	OUT3, OUT3#	NA
7					

**Data Byte 2: Control Register**

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Source Pin
0					
1	Allow control of OUTPUTS with assertion of SRC_STOP# 0 = Free running 1 = Stopped with SRC_Stop#	RW	0 = Free running	OUT0, OUT0#	NA
2		RW	0 = Free running	OUT1, OUT1#	NA
3					
4					
5	Allow control of OUTPUTS with assertion of SRC_STOP# 0 = Free running 1 = Stopped with SRC_Stop#	RW	0 = Free running	OUT2, OUT2#	NA
6		RW	0 = Free running	OUT3, OUT3#	NA
7					

**Data Byte 3: Control Register**

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Source Pin
0	TBD	RW			
1		RW			
2		RW			
3		RW			
4		RW			
5		RW			
6		RW			
7		RW			

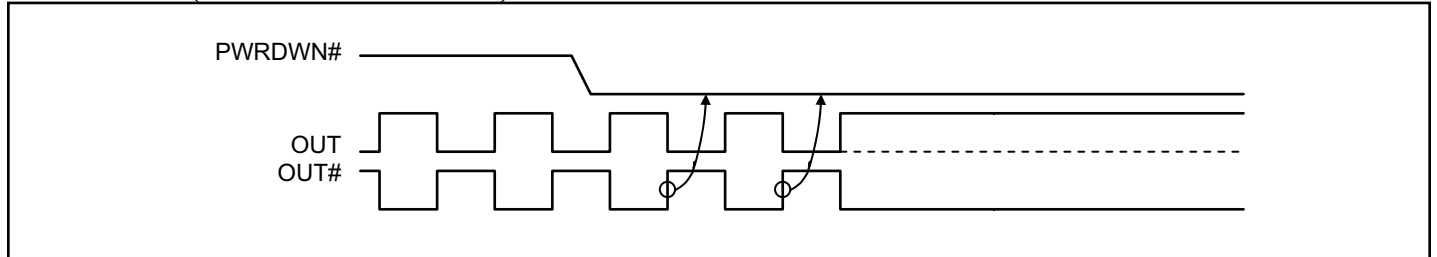
**Data Byte 4: Pericom ID Register**

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Pin
0	Pericom ID	R	0	NA	NA
1		R	0	NA	NA
2		R	0	NA	NA
3		R	0	NA	NA
4		R	0	NA	NA
5		R	1	NA	NA
6		R	0	NA	NA
7		R	0	NA	NA

**Functionality**

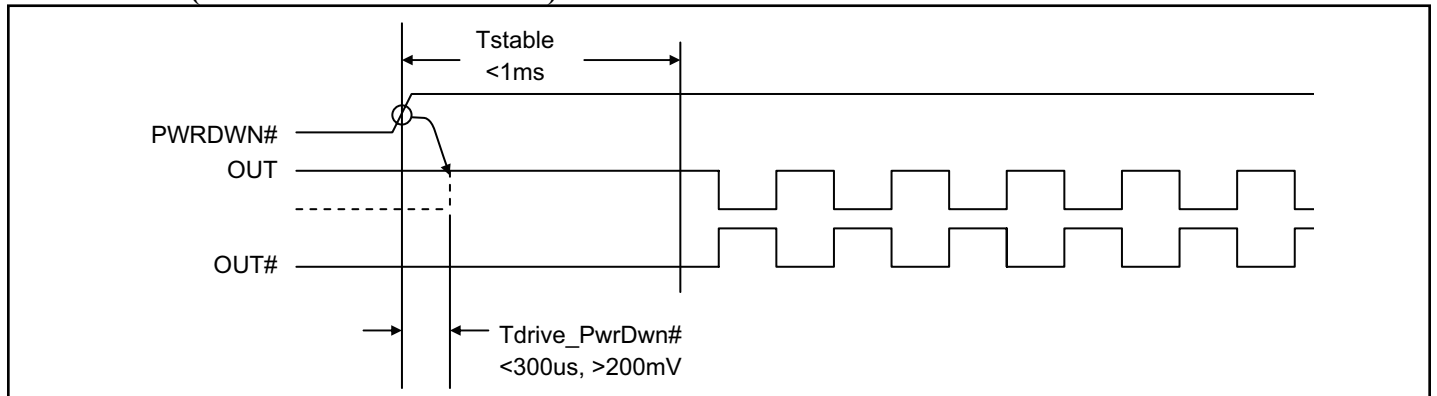
PWRDWN#	OUT	OUT#	SRC_Stop#	OUT	OUT#
1	Normal	Normal	1	Normal	Normal
0	$I_{REF} \times 2$ or Float	Low	0	$I_{REF} \times 6$ or Float	Low

**Power Down (PWRDWN# assertion)**



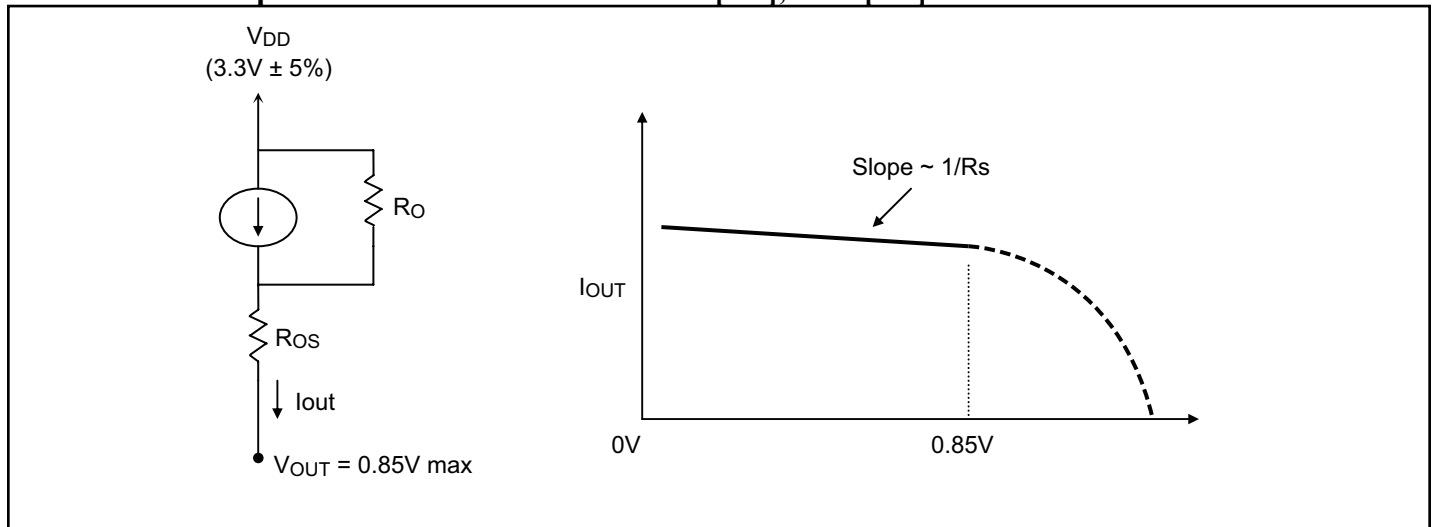
**Figure 1. Power down sequence**

**Power Down (PWRDWN# De-assertion)**



**Figure 2. Power down de-assert sequence**

**Current-mode output buffer characteristics of OUT[0:3], OUT[0:3]#**



**Figure 9. Simplified diagram of current-mode output buffer**

**Differential Clock Buffer characteristics**

Symbol	Minimum	Maximum
RO	3000Ω	N/A
ROS	unspecified	unspecified
VOUT	N/A	850mV

**Current Accuracy**

Symbol	Conditions	Configuration	Load	Min.	Max.
IOUT	VDD = 3.30 ±5%	RREF = 475Ω 1% IREF = 2.32mA	Nominal test load for given configuration	-12% INOMINAL	+12% INOMINAL

**Note:**

1. INOMINAL refers to the expected current based on the configuration of the device.

**Differential Clock Output Current**

Board Target Trace/Term Z	Reference R, Iref = VDD/(3xRr)	Output Current	VOH @ Z
100Ω (100Ω differential ≈ 15% coupling ratio)	RREF = 475Ω 1%, IREF = 2.32mA	IOH = 6 x IREF	0.7V @ 50

**Absolute Maximum Ratings** (Over operating free-air temperature range)

Symbol	Parameters	Min.	Max.	Units
V <sub>DD_A</sub>	3.3V Core Supply Voltage	-0.5	4.6	V
V <sub>DD</sub>	3.3V I/O Supply Voltage	-0.5	4.6	
V <sub>IH</sub>	Input High Voltage		4.6	
V <sub>IL</sub>	Input Low Voltage	-0.5		
T <sub>s</sub>	Storage Temperature	-65	150	°C
V <sub>ESD</sub>	ESD Protection	2000		V

**Note:**

1. Stress beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device.

**DC Electrical Characteristics** (V<sub>DD</sub> = 3.3±5%, V<sub>DD\_A</sub> = 3.3±5%)

Symbol	Parameters	Condition	Min.	Max.	Units
V <sub>DD_A</sub>	3.3V Core Supply Voltage		3.135	3.465	V
V <sub>DD</sub>	3.3V I/O Supply Voltage		3.135	3.465	
V <sub>IH</sub>	3.3V Input High Voltage	V <sub>DD</sub>	2.0	V <sub>DD</sub> + 0.3	
V <sub>IL</sub>	3.3V Input Low Voltage		V <sub>SS</sub> - 0.3	0.8	
I <sub>IK</sub>	Input Leakage Current	0 < V <sub>IN</sub> < V <sub>DD</sub>	-5	+5	µA
V <sub>OH</sub>	3.3V Output High Voltage	I <sub>OH</sub> = -1mA	2.4		V
V <sub>OL</sub>	3.3V Output Low Voltage	I <sub>OL</sub> = 1mA		0.4	
I <sub>OH</sub>	Output High Current	I <sub>OH</sub> = 6 x I <sub>REF</sub> , I <sub>REF</sub> = 2.32mA	12.2	15.6	mA
C <sub>IN</sub>	Input Pin Capacitance		3	5	
C <sub>OUT</sub>	Output Pin Capacitance			6	pF
L <sub>PIN</sub>	Pin Inductance			7	nH
I <sub>DD</sub>	Power Supply Current	V <sub>DD</sub> = 3.465V, F <sub>CPU</sub> = 200MHz		200	mA
I <sub>SS</sub>	Power Down Current	Driven outputs		40	
I <sub>SS</sub>	Power Down Current	Tristate outputs		12	
T <sub>A</sub>	Ambient Temperature		0	70	°C

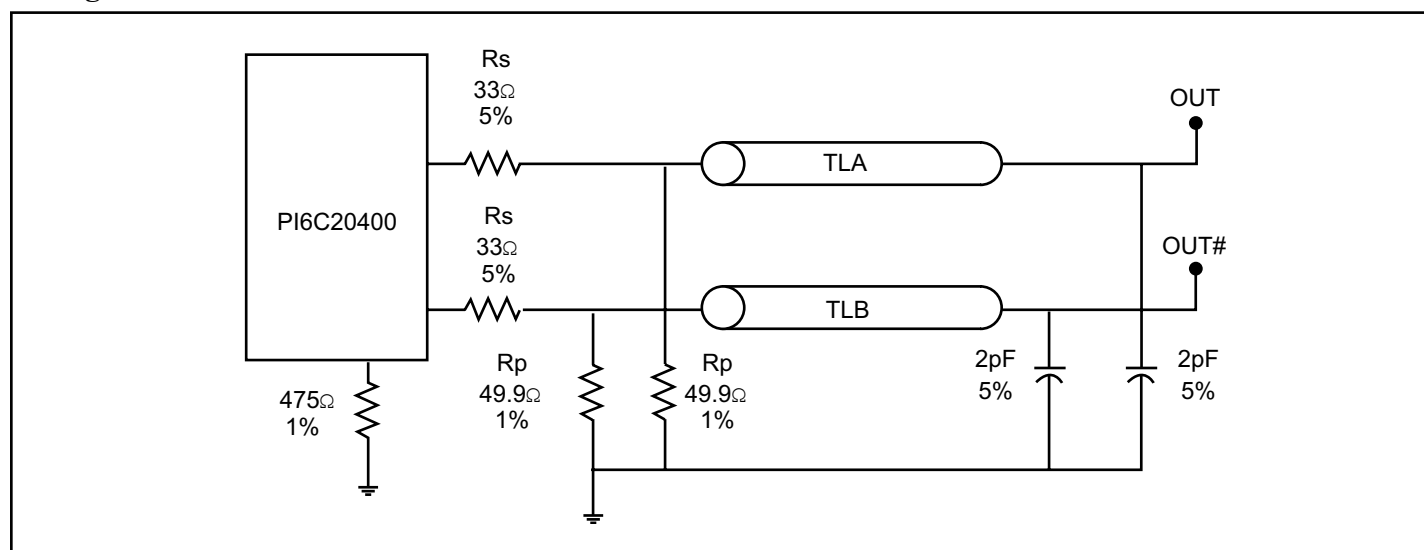
**AC Switching Characteristics** ( $V_{DD} = 3.3 \pm 5\%$ ,  $V_{DD\_A} = 3.3 \pm 5\%$ )

Symbol	Parameters	Min	Max.	Units	Notes
$T_{rise} / T_{fall}$	Rise and Fall Time (measured between 0.175V to 0.525V)	175	700	ps	2
$\Delta T_{rise} / \Delta T_{fall}$	Rise and Fall Time Variation		125	ps	2
	Rise/Fall Matching		20	%	2
$T_{pd}$	PLL Mode		$\pm 250$	ps	
	Non-PLL Mode	2.5	6.5	ns	
$T_{skew}$	Output-to-Output Skew		50	ps	3
$T_{jitter}$	Cycle – Cycle Jitter		50	ps	3, 4
$V_{HIGH}$	Voltage High including overshoot	660	1150	mV	2
$V_{LOW}$	Voltage Low including undershoot	-300		mV	2
$V_{cross}$	Absolute crossing point voltages	250	550	mV	2
$\Delta V_{cross}$	Total Variation of $V_{cross}$ over all edges		140	mV	2
$T_{DC}$	Duty Cycle	45	55	%	3

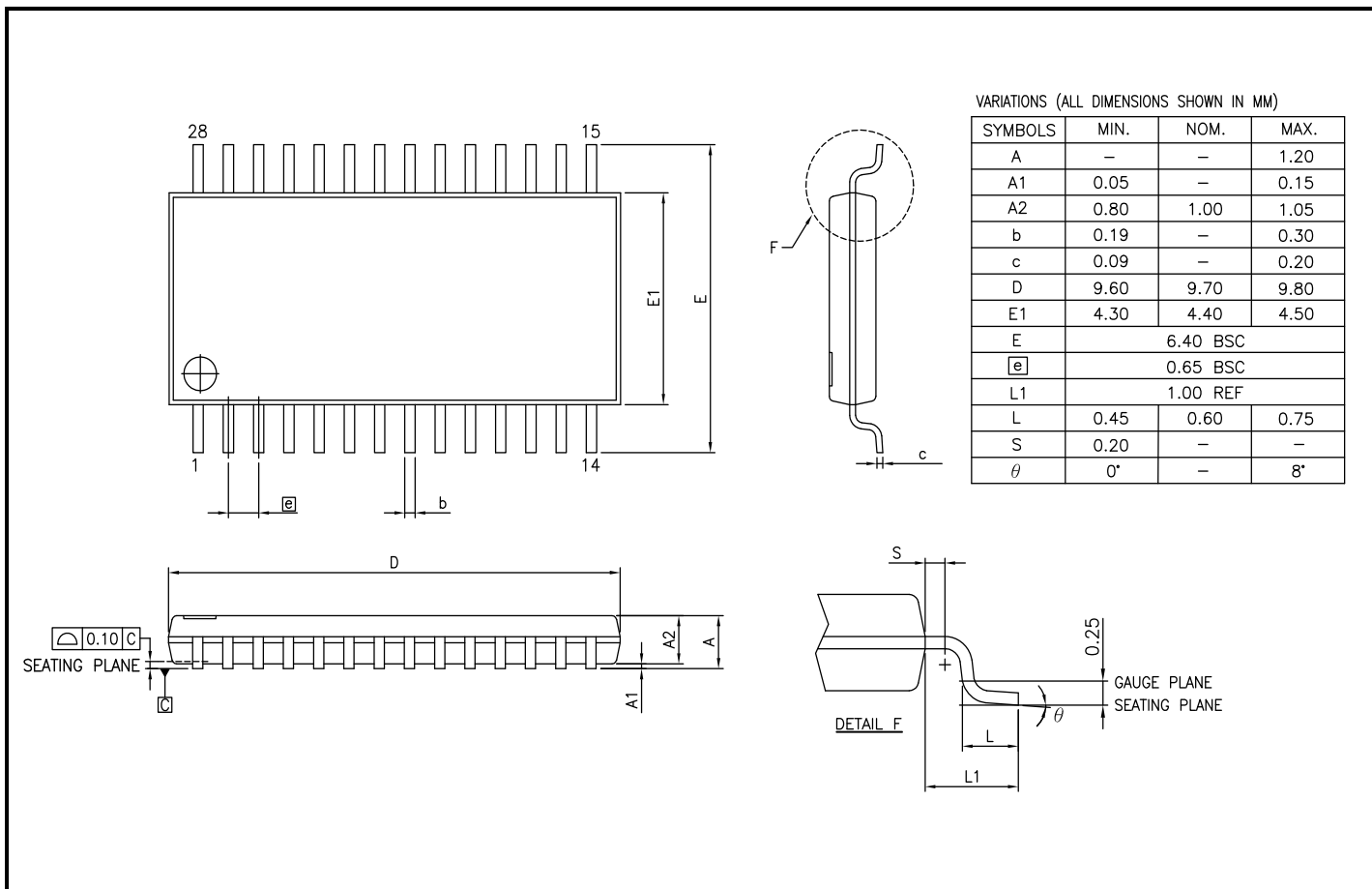
**Notes:**

1. Test configuration is  $R_s = 33.2\Omega$ ,  $R_p = 49.9\Omega$ , and 2pF.
2. Measurement taken from Single Ended waveform.
3. Measurement taken from Differential waveform.
4. Measurement taken using M1 data capture analysis tool.

**Configuration Test Load Board Termination**



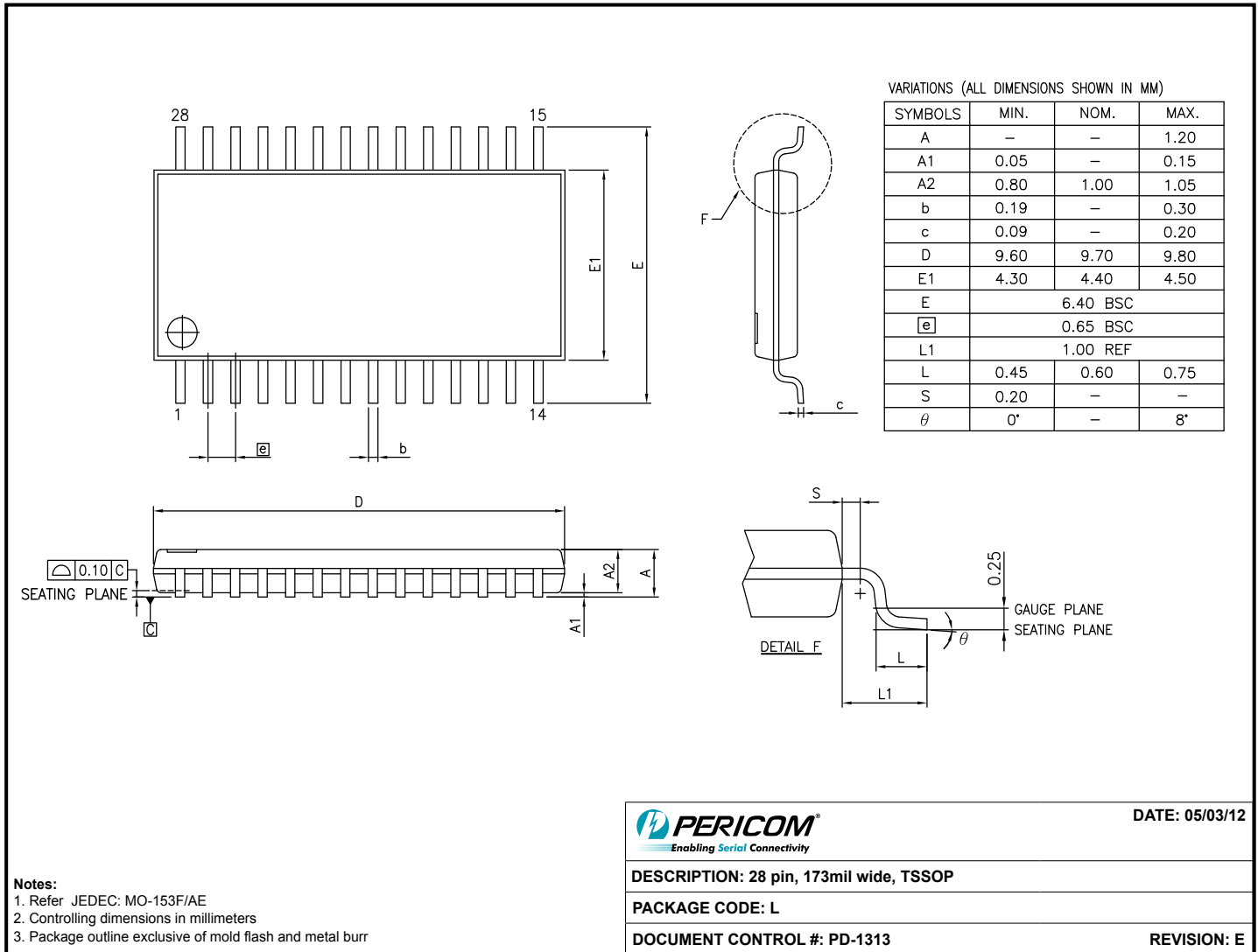




**Notes:**

1. Refer JEDEC: MO-153F/AE
2. Controlling dimensions in millimeters
3. Package outline exclusive of mold flash and metal burr

<p><b>PERICOM</b><sup>®</sup> Enabling Serial Connectivity</p>	DATE: 05/03/12
	DESCRIPTION: 28 pin, 173mil wide, TSSOP
PACKAGE CODE: L	
DOCUMENT CONTROL #: PD-1313	REVISION: E



**Ordering Information<sup>(1-3)</sup>**

Ordering Code	Package Code	Package Description
PI6C20400HE	HE	28-pin, 209-mil wide, SSOP, Pb-Free and Green
PI6C20400LE	LE	28-pin, 173-mil wide, TSSOP, Pb-Free and Green

**Notes:**

1. Thermal characteristics can be found on the company web site at [www.pericom.com/packaging/](http://www.pericom.com/packaging/)
2. E = Pb-free and Green
3. Adding an X suffix = Tape/Reel

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