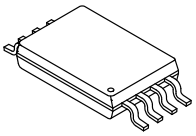
N01S830HA, N01S830BA

1 Mb Ultra-Low Power Serial SRAM

Standard SPI Interface and Multiplex DUAL and QUAD Interface

ON Semiconductor®

http://onsemi.com



TSSOP8 3x4.4
CASE 948BH

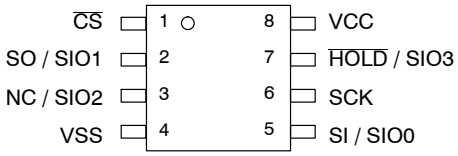
Overview

The ON Semiconductor serial SRAM family includes several integrated memory devices including this 1 Mb serially accessed Static Random Access Memory, internally organized as 128 K words by 8 bits. The devices are designed and fabricated using ON Semiconductor's advanced CMOS technology to provide both high-speed performance and low power. The devices operate with a single chip select ($\overline{CS}$) input and use a simple Serial Peripheral Interface (SPI) protocol. In SPI mode, a single data-in (SI) and data-out (SO) line is used along with the clock (SCK) to access data within the device. In DUAL mode, two multiplexed data-in/data-out (SIO0-SIO1) lines are used and in QUAD mode, four multiplexed data-in/data-out (SIO0-SIO3) lines are used with the clock to access the memory. The devices can operate over a wide temperature range of −40°C to +85°C and are available in a 8-lead TSSOP package. The N01S830xA device has two different variations, a HOLD version that allows communication to the device to be paused and a battery back-up (BBU) version to be used with a battery to retain data when power is lost.

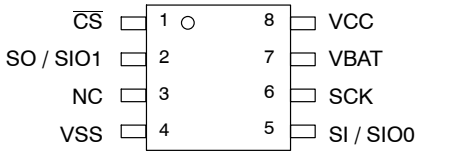
Features

- Power Supply Range: 2.5 to 5.5 V
- Very Low Typical Standby Current < 4 μA
- Very Low Operating Current < 10 mA
- Simple Serial Interface
  - Single-bit SPI Access
  - DUAL-bit and QUAD-bit SPI-like Access
- Flexible Operating Modes
  - Word Mode
  - Page Mode
  - Burst Mode (Full Array)
- High Frequency Read and Write Operation
  - Clock Frequency 20 MHz
- Functional Options
  - HOLD Pin for Pausing Operation
  - VBAT Pin for Battery−Back up
- Built-in Write Protection ($\overline{CS}$ High)
- High Reliability
  - Unlimited Write Cycles
- These Devices are Pb−Free and are RoHS Compliant
  - Green TSSOP

PACKAGE CONFIGURATION



HOLD Version



BBU Version

ORDERING INFORMATION

Device	Package	Shipping†
N01S830HAT22I	TSSOP−8 (Pb−Free)	100 Units / Tube
N01S830BAT22I	TSSOP−8 (Pb−Free)	100 Units / Tube
N01S830HAT22IT	TSSOP−8 (Pb−Free)	3000 / Tape & Reel
N01S830BAT22IT	TSSOP−8 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Table 1. DEVICE OPTIONS

Device / Part Number	Power Supply	Speed	Package	Function
N01S830HAT22I	HV 2.5 V – 5.5 V	20 MHz	TSSOP−8	HOLD
N01S830BAT22I	HV 2.5 V – 5.5 V	20 MHz	TSSOP−8	BBU – Battery Back-up

Table 2. PIN NAMES

Pin Name	Pin Function
$\overline{CS}$	Chip Select
SCK	Serial Clock
SI / SIO0	Data Input – SPI mode Data Input/Output 0 – DUAL and QUAD mode
SO / SIO1	Data Output – SPI mode Data Input/Output 1 – DUAL and QUAD mode
NC / SIO2	No Connect – SPI and DUAL mode Data Input/Output 2 – QUAD mode
$\overline{HOLD}$ / SIO3	HOLD Version HOLD Input – SPI and DUAL mode Data Input/Output 3 – QUAD mode
VBAT	BBU Version Battery Supply – SPI and DUAL mode
V_{CC}	Power
V_{SS}	Ground

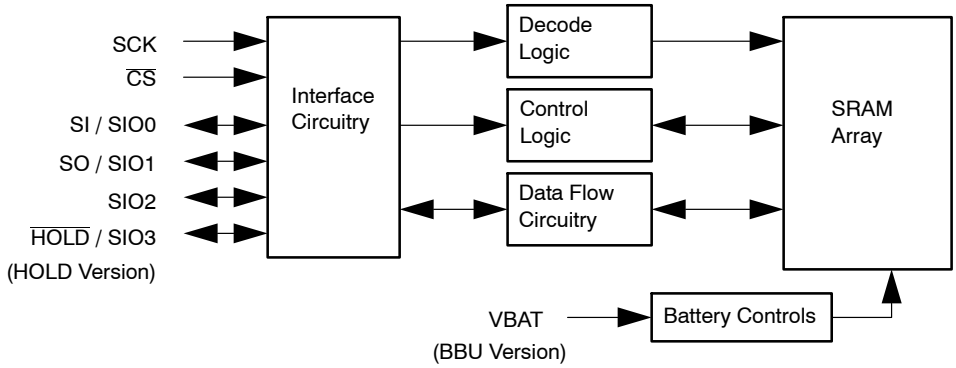


Figure 1. Functional Block Diagram

Table 3. CONTROL SIGNAL DESCRIPTIONS

Signal	Mode Used	Name	Description
$\overline{CS}$	All	Chip Select	A low level selects the device and a high level puts the device in standby mode. If $\overline{CS}$ is brought high during a program cycle, the cycle will complete and then the device will enter standby mode. When $\overline{CS}$ is high, SO is in high-Z. $\overline{CS}$ must be driven low after power-up prior to any sequence being started.
SCK	All	Serial Clock	Synchronizes all activities between the memory and controller. All incoming addresses, data and instructions are latched on the rising edge of SCK. Data out is updated after the falling edge of SCK.
SI	SPI	Serial Data In	Receives instructions, addresses and data on the rising edge of SCK.
SO	SPI	Serial Data Out	Data is transferred out after the falling edge of SCK.
$\overline{HOLD}$	SPI and DUAL	Hold	A high level is required for normal operation. Once the device is selected and a serial sequence is started, this input may be taken low to pause serial communication without resetting the serial sequence. The pin must be brought low while SCK is low for immediate use. If SCK is not low, the HOLD function will not be invoked until the next SCK high to low transition. The device must remain selected during this sequence. SO is high-Z during the Hold time and SI and SCK are inputs are ignored. To resume operations, $\overline{HOLD}$ must be pulled high while the SCK pin is low. Lowering the $\overline{HOLD}$ input at any time will take to SO output to High-Z.
VBAT	SPI and DUAL	Battery Voltage	Provides the battery power connection to retain data in battery backed mode.

Table 3. CONTROL SIGNAL DESCRIPTIONS

Signal	Mode Used	Name	Description
SIO0 - 1	DUAL	Serial Data Input / Output	Receives instructions, addresses and data on the rising edge of SCK. Data is transferred out after the falling edge of SCK. The instruction must be set after power-up to enable the DUAL access mode.
SIO0 - 3	QUAD	Serial Data Input / Output	Receives instructions, addresses and data on the rising edge of SCK. Data is transferred out after the falling edge of SCK. The instruction must be set after power-up to enable the QUAD access mode.

Basic Operation

The 1 Mb serial SRAM is designed to interface directly with a standard Serial Peripheral Interface (SPI) common on many standard micro-controllers in the default state. It may also interface with other non-SPI ports by programming discrete I/O lines to operate the device.

The serial SRAM contains an 8-bit instruction register and is accessed via the SI pin. The $\overline{CS}$ pin must be low and the $\overline{HOLD}$ pin must be high for the entire operation. Data is sampled on the first rising edge of SCK after $\overline{CS}$ goes low. If the clock line is shared, the user can assert the $\overline{HOLD}$ input and place the device into a Hold mode. After releasing the $\overline{HOLD}$ pin, the operation will resume from the point where it was held. The Hold operation is only supported in SPI and DUAL modes.

By programming the device through a command instruction, the dual and quad access modes may be initiated. In these modes, multiplexed I/O lines take the place of the SPI SI and SO pins and along with the $\overline{CS}$ and SCK control the device in a SPI-like, two bit (DUAL) and four bit (QUAD) wide serial manner. Once the device is put into either the DUAL or QUAD mode, the device will remain operating in that mode until powered down or the Reset Mode operation is programmed.

The following table contains the possible instructions and formats. All instructions, addresses and data are transferred MSB first and LSB last.

Table 4. INSTRUCTION SET

Instruction	Command	Description
READ	03h	Read data from memory starting at selected address
WRITE	02h	Write (program) data to memory starting at selected address
EQIO	38h	Enable QUAD I/O access
EDIO	3Bh	Enable DUAL I/O access
RSTQIO	FFh	Reset from QUAD and DUAL to SPI I/O access
RDMR	05h	Read mode register
WRMR	01h	Write mode register

DEVICE OPERATIONS

Read Operation

The serial SRAM Read operation is started by by enabling $\overline{CS}$ low. First, the 8-bit Read instruction is transmitted to the device through the SI (or SIO0-3) pin(s) followed by the 24-bit address with the 7 MSBs of the address being “don’t care” bits and ignored. In SPI mode, after the READ instruction and address bits are sent, the data stored at that address in memory is shifted out on the SO pin after the output valid time. Additional “dummy” clock cycles (four in DUAL and two in QUAD) are required to follow the instruction and address inputs prior to the data being driven out on the SIO0-3 pins while operating in these two modes.

By continuing to provide clock cycles to the device, data can continue to be read out of the memory array in sequentially. The internal address pointer is automatically incremented to the next higher address after each byte of data is read out until the highest memory address is reached. When the highest memory address is reached, 1FFFFh, the address pointer wraps to the address 00000h. This allows the read cycles to be continued indefinitely. All Read operations are terminated by pulling $\overline{CS}$ high.

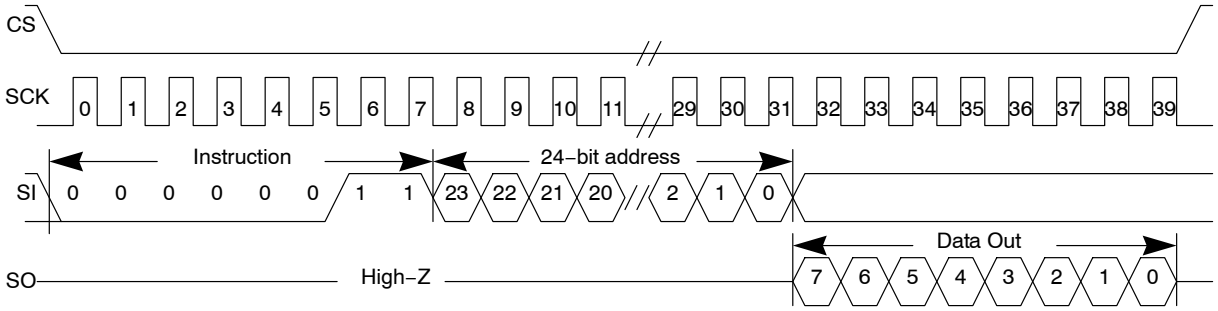


Figure 2. SPI Read Sequence (Single Byte)

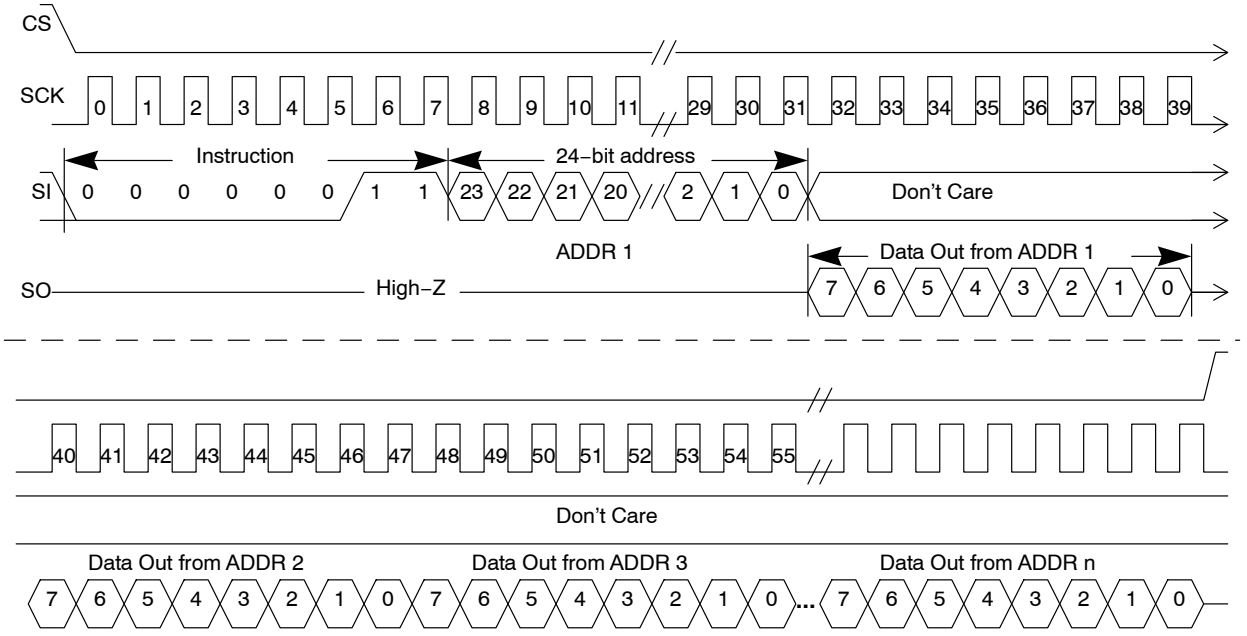
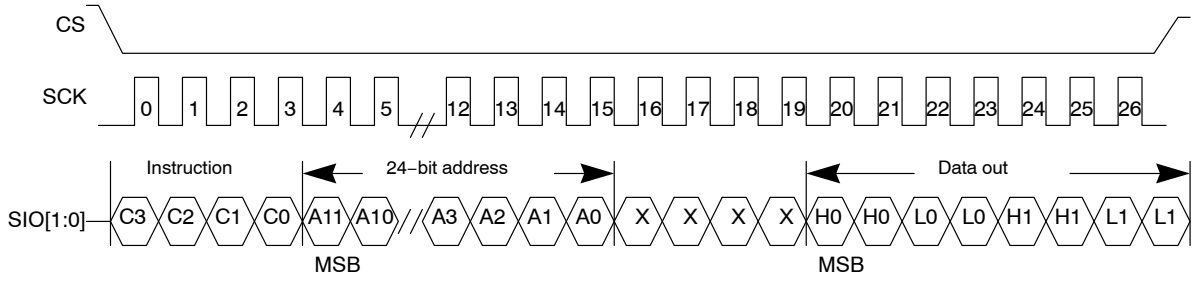
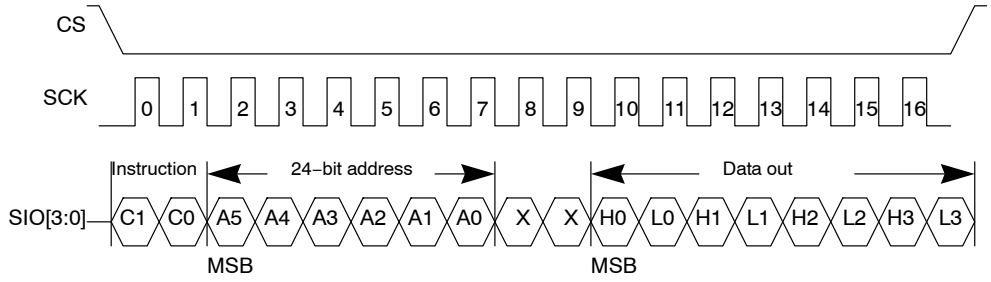


Figure 3. SPI Read Sequence (Sequential Bytes)



Notes: C[3:0] = 03h
H0 = 2 high order bits of data byte 0
L0 = 2 low order bits of data byte 0
H1 = 2 high order bits of data byte 1
L1 = 2 low order bits of data byte 1

Figure 4. DUAL Read Sequence



Notes: C[1:0] = 03h
H0 = 4 high order bits of data byte 0
L0 = 4 low order bits of data byte 0
H1 = 4 high order bits of data byte 1
L1 = 4 low order bits of data byte 1

Figure 5. QUAD Read Sequence

Write Operation

The serial SRAM WRITE is selected by enabling $\overline{CS}$ low. First, the 8-bit WRITE instruction is transmitted to the device followed by the 24-bit address with the 7 MSBs being don't care. After the WRITE instruction and addresses are sent, the data to be stored in memory is shifted in on the SI pin.

If operating in page mode, after the initial word of data is shifted in, additional data words can be written as long as the address requested is sequential on the same page. Simply write the data on SI pin and continue to provide clock pulses. The internal address pointer is automatically incremented to the next higher address on the page after each word of data is written in. This can be continued for the entire page length of 32 words long. At the end of the page, the addresses pointer will be wrapped to the 0 word address within the page and the operation can be continuously looped over the 32 words of the same page. The new data will replace data already stored in the memory locations.

If operating in burst mode, after the initial word of data is shifted in, additional data words can be written to the next sequential memory locations by continuing to provide clock pulses. The internal address pointer is automatically incremented to the next higher address after each word of data is read out. This can be continued for the entire array and when the highest address is reached, 1FFFFh, the address counter wraps to the address 00000h. This allows the burst write cycle to be continued indefinitely. Again, the new data will replace data already stored in the memory locations.

All WRITE operations are terminated by pulling $\overline{CS}$ high.

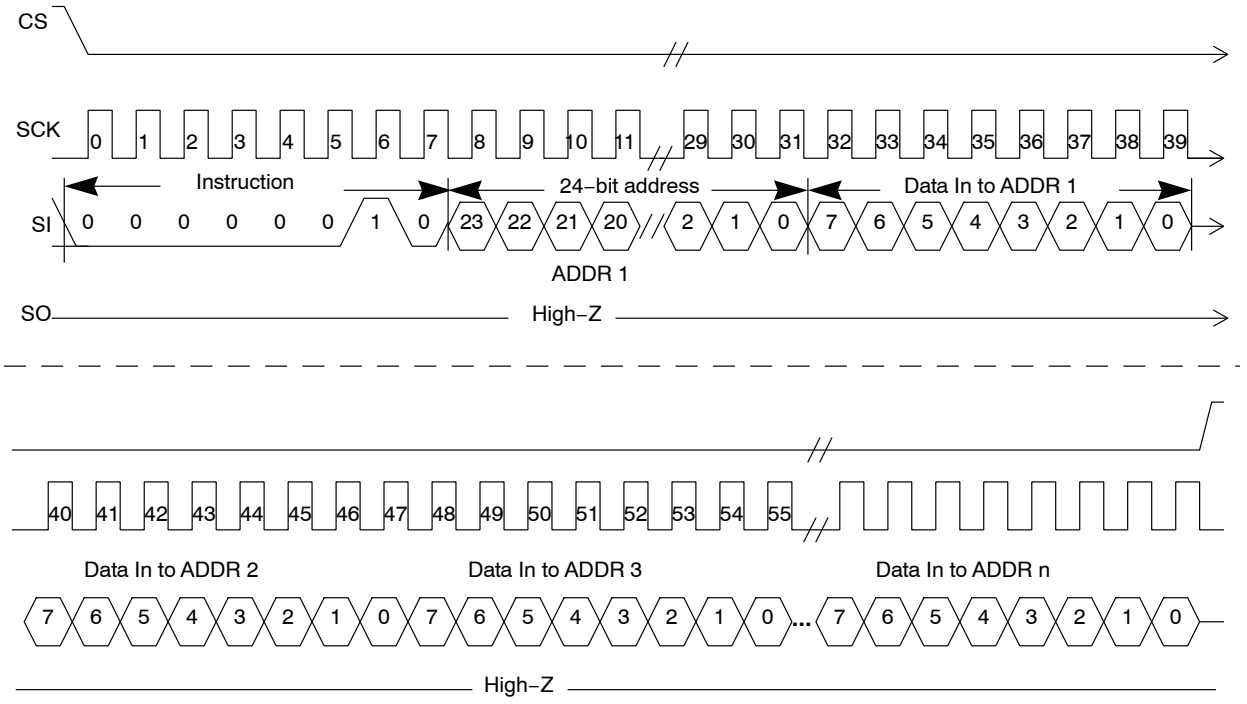
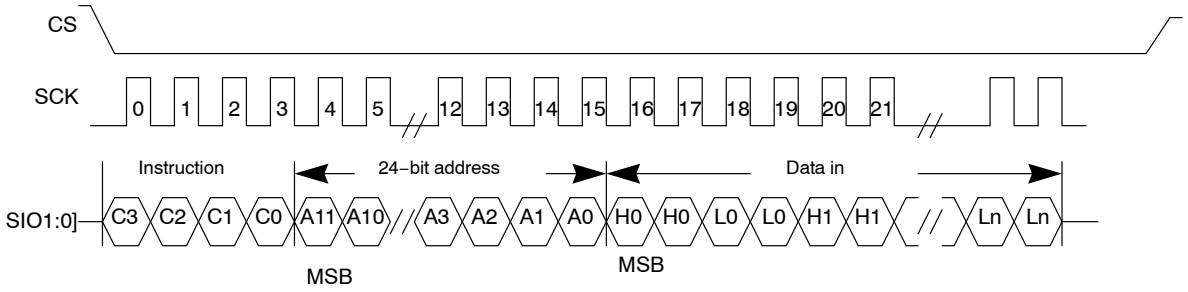
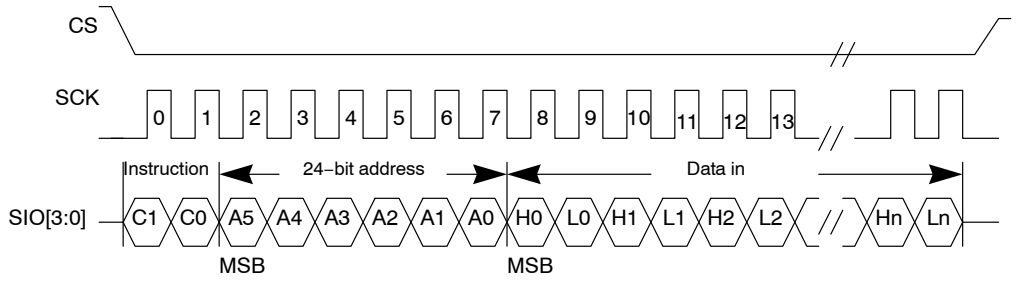


Figure 6. SPI Write Sequence



Notes: C[3:0] = 02h
H0 = 2 high order bits of data byte 0
L0 = 2 low order bits of data byte 0
H1 = 2 high order bits of data byte 1
L1 = 2 low order bits of data byte 1

Figure 7. DUAL Write Sequence



Notes: C[1:0] = 02h
H0 = 4 high order bits of data byte 0
L0 = 4 low order bits of data byte 0
H1 = 4 high order bits of data byte 1
L1 = 4 low order bits of data byte 1

Figure 8. QUAD Write Sequence

READ Mode Register (RDMR)

This instruction provides the ability to read the mode register. The register may be read at any time including during a Write operation. The Read Mode Register operation is executed by driving $\overline{CS}$ low, then sending the RDMR instruction to the device. Immediately after the instruction, the device outputs data on the SO (SIO0-3) pin(s). To complete the operation, drive $\overline{CS}$ high to terminate the register read.

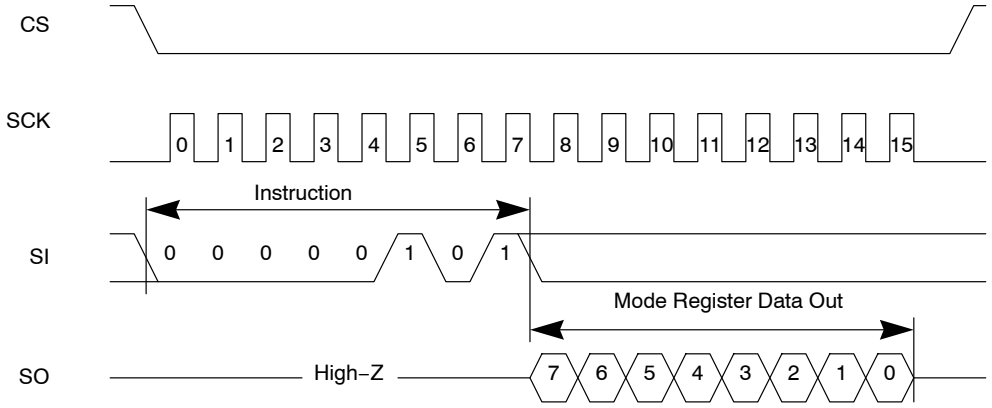
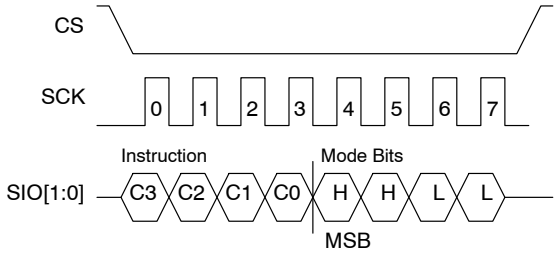
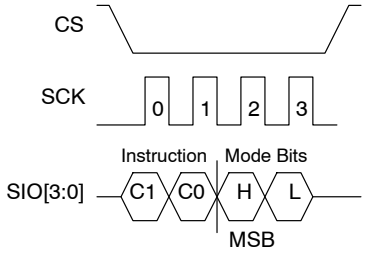


Figure 9. SPI Read Mode Register Sequence (RDMR)



Notes: C[3:0] = 05h

Figure 10. DUAL Read Mode Register Sequence (RDMR)



Notes: C[1:0] = 05h

Figure 11. QUAD Read Mode Register Sequence (RDMR)

Write Mode Register (WRMR)

This instruction provides the ability to write the mode register. The Write Mode Register operation is executed by driving $\overline{CS}$ low, then sending the WRMR instruction to the device. Immediately after the instruction, the data is driven to the device on the SO (SIO0-3) pin(s). To complete the operation, drive $\overline{CS}$ high to terminate the register write.

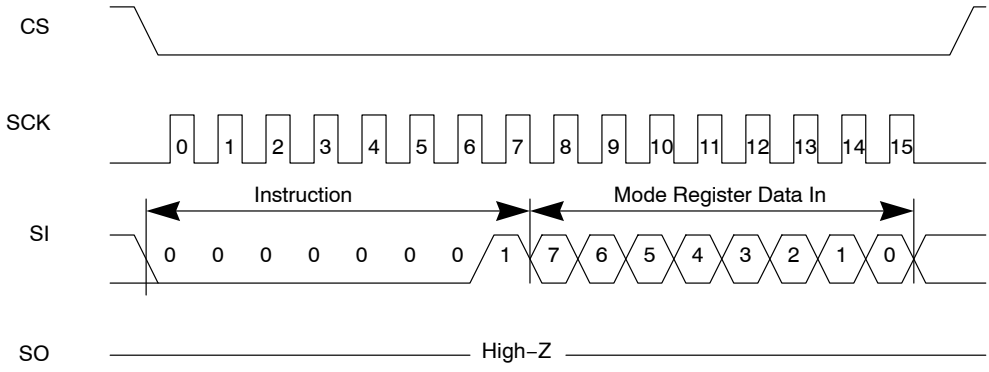
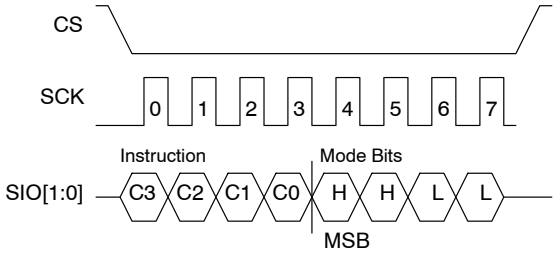
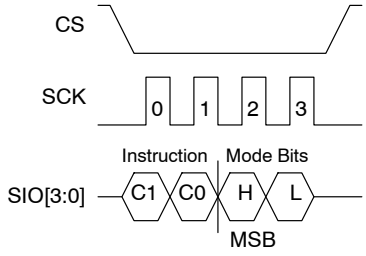


Figure 12. SPI Write Mode Register Sequence



Notes: C[3:0] = 01h

Figure 13. DUAL Write Mode Register Sequence



Notes: C[1:0] = 01h

Figure 14. QUAD Write Mode Register Sequence

Table 5. MODE REGISTER

Bit	Function
0	Hold Function 1 = Hold function disabled 0 = Hold function enabled (Default)
1	Reserved
2	Reserved
3	Reserved
4	Reserved
5	Reserved
6	Operating Mode Bit 7 Bit 6 0 0 = Word Mode 1 0 = Page Mode
7	0 1 = Burst Mode (Default) 1 1 = Reserved

Power-Up State

The serial SRAM enters a know state at power-up time. The device is in low-power standby state with $\overline{CS}$ = 1. A low level on $\overline{CS}$ is required to enter a active state.

Battery Back-Up Operation

The Battery Back-Up function is available on the BBU version of the serial SRAM. This version of the SRAM cannot operate in the QUAD mode since the SIO3 input is used for the VBAT connection. A standard coin cell battery should be connected to the VBAT pin. On chip circuitry monitors the V_{CC} pin and when it is determined that the main V_{CC} power supply is turning off, the device automatically switches the memory array to VBAT power input. When in battery back-up mode and 3.0 to 3.4 V power supplied to the VBAT input, memory data is retained in the SRAM array and all existing interface and operating mode information is retained.

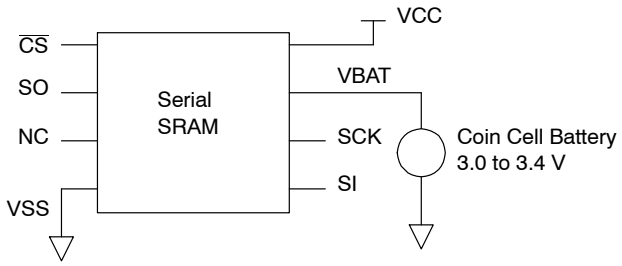


Figure 15. Battery Back-Up Version Schematics

Table 6. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	$V_{IN,OUT}$	–0.3 to V_{CC} + 0.3	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	–0.3 to 5.5	V
Power Dissipation	P_D	500	mW
Storage Temperature	T_{STG}	–40 to 125	°C
Operating Temperature	T_A	-40 to +85	°C
Soldering Temperature and Time	T_{SOLDER}	260°C, 10 sec	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 7. OPERATING CHARACTERISTICS (OVER SPECIFIED TEMPERATURE RANGE)

Item	Symbol	Test Conditions	Min	Typ (Note 1)	Max	Units
Supply Voltage	V_{CC}		2.5		5.5	V
Data Retention Voltage (Note 2)	V_{DR}			1.0		V
Input High Voltage	V_{IH}		0.7 V_{CC}		V_{CC} + 0.3	V
Input Low Voltage	V_{IL}		–0.3		0.1 V_{CC}	V
Output High Voltage	V_{OH}	I_{OH} = –0.4 mA	V_{CC} – 0.2			V
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.2	V
Input Leakage Current	I_{LI}	$\overline{CS}$ = V_{CC}, V_{IN} = 0 to V_{CC}			1.0	μA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{CC}, V_{OUT} = 0 to V_{CC}			1.0	μA
Operating Current	I_{CC}	f = 20 MHz, I_{OUT} = 0, SPI / DUAL			10	mA
		f = 20 MHz, I_{OUT} = 0, QUAD			20	
Standby Current	I_{SB}	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}		4	10	μA

1. Typical values are measured at V_{CC} = V_{CC} Typ., T_A = 25°C and are not 100% tested.
2. Typical lower limit of VCC when data will be retained in the memory array, not 100% tested.

Table 8. CAPACITANCE (Note 3)

Item	Symbol	Test Conditions	Min	Max	Units
Input Capacitance	C_{IN}	V_{IN} = 0 V, f = 1 MHz, T_A = 25°C		7	pF
I/O Capacitance	$C_{I/O}$	V_{IN} = 0 V, f = 1 MHz, T_A = 25°C		7	pF

3. These parameters are verified in device characterization and are not 100% tested.

Table 9. TIMING TEST CONDITIONS

Item	Value
Input Pulse Level	0.1 V_{CC} to 0.9 V_{CC}
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Levels	0.5 V_{CC}
Output Load	CL = 30 pF
Operating Temperature	−40 to +85°C

Table 10. TIMING

Item	Symbol	Min	Max	Units
Clock Frequency	f_{CLK}		20	MHz
Clock Period	t_{CLK}	50		ns
Clock Rise Time	t_R		20	ns
Clock Fall Time	t_F		20	ns
Clock High Time	t_{HI}	25		ns
Clock Low Time	t_{LO}	25		ns
Clock Delay Time	t_{CLD}	25		ns
$\overline{CS}$ Setup Time	t_{CSS}	25		ns
$\overline{CS}$ Hold Time	t_{CSH}	50		ns
$\overline{CS}$ Disable Time	t_{CSD}	25		ns
SCK to $\overline{CS}$	t_{SCS}	5		ns
Data Setup Time	t_{SU}	10		ns
Data Hold Time	t_{HD}	10		ns
Output Valid From Clock Low	t_V		25	ns
Output Hold Time	t_{HO}	0		ns
Output Disable Time	t_{DIS}		20	ns
$\overline{HOLD}$ Setup Time	t_{HS}	10		ns
$\overline{HOLD}$ Hold Time	t_{HH}	10		ns
$\overline{HOLD}$ Low to Output High-Z	t_{HZ}	10		ns
$\overline{HOLD}$ High to Output Valid	t_{HV}		50	ns

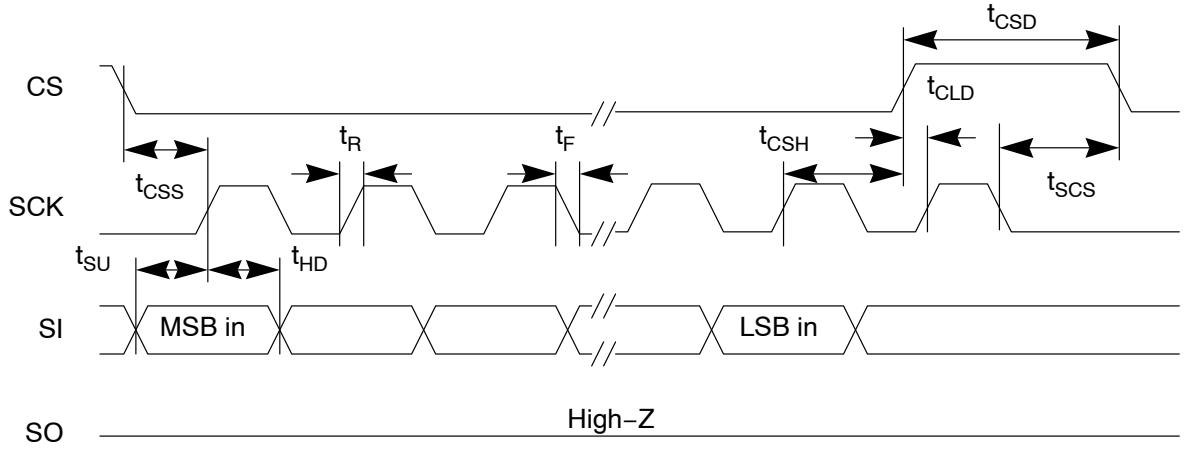


Figure 16. SPI Input Timing

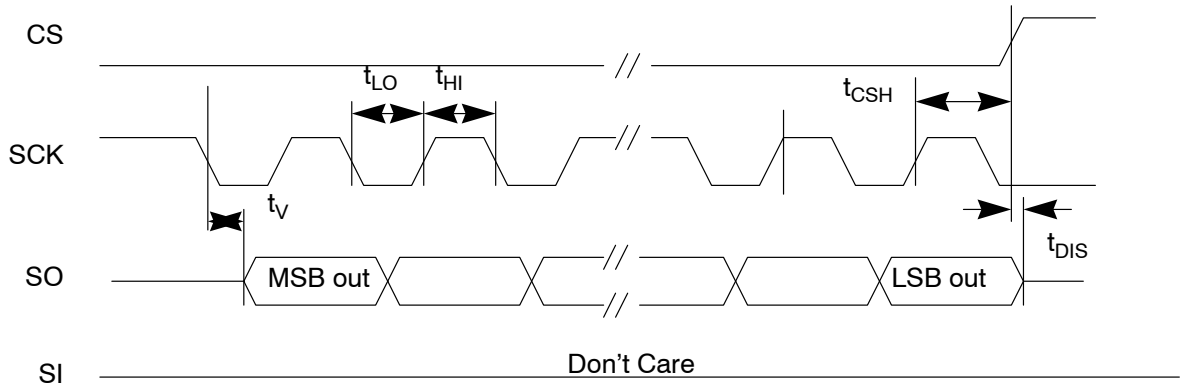


Figure 17. SPI Output Timing

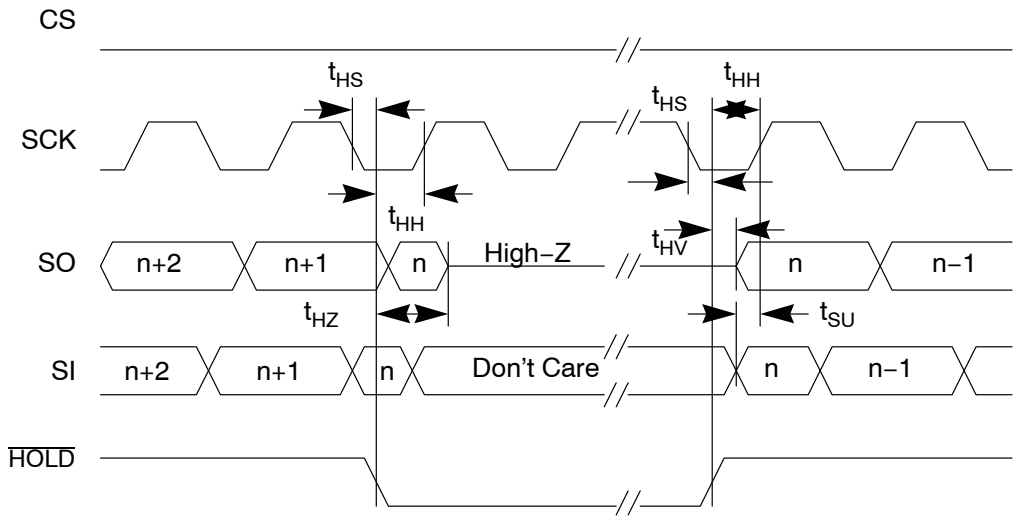


Figure 18. SPI Hold Timing

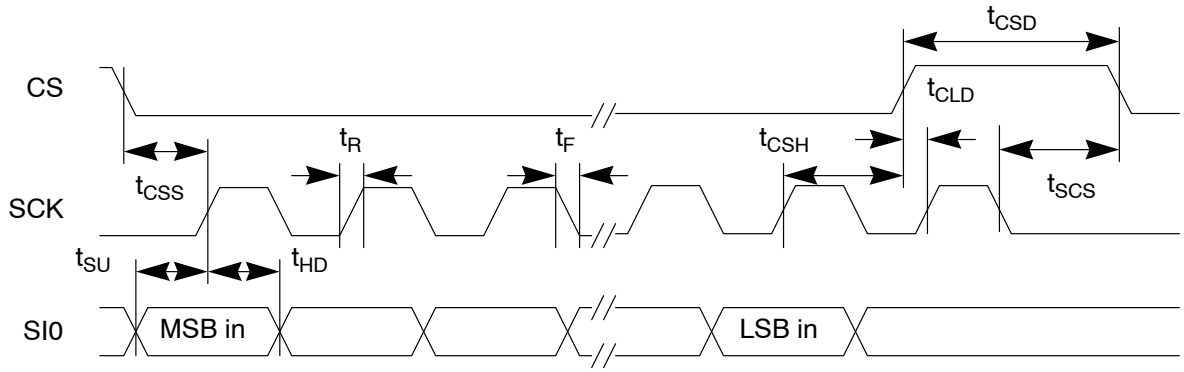


Figure 19. QUAD Input Timing

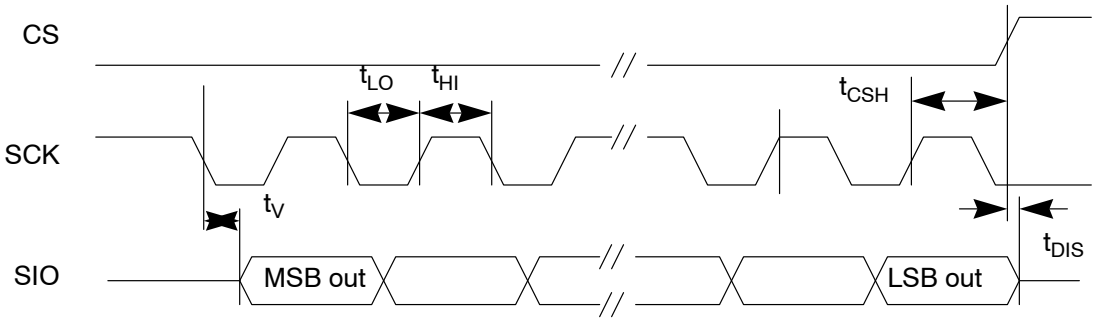
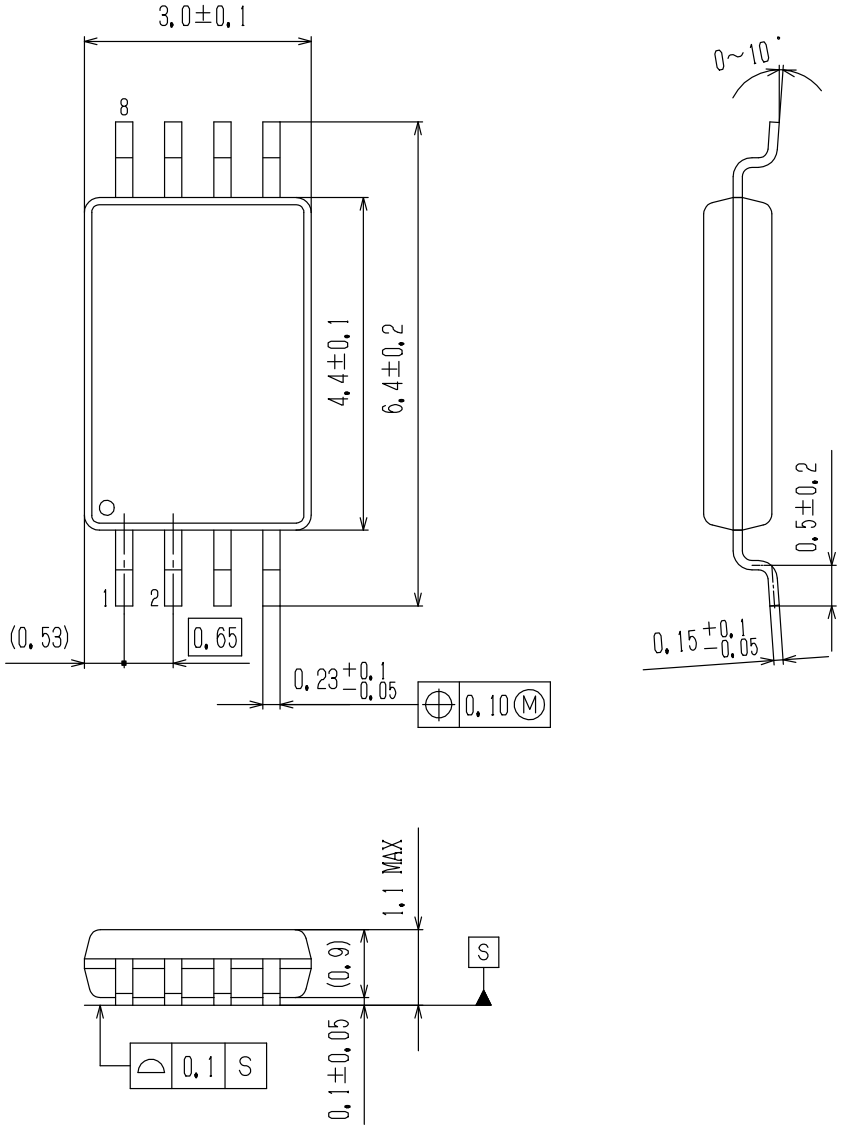


Figure 20. QUAD Output Timing

PACKAGE DIMENSIONS

TSSOP8 3x4.4 / TSSOP8 (225 mil)
CASE 948BH
ISSUE O



PUBLICATION ORDERING INFORMATION

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