Features

- High Performance, Low Power Atmel® AVR® 8-bit Microcontroller
- Advanced RISC Architecture
  - 129 Powerful Instructions - Most Single Clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 1 MIPS throughput per MHz
  - On-chip 2-cycle Multiplier
- Data and Non-Volatile Program Memory
  - 8K Bytes Flash of In-System Programmable Program Memory
    - Endurance: 10,000 Write/Erase Cycles
  - Optional Boot Code Section with Independent Lock Bits
- In-System Programming by On-chip Boot Program
- True Read-While-Write Operation
  - 512 Bytes of In-System Programmable EEPROM
- Endurance: 100,000 Write/Erase Cycles
  - 512 Bytes Internal SRAM
  - Programming Lock for Flash Program and EEPROM Data Security
- On Chip Debug Interface (debugWIRE)
- Peripheral Features
  - Two or three 12-bit High Speed PSC (Power Stage Controllers) with 4-bit Resolution Enhancement
    - Non Overlapping Inverted PWM Output Pins With Flexible Dead-Time
    - Variable PWM duty Cycle and Frequency
    - Synchronous Update of all PWM Registers
    - Auto Stop Function for Event Driven PFC Implementation
    - Less than 25 Hz Step Width at 150 kHz Output Frequency
    - PSC2 with four Output Pins and Output Matrix
  - One 8-bit General purpose Timer/Counter with Separate Prescaler and Capture Mode
  - One 16-bit General purpose Timer/Counter with Separate Prescaler, Compare Mode and Capture Mode
  - Programmable Serial USART
    - Standard UART mode
    - 16/17 bit Biphase Mode for DALI Communications
  - Master/Slave SPI Serial Interface
  - 10-bit ADC
    - Up To 11 Single Ended Channels and 2 Fully Differential ADC Channel Pairs
    - Programmable Gain (5x, 10x, 20x, 40x on Differential Channels)
    - Internal Reference Voltage
  - 10-bit DAC
  - Two or three Analog Comparator with Resistor-Array to Adjust Comparison Voltage
  - 4 External Interrupts
  - Programmable Watchdog Timer with Separate On-Chip Oscillator
- Special Microcontroller Features
  - Low Power Idle, Noise Reduction, and Power Down Modes
  - Power On Reset and Programmable Brown Out Detection
  - Flag Array in Bit-programmable I/O Space (4 bytes)

Atmel

8-bit Atmel Microcontroller with 8K Bytes In-System Programmable Flash

AT90PWM2
AT90PWM3

AT90PWM2B
AT90PWM3B

Summary

4317KS–AVR–03/2013

  - **In-System Programmable via SPI Port**
  - **Internal Calibrated RC Oscillator (8 MHz)**
  - **On-chip PLL for fast PWM (32 MHz, 64 MHz) and CPU (16 MHz)**
- **Operating Voltage: 2.7V - 5.5V**
- **Extended Operating Temperature:**
  - **-40°C to +105°C**

Product	Package	12 bit PWM with deadtime	ADC Input	ADC Diff	Analog Compar	Application
AT90PWM2 AT90PWM2B	SO24	2 x 2	8	1	2	One fluorescent ballast
AT90PWM3 AT90PWM3B	SO32, QFN32	3 x 2	11	2	3	HID ballast, fluorescent ballast, Motor control

1. History

Product	Revision
AT90PWM2 AT90PWM3	First revision of parts, only for running production.
AT90PWM2B AT90PWM3B	Second revision of parts, for all new developments. The major changes are : • complement the PSCOUT01, PSCOUT11, PSCOUT21 polarity in centered mode - See “PSCn0 & PSCn1 Basic Waveforms in Center Aligned Mode” on page 140. • Add the PSC software triggering capture - See “PSC 0 Input Capture Register – PICR0H and PICR0L” on page 171. • Add bits to read the PSC output activity - See “PSC0 Interrupt Flag Register – PIFR0” on page 173. • Add some clock configurations - See “Device Clocking Options Select AT90PWM2B/3B” on page 31. • Change Amplifier Synchonization - See “Amplifier” on page 252. and See “” on page 254. • Correction of the Errata - See “Errata” on page 351.

This datasheet deals with product characteristics of AT90PW2 and AT90WM3. It will be updated as soon as characterization will be done.

2. Disclaimer

Typical values contained in this datasheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology. Min and Max values will be available after the device is characterized.

3. Pin Configurations

Figure 3-1. SOIC 24-pin Package

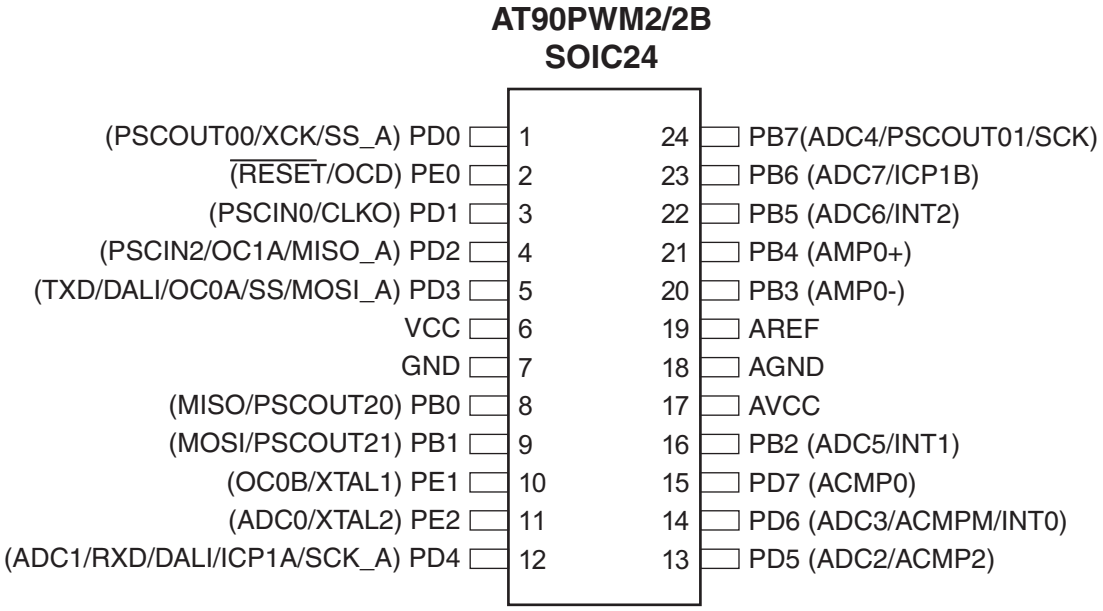


Figure 3-2. SOIC 32-pin Package

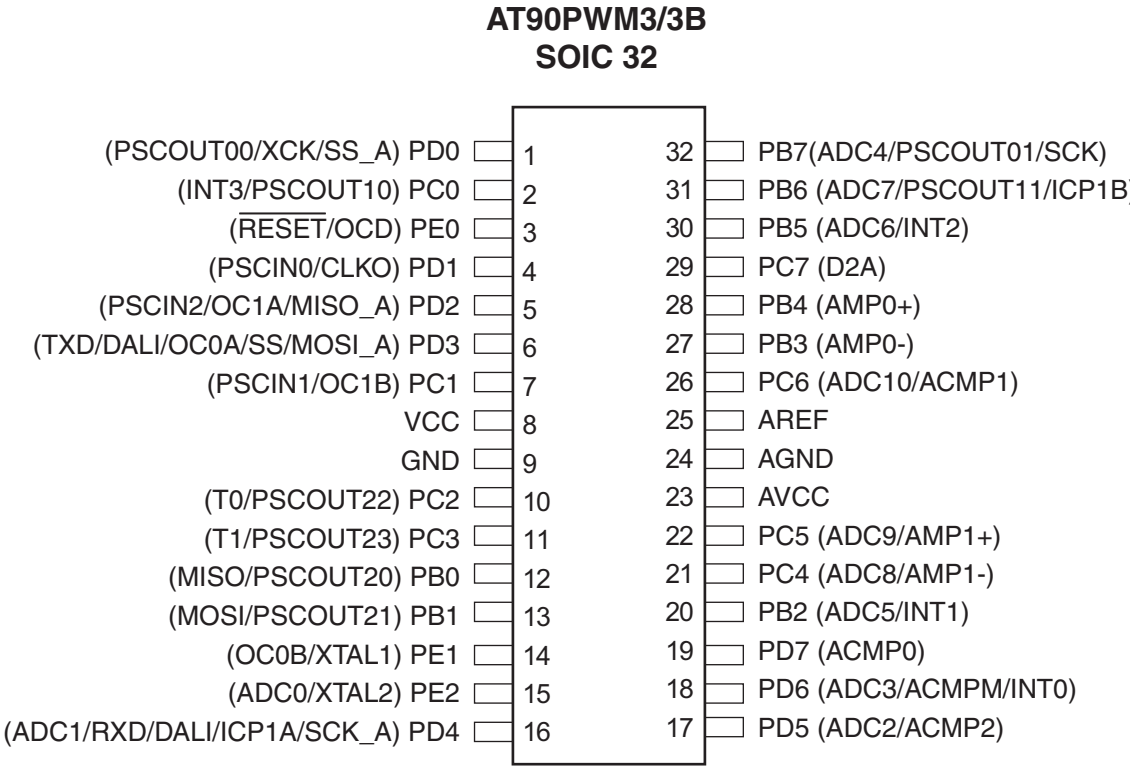
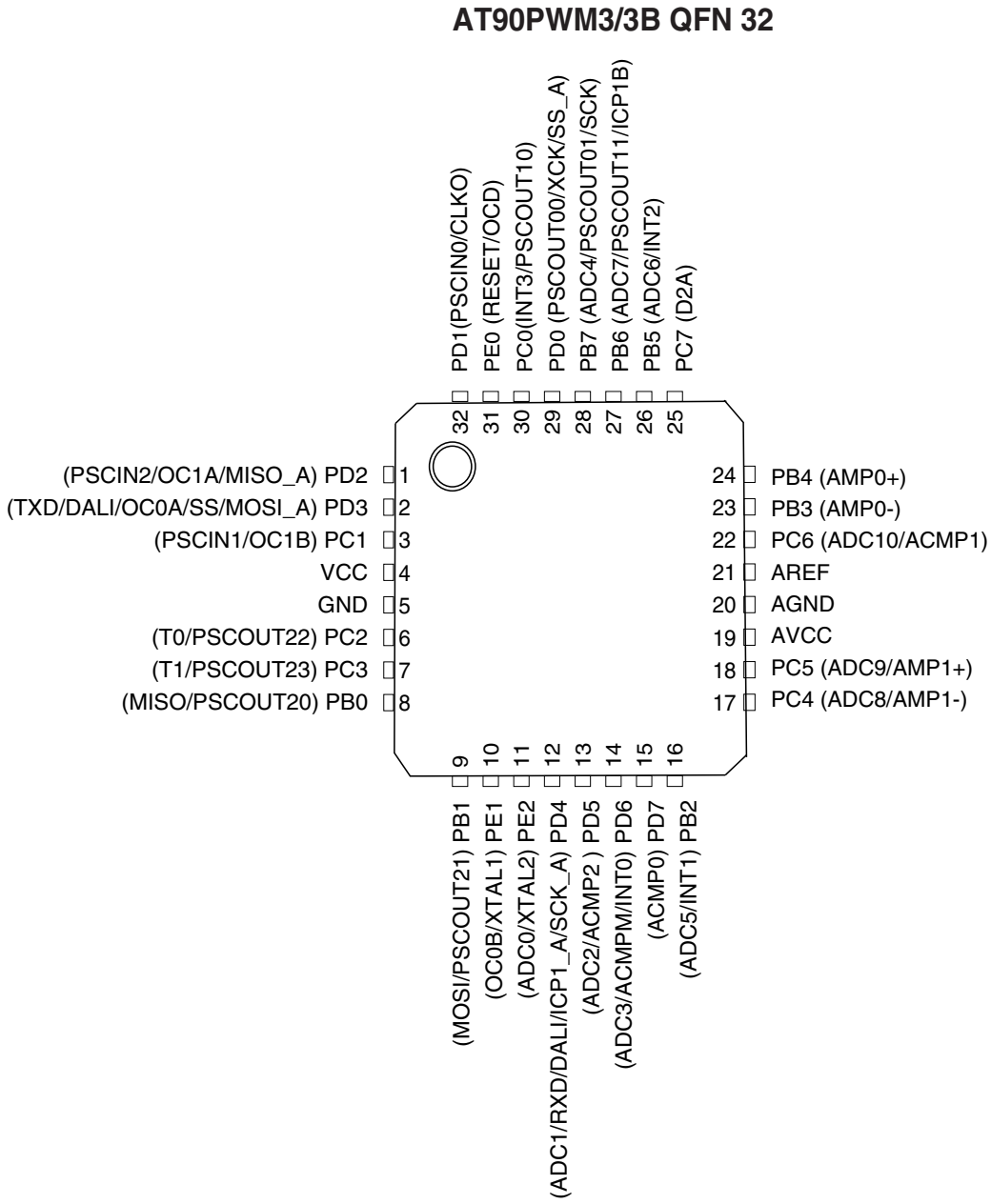


Figure 3-3. QFN32 (7*7 mm) Package.



Note: The Center GND PADDLE has to be connected to GND.

3.1 Pin Descriptions

Table 3-1. Pin out description

S024 Pin Number	SO32 Pin Number	QFN32 Pin Number	Mnemonic	Type	Name, Function & Alternate Function
7	9	5	GND	Power	**Ground:** 0V reference
18	24	20	AGND	Power	**Analog Ground:** 0V reference for analog part
6	8	4	VCC	power	**Power Supply:**
17	23	19	AVCC	Power	**Analog Power Supply:** This is the power supply voltage for analog part For a normal use this pin must be connected.
19	25	21	AREF	Power	**Analog Reference :** reference for analog converter . This is the reference voltage of the A/D converter. As output, can be used by external analog
8	12	8	PBO	I/O	MISO (SPI Master In Slave Out) PSCOUT20 output
9	13	9	PB1	I/O	MOSI (SPI Master Out Slave In) PSCOUT21 output
16	20	16	PB2	I/O	ADC5 (Analog Input Channel5) INT1
20	27	23	PB3	I/O	AMP0- (Analog Differential Amplifier 0 Input Channel)
21	28	24	PB4	I/O	AMP0+ (Analog Differential Amplifier 0 Input Channel)
22	30	26	PB5	I/O	ADC6 (Analog Input Channel 6) INT 2
23	31	27	PB6	I/O	ADC7 (Analog Input Channel 7) ICP1B (Timer 1 input capture alternate input) PSCOUT11 output (see note 1)
24	32	28	PB7	I/O	PSCOUT01 output ADC4 (Analog Input Channel 4) SCK (SPI Clock)

Table 3-1. Pin out description (Continued)

S024 Pin Number	SO32 Pin Number	QFN32 Pin Number	Mnemonic	Type	Name, Function & Alternate Function
NA	2	30	PC0	I/O	PSCOUT10 output (see note 1) INT3
	7	3	PC1	I/O	PSCIN1 (PSC 1 Digital Input) OC1B (Timer 1 Output Compare B)
	10	6	PC2	I/O	T0 (Timer 0 clock input) PSCOUT22 output
	11	7	PC3	I/O	T1 (Timer 1 clock input) PSCOUT23 output
	21	17	PC4	I/O	ADC8 (Analog Input Channel 8) AMP1- (Analog Differential Amplifier 1 Input Channel)
	22	18	PC5	I/O	ADC9 (Analog Input Channel 9) AMP1+ (Analog Differential Amplifier 1 Input Channel)
	26	22	PC6	I/O	ADC10 (Analog Input Channel 10) ACMP1 (Analog Comparator 1 Positive Input)
	29	25	PC7	I/O	D2A : DAC output
1	1	29	PD0	I/O	PSCOUT00 output XCK (UART Transfer Clock) SS_A (Alternate SPI Slave Select)
3	4	32	PD1	I/O	PSCIN0 (PSC 0 Digital Input) CLKO (System Clock Output)
4	5	1	PD2	I/O	PSCIN2 (PSC 2 Digital Input) OC1A (Timer 1 Output Compare A) MISO_A (Programming & alternate SPI Master In Slave Out)
5	6	2	PD3	I/O	TXD (Dali/UART Tx data) OC0A (Timer 0 Output Compare A) SS (SPI Slave Select) MOSI_A (Programming & alternate Master Out SPI Slave In)
12	16	12	PD4	I/O	ADC1 (Analog Input Channel 1) RXD (Dali/UART Rx data) ICP1A (Timer 1 input capture) SCK_A (Programming & alternate SPI Clock)
13	17	13	PD5	I/O	ADC2 (Analog Input Channel 2) ACMP2 (Analog Comparator 2 Positive Input)
14	18	14	PD6	I/O	ADC3 (Analog Input Channel 3) ACMPM reference for analog comparators INT0
15	19	15	PD7	I/O	ACMP0 (Analog Comparator 0 Positive Input)
2	3	31	PE0	I/O or I	RESET (Reset Input) OCD (On Chip Debug I/O)
10	14	10	PE1	I/O	XTAL1: XTAL Input OC0B (Timer 0 Output Compare B)

Table 3-1. Pin out description (Continued)

S024 Pin Number	SO32 Pin Number	QFN32 Pin Number	Mnemonic	Type	Name, Function & Alternate Function
11	15	11	PE2	I/O	XTAL2: XTAL OuTput ADC0 (Analog Input Channel 0)

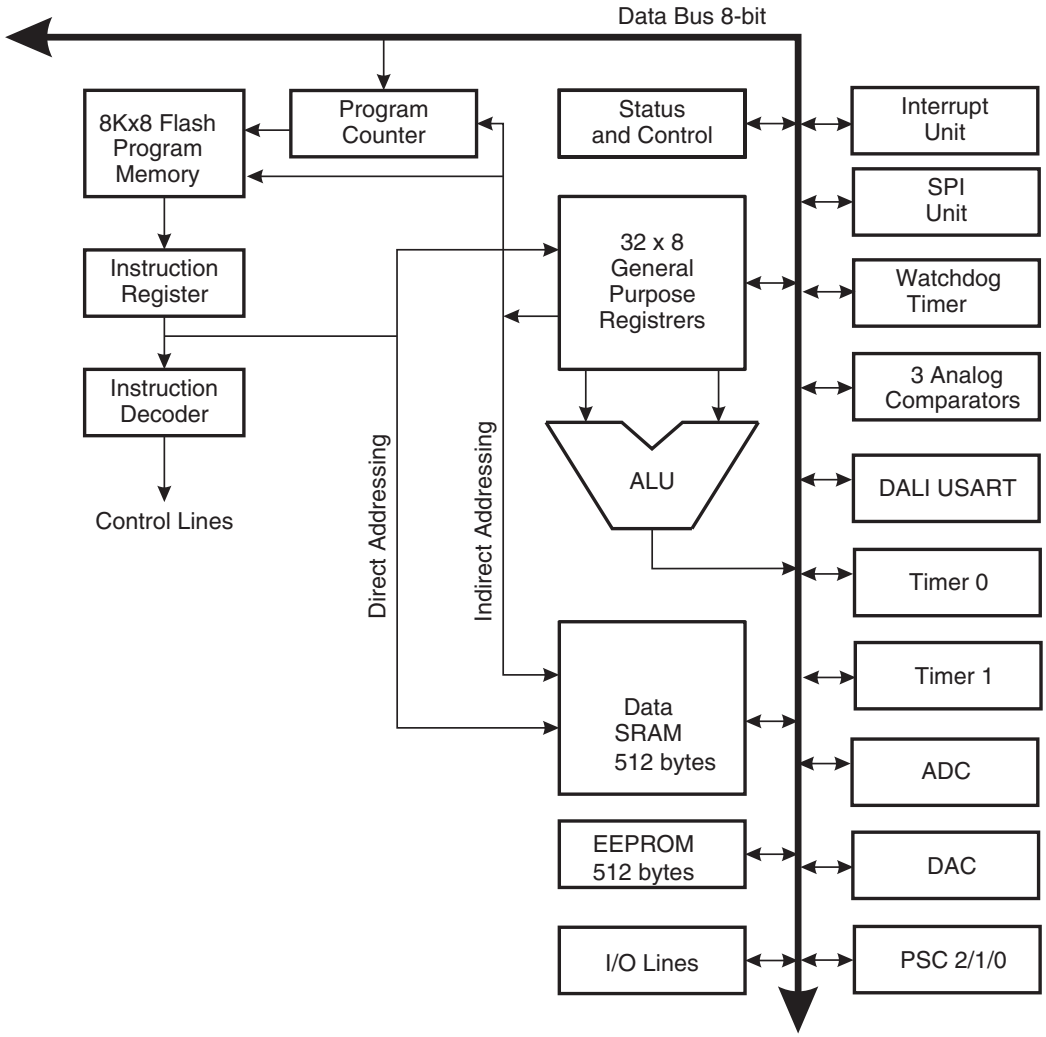
1. PSCOUT10 & PSCOUT11 are not present on 24 pins package

4. Overview

The AT90PWM2/2B/3/3B is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the AT90PWM2/2B/3/3B achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

4.1 Block Diagram

Figure 4-1. Block Diagram



The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The AT90PWM2/2B/3/3B provides the following features: 8K bytes of In-System Programmable Flash with Read-While-Write capabilities, 512 bytes EEPROM, 512 bytes SRAM, 53 general purpose I/O lines, 32 general purpose working registers, three Power Stage Controllers, two flexible Timer/Counters with compare modes and PWM, one USART with DALI mode, an 11-channel 10-bit ADC with two differential input stage with programmable gain, a 10-bit DAC, a programmable Watchdog Timer with Internal Oscillator, an SPI serial port, an On-chip Debug system and four software selectable power saving modes.

The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, SPI ports and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or Hardware Reset. The ADC Noise Reduction mode stops the CPU and all I/O modules except ADC, to minimize switching noise during ADC conversions. In Standby mode, the Crystal/Resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low power consumption.

The device is manufactured using Atmel's high-density nonvolatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed in-system through an SPI serial interface, by a conventional nonvolatile memory programmer, or by an On-chip Boot program running on the AVR core. The boot program can use any interface to download the application program in the application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel AT90PWM2/3 is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The AT90PWM2/3 AVR is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, in-circuit emulators, and evaluation kits.

4.2 Pin Descriptions

4.2.1 VCC

Digital supply voltage.

4.2.2 GND

Ground.

4.2.3 Port B (PB7..PB0)

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B also serves the functions of various special features of the AT90PWM2/2B/3/3B as listed on page 69.

4.2.4 Port C (PC7..PC0)

Port C is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port C is not available on 24 pins package.

Port C also serves the functions of special features of the AT90PWM2/2B/3/3B as listed on page 72.

4.2.5 Port D (PD7..PD0)

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port D also serves the functions of various special features of the AT90PWM2/2B/3/3B as listed on page 75.

4.2.6 Port E (PE2..0) $\overline{\text{RESET}}$/ XTAL1/ XTAL2

Port E is an 3-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port E output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port E pins that are externally pulled low will source current if the pull-up resistors are activated. The Port E pins are tri-stated when a reset condition becomes active, even if the clock is not running.

If the RSTDISBL Fuse is programmed, PE0 is used as an I/O pin. Note that the electrical characteristics of PE0 differ from those of the other pins of Port C.

If the RSTDISBL Fuse is unprogrammed, PE0 is used as a Reset input. A low level on this pin for longer than the minimum pulse length will generate a Reset, even if the clock is not running. The minimum pulse length is given in Table 9-1 on page 47. Shorter pulses are not guaranteed to generate a Reset.

Depending on the clock selection fuse settings, PE1 can be used as input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

Depending on the clock selection fuse settings, PE2 can be used as output from the inverting Oscillator amplifier.

The various special features of Port E are elaborated in “Alternate Functions of Port E” on page 78 and “Clock Systems and their Distribution” on page 29.

4.2.7 AVCC

AVCC is the supply voltage pin for the A/D Converter. It should be externally connected to V_{CC}, even if the ADC is not used. If the ADC is used, it should be connected to V_{CC} through a low-pass filter.

4.2.8 AREF

This is the analog reference pin for the A/D Converter.

4.3 About Code Examples

This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.

5. Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
16	2.7 - 5.5V	AT90PWM3-16SQ	SO32	Extended (-40°C to 105°C)
16	2.7 - 5.5V	AT90PWM3-16MQT	QFN32	Extended (-40°C to 105°C)
16	2.7 - 5.5V	AT90PWM3-16MQ	QFN32	Extended (-40°C to 105°C)
16	2.7 - 5.5V	AT90PWM2-16SQ	SO24	Extended (-40°C to 105°C)
16	2.7 - 5.5V	AT90PWM3B-16SE	SO32	Engineering Samples
16	2.7 - 5.5V	AT90PWM3B-16ME	QFN32	Engineering Samples
16	2.7 - 5.5V	AT90PWM2B-16SE	SO24	Engineering Samples
16	2.7 - 5.5V	AT90PWM3B-16SU	SO32	Extended (-40°C to 105°C)
16	2.7 - 5.5V	AT90PWM3B-16MU	QFN32	Extended (-40°C to 105°C)
16	2.7 - 5.5V	AT90PWM2B-16SU	SO24	Extended (-40°C to 105°C)

Note: All packages are Pb free, fully LHF

Note: This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

Note: Parts numbers are for shipping in sticks (SO) or in trays (QFN). These devices can also be supplied in Tape and Reel. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

Note: 16MQT = Trays

Note: 16MQ = Tape and Reel

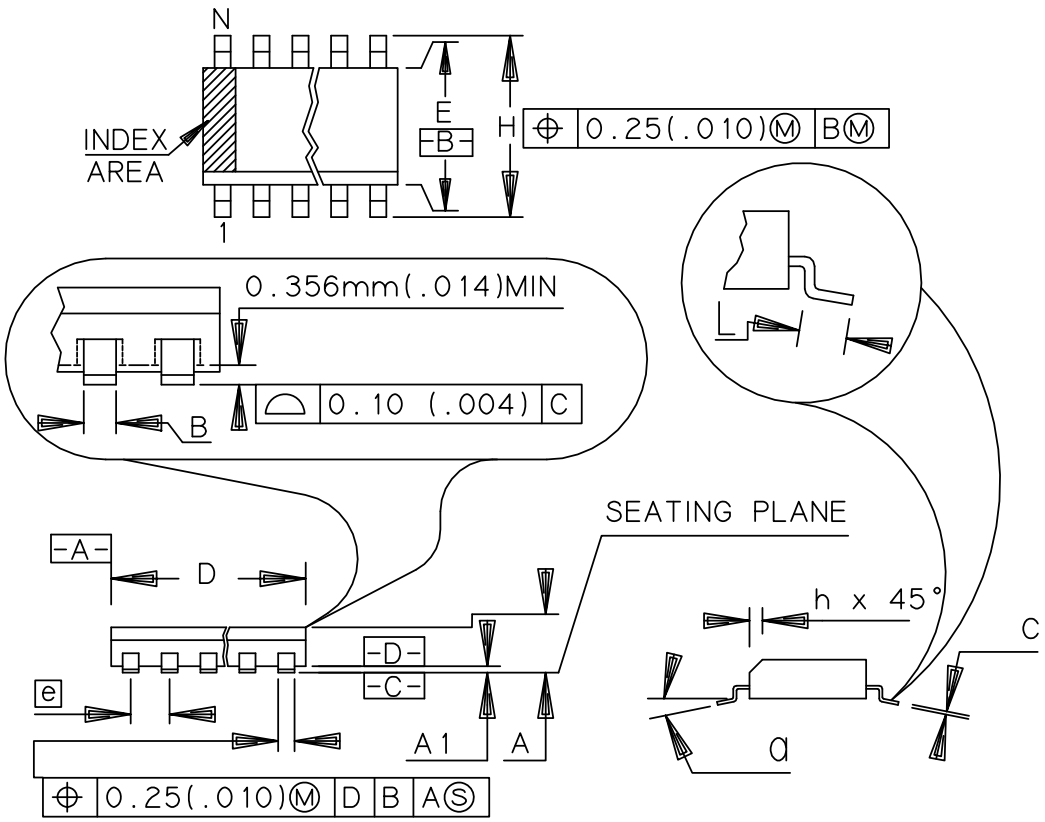
Note: PWM2 is not recommended for new designs, use PWM2B for your developments

Note: PWM3 is not recommended for new designs, use PWM3B for your developments

6. Package Information

Package Type	
SO24	24-Lead, Small Outline Package
SO32	32-Lead, Small Outline Package
QFN32	32-Lead, Quad Flat No lead

6.1 SO24

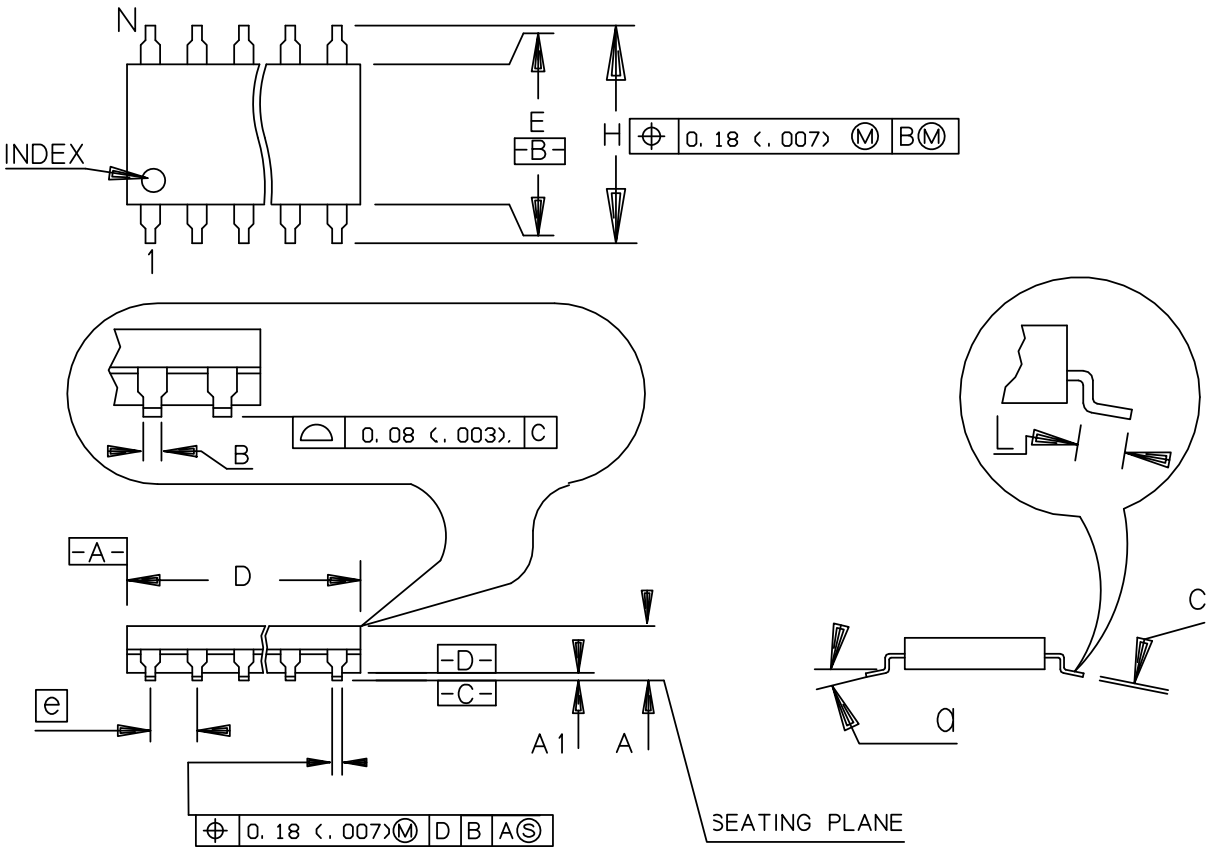


	MM		INCH	
A	2.35	2.65	.093	.104
A1	0.10	0.30	.004	.012
B	0.35	0.49	.014	.019
C	0.23	0.32	.009	.013
D	15.20	15.60	.599	.614
E	7.40	7.60	.291	.299
e	1.27	BSC	.050	BSC
H	10.00	10.65	.394	.419
h	0.25	0.75	.010	.029
L	0.40	1.27	.016	.050
N	24		24	
a	0°		8°	

07/27/07

Atmel Nantes S.A. La Chantrerie - BP 70602 44306 Nantes Cedex 3 - France	TITLE TD, 24 - Lead, 0.300" Body Width Plastic Gull Wing Small Outline Package (SOIC)	DRAWING No. TD	REV. A

6.2 SO32

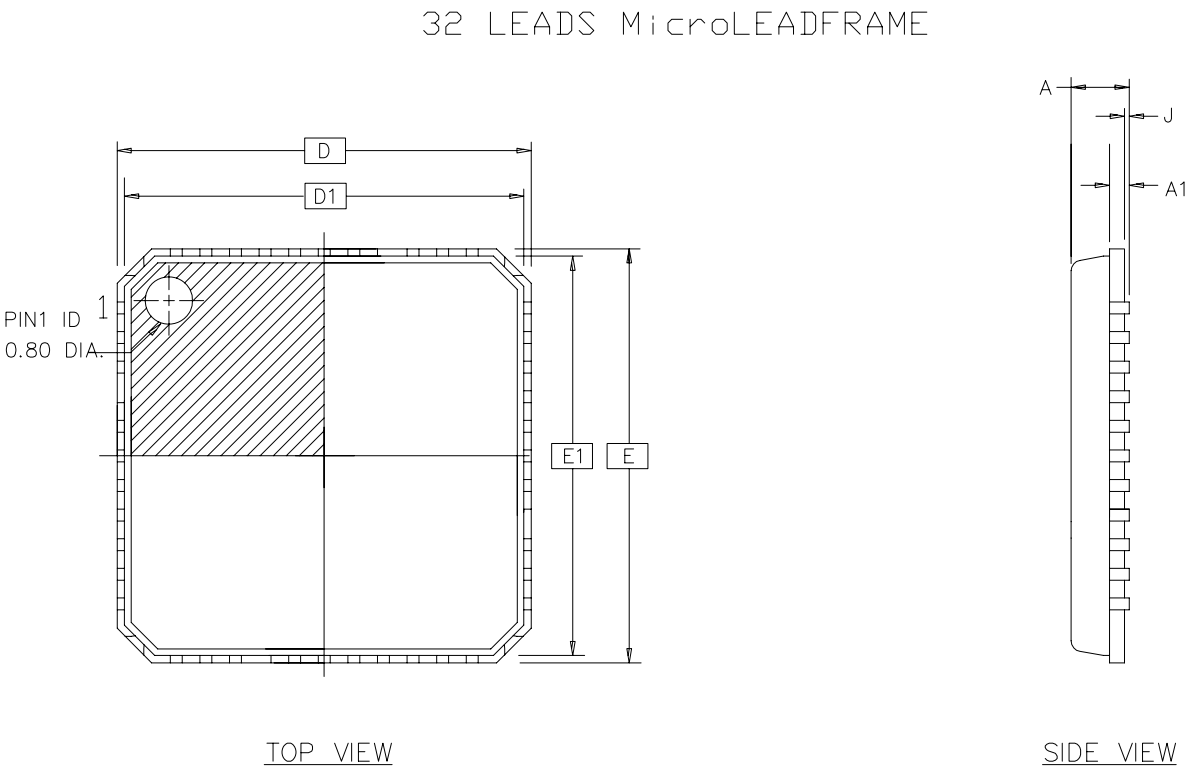


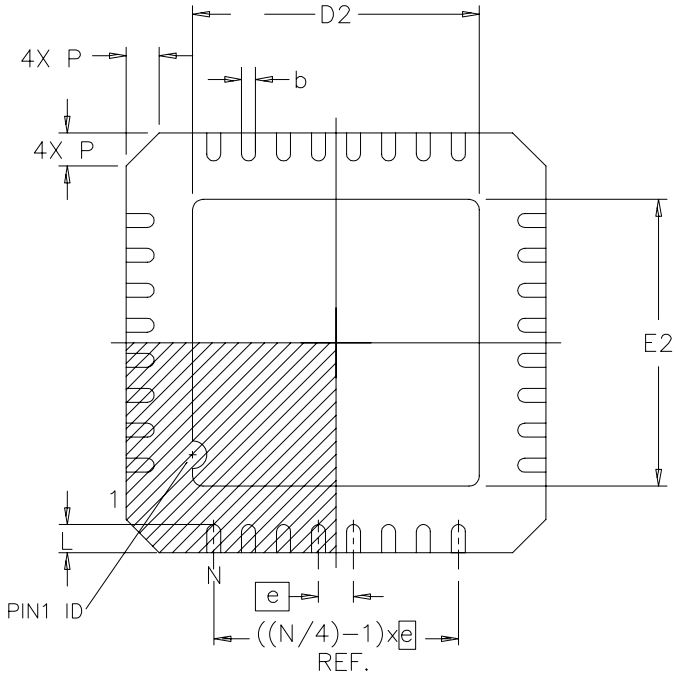
	MM		INCH	
	Min	Max	Min	Max
A	2.29	2.54	.090	.100
A1	0.10	0.25	.004	.010
B	0.36	0.51	.014	.020
C	0.15	0.32	.006	.013
D	20.57	20.88	.810	.822
E	7.42	7.60	.292	.299
e	1.27	BSC	.050	BSC
H	10.29	10.64	.405	.419
L	0.53	1.04	.021	.041
N	32		32	
α	4°		4°	

07/27/07

Atmel Nantes S.A. La Chantrerie - BP 70602 44306 Nantes Cedex 3 - France	TITLE T4, 32 - Lead, 0.300" Body Width Plastic Gull Wing Small Outline Package (SOIC)	DRAWING No. T4	REV. A

6.3 QFN32





	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	-	1.00	.032	-	.040
J	0.00	0.01	0.05	.000	.000	.002
A1		0.20 ref			.008 ref	
D/E		7.00 BSC			.276 BSC	
D1/E1		6.75 BSC			.266 BSC	
D2/E2	2.25	-	5.25	.090	-	.207
N			32			
P	0.24	0.42	0.60	.009	.016	.024
e		0.65 BSC			.026 BSC	
L	0.35	-	0.75	.014	-	.030
b	0.23	-	0.35	.009	-	.014

NOTES: MLF PACKAGE FAMILY

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM(.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
4. PACKAGE WARPAGE MAX 0.08mm.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FIXTURE IS OPTIONAL

7. Errata

7.1 AT90PWM2&3 Rev. A (Mask Revision)

- **PGM: PSCxRB Fuse**
- **PSC: Prescaler**
- **PSC: PAOCnA and PAOCnB Register Bits (Asynchronous output control)**
- **PSC: PEVxA/B Flag Bits**
- **PSC: Output Polarity in Centered Mode**
- **PSC: Output Activity**
- **VREF**
- **DALI**
- **DAC: Register Update**
- **DAC: Output spikes**
- **DAC driver: Output Voltage linearity**
- **ADC: Conversion accuracy**
- **Analog comparator: Offset value**
- **Analog comparator: Output signal**
- **PSC: Autolock modes**
- **DALI: 17th bit detection**
- **PSC: One ramp mode with PSC input mode 8**

1. **PGM: PSCnRB Fuse**

   The use of PSCnRB fuse can make the parallel ISP fail.

   Workaround:

   When PSCnRB fuses are used, use the serial programming mode to load a new program version.

2. **PSC: Prescaler**

   The use of PSC's prescaler have the following effects :

   It blocks the sample of PSC inputs until the two first cycles following the set of PSC run bit.

   A fault is not properly transferred to other (slave) PSC.

   Workaround:

   Clear the prescaler PPREx bit when stopping the PSC (prun = 0), and set them to appropriate value when starting the PSC (prun = 1), these bits are in the same PCTL register

   Do not use the prescaler when a fault on one PSC should affect other PSC’s

3. **PSC: PAOCnA and PAOCnB Register Bits (Asynchronous output control)**

   These register bits are malfunctioning.

   Workaround:

   Do not use this feature.

4. **PSC: PEVnA/B flag bits**

   These flags are set when a fault arises, but can also be set again during the fault itself.

   Workaround:

   Don't clear these flags before the fault disappears.

5. **PSC: Output Polarity in Centered Mode**

   In centered mode, PSCOUTn1 outputs are not inverted, so they are active at the same time as PSCOUTn0.

   Workaround:

   Use an external inverter (or a driver with inverting output) to drive the load on PSCOUTn1.

6. **PSC : POACnA/B Output Activity**

   These register bits are not implemented in rev A.

   Workaround:

   Do not use this feature.

7. **VREF**

   Remark: To have Internal Vref on AREF pin select an internal analog feature such as DAC or ADC.

   Some stand by power consuption may be observed if Vref equals AVcc

8. **DALI**

   Some troubles on Dali extension when edges are not symmetric.

   Workaround:

   Use an optocoupler providing symmetric edges on Rx and Tx DALI lines (only recommanded for software validation purpose).

9. **DAC: Register Update**

   Registers DACL & DACH are not written when the DAC is not enabled.

   Workaround:

   Enable DAC with DAEN before writing in DACL & DACH. To prevent an unwanted zero output on DAC pin, enable DAC output, with DAOE afterwards.

10. **DAC : Output spikes**

    During transition between two codes, a spike may appears

    Work around:

    Filter spike or wait for steady state

    No spike appears if the 4 last signifiant bits remain zero.

11. **DAC driver: Output Voltage linearity**

    The voltage linearity of the DAC driver is limited when the DAC output goes above Vcc - 1V.

    Work around:

    Do not use AVcc as Vref ; internal Vref gives good results

12. **ADC : Conversion accuracy**

    The conversion accuracy degrades when the ADC clock is 1 & 2 MHz.

    Work around:

    When a 10 bit conversion accuracy is required, use an ADC clock of 500 kHz or below.

13. **Analog comparator: Offset value**

    The offset value increases when the common mode voltage is above Vcc - 1.5V.

    Work around:

    Limit common mode voltage

14. **Analog comparator: Output signal**

    The comparator output toggles at the comparator clock frequency when the voltage difference between both inputs is lower than the offset. This may occur when comparing signal with small slew rate.

    Work around:

    This effect normally do not impact the PSC, as the transition is sampled once per PSC cycle

    Be carefull when using the comparator as an interrupt source.

15. **PSC : Autolock mode**

    This mode is not properly handled when CLKPSC is different from CLK IO.

    Work around:

    With CLKPSC equals 64/32 MHz (CLKPLL), use LOCK mode

16. **DALI : 17th bit detection**

    17th bit detection do not occurs if the signal arrives after the sampling point.

    Workaround:

    Use this feature only for sofware development and not in field conditions

17. **PSC : One ramp mode with PSC input mode 8**

    The retriggering is not properly handled in this case.

    Work around:
    Do not program this case.

18. **PSC : Desactivation of outputs in mode 14**

    See “PSC Input Mode 14: Fixed Frequency Edge Retrigger PSC and Disactivate Output” on page 156.

    Work around:
    Do not use this mode to desactivate output if retrigger event do not occurs during On-Time.

7.2 AT90PWM2B/3B

- **PSC : Double End-Of-Cycle Interrupt Request in Centered Mode**
- **ADC : Conversion accuracy**

1. **PSC : Double End-Of-Cycle Interrupt Request in Centered Mode**

   In centered mode, after the “expected” End-Of-Cycle Interrupt, a second unexpected Interrupt occurs 1 PSC cycle after the previous interrupt.

   Work around:

   While CPU cycle is lower than PSC clock, the CPU sees only one interrupt request. For PSC clock period greater than CPU cycle, the second interrupt request must be cleared by software.

2. **ADC : Conversion accuracy**

   The conversion accuracy degrades when the ADC clock is 2 MHz.

   Work around:

   When a 10 bit conversion accuracy is required, use an ADC clock of 1 MHz or below.

   At 2 Mhz the ADC can be used as a 7 bits ADC.

3. **DAC Driver linearity above 3.6V**

   With 5V Vcc, the DAC driver linearity is poor when DAC output level is above Vcc-1V. At 5V, DAC output for 1023 will be around 5V - 40mV.

Work around: .

Use, when Vcc=5V, Vref below Vcc-1V.

Or, when Vref=Vcc=5V, do not uses codes above 800.

4. **DAC Update in Autotrig mode**

   If the cpu writes in DACH register at the same instant that the selected trigger source occurs and DAC Auto Trigger is enabled, the DACH register is not updated by the new value.

   Work around: .

   When using the autotrig mode, write twice in the DACH register. The time between the two CPU writes, must be different than the trigger source frequency.

8. Errata

8.1 AT90PWM2&3 Rev. A (Mask Revision)

- **PGM: PSCxRB Fuse**
- **PSC: Prescaler**
- **PSC: PAOCnA and PAOCnB Register Bits (Asynchronous output control)**
- **PSC: PEVxA/B Flag Bits**
- **PSC: Output Polarity in Centered Mode**
- **PSC: Output Activity**
- **VREF**
- **DALI**
- **DAC: Register Update**
- **DAC: Output spikes**
- **DAC driver: Output Voltage linearity**
- **ADC: Conversion accuracy**
- **Analog comparator: Offset value**
- **Analog comparator: Output signal**
- **PSC: Autolock modes**
- **DALI: 17th bit detection**
- **PSC: One ramp mode with PSC input mode 8**

1. **PGM: PSCnRB Fuse**

   The use of PSCnRB fuse can make the parallel ISP fail.

   Workaround:

   When PSCnRB fuses are used, use the serial programming mode to load a new program version.

2. **PSC: Prescaler**

   The use of PSC's prescaler have the following effects:

   It blocks the sample of PSC inputs until the two first cycles following the set of PSC run bit.

   A fault is not properly transferred to other (slave) PSC.

   Workaround:

   Clear the prescaler PPREx bit when stopping the PSC (prun = 0), and set them to appropriate value when starting the PSC (prun = 1), these bits are in the same PCTL register

   Do not use the prescaler when a fault on one PSC should affect other PSC's

3. **PSC: PAOCnA and PAOCnB Register Bits (Asynchronous output control)**

   These register bits are malfunctioning.

   Workaround:

   Do not use this feature.

4. **PSC: PEVnA/B flag bits**

   These flags are set when a fault arises, but can also be set again during the fault itself.

   Workaround:

   Don't clear these flags before the fault disappears.

5. **PSC: Output Polarity in Centered Mode**

   In centered mode, PSCOUTn1 outputs are not inverted, so they are active at the same time as PSCOUTn0.

   Workaround:

   Use an external inverter (or a driver with inverting output) to drive the load on PSCOUTn1.

6. **PSC: POACnA/B Output Activity**

   These register bits are not implemented in rev A.

   Workaround:

   Do not use this feature.

7. **VREF**

   Remark: To have Internal Vref on AREF pin select an internal analog feature such as DAC or ADC.

   Some stand by power consuption may be observed if Vref equals AVcc

8. **DALI**

   Some troubles on Dali extension when edges are not symmetric.

   Workaround:

   Use an optocoupler providing symmetric edges on Rx and Tx DALI lines (only recommanded for software validation purpose).

9. **DAC: Register Update**

   Registers DACL & DACH are not written when the DAC is not enabled.

   Workaround:

   Enable DAC with DAEN before writing in DACL & DACH. To prevent an unwanted zero output on DAC pin, enable DAC output, with DAOE afterwards.

10. **DAC : Output spikes**

    During transition between two codes, a spike may appears

    Work around:

    Filter spike or wait for steady state

    No spike appears if the 4 last signifiant bits remain zero.

11. **DAC driver: Output Voltage linearity**

    The voltage linearity of the DAC driver is limited when the DAC output goes above Vcc - 1V.

    Work around:

    Do not use AVcc as Vref ; internal Vref gives good results

12. **ADC : Conversion accuracy**

    The conversion accuracy degrades when the ADC clock is 1 & 2 MHz.

    Work around:

    When a 10 bit conversion accuracy is required, use an ADC clock of 500 kHz or below.

13. **Analog comparator: Offset value**

    The offset value increases when the common mode voltage is above Vcc - 1.5V.

    Work around:

    Limit common mode voltage

14. **Analog comparator: Output signal**

    The comparator output toggles at the comparator clock frequency when the voltage difference between both inputs is lower than the offset. This may occur when comparing signal with small slew rate.

    Work around:

    This effect normally do not impact the PSC, as the transition is sampled once per PSC cycle

    Be careful when using the comparator as an interrupt source.

15. **PSC : Autolock mode**

    This mode is not properly handled when CLKPSC is different from CLK IO.

    Work around:

    With CLKPSC equals 64/32 MHz (CLKPLL), use LOCK mode

16. **DALI : 17th bit detection**

    17th bit detection do not occurs if the signal arrives after the sampling point.

    Workaround:

    Use this feature only for sofware development and not in field conditions

17. **PSC : One ramp mode with PSC input mode 8**

    The retriggering is not properly handled in this case.

    Work around:
    Do not program this case.

18. **PSC : Desactivation of outputs in mode 14**

    See “PSC Input Mode 14: Fixed Frequency Edge Retrigger PSC and Disactivate Output” on page 156.

    Work around:
    Do not use this mode to deactivate output if retrigger event do not occurs during On-Time.

8.2 AT90PWM2B/3B

- **PSC : Double End-Of-Cycle Interrupt Request in Centered Mode**
- **ADC : Conversion accuracy**

1. **PSC : Double End-Of-Cycle Interrupt Request in Centered Mode**

    In centered mode, after the “expected” End-Of-Cycle Interrupt, a second unexpected Interrupt occurs 1 PSC cycle after the previous interrupt.

    Work around:

    While CPU cycle is lower than PSC clock, the CPU sees only one interrupt request. For PSC clock period greater than CPU cycle, the second interrupt request must be cleared by software.

2. **ADC : Conversion accuracy**

    The conversion accuracy degrades when the ADC clock is 2 MHz.

    Work around:

    When a 10 bit conversion accuracy is required, use an ADC clock of 1 MHz or below.

    At 2 Mhz the ADC can be used as a 7 bits ADC.

3. **DAC Driver linearity above 3.6V**

    With 5V Vcc, the DAC driver linearity is poor when DAC output level is above Vcc-1V. At 5V, DAC output for 1023 will be around 5V - 40mV.

Work around:

Use, when Vcc=5V, Vref below Vcc-1V.

Or, when Vref=Vcc=5V, do not uses codes above 800.

4. **DAC Update in Autotrig mode**

   If the cpu writes in DACH register at the same instant that the selected trigger source occurs and DAC Auto Trigger is enabled, the DACH register is not updated by the new value.

   Work around:

   When using the autotrig mode, write twice in the DACH register. The time between the two CPU writes, must be different than the trigger source frequency.

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