User Defined Fault Protection and Detection, 10 Ω R_{ON}, Quad Channel Protector

Data Sheet

ADG5462F

FEATURES

- User defined secondary supplies set overvoltage level
  - Overvoltage protection up to −55 V and +55 V
  - Power-off protection up to −55 V and +55 V
  - Overvoltage detection on source pins
  - Minimum secondary supply level: 4.5 V single-supply
  - Interrupt flag indicates fault status
- Low on resistance: 10 Ω typical
  - On-resistance flatness: 0.5 Ω maximum
- 4 kV human body model (HBM) ESD rating
- Latch-up immune under any circumstance
- V_{SS} to V_{DD} analog signal range
  - ±5 V to ±22 V dual supply operation
  - 8 V to 44 V single-supply operation
  - Fully specified at ±15 V, ±20 V, +12 V, and +36 V

APPLICATIONS

- Analog input/output modules
- Process control/distributed control systems
- Data acquisition
- Instrumentation
- Avionics
- Automatic test equipment
- Communication systems

FUNCTIONAL BLOCK DIAGRAM

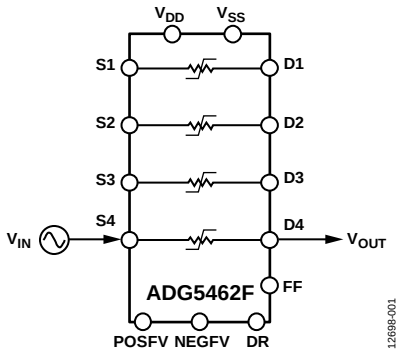

Figure 1.

GENERAL DESCRIPTION

The ADG5462F contains four channels that are overvoltage protected. The channel protector is placed in series with the signal path and protects sensitive components from overvoltage faults in that path. The channel protector prevents overvoltages when powered and unpowered, and it is ideal for use in applications where correct power supply sequencing cannot always be guaranteed. The primary supply voltages define the on-resistance profile, while the secondary supply voltages define the voltage level at which the overvoltage protection engages.

When no power supplies are present, the channel remains in the off condition, and the channel inputs are high impedance. Under normal operating conditions, if the analog input signal levels on any Sx pin exceed positive fault voltage (POSFV) or negative fault voltage (NEGFV) by a threshold voltage (V_T), the channel turns off and that Sx pin becomes high impedance. If the DR pin is driven low, the drain pin (Dx) is pulled to the secondary supply voltage that was exceeded. The output profile for each DR voltage level is shown in Figure 49. Input signal levels up to −55 V or +55 V relative to ground are blocked in both the powered and unpowered conditions.

The low on-resistance of these switches, combined with the on-resistance flatness over a significant portion of the signal range make them an ideal solution for data acquisition and instrumentation applications where excellent linearity and low distortion are critical.

PRODUCT HIGHLIGHTS

1. Source pins (Sx) are protected against voltages greater than the secondary supply rails (POSFV and NEGFV), up to −55 V and +55 V.
2. In an unpowered state, source pins (Sx) are protected against voltages from −55 V to +55 V.
3. Overvoltage detection with digital output indicates the operating state of the channels.
4. Trench isolation guards against latch-up.
5. Optimized for low on-resistance and on-resistance flatness.
6. The ADG5462F operates from a dual power supply range of ±5 V to ±22 V or a single power supply range of 8 V to 44 V.

Rev. C
Document Feedback

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SPECIFICATIONS

±15 V DUAL SUPPLY

V_{DD} = 15 V ± 10%, V_{SS} = −15 V ± 10%, GND = 0 V, $C_{DECOUPLING}$ = 0.1 µF, unless otherwise noted.

Table 1.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = +13.5 V, V_{SS} = −13.5 V, see Figure 35
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	10			Ω typ	V_S = ±10 V, I_S = −10 mA
	11.2	14	16.5	Ω max	
	9.5			Ω typ	V_S = ±9 V, I_S = −10 mA
	10.7	13.5	16	Ω max	
On-Resistance Match Between Channels, ΔR_{ON}	0.05			Ω typ	V_S = ±10 V, I_S = −10 mA
	0.5	0.6	0.7	Ω max	
	0.05			Ω typ	V_S = ±9 V, I_S = −10 mA
	0.35	0.5	0.5	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	0.6			Ω typ	V_S = ±10 V, I_S = −10 mA
	0.9	1.1	1.1	Ω max	
	0.1			Ω typ	V_S = ±9 V, I_S = −10 mA
	0.4	0.5	0.5	Ω max	
Threshold Voltage, V_T	0.7			V typ	See Figure 23
LEAKAGE CURRENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
Channel On Leakage, I_D (On), I_S (On)	±0.3			nA typ	V_S = V_D = ±10 V, see Figure 36
	±1.5	±2.0	±4.5	nA max	
FAULT					
Source Leakage Current, I_S					
With Overvoltage			±78	µA typ	V_{DD} = +16.5 V, V_{SS} = −16.5 V, GND = 0 V, V_S = ±55 V, see Figure 37
Power Supplies Grounded or Floating			±40	µA typ	V_{DD} = 0 V or floating, V_{SS} = 0 V or floating, GND = 0 V, V_S = ±55 V, see Figure 38
Drain Leakage Current, I_D					DR = floating or V_{DD}
With Overvoltage	±2.0			nA typ	V_{DD} = +16.5 V, V_{SS} = −16.5 V, GND = 0 V, V_S = ±55 V, see Figure 37
	±20	±30	±65	nA max	
Power Supplies Grounded	±10			nA typ	V_{DD} = 0 V, V_{SS} = 0 V, GND = 0 V, V_S = ±55 V, see Figure 38
	±30	±50	±100	nA max	
Power Supplies Floating	±10	±10	±10	µA typ	V_{DD} = floating, V_{SS} = floating, GND = 0 V, V_S = ±55 V, see Figure 38
DIGITAL INPUTS/OUTPUTS (DR/FF)					
Input Voltage High, V_{INH}			2.0	V min	
Input Voltage Low, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	±0.7			µA typ	V_{IN} = V_{GND} or V_{DD}
			±1.2	µA max	
Digital Input Capacitance, C_{IN}	5.0			pF typ	
Output Voltage High, V_{OH}	2.0			V min	
Output Voltage Low, V_{OL}	0.8			V max	

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
DYNAMIC CHARACTERISTICS[1]					
Overvoltage Response Time, $t_{RESPONSE}$	460			ns typ	R_L = 1 kΩ, C_L = 2 pF, see Figure 42
	585	615	630	ns max	
Overvoltage Recovery Time, $t_{RECOVERY}$	720			ns typ	R_L = 1 kΩ, C_L = 2 pF, see Figure 43
	930	1050	1100	ns max	
Drain Pull-Up/Pull-Down Time Following Overvoltage, $t_{RESPONSE}$ (DR)	4			µs typ	C_L = 12 pF, see Figure 47
Interrupt Flag Response Time, $t_{DIGRESP}$	85		115	ns typ	C_L = 12 pF, see Figure 44
Interrupt Flag Recovery Time, t_{DIGREC}	60		85	µs typ	C_L = 12 pF, see Figure 45
	600			ns typ	C_L = 12 pF, R_{PULLUP} = 1 kΩ, see Figure 46
Channel-to-Channel Crosstalk	−90			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 39
Total Harmonic Distortion Plus Noise, THD + N	0.0015			% typ	R_L = 10 kΩ, V_S = 15 V p-p, f = 20 Hz to 20 kHz, see Figure 41
−3 dB Bandwidth	318			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 40
Insertion Loss	−0.8			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 40
C_D (On), C_S (On)	24			pF typ	V_S = 0 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = POSFV = +16.5 V, V_{SS} = NEGFV = −16.5 V, GND = 0 V
Normal Mode					
I_{DD}	0.9			mA typ	
I_{POSFV}	0.1			mA typ	
I_{DD} + I_{POSFV}	1.2		1.3	mA max	
I_{GND}	0.4			mA typ	
	0.55		0.6	mA max	
I_{SS}	0.5			mA typ	
I_{NEGFV}	0.1			mA typ	
I_{SS} + I_{NEGFV}	0.65		0.7	mA max	
Fault Mode					V_S = ±55 V
I_{DD}	1.2			mA typ	
I_{POSFV}	0.1			mA typ	
I_{DD} + I_{POSFV}	1.6		1.8	mA max	
I_{GND}	0.8			mA typ	
	1.0		1.1	mA max	
I_{SS}	0.5			mA typ	
I_{NEGFV}	0.1			mA typ	
I_{SS} + I_{NEGFV}	1.0		1.8	mA max	
V_{DD}/V_{SS}			±5	V min	GND = 0 V
			±22	V max	GND = 0 V

[1] Guaranteed by design; not subject to production test.

±20 V DUAL SUPPLY

V_{DD} = 20 V ± 10%, V_{SS} = −20 V ± 10%, GND = 0 V, $C_{DECOUPLING}$ = 0.1 µF, unless otherwise noted.

Table 2.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = +18 V, V_{SS} = −18 V, see Figure 35
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	10			Ω typ	V_S = ±15 V, I_S = −10 mA
	11.5	14.5	16.5	Ω max	
	9.5			Ω typ	V_S = ±13.5 V, I_S = −10 mA
	11	14	16.5	Ω max	
On-Resistance Match Between Channels, ΔR_{ON}	0.05			Ω typ	V_S = ±15 V, I_S = −10 mA
	0.35	0.5	0.5	Ω max	
	0.05			Ω typ	V_S = ±13.5 V, I_S = −10 mA
	0.35	0.5	0.5	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	1.0			Ω typ	V_S = ±15 V, I_S = −10 mA
	1.4	1.5	1.5	Ω max	
	0.1			Ω typ	V_S = ±13.5 V, I_S = −10 mA
	0.4	0.5	0.5	Ω max	
Threshold Voltage, V_T	0.7			V typ	See Figure 23
LEAKAGE CURRENTS					V_{DD} = +22 V, V_{SS} = −22 V
Channel On Leakage, I_D (On), I_S (On)	±0.3			nA typ	V_S = V_D = ±15 V, see Figure 36
	±1.5	±2.0	±4.5	nA max	
FAULT					
Source Leakage Current, I_S					
With Overvoltage			±78	µA typ	V_{DD} = +22 V, V_{SS} = −22 V, GND = 0 V, V_S = ±55 V, see Figure 37
Power Supplies Grounded or Floating			±40	µA typ	V_{DD} = 0 V or floating, V_{SS} = 0 V or floating, GND = 0 V, V_S = ±55 V, see Figure 38
Drain Leakage Current, I_D					DR = floating or V_{DD}
With Overvoltage	±5.0			nA typ	V_{DD} = +22 V, V_{SS} = −22 V, GND = 0 V, V_S = ±55 V, see Figure 37
	±1.0	±1.0	±1.0	µA max	
Power Supplies Grounded	±10			nA typ	V_{DD} = 0 V, V_{SS} = 0 V, GND = 0 V, V_S = ±55 V, see Figure 38
	±30	±50	±100	nA max	
Power Supplies Floating	±10	±10	±10	µA typ	V_{DD} = floating, V_{SS} = floating, GND = 0 V, V_S = ±55 V, see Figure 38
DIGITAL INPUTS/OUTPUTS					
Input Voltage High, V_{INH}			2.0	V min	
Input Voltage Low, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.7			µA typ	V_{IN} = V_{GND} or V_{DD}
			1.2	µA max	
Digital Input Capacitance, C_{IN}	5.0			pF typ	
Output Voltage High, V_{OH}	2.0			V min	
Output Voltage Low, V_{OL}	0.8			V max	

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
DYNAMIC CHARACTERISTICS[1]					
Overvoltage Response Time, $t_{RESPONSE}$	370			ns typ	R_L = 1 kΩ, C_L = 2 pF, see Figure 42
	480	500	515	ns max	
Overvoltage Recovery Time, $t_{RECOVERY}$	840			ns typ	R_L = 1 kΩ, C_L = 2 pF, see Figure 43
	1200	1400	1700	ns max	
Drain Pull-Up/Pull-Down Time Following Overvoltage, $t_{RESPONSE}$ (DR)	4			µs typ	C_L = 12 pF, see Figure 47
Interrupt Flag Response Time, $t_{DIGRESP}$	85		115	ns typ	C_L = 12 pF, see Figure 44
Interrupt Flag Recovery Time, t_{DIGREC}	60		85	µs typ	C_L = 12 pF, see Figure 45
	600			ns typ	C_L = 12 pF, R_{PULLUP} = 1 kΩ, see Figure 46
Channel-to-Channel Crosstalk	−90			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 39
Total Harmonic Distortion Plus Noise, THD + N	0.001			% typ	R_L = 10 kΩ, V_S = 20 V p-p, f = 20 Hz to 20 kHz, see Figure 41
−3 dB Bandwidth	310			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 40
Insertion Loss	−0.8			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 40
C_D (On), C_S (On)	23			pF typ	V_S = 0 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = POSFV = +22 V, V_{SS} = NEGFV = −22 V
Normal Mode					
I_{DD}	0.9			mA typ	
I_{POSFV}	0.1			mA typ	
I_{DD} + I_{POSFV}	1.2		1.3	mA max	
I_{GND}	0.4			mA typ	
	0.55		0.6	mA max	
I_{SS}	0.5			mA typ	
I_{NEGFV}	0.1			mA typ	
I_{SS} + I_{NEGFV}	0.65		0.7	mA max	
Fault Mode					V_S = ±55 V
I_{DD}	1.2			mA typ	
I_{POSFV}	0.1			mA typ	
I_{DD} + I_{POSFV}	1.6		1.8	mA max	
I_{GND}	0.8			mA typ	
	1.0		1.1	mA max	
I_{SS}	0.5			mA typ	
I_{NEGFV}	0.1			mA typ	
I_{SS} + I_{NEGFV}	1.0		1.8	mA max	
V_{DD}/V_{SS}			±5	V min	GND = 0 V
			±22	V max	GND = 0 V

[1] Guaranteed by design; not subject to production test.

12 V SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, GND = 0 V, $C_{DECOUPLING}$ = 0.1 µF, unless otherwise noted.

Table 3.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = +10.8 V, V_{SS} = 0 V, see Figure 35
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	22			Ω typ	V_S = 0 V to +10 V, I_S = −10 mA
	24.5	31	37	Ω max	
	10			Ω typ	V_S = +3.5 V to +8.5 V, I_S = −10 mA
	11.2	14	16.5	Ω max	
On-Resistance Match Between Channels, ΔR_{ON}	0.05			Ω typ	V_S = 0 V to +10 V, I_S = −10 mA
	0.5	0.6	0.7	Ω max	
	0.05			Ω typ	V_S = +3.5 V to +8.5 V, I_S = −10 mA
	0.5	0.6	0.7	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	12.5			Ω typ	V_S = 0 V to +10 V, I_S = −10 mA
	14.5	19	23	Ω max	
	0.6			Ω typ	V_S = +3.5 V to +8.5 V, I_S = −10 mA
	0.9	1.1	1.3	Ω max	
Threshold Voltage, V_T	0.7			V typ	See Figure 23
LEAKAGE CURRENTS					V_{DD} = +13.2 V, V_{SS} = 0 V
Channel On Leakage, I_D (On), I_S (On)	±0.3			nA typ	V_S = V_D = 1 V/10 V, see Figure 36
	±1.5	±2.0	±4.5	nA max	
FAULT					
Source Leakage Current, I_S					
With Overvoltage			±78	µA typ	V_{DD} = +13.2 V, V_{SS} = 0 V, GND = 0 V, V_S = ±55 V, see Figure 37
Power Supplies Grounded or Floating			±40	µA typ	V_{DD} = 0 V or floating, V_{SS} = 0 V or floating, GND = 0 V, V_S = ±55 V, see Figure 38
Drain Leakage Current, I_D					DR = floating or V_{DD}
With Overvoltage	±2.0			nA typ	V_{DD} = +13.2 V, V_{SS} = 0 V, GND = 0 V, V_S = ±55 V, see Figure 37
	±20	±30	±65	nA max	
Power Supplies Grounded	±10			nA typ	V_{DD} = 0 V, V_{SS} = 0 V, GND = 0 V, V_S = ±55 V, see Figure 38
	±30	±50	±100	nA max	
Power Supplies Floating	±10	±10	±10	µA typ	V_{DD} = floating, V_{SS} = floating, GND = 0 V, V_S = ±55 V, see Figure 38
DIGITAL INPUTS/OUTPUTS					
Input Voltage High, V_{INH}			2.0	V min	
Input Voltage Low, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.7			µA typ	V_{IN} = V_{GND} or V_{DD}
			1.2	µA max	
Digital Input Capacitance, C_{IN}	5.0			pF typ	
Output Voltage High, V_{OH}	2.0			V min	
Output Voltage Low, V_{OL}	0.8			V max	

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
DYNAMIC CHARACTERISTICS[1]					
Overvoltage Response Time, $t_{RESPONSE}$	560			ns typ	R_L = 1 kΩ, C_L = 2 pF, see Figure 42
	660	700	720	ns max	
Overvoltage Recovery Time, $t_{RECOVERY}$	640			ns typ	R_L = 1 kΩ, C_L = 2 pF, see Figure 43
	800	865	960	ns max	
Drain Pull-Up/Pull-Down Time Following Overvoltage, $t_{RESPONSE}$ (DR)	4			µs typ	C_L = 12 pF, see Figure 47
Interrupt Flag Response Time, $t_{DIGRESP}$	85		115	ns typ	C_L = 12 pF, see Figure 44
Interrupt Flag Recovery Time, t_{DIGREC}	60		85	µs typ	C_L = 12 pF, see Figure 45
	600			ns typ	C_L = 12 pF, R_{PULLUP} = 1 kΩ, see Figure 46
Channel-to-Channel Crosstalk	−90			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 39
Total Harmonic Distortion Plus Noise, THD + N	0.007			% typ	R_L = 10 kΩ, V_S = 6 V p-p, f = 20 Hz to 20 kHz, see Figure 41
−3 dB Bandwidth	284			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 40
Insertion Loss	−0.9			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 40
C_D (On), C_S (On)	25			pF typ	V_S = 6 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = +13.2 V, V_{SS} = 0 V, digital inputs = 0 V, 5 V, or V_{DD}
Normal Mode					
I_{DD}	0.9			mA typ	
I_{POSFV}	0.1			mA typ	
I_{DD} + I_{POSFV}	1.2		1.3	mA max	
I_{GND}	0.4			mA typ	
	0.55		0.6	mA max	
I_{SS}	0.5			mA typ	
I_{NEGFV}	0.1			mA typ	
I_{SS} + I_{NEGFV}	0.65		0.7	mA max	
Fault Mode					V_S = ±55 V
I_{DD}	1.2			mA typ	
I_{POSFV}	0.1			mA typ	
I_{DD} + I_{POSFV}	1.6		1.8	mA max	
I_{GND}	0.8			mA typ	
	1.0		1.1	mA max	
I_{SS}	0.5			mA typ	Digital inputs = 5 V
I_{NEGFV}	0.1			mA typ	
I_{SS} + I_{NEGFV}	1.0		1.8	mA max	V_S = ±55 V, V_D = 0 V
V_{DD}			8	V min	GND = 0 V
			44	V max	GND = 0 V

[1] Guaranteed by design; not subject to production test.

36 V SINGLE SUPPLY

V_{DD} = 36 V ± 10%, V_{SS} = 0 V, GND = 0 V, $C_{DECOUPLING}$ = 0.1 µF, unless otherwise noted.

Table 4.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = +32.4 V, V_{SS} = 0 V, see Figure 35
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	22			Ω typ	V_S = 0 V to +30 V, I_S = −10 mA
	24.5	31	37	Ω max	
	10			Ω typ	V_S = +4.5 V to +28 V, I_S = −10 mA
	11	14	16.5	Ω max	
On-Resistance Match Between Channels, ΔR_{ON}	0.05			Ω typ	V_S = 0 V to +30 V, I_S = −10 mA
	0.5	0.6	0.7	Ω max	
	0.05			Ω typ	V_S = +4.5 V to +28 V, I_S = −10 mA
	0.35	0.5	0.5	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	12.5			Ω typ	V_S = 0 V to +30 V, I_S = −10 mA
	14.5	19	23	Ω max	
	0.1			Ω typ	V_S = +4.5 V to +28 V, I_S = −10 mA
	0.4	0.5	0.5	Ω max	
Threshold Voltage, V_T	0.7			V typ	See Figure 23
LEAKAGE CURRENTS					V_{DD} = +39.6 V, V_{SS} = 0 V
Channel On Leakage, I_D (On), I_S (On)	±0.3			nA typ	V_S = V_D = 1 V/30 V, see Figure 36
	±1.5	±2.0	±4.5	nA max	
FAULT					
Source Leakage Current, I_S					
With Overvoltage			±78	µA typ	V_{DD} = +39.6 V, V_{SS} = 0 V, GND = 0 V, V_S = −40 V to +55 V, see Figure 37
Power Supplies Grounded or Floating			±40	µA typ	V_{DD} = 0 V or floating, V_{SS} = 0 V or floating, GND = 0 V, V_S = +55 V, −40 V, see Figure 38
Drain Leakage Current, I_D					DR = floating or V_{DD}
With Overvoltage	±2.0			nA typ	V_{DD} = +39.6 V, V_{SS} = 0 V, GND = 0 V, V_S = −40 V to +55 V, see Figure 37
	±20	±30	±65	nA max	
Power Supplies Grounded	±10			nA typ	V_{DD} = 0 V, V_{SS} = 0 V, GND = 0 V, V_S = −40 V to +55 V, see Figure 38
	±30	±50	±100	nA max	
Power Supplies Floating	±10	±10	±10	µA typ	V_{DD} = floating, V_{SS} = floating, GND = 0 V, V_S = −40 V to +55 V, see Figure 38
DIGITAL INPUTS/OUTPUTS					
Input Voltage High, V_{INH}			2.0	V min	
Input Voltage Low, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.7			µA typ	V_{IN} = V_{GND} or V_{DD}
			1.2	µA max	
Digital Input Capacitance, C_{IN}	5.0			pF typ	
Output Voltage High, V_{OH}	2.0			V min	
Output Voltage Low, V_{OL}	0.8			V max	

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
DYNAMIC CHARACTERISTICS[1]					
Overvoltage Response Time, $t_{RESPONSE}$	250			ns typ	R_L = 1 kΩ, C_L = 2 pF, see Figure 42
	350	360	375	ns max	
Overvoltage Recovery Time, $t_{RECOVERY}$	1500			ns typ	R_L = 1 kΩ, C_L = 2 pF, see Figure 43
	2000	2300	2700	ns max	
Drain Pull-Up/Pull-Down Time Following Overvoltage, $t_{RESPONSE}$ (DR)	4			µs typ	C_L = 12 pF, see Figure 47
Interrupt Flag Response Time, $t_{DIGRESP}$	85		115	ns typ	C_L = 12 pF, see Figure 44
Interrupt Flag Recovery Time, t_{DIGREC}	60		85	µs typ	C_L = 12 pF, see Figure 45
	600			ns typ	C_L = 12 pF, R_{PULLUP} = 1 kΩ, see Figure 46
Channel-to-Channel Crosstalk	−90			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 39
Total Harmonic Distortion Plus Noise, THD + N	0.001			% typ	R_L = 10 kΩ, V_S = 18 V p-p, f = 20 Hz to 20 kHz, see Figure 41
−3 dB Bandwidth	321			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 40
Insertion Loss	−0.8			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 40
C_D (On), C_S (On)	23			pF typ	V_S = 18 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 39.6 V, V_{SS} = 0 V, digital inputs = 0 V, 5 V, or V_{DD}
Normal Mode					
I_{DD}	0.9			mA typ	
I_{POSFV}	0.1			mA typ	
I_{DD} + I_{POSFV}	1.2		1.3	mA max	
I_{GND}	0.4			mA typ	
	0.55		0.6	mA max	
I_{SS}	0.5			mA typ	
I_{NEGFV}	0.1			mA typ	
I_{SS} + I_{NEGFV}	0.65		0.7	mA max	
Fault Mode					V_S = −40 V to +55 V
I_{DD}	1.2			mA typ	
I_{POSFV}	0.1			mA typ	
I_{DD} + I_{POSFV}	1.6		1.8	mA max	
I_{GND}	0.8			mA typ	
	1.0		1.1	mA max	
I_{SS}	0.5			mA typ	
I_{NEGFV}	0.1			mA typ	
I_{SS} + I_{NEGFV}	1.0		1.8	mA max	
V_{DD}			8	V min	GND = 0 V
			44	V max	GND = 0 V

[1] Guaranteed by design; not subject to production test.

CONTINUOUS CURRENT PER CHANNEL, Sx OR Dx

Table 5.

Parameter	25°C	85°C	125°C	Unit	Test Conditions/Comments
16-Lead TSSOP					
θ_{JA} = 112.6°C/W	83	59	39	mA max	V_S = V_{SS} + 4.5 V to V_{DD} − 4.5 V
	64	48	29	mA max	V_S = V_{SS} to V_{DD}
16-Lead LFCSP					
θ_{JA} = 30.4°C/W	152	99	61	mA max	V_S = V_{SS} + 4.5 V to V_{DD} − 4.5 V
	118	81	53	mA max	V_S = V_{SS} to V_{DD}

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
V_{DD} to V_{SS}	48 V
V_{DD} to GND	−0.3 V to +48 V
V_{SS} to GND	−48 V to +0.3 V
POSFV to GND	−0.3 V to V_{DD} + 0.3 V
NEGFV to GND	V_{SS} − 0.3V to +0.3 V
Sx Pins to GND	−55 V to +55 V
Sx to V_{DD} or V_{SS}	80 V
V_S to V_D	80 V
Dx Pins[1, 2] to GND	NEGFV − 0.7 V to POSFV + 0.7 V or 30 mA, whichever occurs first
Digital Input (DR pin) to GND	GND − 0.7 V to 48 V or 30 mA, whichever occurs first
Peak Current, Sx or Dx Pins	288 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, Sx or Dx Pins	Data[3] + 15%
Digital Output (FF pin)	GND − 0.7 V to 6 V or 30 mA, whichever occurs first
Dx Pins, Overvoltage State, DR = GND, Load Current	1 mA
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Thermal Impedance, θ_{JA}	
16-Lead TSSOP (4-Layer Board)	112.6°C/W
16-Lead LFCSP (4-Layer Board)	30.4°C/W
Reflow Soldering Peak Temperature, Pb-Free	As per JEDEC J-STD-020
ESD (HBM: ESDA/JEDEC JS-001-2011)	
Input/Output Port to Supplies	4 kV
Input/Output Port to Input/Output Port	4 kV
All Other Pins	4 kV

[1] Overvoltages at the Dx pins are clamped by internal diodes. Limit current to the maximum ratings given.
[2] POSFV and NEGFV must not exceed V_{DD} and V_{SS}, respectively.
[3] See Table 5.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

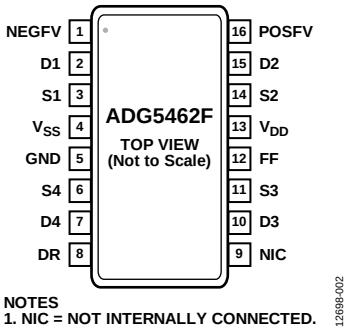


Figure 2. TSSOP Pin Configuration

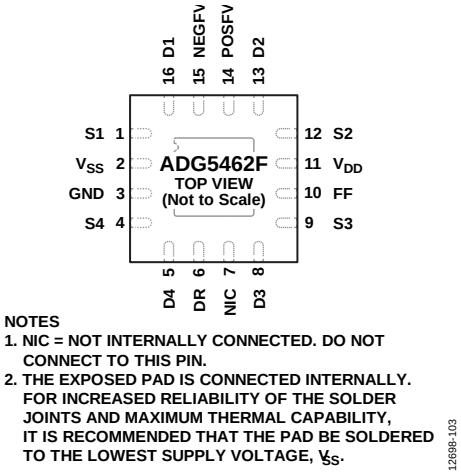


Figure 3. LFCSP Pin Configuration

Table 7. Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
1	15	NEGFV	Negative Fault Voltage. This pin provides the negative supply voltage that determines the overvoltage protection level. If a secondary supply is not used, connect this pin to V_{SS}.
2	16	D1	Drain Terminal 1. This pin can be an input or an output.
3	1	S1	Overvoltage Protected Source Terminal 1. This pin can be an input or an output.
4	2	V_{SS}	Most Negative Power Supply Potential.
5	3	GND	Ground (0 V) Reference.
6	4	S4	Overvoltage Protected Source Terminal 4. This pin can be an input or an output.
7	5	D4	Drain Terminal 4. This pin can be an input or an output.
8	6	DR	Drain Response Digital Input. Tying this pin to GND enables the drain to pull to POSFV or NEGFV during an overvoltage fault condition. The default condition of the drain is open-circuit when the pin is left floating or if it is tied to V_{DD}.
9	7	NIC	Not Internally Connected.
10	8	D3	Drain Terminal 3. This pin can be an input or an output.
11	9	S3	Overvoltage Protected Source Terminal 3. This pin can be an input or an output.
12	10	FF	Fault Flag Digital Output. This pin has a high output (nominally 3 V) when the device is in normal operation or a low output when a fault condition occurs on any of the Sx inputs. The FF pin has a weak internal pull-up that allows the signals to be combined into a single interrupt for larger modules that contain multiple devices.
13	11	V_{DD}	Most Positive Power Supply Potential.
14	12	S2	Overvoltage Protected Source Terminal 2. This pin can be an input or an output.
15	13	D2	Drain Terminal 2. This pin can be an input or an output.
16	14	POSFV	Positive Fault Voltage. This pin provides the positive supply voltage that determines the overvoltage protection level. If a secondary supply is not used, connect this pin to V_{DD}.
	EP	Exposed Pad	The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the lowest supply voltage, V_{SS}.

TYPICAL PERFORMANCE CHARACTERISTICS

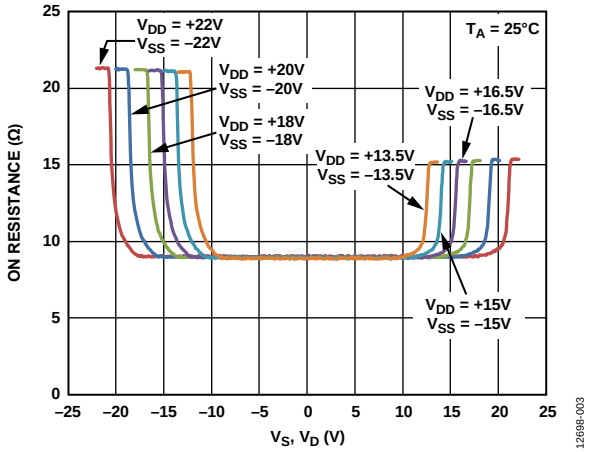


Figure 4. On Resistance (R_{ON}) as a Function of V_S, V_D (Dual Supply)

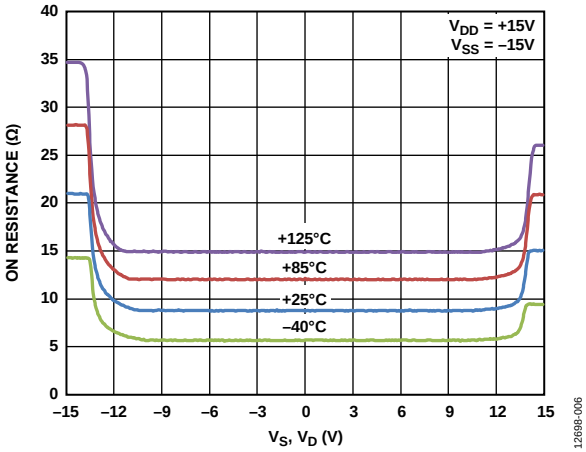


Figure 7. On Resistance (R_{ON}) as a Function of V_S, V_D for Different Temperatures, ±15 V Dual Supply

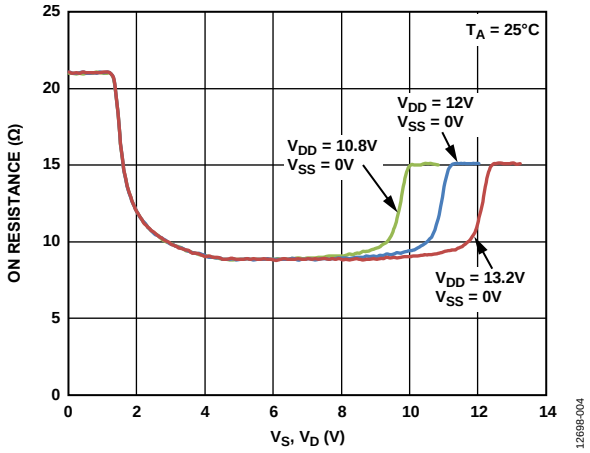


Figure 5. On Resistance (R_{ON}) as a Function of V_S, V_D (12 V Single Supply)

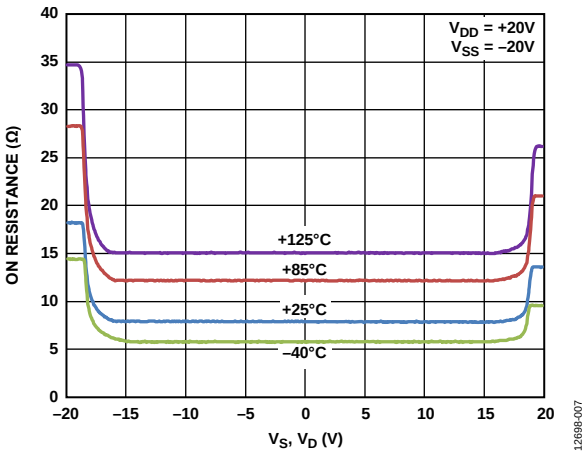


Figure 8. On Resistance (R_{ON}) as a Function of V_S, V_D for Different Temperatures, ±20 V Dual Supply

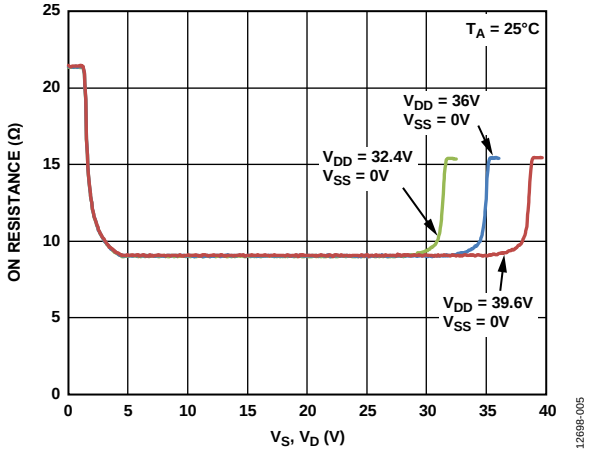


Figure 6. On Resistance (R_{ON}) as a Function of V_S, V_D (36 V Single Supply)

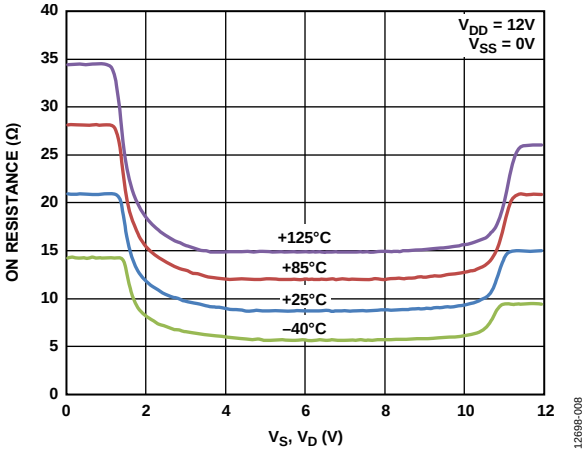


Figure 9. On Resistance (R_{ON}) as a Function of V_S, V_D for Different Temperatures, 12 V Single Supply

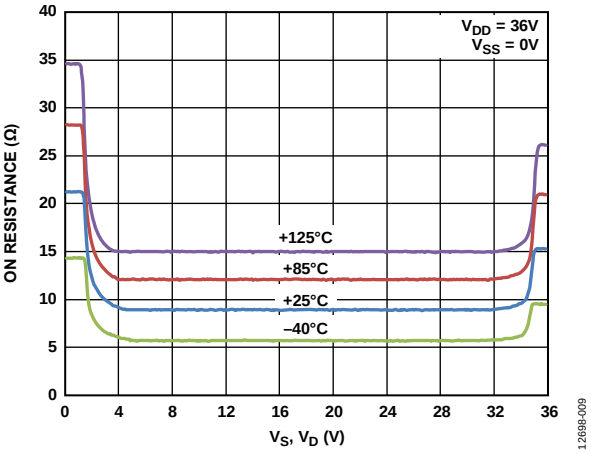


Figure 10. On Resistance (R_{ON}) as a Function of V_S, V_D for Different Temperatures, 36 V Single Supply

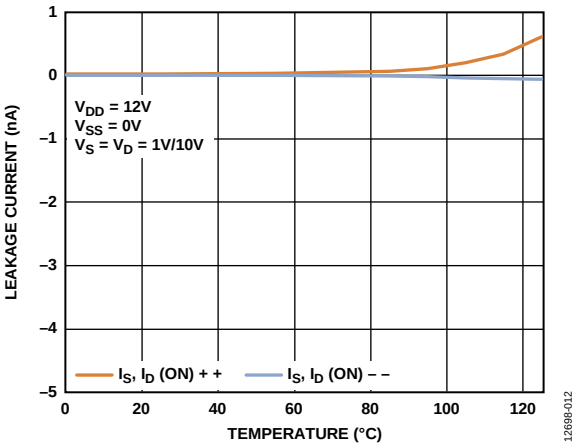


Figure 13. Leakage Current vs. Temperature, 12 V Single Supply

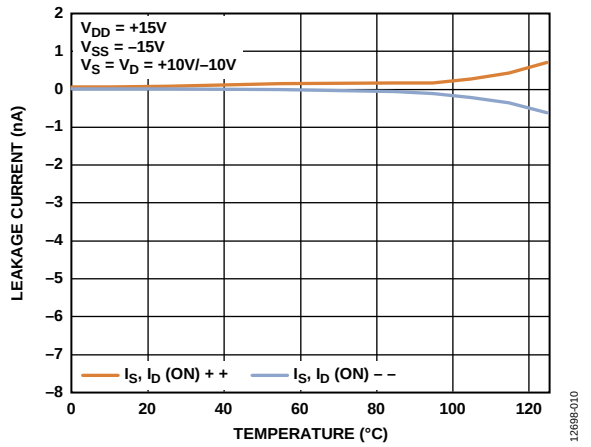


Figure 11. Leakage Current vs. Temperature, ±15 V Dual Supply

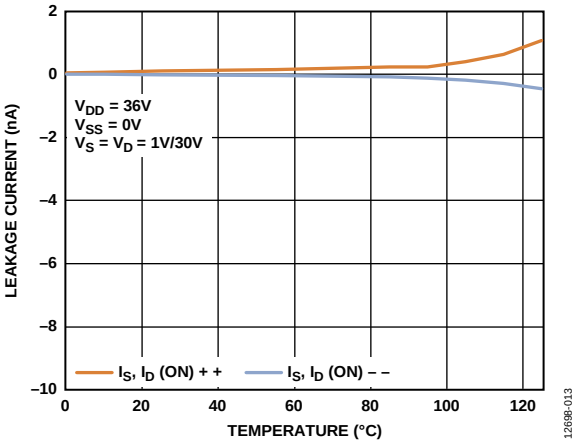


Figure 14. Leakage Current vs. Temperature, 36 V Single Supply

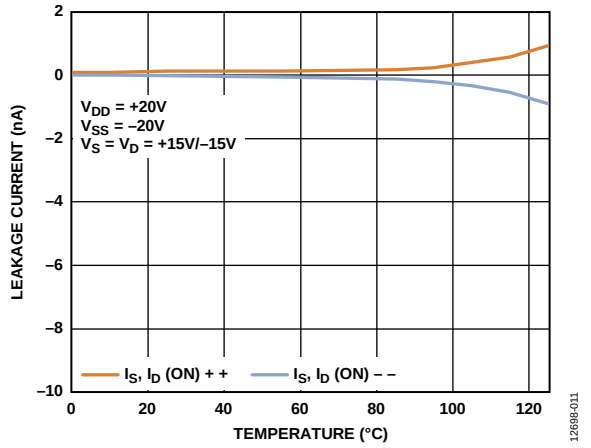


Figure 12. Leakage Current vs. Temperature, ±20 V Dual Supply

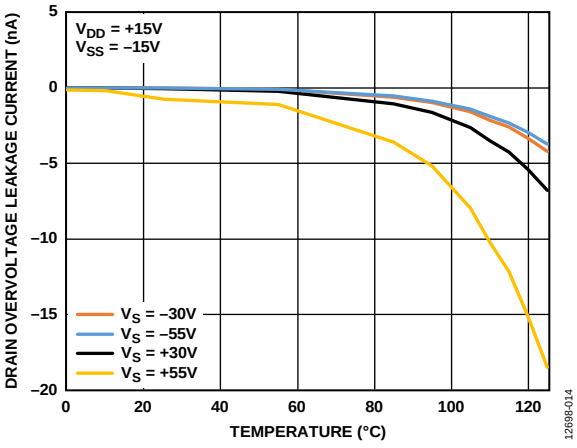


Figure 15. Drain Overvoltage Leakage Current vs. Temperature, ±15 V Dual Supply

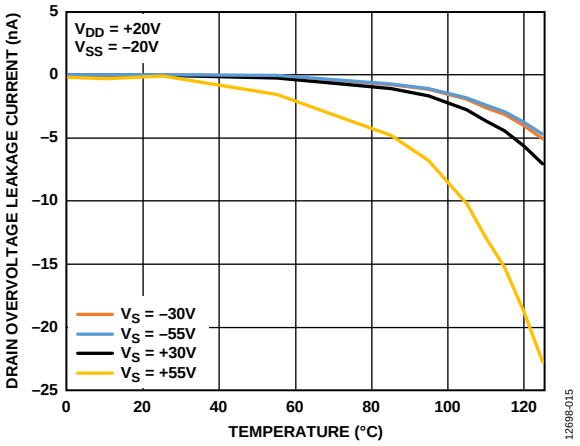


Figure 16. Drain Overvoltage Leakage Current vs. Temperature, ±20 V Dual Supply

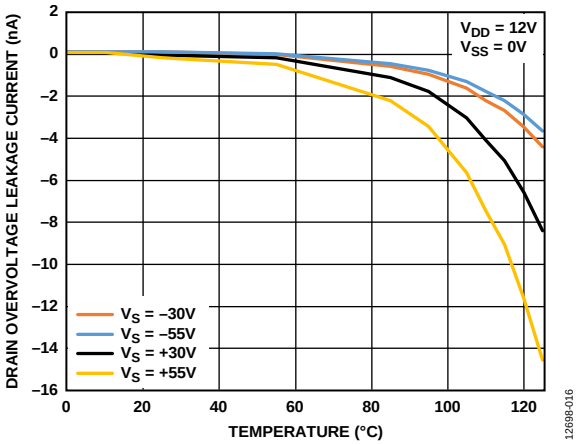


Figure 17. Drain Overvoltage Leakage Current vs. Temperature, 12 V Single Supply

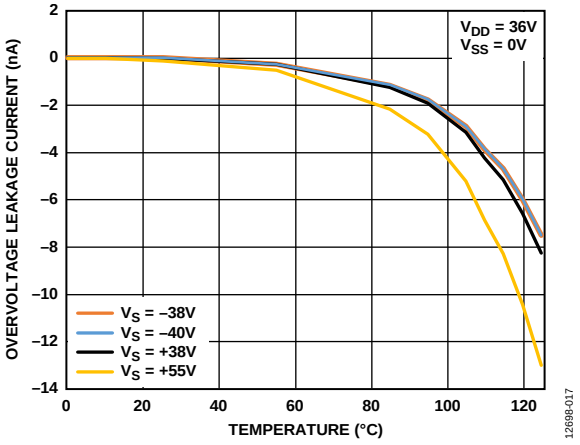


Figure 18. Overvoltage Leakage Current vs. Temperature, 36 V Single Supply

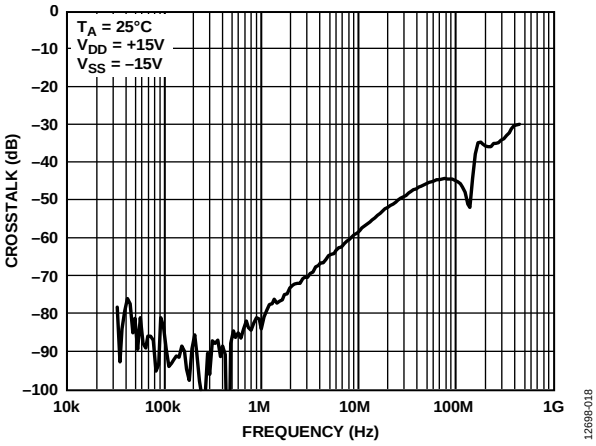


Figure 19. Crosstalk vs. Frequency, ±15 V Dual Supply

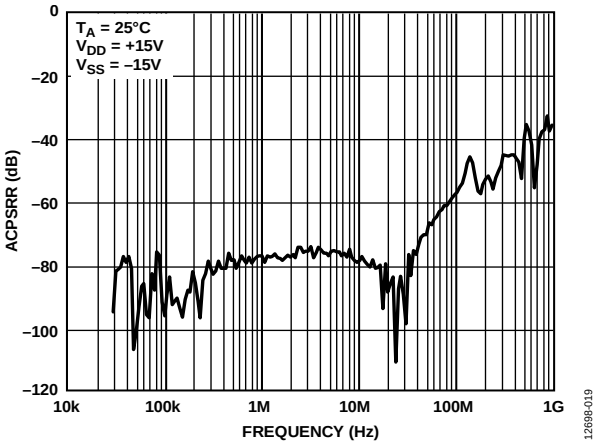


Figure 20. AC Power Supply Rejection Ratio (ACPSRR) vs. Frequency, ±15 V Dual Supply

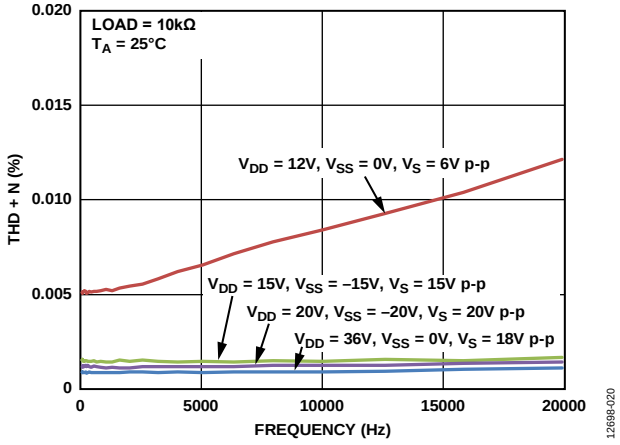


Figure 21. THD + N vs. Frequency, ±15 V Dual Supply

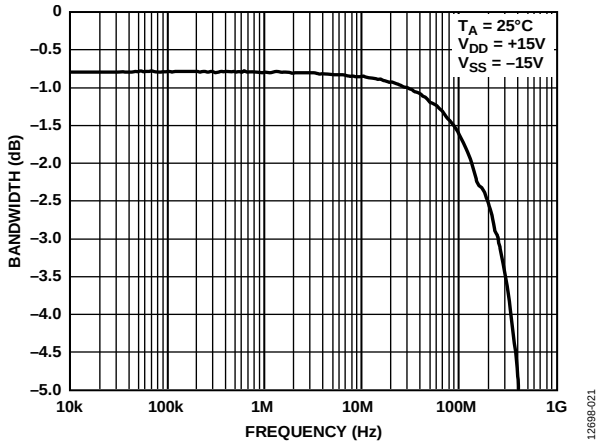


Figure 22. Bandwidth vs. Frequency

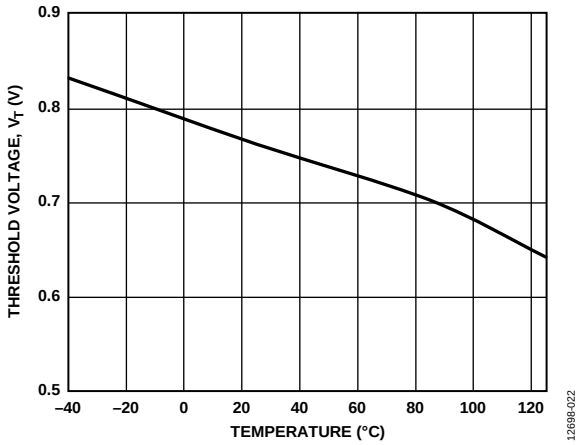


Figure 23. Threshold Voltage (V_T) vs. Temperature

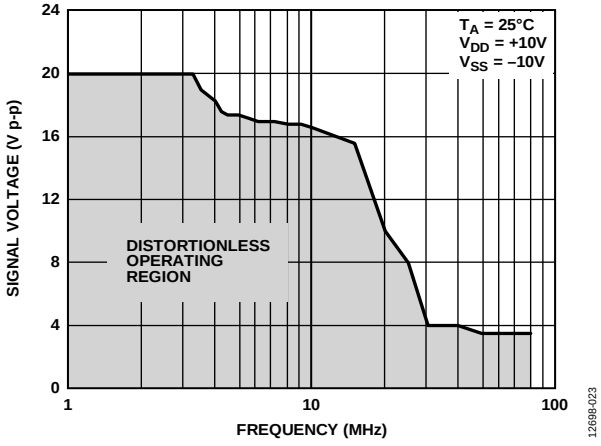


Figure 24. Large Voltage Signal Tracking vs. Frequency

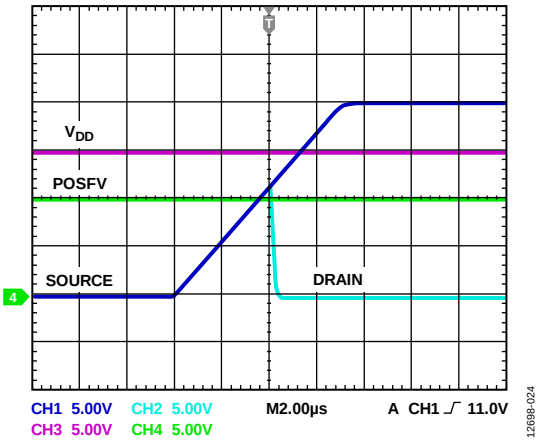


Figure 25. Drain Output Response to Positive Overvoltage (DR = Floating or High)

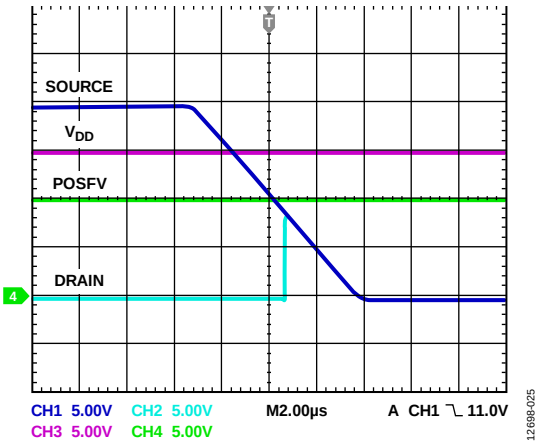


Figure 26. Drain Output Recovery from Positive Overvoltage (DR = Floating or High)

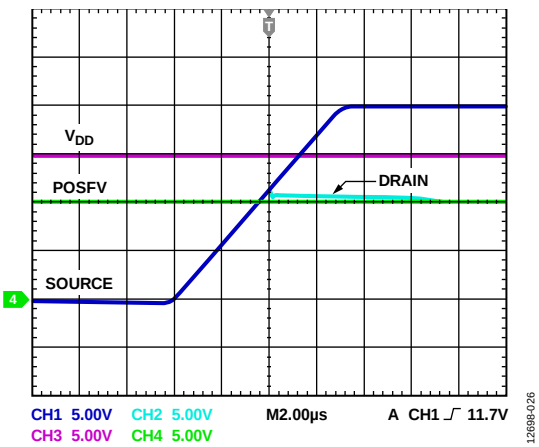


Figure 27. Drain Output Response to Positive Overvoltage (DR = GND)

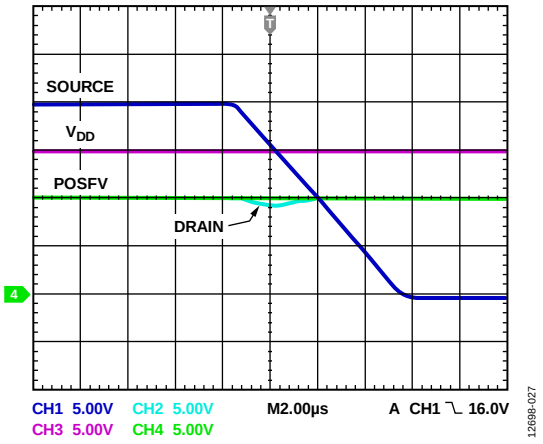


Figure 28. Drain Output Recovery from Positive Overvoltage (DR = GND)

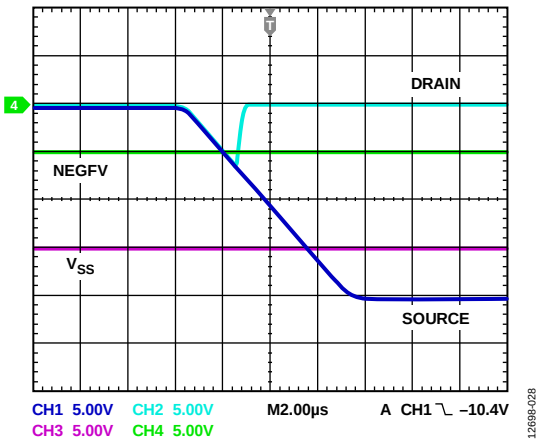


Figure 29. Drain Output Response to Negative Overvoltage (DR = Floating or High)

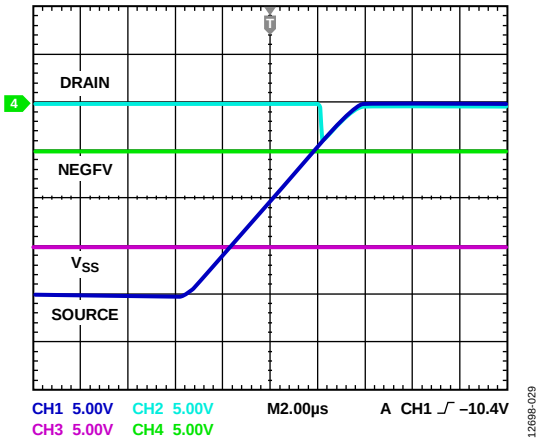


Figure 30. Drain Output Recovery from Negative Overvoltage (DR = Floating or High)

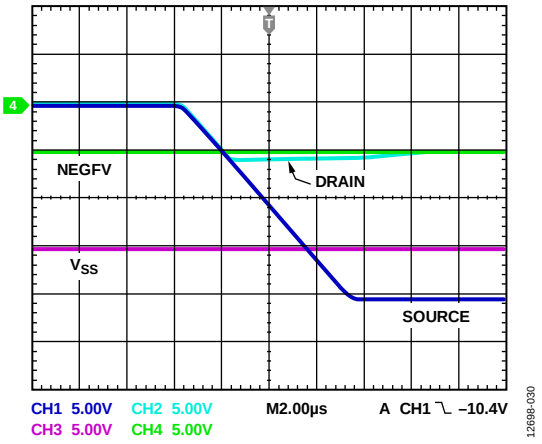


Figure 31. Drain Output Response to Negative Overvoltage (DR = GND)

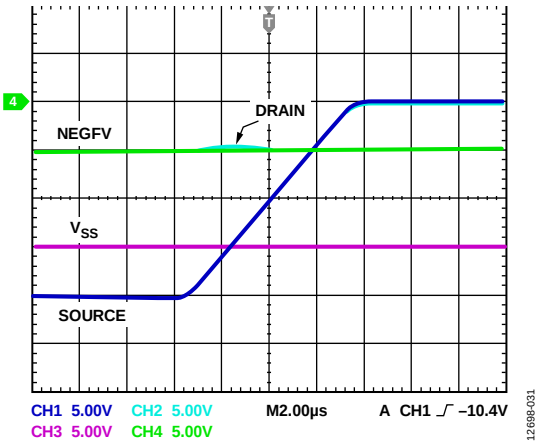


Figure 32. Drain Output Recovery from Negative Overvoltage (DR = GND)

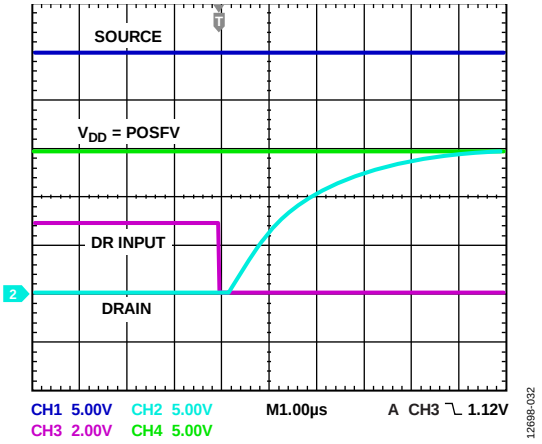


Figure 33. Drain Output Response to Positive Overvoltage (DR = High to Low)

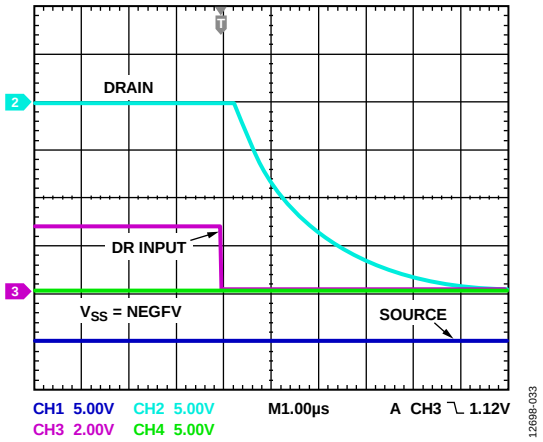


Figure 34. Drain Output Response to Negative Overvoltage (DR = High to Low)

TEST CIRCUITS

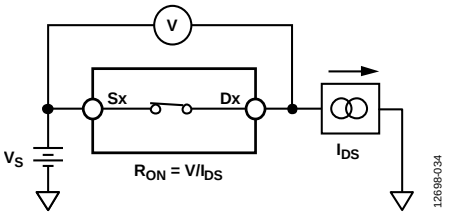


Figure 35. On Resistance

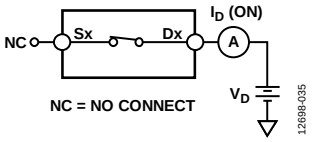


Figure 36. On Leakage

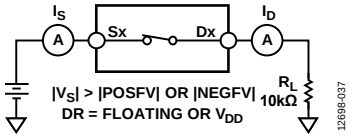


Figure 37. Switch Overvoltage Leakage

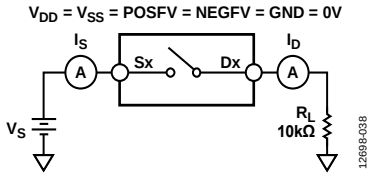


Figure 38. Switch Unpowered Leakage

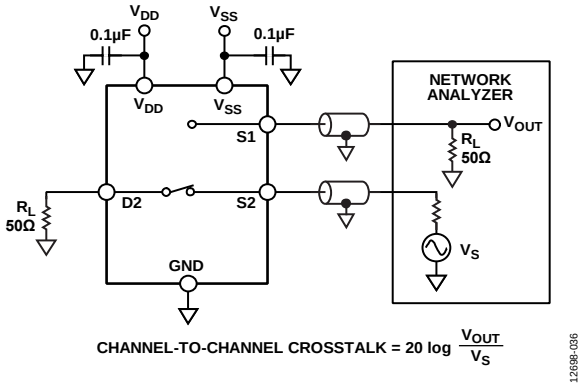


Figure 39. Channel-to-Channel Crosstalk

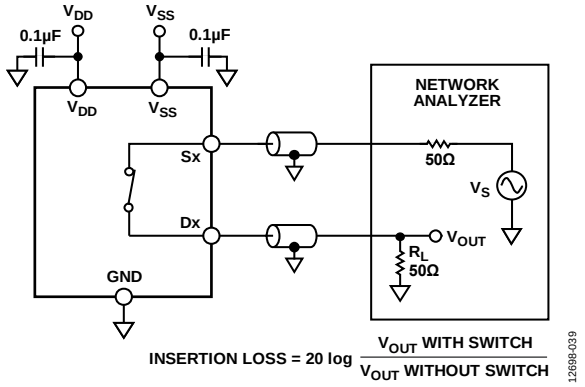


Figure 40. Bandwidth

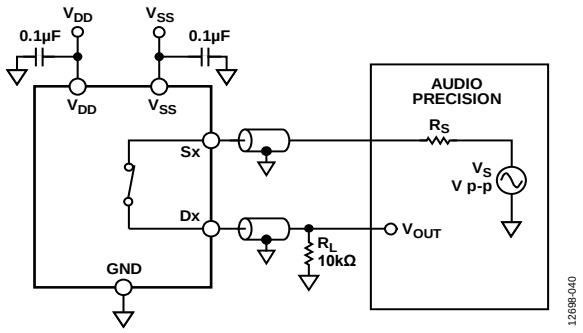


Figure 41. THD + N

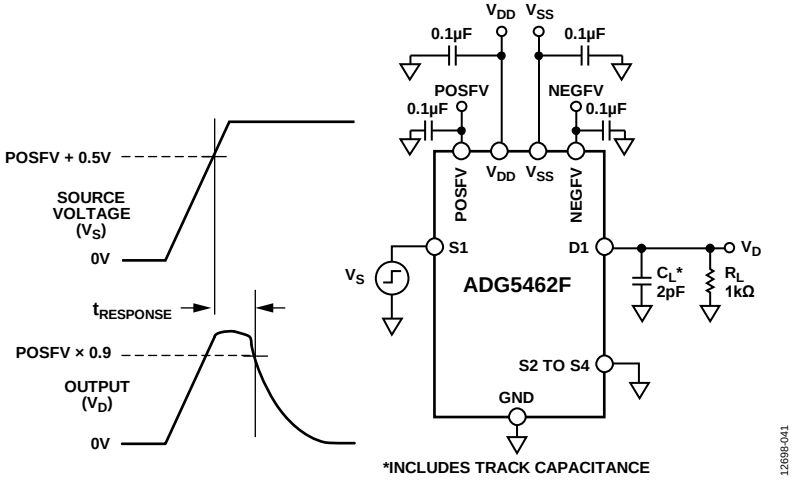


Figure 42. Overvoltage Response Time, $t_{RESPONSE}$

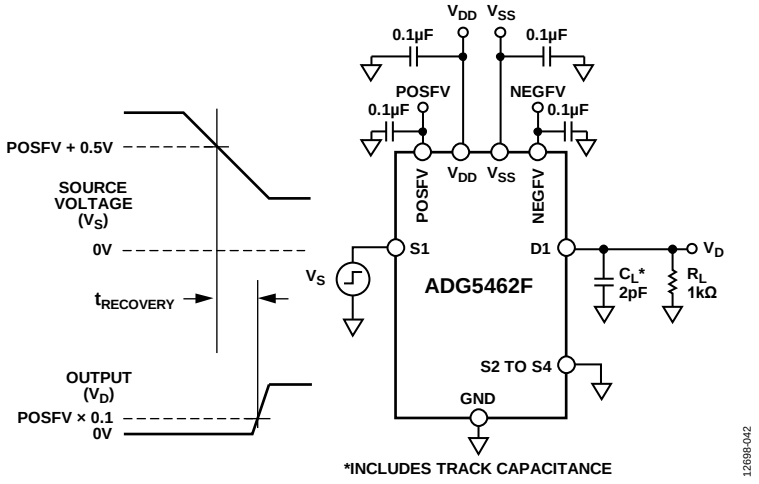


Figure 43. Overvoltage Recovery Time, $t_{RECOVERY}$

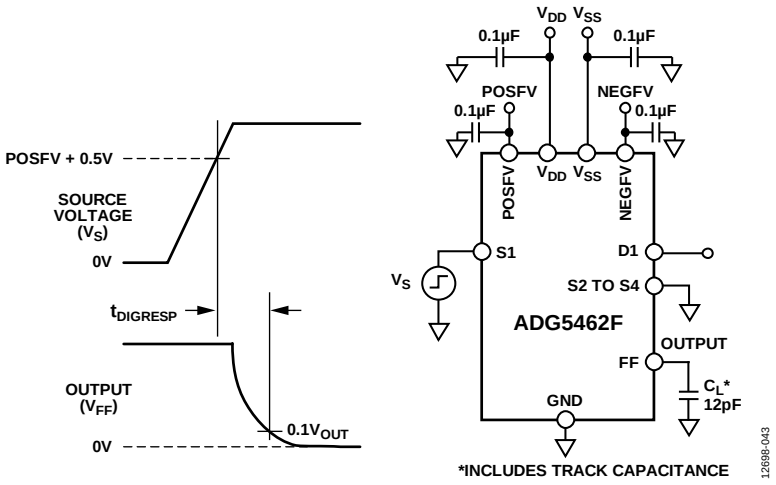


Figure 44. Interrupt Flag Response Time, $t_{DIGRESP}$

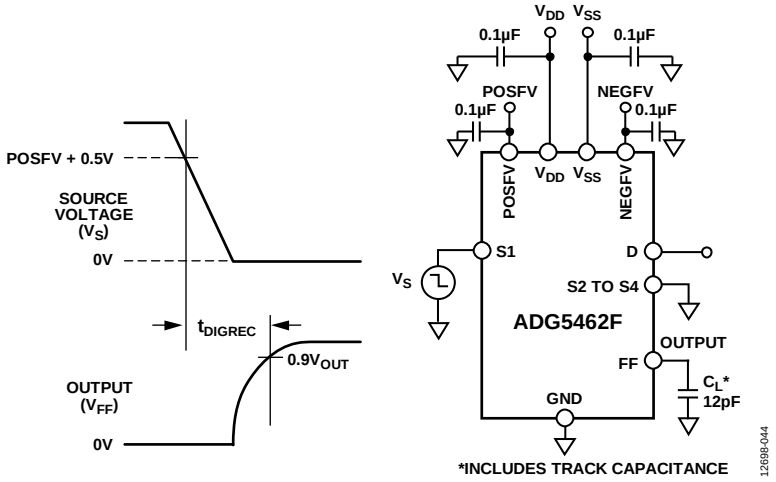


Figure 45. Interrupt Flag Recovery Time, t_{DIGREC}

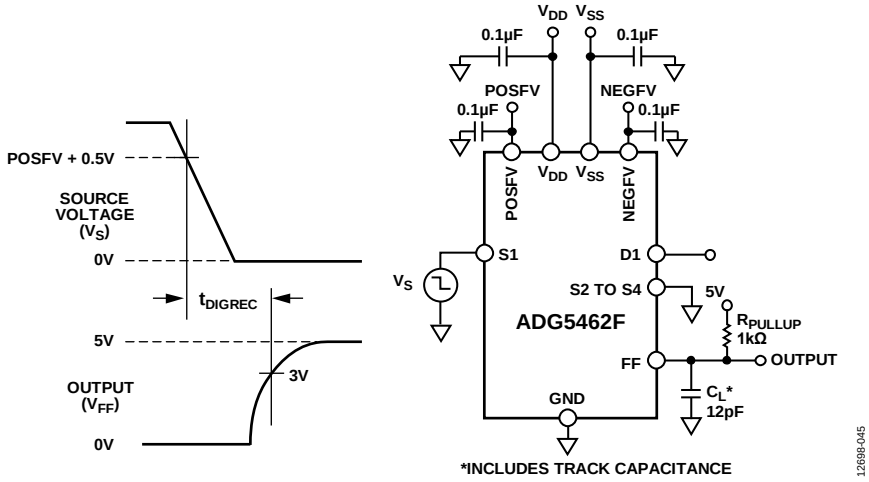


Figure 46. Interrupt Flag Recovery Time, t_{DIGREC}, with a 1 kΩ Pull-Up Resistor

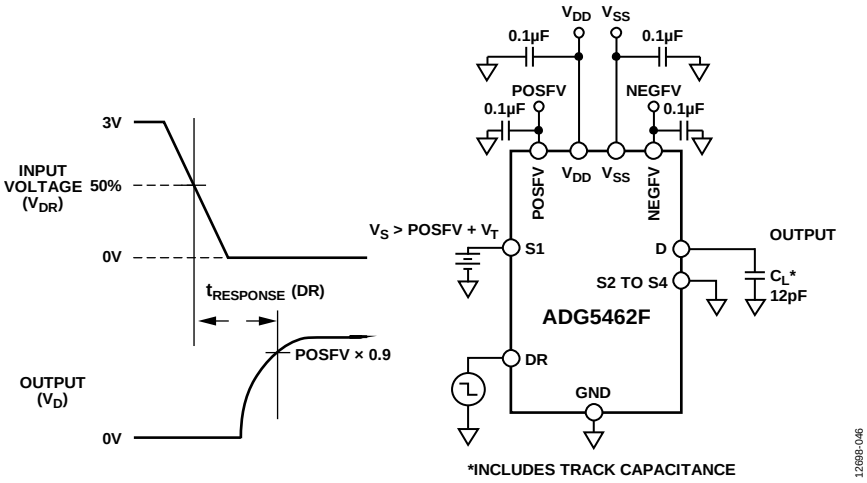


Figure 47. Drain Enable Time with Overvoltage, $t_{RESPONSE}$ (DR)

TERMINOLOGY

I_{DD}
I_{DD} represents the positive primary supply current.

I_{SS}
I_{SS} represents the negative primary supply current.

I_{POSFV}
I_{POSFV} represents the positive secondary supply current.

I_{NEGFV}
I_{NEGFV} represents the negative secondary supply current.

V_D, V_S
V_D and V_S represent the analog voltage on the Dx pins and the Sx pins, respectively.

R_{ON}
R_{ON} represents the ohmic resistance between the Dx pins and the Sx pins.

ΔR_{ON}
ΔR_{ON} represents the difference between the R_{ON} of any two channels.

$R_{FLAT(ON)}$
$R_{FLAT(ON)}$ is the flatness that is defined as the difference between the maximum and minimum value of on resistance measured over the specified analog signal range.

I_D (On), I_S (On)
I_D (On) and I_S (On) represent the channel leakage currents with the switch on.

V_{INL}
V_{INL} is the maximum input voltage for Logic 0.

V_{INH}
V_{INH} is the minimum input voltage for Logic 1.

I_{INL}, I_{INH}
I_{INL} and I_{INH} represent the low and high input currents of the digital inputs.

C_D (On), C_S (On)
C_D (On) and C_S (On) represent the on switch capacitances, which are measured with reference to ground.

C_{IN}
C_{IN} is the digital input capacitance.

$t_{DIGRESP}$
$t_{DIGRESP}$ is the time required for the FF pin to go low (0.3 V), measured with respect to voltage on the source pin exceeding the supply voltage by 0.5 V.

t_{DIGREC}
t_{DIGREC} is the time required for the FF pin to return high, measured with respect to voltage on the Sx pin falling below the supply voltage plus 0.5 V.

$t_{RESPONSE}$
$t_{RESPONSE}$ represents the delay between the source voltage exceeding the supply voltage by 0.5 V and the drain voltage falling to 90% of the supply voltage.

$t_{RECOVERY}$
$t_{RECOVERY}$ represents the delay between an overvoltage on the Sx pin falling below the supply voltage plus 0.5 V and the drain voltage rising from 0 V to 10% of the supply voltage.

$t_{RESPONSE}$ (DR)
$t_{RESPONSE}$ (DR) represents the delay between the voltage at the DR pin falling from a high to low signal and the output of the drain pin reaching 90% of either POSFV or NEGFV

Channel-to-Channel Crosstalk
Crosstalk is a measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

−3 dB Bandwidth
Bandwidth is the frequency at which the output is attenuated by 3 dB.

On Response
On response is the frequency response of the on switch.

Insertion Loss
Insertion loss is the loss due to the on resistance of the switch.

Total Harmonic Distortion Plus Noise (THD + N)
THD + N is the ratio of the harmonic amplitude plus noise of the signal to the fundamental.

AC Power Supply Rejection Ratio (ACPSRR)
ACPSRR is the ratio of the amplitude of signal on the output to the amplitude of the modulation. ACPSRR is a measure of the ability of the device to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p.

V_T
V_T is the voltage threshold at which the overvoltage protection circuitry engages. See Figure 23

THEORY OF OPERATION

SWITCH ARCHITECTURE

Each channel of the ADG5462F consists of a parallel pair of NDMOS and PDMOS transistors. This construction provides excellent performance across the signal range. The ADG5462F channels present only as a typical impedance of 10 Ω when input signals with a voltage between POSFV and NEGFV are applied.

Additional internal circuitry enables the switch to detect overvoltage inputs by comparing the voltage on the source pin (Sx) with POSFV and NEGFV. A signal is considered overvoltage if it exceeds the secondary supply voltages by the voltage threshold (V_T). The threshold voltage is typically 0.7 V, but it ranges from 0.8 V at −40°C down to 0.6 V at +125°C. See Figure 23 to see the change in V_T with operating temperature.

The maximum voltage that can be applied to any source input is −55 V or +55 V. When the device is powered using a single supply of 25 V or greater, the maximum negative signal level is reduced. It reduces from −55 V at V_{DD} = +25 V to −40 V at V_{DD} = +40 V to remain within the 80 V maximum rating. Construction of the silicon process allows the channel to withstand 80 V across the switch when it is opened. These overvoltage limits apply whether the power supplies are present or not.

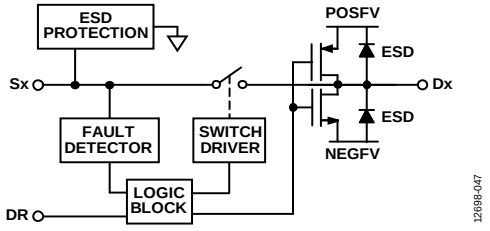


Figure 48. Switch Channel and Control Function

When an overvoltage condition is detected on a source pin (Sx), the switch automatically opens and the source pin (Sx) becomes high impedance and ensures that no current flows through the switch. If the DR pin is driven low, the drain pin (Dx) is pulled to the supply that was exceeded. For example, if the source voltage exceeds POSFV, the drain output pulls to POSFV. The same is true for NEGFV. In Figure 27, the voltage on the drain pin (Dx) clamps to the POSFV voltage when the source voltage exceeds POSFV by V_T. If the DR pin is allowed to float or is driven high, the drain pin (Dx) also goes open circuit. In Figure 25, the voltage on the drain pin (Dx) follows the voltage on the source pin (Sx) until the switch turns off completely and the drain voltage discharges through the load. The output response for each drain pin configuration is shown in Figure 49. The maximum voltage on the drain is limited by the internal ESD diodes and the rate at which the output voltage discharges is dependent on the load at the pin.

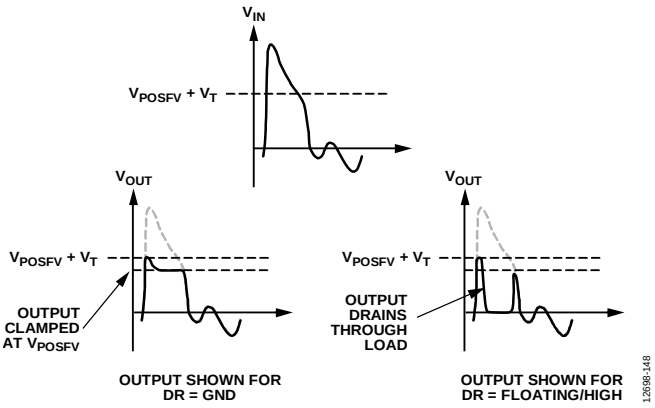


Figure 49. Drain Output Response During Overvoltage Condition

During overvoltage conditions, the leakage current into and out of the source pins (Sx) is limited to tens of microamperes. If the DR pin is allowed to float or is driven high, only nanoamperes of leakage are seen on the drain pins (Dx). If the DR pin is driven low, the drain pin (Dx) is pulled to the rail. The device that pulls the drain pin to the rail has an impedance of approximately 40 kΩ; therefore, the Dx pin current is limited to about 1 mA during a shorted load condition. This internal impedance also determines the minimum external load resistance required to ensure that the drain pin is pulled to the desired voltage level during a fault.

When an overvoltage event occurs, the channels undisturbed by the overvoltage input continue to operate normally without additional crosstalk.

ESD Performance

The ADG5462F has an ESD rating of 4 kV for the human body model.

The drain pins (Dx) have ESD protection diodes to the secondary supply rails, and the voltage at these pins must not exceed the secondary supply voltage.

The source pins (Sx) have specialized ESD protection that allows the signal voltage to reach ±55 V with a ±22 V dual supply, and from −40 V to +55 V with a +40 V single supply. See Figure 48 for the switch channel overview. Exceeding ±55 V on any source input may damage the ESD protection circuitry on the device.

Trench Isolation

In the ADG5462F, an insulating oxide layer (trench) is placed between the NDMOS and the PDMOS transistors of each channel. Parasitic junctions, which occur between the transistors in junction isolated switches, are eliminated, and the result is a switch that is latch-up immune under all circumstances. This device passes a JESD78D latch-up test of ±500 mA for 1 sec, which is the harshest test in the specification.

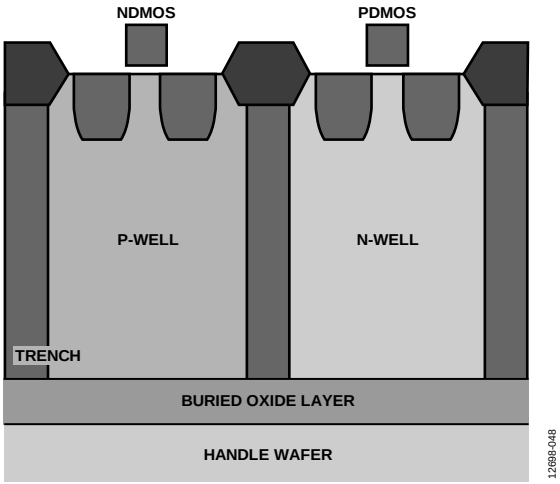


Figure 50. Trench Isolation

USER DEFINED FAULT PROTECTION

POSFV and NEGFV are required secondary power supplies that set the level at which the overvoltage protection is engaged. POSFV can be supplied from 4.5 V up to V_{DD}, and NEGFV can be supplied from V_{SS} to 0 V. If a secondary supply is not available, these pins (POSFV and NEGFV) must be connected to V_{DD} (POSFV) and V_{SS} (NEGFV). The overvoltage protection then engages at the primary supply voltages. When the voltages at the source inputs exceed POSFV or NEGFV by V_T, the channel turns off or, if the device is unpowered, the channel remains off. The source input remains high impedance, and if the DR pin is driven low, the drain pulls to either POSFV or NEGFV. Signal levels up to −55 V and +55 V are blocked in both the powered and unpowered condition as long as the 80 V limitation between the source and supply pins is met.

Power-On Protection

For the channel to be in the on condition, the following three conditions must be satisfied:

- The primary supply must be V_{DD} to $V_{SS} \geq 8$ V.
- For POSFV, the secondary supply must be between 4.5 V and V_{DD}, and for NEGFV, the secondary supply must be between V_{SS} and 0 V.
- The input signal must be between NEGFV − V_T and POSFV + V_T.

When the channel is on, signal levels up to the secondary supply rails are passed.

The channel responds to an analog input that exceeds POSFV or NEGFV by a threshold voltage (V_T) by turning off. The absolute input voltage limits are −55 V and +55 V, while maintaining an 80 V limit between the source pin (Sx) and the supply rails. The switch remains off until the voltage at the source pin (Sx) returns to between POSFV and NEGFV.

The fault response time ($t_{RESPONSE}$) when powered by a ±15 V dual supply is typically 460 ns, and the fault recovery time ($t_{RECOVERY}$) is 720 ns. These values vary with supply voltage and output load conditions.

The maximum stress across the channel and between the source pin (Sx) and any supply pin is 80 V; therefore, pay close attention to this limit if using the device in a single-supply configuration and a negative overvoltage is applied to the device.

For example, consider the case where the device is set up in a single supply configuration, as shown in Figure 51.

- V_{DD} = POSFV = 36 V, V_{SS} = NEGFV = GND = 0 V
- S1 = +36 V, S2 = +5 V, and S3 = −40 V
- The voltage difference from S1 to V_{DD}/POSFV = 0 V, and to V_{SS}/NEGFV = 36 V
- The voltage difference from S2 to V_{DD}/POSFV = 31 V, and to V_{SS}/NEGFV = 5 V
- The voltage difference from S3 to V_{DD}/POSFV = 76 V, and to V_{SS}/NEGFV = 40 V

These calculations are all within device specifications: 55 V maximum fault on source inputs and a maximum of 80 V across the channel or to a supply pin. The voltage on a source pin (Sx) cannot go below −44 V to stay within +80 V maximum.

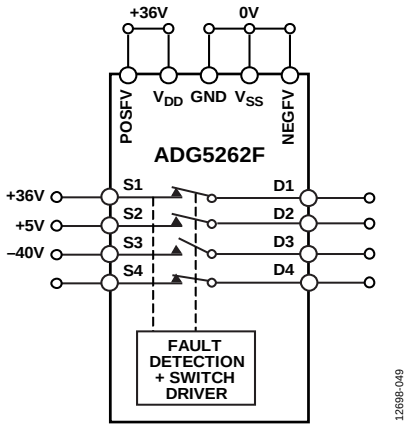


Figure 51. ADG5462F in Single-Supply Configuration Under Overvoltage Conditions

Power-Off Protection

When no power supplies are present, the channel remains in the off condition, and the switch inputs are high impedance. This state ensures that no current flows and prevents damage to the switch or downstream circuitry. The switch output is a virtual open circuit.

The switch remains off regardless of whether the primary and secondary supplies are 0 V or floating. A GND reference must always be present to ensure proper operation. Signal levels of up to ±55 V are blocked in the unpowered condition.

Digital Input Protection

The ADG5462F can tolerate digital input signals being present on the device without power. The digital input is protected against positive faults up to 44 V. The digital input does not offer protection against negative overvoltages. ESD protection diodes connected to GND are present on the digital input.

Overvoltage Interrupt Flag

The voltages on the source inputs of the ADG5462F are continuously monitored, and an active low digital output pin (FF) indicates the state of the switches.

The voltage on the FF pin indicates if any of the source input pins are experiencing a fault condition. The output of the FF pin is a nominal 3 V when all source pins (Sx) are within normal operating range. If any source pin (Sx) voltage exceeds the supply voltage by V_T, the FF output reduces to below 0.8 V.

APPLICATIONS INFORMATION

The overvoltage protected family of switches and multiplexers provide robust solutions for instrumentation, industrial, automotive, aerospace, and other harsh environments where overvoltage signals can be present, and the system must remain operational both during and after the overvoltage has occurred.

POWER SUPPLY RAILS

To guarantee correct operation of the device, 0.1 µF decoupling capacitors are required on the primary and secondary supplies. If they are driven from the same supply, then one set of 0.1 µF decoupling capacitors is sufficient.

The secondary supplies (POSFV and NEGFV) provide the current required to operate the fault protection and, therefore, must be low impedance supplies. Therefore, they can be derived from the primary supply by using a resistor divider and buffer.

The secondary supply rails (POSFV and NEGFV) must not exceed the primary supply rails (V_{DD} and V_{SS}) because this can lead to a signal passing through the switch unintentionally.

The ADG5462F can operate with bipolar supplies between ±5 V and ±22 V. The supplies on V_{DD} and V_{SS} need not be symmetrical but the V_{DD} and V_{SS} range must not exceed 44 V. The ADG5462F can also operate with single supplies between 8 V and 44 V with V_{SS} connected to GND.

The ADG5462F is fully specified at ±15 V, ±20 V, +12 V, and +36 V supply ranges.

POWER SUPPLY SEQUENCING PROTECTION

The channels remain open when the device is unpowered and signals from −55 V to +55 V can be applied without damaging the device. Only when the supplies are connected, and the signal is within normal operating range, do the channels close. Placing the ADG5462F between external connectors and sensitive components offers protection in systems where a signal is presented to the source pins (Sx) before the supply voltages are available.

POWER SUPPLY RECOMMENDATIONS

Analog Devices, Inc., has a wide range of power management products to meet the requirements of most high performance signal chains.

An example of a bipolar power solution is shown in Figure 52. The ADP7118 and ADP7182 can be used to generate clean positive and negative rails from the dual switching regulator output. These rails can power the ADG5462F, an amplifier, and/or a precision converter in a typical signal chain.

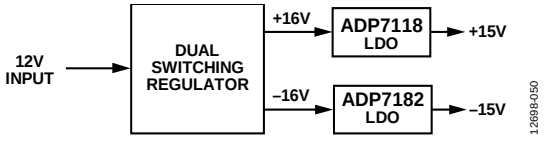


Figure 52. Bipolar Power Solution

Table 8. Recommended Power Management Devices

Product	Description
ADP7118	20 V, 200 mA, low noise, CMOS low dropout regulator (LDO)
ADP7142	40 V, 200 mA, low noise, CMOS LDO
ADP7182	−28 V, −200 mA, low noise, linear regulator

USER DEFINED SIGNAL RANGE

The primary supplies define the on-resistance profile of the channels, while the secondary supplies define the signal range. Using voltages on POSFV and NEGFV that are lower than V_{DD} and V_{SS}, the required signal can benefit from the flat on resistance in the center of the full signal capabilities of the device.

LOW IMPEDANCE CHANNEL PROTECTION

The ADG5462F can be used as a protective element in signal chains that are sensitive to both channel impedance and overvoltage signals. Traditionally, series resistors are used to limit the current during an overvoltage condition to protect susceptible components.

These series resistors affect the performance of the signal chain and reduce the precision that can be reached. A compromise must be reached on the value of the series resistance that is high enough to sufficiently protect sensitive components but low enough that the precision performance of the signal chain is not sacrificed.

The ADG5462F enables the designer to remove these resistors and retain the precision performance without compromising the protection of the circuit.

HIGH VOLTAGE SURGE SUPPRESSION

The ADG5462F is not intended for use in very high voltage applications. The maximum operating voltage of the transistor is 80 V. In applications where the inputs are likely to be subject to overvoltages exceeding the breakdown voltage, use transient voltage suppressors (TVSs) or similar.

INTELLIGENT FAULT DETECTION

The ADG5462F digital output pin (FF) can interface with a microprocessor or control system and be used as an interrupt flag. This feature provides real-time diagnostic information on the state of the device and the system to which it connects.

The control system can use the digital interrupt to start a variety of actions, such as

- Initiating investigation into the source of the overvoltage fault
- Shutting down critical systems in response to the overvoltage
- Signaling the data recorders to mark data during these events as unreliable or out of specification

For systems that are sensitive during a start-up sequence, the active low operation of the flag allows the system to ensure that the ADG5462F is powered on and that all input voltages are within normal operating range before initiating operation.

The FF pin is a weak pull-up, which allows the signals to be combined into a single interrupt for larger modules that contain multiple devices.

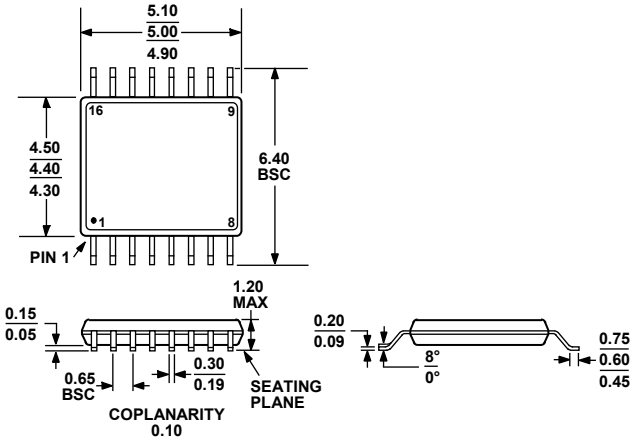
The interrupt flag recovery time, t_{DIGREC}, can be decreased from a typical 60 µs to 600 ns by using a 1 kΩ pull-up resistor.

The DR pin can also be used for diagnostic purposes. The FF pin provides an interrupt that indicates one of the four channels has a fault. The DR pin can then be pulled low to find which of the channels has a fault as well as the polarity of the fault. For example, if an ADC downstream is monitoring the channel, a full-scale reading then indicates a positive fault, and a zero-scale reading indicates a negative fault.

LARGE VOLTAGE, HIGH FREQUENCY SIGNALS

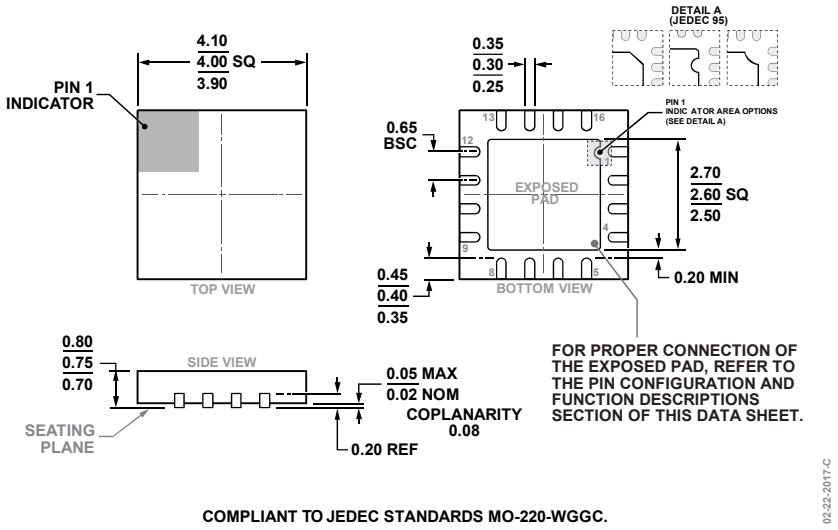
Figure 24 illustrates the voltage range and frequencies that the ADG5462F can reliably convey. For signals that extend across the full signal range from V_{SS} to V_{DD}, keep the frequency less than 3 MHz. If the required frequency is greater than 3 MHz, decrease the signal range appropriately to ensure signal integrity.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 53. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WGGC.

Figure 54. 16-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-16-17)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADG5462FBRUZ	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG5462FBRUZ-RL7	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG5462FBCPZ-RL7	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-17
EVAL-ADG5426FEBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

Стандарт Электрон Связь

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