



A. HE89410 Introduction

HE89410 is a member of 8-bit Micro-controller series used for telephone communication developed by King Billion Electronics Ltd. The built-in DTMF generator can generate the PSTN dialing tone directly. It can be applicable as Small/ Medium class telephone or communication product etc..

The instruction set of HE89410 are quite easy to learn and simple to use. Only about thirty instructions with four-type addressing mode are provided. Most of instructions take only 3 oscillator clocks (machine cycles). The processing power is enough to most of battery operation system.

B. HE89410 Features

- Operation Voltage : 2.4V – 5.5V
- System Clock : DC ~ 8MHz @ 5.0V
- DC ~ 4MHz @ 2.4V
- Internal ROM : 4K Bytes(4K Program ROM)
- Internal RAM : 256 Bytes.
- Dual Clock System : Normal (Fast) clock : 32.768K ~ 8MHz
- Slow clock : 32.768KHz
- Operation Mode : DUAL、FAST、SLOW、IDLE、SLEEP Mode.
- With WDT (WATCH DOG TIMER) to prevent deadlock condition..
- 12 bit Bi-directional I/O port. Mask Option can select PUSH-PULL or OPEN DRAIN output mode for each I/O pin.
- Built-in DTMF Generator.
- Two external interrupts and three internal timer interrupts.
- Two 16-bit timers and one Time Base timer.
- Instruction set : 32 instructions, 4 addressing mode. 8-bit DATA POINTER for RAM and 12-bit TABLE POINTER for ROM.

C. Internal Block

Please always take in mind that ICE is different from IC. ICE is the whole set of HE80000 series IC, but each IC is a subset of ICE. Never use any hardware resource that real IC didn't have, especially RAM and register. KBIDS and compiler cannot prevent user to use some hardware resource that didn't exist. Please check the following table and refer the abbreviation in HE80000 user's manual.

I.F.C.	E.S.C.	I.P.R	PROM	DROM	TP	TP+1	RAM	PP	DP	I/O	DTMF	WDT	Timer
⊙	⊙	⊙	4KB	—	12-bit	⊙	256B	—	8-bit	12	⊙	⊙	T1,T2,TB
VO	DAO	OP	PWM	LCD	COM*SEG	Bias	Rgr	ChrgPmp	LV2	LR	LVG	REC	S.R.
—	—	—	—	—	—	—	—	—	—	—	—	—	—

D. Pin Description

Pin #	Pin name	I/O	Function	Description
27 26	FXI, FXO	B, O	External fast clock pin. Connecting to crystal or RC to generate 32.768 kHz ~ 8MHz frequency.	Mask option setting : MO_FCK/SCKN= 00 : Slow Clock only 01 : Illegal 10 : Dual Clock 11 : Fast Clock only
30 29	SXI, SXO	I, O	External slow clock pin. Connecting with 32768 Hz crystal or resistor as slow clock and providing clock source for LCD display, TIMER1, Time-Base and other internal blocks.	MO_FOSCE = 0 : Internal fast osc. = 1 : External fast osc. MO_FXTAL = 0 : RC osc. for fast clock = 1 : X'tal osc. for fast clock MO_SXTAL = 0 : RC for 32768 Hz clock = 1 : X'tal for 32768 Hz clock Use OP1 and OP2 to switch among different operation mode (NORMAL, SLOW, IDEL and SLEEP). In Dual Clock mode, the main system clock is still the Fast Clock. The 32768 Hz clock is for LCD and Timer 1 only.
25	RSTP_N	I	System Reset.	Level trigger, active low. Except for using this pin, using mask option (MO_PORE=1) could enable IC build-in Power-on reset circuit. Besides, MO_WDTE can set Watch Dog Timer : MO_WDTE=0 : Disable Watch Dog Timer =1 : Enable Watch Dog Timer
28	TSTP_P	I	Test Pin	Please bond this pin and add a test point on PCB for debugging. Leave this pin floating is OK.
12..15	PRTC[3:0]	B	4-pin bi-directional I/O port.	Mask options : MO_CPP[3..0]=1 ~ Push-pull. =0 ~ Open-drain. Output must be "1" before reading whenever use them as input (No tri-state structure).
36 1..7	PRTD[7:0]	B	8-pin bi-directional I/O port. PRTD[7..2] as wake-up pin. PRTD[7..6] as external interrupt pin.	Mask options : MO_DPP[7..0]=1 ~ Push-pull. =0 ~ Open-drain. Output must be "1" before reading whenever use them as input (No tri-state structure).
33	DTMFO	O	DTMF Output	Through PRT12 we can turn on/off DTMF and write data. Using Mask Option MO_DTMFSCK set the clock source of DTMF block. MO_DTMFSCK=0 ; Clock Source=3.579545 MHz =1 ; Clock Source=32768 Hz
32	MUTE	O	MUTE Output for Dialer	User can turn on/off MUTE pin by port12.
34	SDO	O	Serial Data Output	We can turn on/off SDO block or write data by port12.
35	KEYTONE	O	1024-Hz 50% duty square wave	User can turn on/off key tone by port12.
31	VDD	P	Positive Power Input	Adding 0.1 μ F capacitor as by-pass capacitor is between VDD and GND is necessary.
24	GND	P	Power Ground Input	



F. Pin Diagram

PIN Number	PIN Name	X Coordinate	Y Coordinate
1	PRTD[6]	X= -929.05	Y= 551.25
2	PRTD[5]	X= -929.05	Y= 435.75
3	PRTD[4]	X= -929.05	Y= 320.25
4	PRTD[3]	X= -929.05	Y= 204.75
5	PRTD[2]	X= -929.05	Y= 89.25
6	PRTD[1]	X= -929.05	Y= -26.25
7	PRTD[0]	X= -929.05	Y= -141.75
12	PRTC[3]	X= 210.35	Y= -910.45
13	PRTC[2]	X= 325.85	Y= -910.45
14	PRTC[1]	X= 441.35	Y= -910.45
15	PRTC[0]	X= 556.85	Y= -910.45
24	GND	X= 927.10	Y= -45.75
25	RSTP_N	X= 927.10	Y= 69.75
26	FXO	X= 927.10	Y= 185.25
27	FXI	X= 927.10	Y= 300.75
28	TSTP_P	X= 403.00	Y= 909.10
29	SXO	X= 287.50	Y= 909.10
30	SXI	X= 172.00	Y= 909.10
31	VDD	X= 56.50	Y= 909.10
32	MUTE	X= -59.00	Y= 909.10
33	DTMFO	X= -174.50	Y= 909.10
34	SDO	X= -290.00	Y= 909.10
35	KEYTONE	X= -405.50	Y= 909.10
36	PRTD[7]	X= -520.95	Y= 909.10

G. 電氣特性

Absolute Maximum Rating

Item	Sym.	Rating	Condition
Supply Voltage	V_{dd}	$-0.5V \sim 8V$	
Input Voltage	V_{in}	$-0.5V \sim V_{dd}+0.5V$	
Output Voltage	V_o	$-0.5V \sim V_{dd}+0.5V$	
Operating Temperature	T_{op}	$0^{\circ}C \sim 70^{\circ}C$	
Storage Temperature	T_{st}	$-50^{\circ}C \sim 100^{\circ}C$	

Recommended Operating Conditions

Item	Sym.	Rating	Condition
Supply Voltage	V_{dd}	$2.4V \sim 5.5V$	
Input Voltage	V_{ih}	$0.9 V_{dd} \sim V_{dd}$	
	V_{il}	$0.0V \sim 0.1V_{dd}$	
Operating Frequency	F_{max}	8MHz	$V_{dd}=5.0V$
		4MHz	$V_{dd}=2.4V$
Operating Temperature	T_{op}	$0^{\circ}C \sim 70^{\circ}C$	
Storage Temperature	T_{st}	$-50^{\circ}C \sim 100^{\circ}C$	

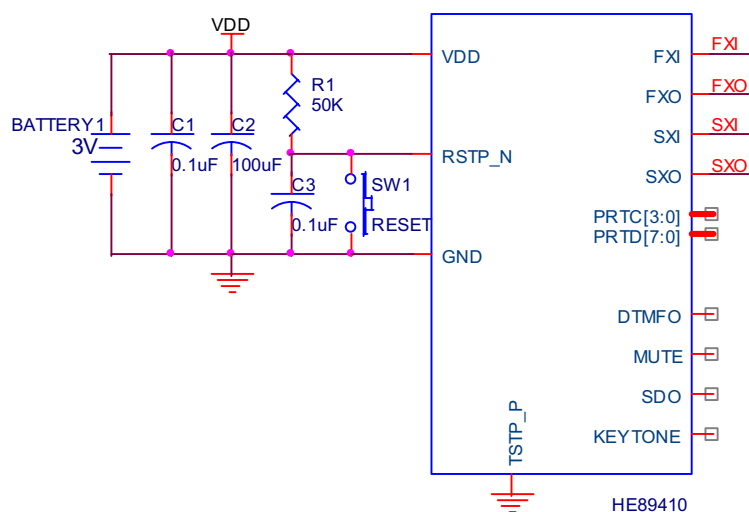
Test Condition: TEMP=25°C, VDD=3V+/-10%, GND=0V

	PARAMETER		CONDITION	MIN	TYP	MAX	UNIT
I_{Fast}	NORMAL Mode Current	System	2M ext. R/C		0.75	1	mA
I_{Slow}	SLOW Mode Current	System	32.768K X'tal		6	9	μA
I_{Idle}	IDLE Mode Current	System	32.769K X'tal		4	7	μA
I_{Sleep}	Sleep Mode Current	System				1	μA
V_{iH}	Input High Voltage	I/O pins		0.8 V_{DD}			V
V_{iL}	Input Low Voltage	I/O pins				0.2 V_{DD}	V
V_{hys}	Input Hysteresis Width	I/O, RSTP_N	Threshold=2/3 V_{DD} (input from low to high) Threshold=1/3 V_{DD} (input from high to low)		1/3 V_{DD}		V
I_{oH}	Output Drive Current	I/O pull-high ^{*1}	$V_{oL}=2.0V$	50			μA
$I_{oL\ 1}$	Output Sink Current	I/O pull-low ^{*1}	$V_{oL}=0.4V$	1.0			mA
$I_{iL\ 1}$	Input Low Current	RSTP_N	$V_{iL}=GND$, pull high Internally		20		μA
$I_{iL\ 2}$	Input Low Current	I/O	$V_{iL}=GND$, if pull high Internally by user		100		μA

Note: *1: Drive Current Spec. for Push-Pull I/O port only

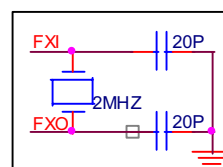
Sink Current Spec. for both Push-Pull and Open-Drain I/O port.

H. Application Circuit

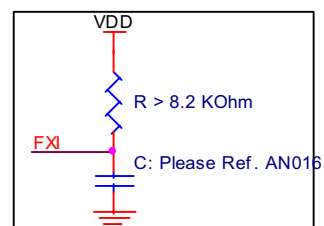


No External Parts is necessary if user adopt Internal Fast RC Clock

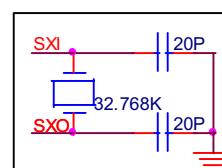
External Fast Clock:
Crystal osc.



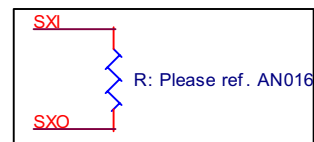
External Fast Clock:
RC osc.



External Slow Clock:
Crystal osc.

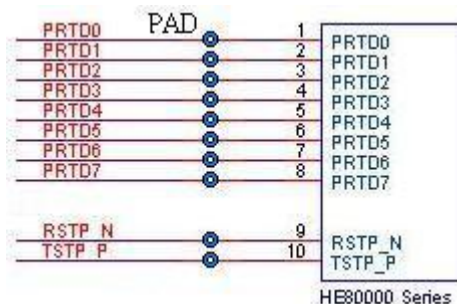


External Slow Clock:
RC osc.



I. Important Note

1. Please bonds the TSTP_P, RSTP_N and PRTD[7:0] with test point on PCB (can be soldered and probed) as you can, then KB can do some IC testing job on PCB. Neither VDD nor GND connection is necessary for TSTP_P. The following figure is an example (Testing point with through hole).



J. Updated Record

Version	Date	Section	Original Content	New Content
V3.1	Dec 24,2001	B, H	2.2V (VDD operation voltage)	2.4V
		C,I		New Section



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