

R1LV0108E Series

1Mb Advanced LPSRAM (128k word x 8bit)

R10DS0271EJ0200
Rev.2.00
2019.10.29

Description

The R1LV0108E Series is a family of low voltage 1-Mbit static RAMs organized as 131,072-word by 8-bit, fabricated by Renesas's high-performance 0.15μm CMOS and TFT technologies. The R1LV0108E Series has realized higher density, higher performance and low power consumption. The R1LV0108E Series is suitable for memory applications where a simple interfacing, battery operating and battery backup are the important design objectives. It has been packaged in 32-pin SOP, 32-pin TSOP and 32-pin sTSOP.

Features

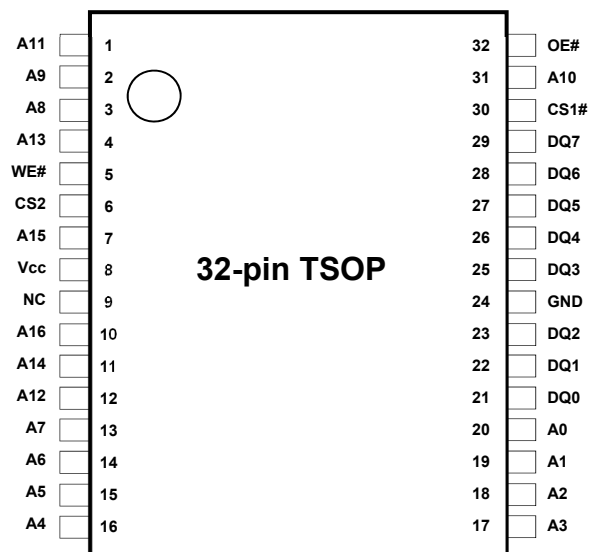
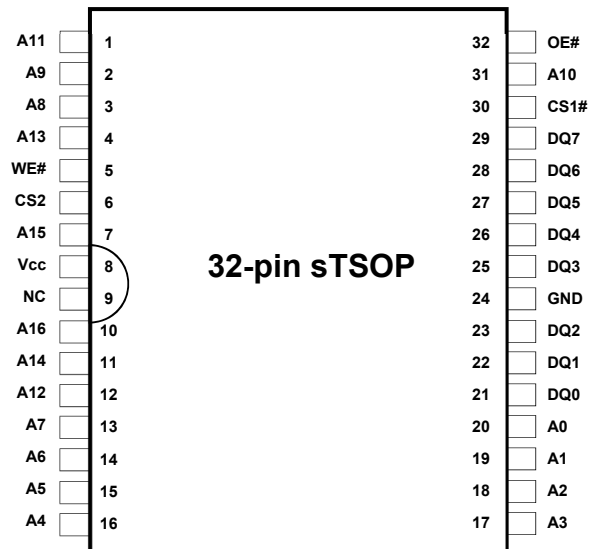
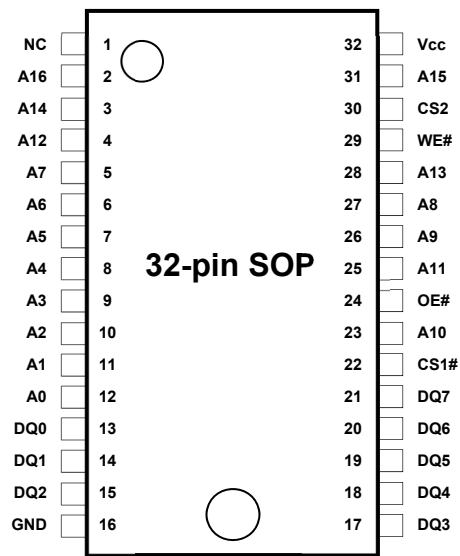
- Single 2.7V~3.6V power supply
- Small stand-by current: 0.6μA (3.0V, typical)
- No clocks, No refresh
- All inputs and outputs are TTL compatible.
- Easy memory expansion by CS1# and CS2
- Common Data I/O
- Three-state outputs: OR-tie Capability
- OE# prevents data contention on the I/O bus

Ordering Information

Orderable part name	Access time	Temperature range	Package	Shipping container
R1LV0108ESN-5SI#B*	55 ns	-40 ~ +85°C	525-mil 32-pin plastic SOP	Tube (Magazine)
R1LV0108ESN-5SI#S*				Embossed tape
R1LV0108ESA-5SI#B*			8mm×13.4mm 32-pin plastic sTSOP	Tray
R1LV0108ESA-5SI#S*				Embossed tape
R1LV0108ESF-5SI#B*			8mm×20mm 32-pin plastic TSOP	Tray
R1LV0108ESF-5SI#S*				Embossed tape

Note 1. * = Revision code for Assembly site change, etc. (* = 0, 1, etc.)

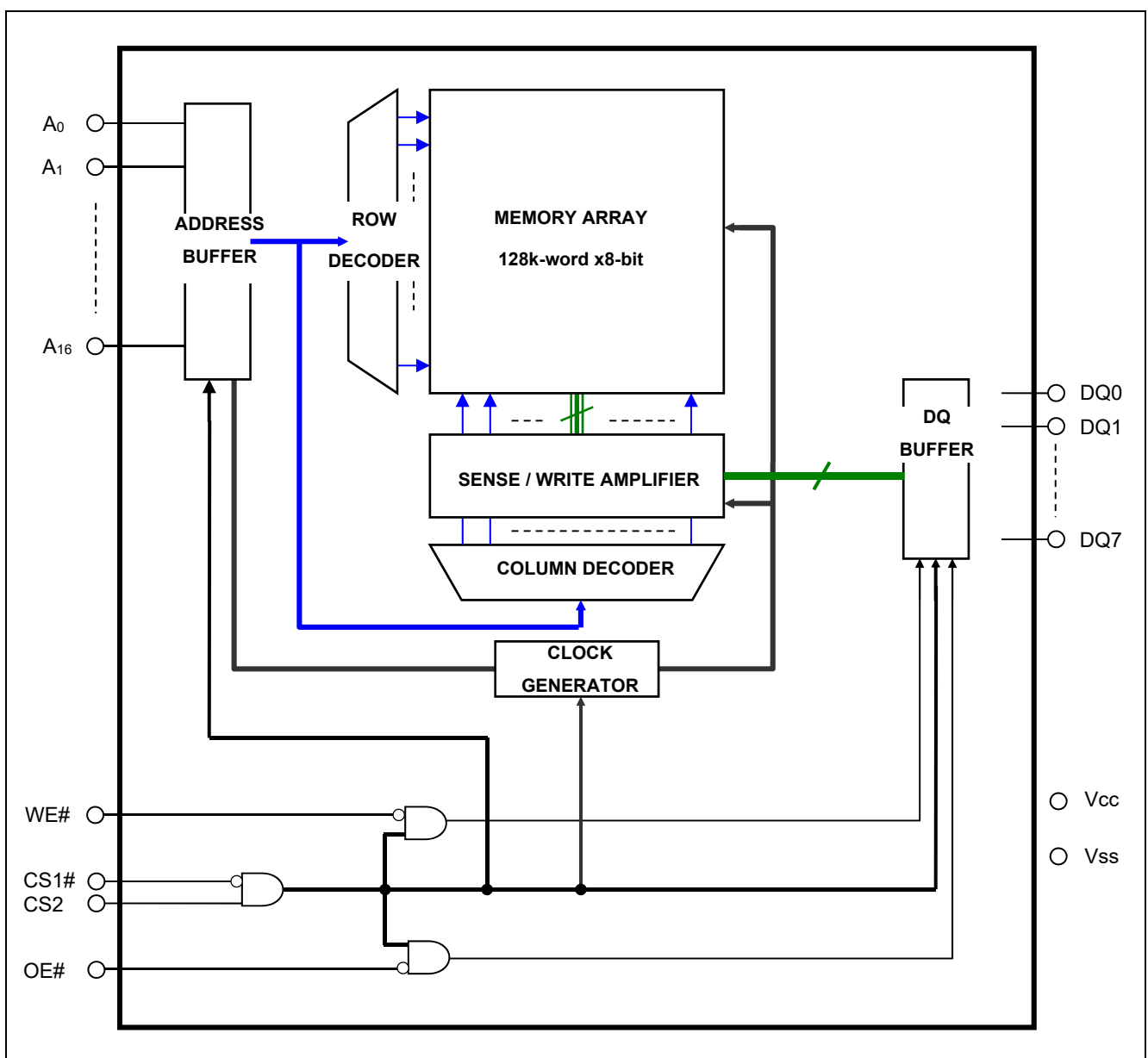
Pin Arrangement



Pin Description

Pin name	Function
Vcc	Power supply
Vss (GND)	Ground
A0 to A16	Address input
DQ0 to DQ7	Data input/output
CS1#	Chip select 1
CS2	Chip select 2
WE#	Write enable
OE#	Output enable
NC	Non connection

Block Diagram



Operation Table

CS1#	CS2	WE#	OE#	DQ0~7	Operation
X	L	X	X	High-Z	Stand-by
H	X	X	X	High-Z	Stand-by
L	H	L	X	Din	Write
L	H	H	L	Dout	Read
L	H	H	H	High-Z	Output disable

Note 1. H: V_{IH} L: V_{IL} X: V_{IH} or V_{IL}

Absolute Maximum

Parameter	Symbol	Value	unit
Power supply voltage relative to Vss	V_{CC}	-0.3 to +4.6	V
Terminal voltage on any pin relative to Vss	V_T	-0.3^{*1} to $V_{CC}+0.3^{*2}$	V
Power dissipation	P_T	0.7	W
Operation temperature	T_{opr}	-40 to +85	°C
Storage temperature range	T_{stg}	-65 to 150	°C
Storage temperature range under bias	T_{bias}	-40 to +85	°C

Note 1. -3.0V for pulse ≤ 30 ns (full width at half maximum)

2. Maximum voltage is +4.6V.

DC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage	V _{CC}	2.7	3.0	3.6	V	
	V _{SS}	0	0	0	V	
Input high voltage	V _{IH}	2.0	-	V _{CC} +0.3	V	
Input low voltage	V _{IL}	-0.3	-	0.6	V	1
Ambient temperature range	T _a	-40	-	+85	°C	

Note 1. -3.0V for pulse ≤ 30ns (full width at half maximum)

DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	
Input leakage current	I _{LI}	-	-	1	μA	Vin = Vss to Vcc	
Output leakage current	I _{LO}	-	-	1	μA	CS1# =VIH or CS2 =VIL or OE# =VIH, VI/O =Vss to Vcc	
Average operating current	I _{CC1}	-	15	25	mA	Min. cycle, duty =100%, II/O = 0mA, CS1# =VIL, CS2 =VIH, Others = VIH/VIL	
	I _{CC2}	-	2	5	mA	Cycle =1μs, duty =100%, II/O = 0mA, CS1# ≤ 0.2V, CS2 ≥ Vcc-0.2V, VIH ≥ Vcc-0.2V, VIL ≤ 0.2V	
Standby current	I _{SB}	-	-	0.33	mA	“CS2 =VIL” or “CS2 = VIH and CS1# =VIH”, Others = Vss to Vcc	
Standby current	I _{SB1}	-	0.6*1	2	μA	~+25°C	Vin = Vss to Vcc, (1) CS2 ≤ 0.2V or (2) CS1# ≥ Vcc-0.2V, CS2 ≥ Vcc-0.2V
		-	-	3	μA	~+40°C	
		-	-	8	μA	~+70°C	
		-	-	10	μA	~+85°C	
Output high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -0.5mA	
	V _{OH2}	Vcc - 0.5	-	-	V	I _{OH} = -0.05mA	
Output low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA	

Note 1. Typical parameter indicates the value for the center of distribution at 3.0V (T_a = 25°C), and not 100% tested.

Capacitance

(V_{CC} = 2.7V ~ 3.6V, f = 1MHz, T_a = -40 ~ +85°C)

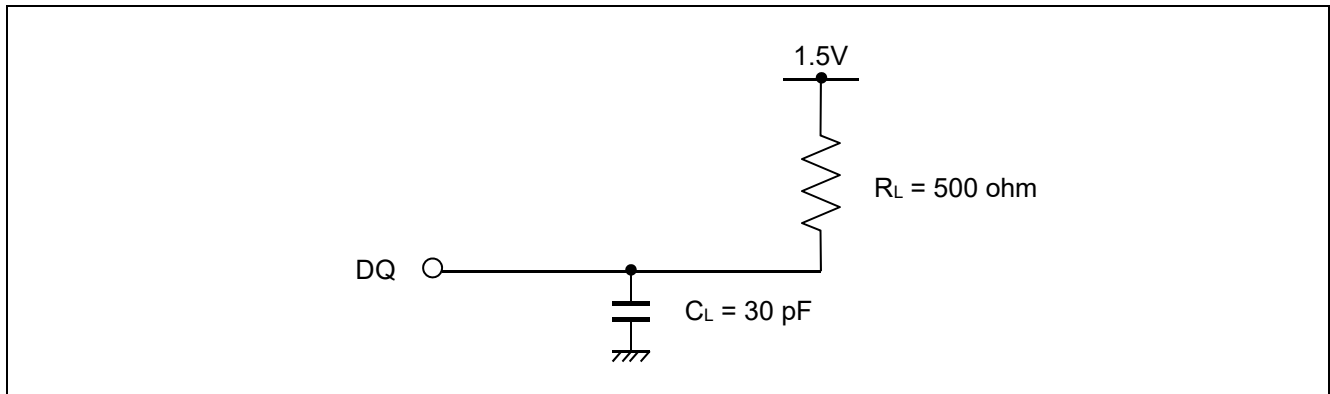
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	Note
Input capacitance	C _{in}	-	-	8	pF	V _{in} = 0V	1
Input / output capacitance	C _{I/O}	-	-	10	pF	V _{I/O} = 0V	1

Note 1. This parameter is sampled and not 100% tested.

AC Characteristics

Test Conditions ($V_{CC} = 2.7V \sim 3.6V$, $T_a = -40 \sim +85^{\circ}C$)

- Input pulse levels: $V_{IL} = 0.4V$, $V_{IH} = 2.2V$
- Input rise and fall time: 5ns
- Input and output timing reference level: 1.5V
- Output load: See figures (Including scope and jig)



Read Cycle

Parameter	Symbol	Min.	Max.	Unit	Note
Read cycle time	t_{RC}	55	-	ns	
Address access time	t_{AA}	-	55	ns	
Chip select access time	t_{ACS1}	-	55	ns	
	t_{ACS2}	-	55	ns	
Output enable to output valid	t_{OE}	-	30	ns	
Output hold from address change	t_{OH}	5	-	ns	
Chip select to output in low-Z	t_{CLZ1}	5	-	ns	2,3
	t_{CLZ2}	5	-	ns	2,3
Output enable to output in low-Z	t_{OLZ}	5	-	ns	2,3
Chip deselect to output in high-Z	t_{CHZ1}	0	20	ns	1,2,3
	t_{CHZ2}	0	20	ns	1,2,3
Output disable to output in high-Z	t_{OHZ}	0	20	ns	1,2,3

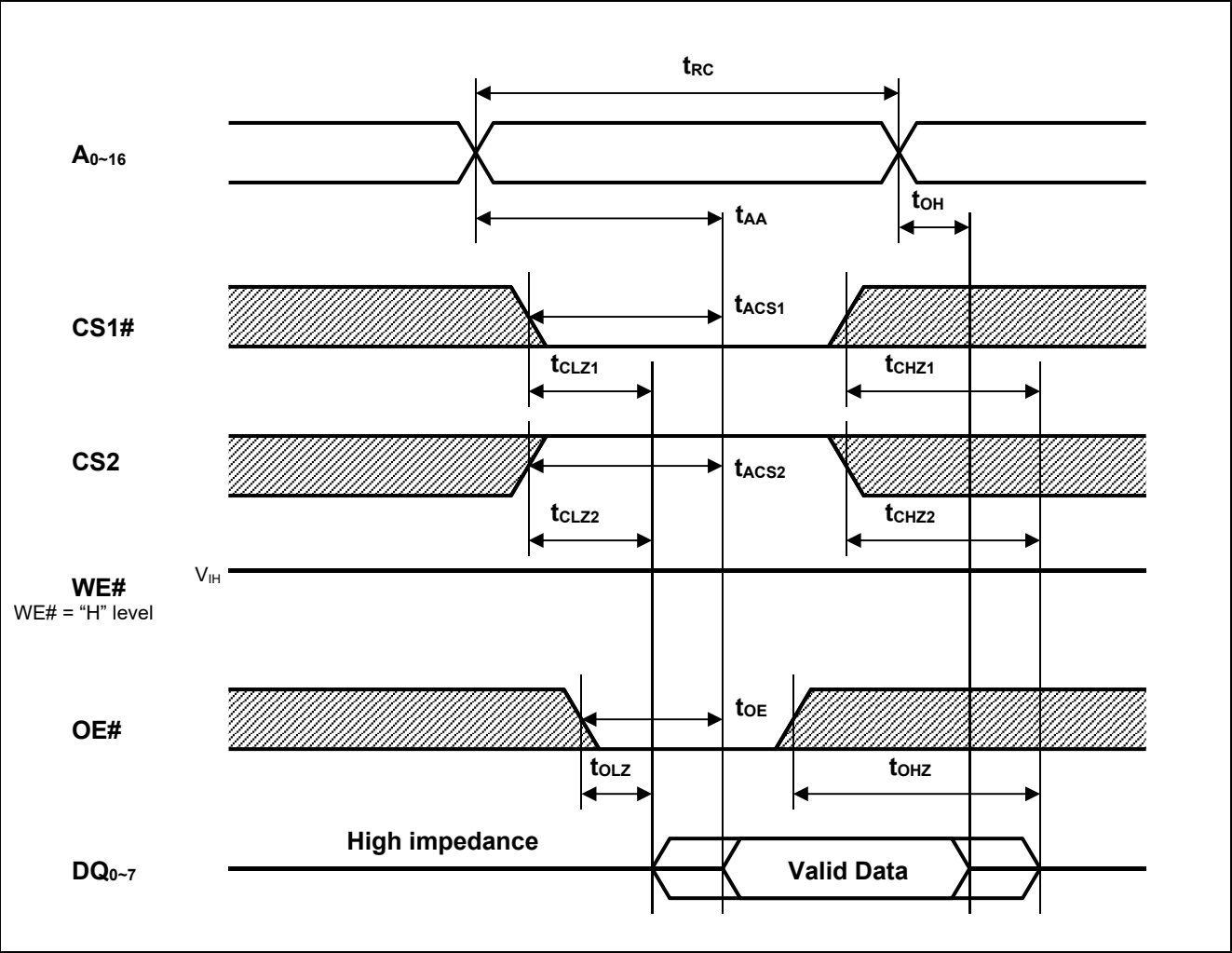
Write Cycle

Parameter	Symbol	Min.	Max.	Unit	Note
Write cycle time	t_{WC}	55	-	ns	
Address valid to end of write	t_{AW}	50	-	ns	
Chip select to end of write	t_{CW}	50	-	ns	5
Write pulse width	t_{WP}	45	-	ns	4
Address setup time	t_{AS}	0	-	ns	6
Write recovery time	t_{WR}	0	-	ns	7
Data to write time overlap	t_{DW}	25	-	ns	
Data hold from write time	t_{DH}	0	-	ns	
Output enable from end of write	t_{OW}	5	-	ns	2
Output disable to output in high-Z	t_{OHZ}	0	20	ns	1,2
Write to output in high-Z	t_{WHZ}	0	20	ns	1,2

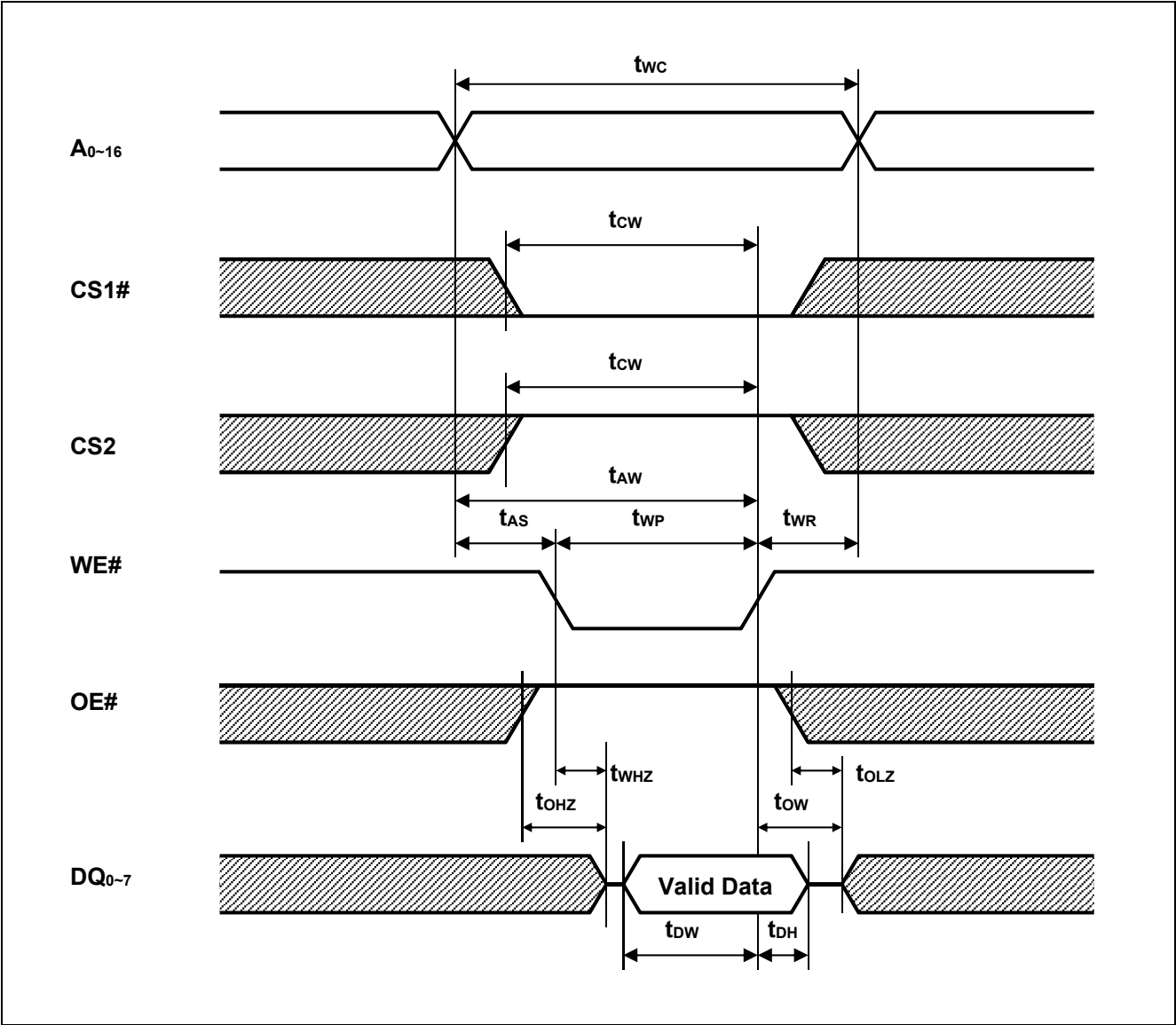
- Note
1. t_{CHZ} , t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
 2. This parameter is sampled and not 100% tested.
 3. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
 4. A write occurs during the overlap of a low CS1#, a high CS2, a low WE#.
A write begins at the latest transition among CS1# going low, CS2 going high and WE# going low.
A write ends at the earliest transition among CS1# going high, CS2 going low and WE# going high.
 t_{WP} is measured from the beginning of write to the end of write.
 5. t_{CW} is measured from the later of CS1# going low or CS2 going high to end of write.
 6. t_{AS} is measured the address valid to the beginning of write.
 7. t_{WR} is measured from the earliest of CS1# or WE# going high or CS2 going low to the end of write cycle.
 8. Don't apply inverted phase signal externally when DQ pin is output mode.

Timing Waveforms

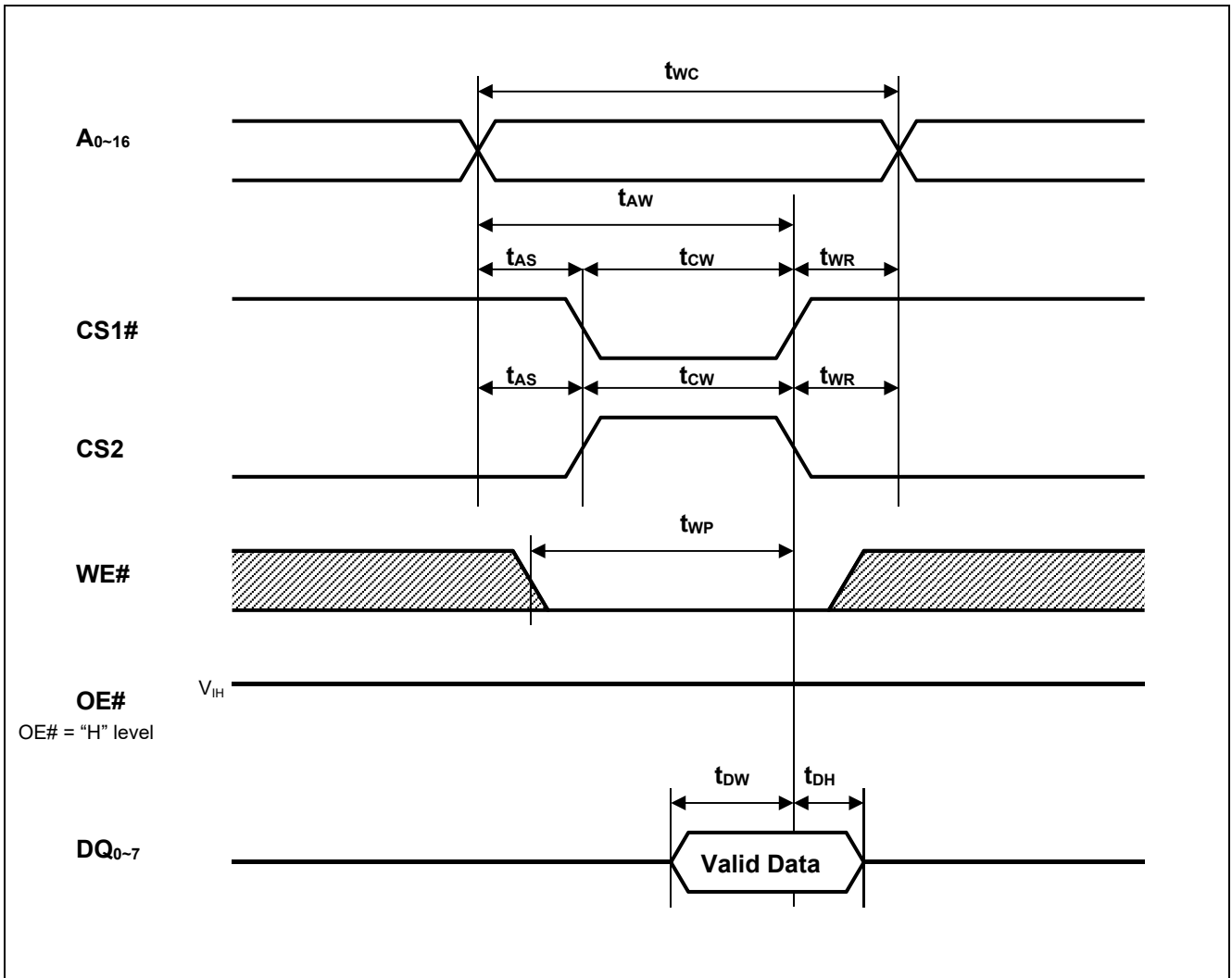
Read Cycle



Write Cycle (1) (WE# CLOCK)



Write Cycle (2) (CS1#, CS2 CLOCK)



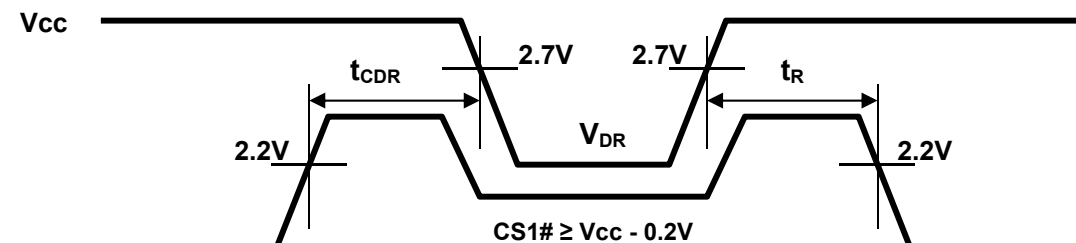
Low Vcc Data Retention Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions ^{*2}	
V _{CC} for data retention	V _{DR}	2.0	-	3.6	V	Vin ≥ 0V, (1) 0V ≤ CS2 ≤ 0.2V or (2) CS1# ≥ Vcc-0.2V, CS2 ≥ Vcc-0.2V	
Data retention current	I _{CCDR}	-	0.6 ^{*1}	2	μA	~+25°C	Vcc=3.0V, Vin ≥ 0V, (1) 0V ≤ CS2 ≤ 0.2V or (2) CS1# ≥ Vcc-0.2V, CS2 ≥ Vcc-0.2V
		-	-	3	μA	~+40°C	
		-	-	8	μA	~+70°C	
		-	-	10	μA	~+85°C	
Chip deselect time to data retention	t _{CDR}	0	-	-	ns	See retention waveform.	
Operation recovery time	t _R	5	-	-	ms		

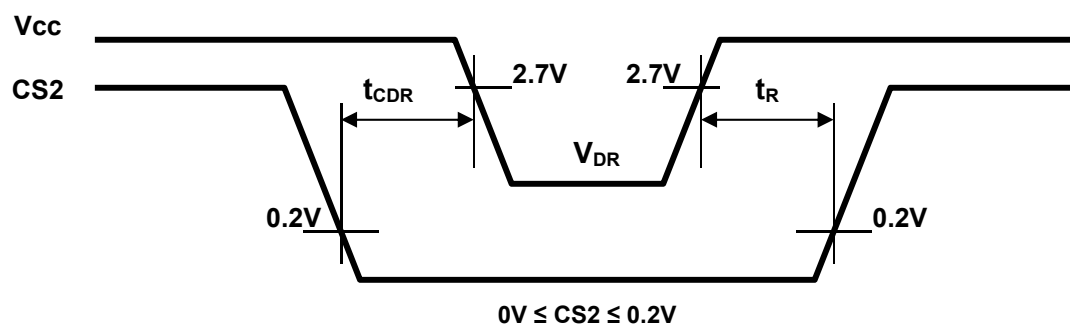
- Note
- Typical parameter indicates the value for the center of distribution at 3.0V (T_a = 25°C), and not 100% tested.
 - CS2 controls address buffer, WE# buffer, CS1# buffer, OE# buffer and Din buffer. If CS2 controls data retention mode, V_{in} levels (address, WE#, CS1#, OE#, DQ) can be in the high impedance state.
If CS1# controls data retention mode, CS2 must be CS2 ≥ V_{CC}-0.2V or 0V ≤ CS2 ≤ 0.2V. The other input levels (address, WE#, OE#, DQ) can be in the high impedance state.

Low Vcc Data Retention Timing Waveforms

(1) CS1# Controlled



(2) CS2 Controlled



Revision History	R1LV0108E Series Data Sheet
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Rev.	Date	Description	
		Page	Summary
1.00	2017.1.27	-	First Edition issued
2.00	2019.10.29	p.1	Revised orderable part name information.

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Renesas Electronics Corporation
TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan

Renesas Electronics America Inc.
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 101-T01, Floor 1, Building 7, Yard No. 7, 8th Street, Shangdi, Haidian District, Beijing 100085, China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai 200333, China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit No 3A-1 Level 3A Tower 8 UOA Business Park, No 1 Jalan Pengaturcara U1/51A, Seksyen U1, 40150 Shah Alam, Selangor, Malaysia
Tel: +60-3-5022-1288, Fax: +60-3-5022-1290

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338



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