

100 V N-channel Trench MOSFET 14 July 2016

Product data sheet

1. **General description**

N-channel enhancement mode Field-Effect Transistor (FET) in a medium power SOT223 (SC-73) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Logic level compatible •
- Very fast switching
- Trench MOSFET technology •
- ElectroStatic Discharge (ESD) protection > 2 kV HBM •
- AEC-Q101 qualified

Applications 3.

- Relay driver
- High-speed line driver
- Low-side loadswitch
- Switching circuits

Quick reference data 4.

Table 1. Quid	ck reference data						
Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	-	100	V
V _{GS}	gate-source voltage			-20	-	20	V
I _D	drain current	V _{GS} = 10 V; T _{amb} = 25 °C	[1]	-	-	1.1	А
Static characteristics							
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 1.1 A; T _j = 25 °C		-	527	715	mΩ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm².

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5. Pinning information

Table 2.	Pinning	information		
Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	4	D
2	D	drain		
3	S	source		G (↓ [↓] ↓ ↓
4	D	drain	∐1	S 017aaa255

6. Ordering information

Table 3. Ordering in	formation						
Type number	Package	e					
	Name	Description	Version				
PMT560ENEA	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223				

7. Marking

Table 4. Marking codes	
Type number	Marking code
PMT560ENEA	56ENEA

8. Limiting values

Table 5.Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

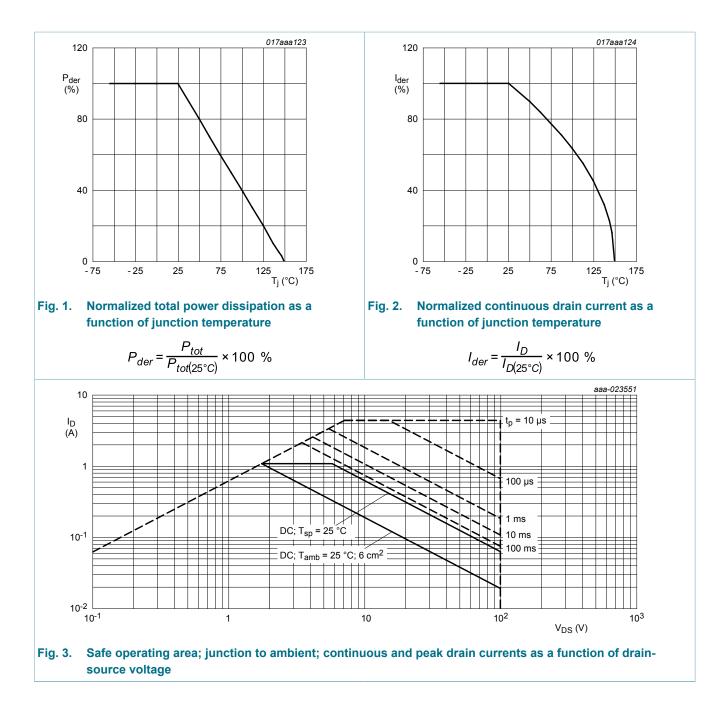
Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	100	V
V _{GS}	gate-source voltage			-20	20	V
I _D	drain current	V _{GS} = 10 V; T _{amb} = 25 °C	[1]	-	1.1	А
		V _{GS} = 10 V; T _{amb} = 100 °C	[1]	-	0.7	А
I _{DM}	peak drain current	T_{amb} = 25 °C; single pulse; $t_p \le 10 \ \mu s$		-	4.4	А
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	$T_{j(init)}$ = 25 °C; I _D = 0.1 A; DUT in avalanche (unclamped)		-	5.3	mJ
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	750	mW
			[1]	-	1.9	W
		T _{sp} = 25 °C		-	6.25	W
Tj	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drai	in diode					
I _S	source current	T _{amb} = 25 °C	[1]	-	1.1	А
ESD maxim	num rating					
V _{ESD}	electrostatic discharge voltage	НВМ	[3]	-	2000	V
		1		1		1

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm².

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[3] Measured between all pins.

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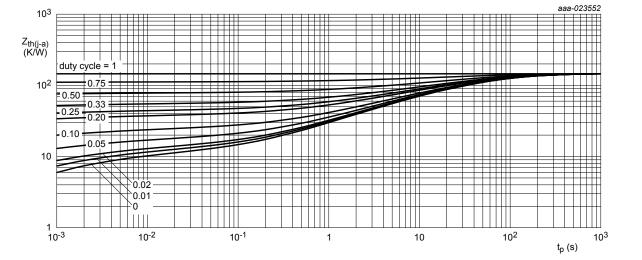
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9. Thermal characteristics

Table 6. Thermal characteristics							
Symbol	Parameter	Conditions		Min	Тур	Мах	Unit
fr	thermal resistance i from junction to ambient	in free air	[1]	-	145	167	K/W
			[2]	-	57	66	K/W
R _{th(j-sp)}	thermal resistance from junction to solder point			-	13	20	K/W

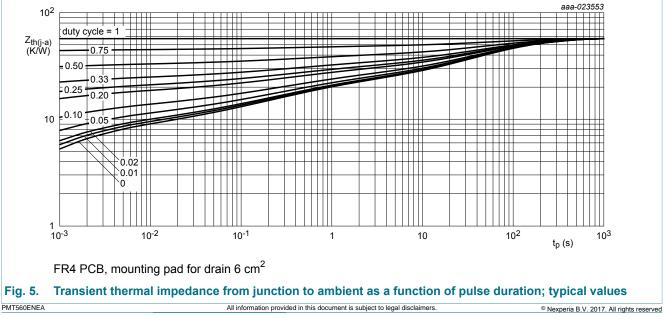
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm².



FR4 PCB, standard footprint





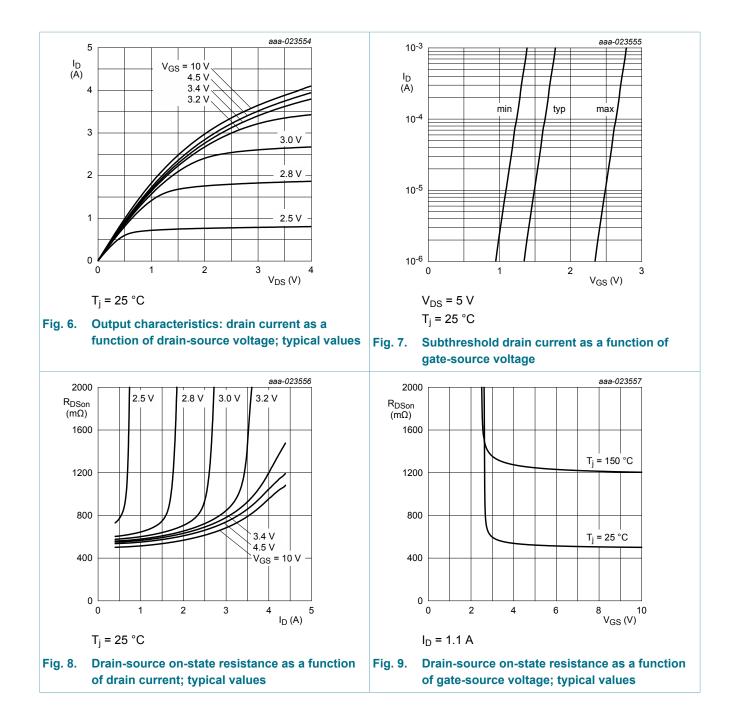
10. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	octeristics					
V _{(BR)DSS}	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C	100	-	-	V
V _{GSth}	gate-source threshold voltage	I_D = 250 µA; V_{DS} = V_{GS} ; T_j = 25 °C	1.3	1.7	2.7	V
I _{DSS}	drain leakage current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	-	1	μA
I _{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C	-	-	15	μA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C	-	-	-15	μA
		V_{GS} = 10 V; V_{DS} = 0 V; T_j = 25 °C	-	-	1	μA
		V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25 °C	-	-	-1	μA
R _{DSon}	drain-source on-state	V_{GS} = 10 V; I _D = 1.1 A; T _j = 25 °C	-	527	715	mΩ
re	resistance	V _{GS} = 10 V; I _D = 1.1 A; T _j = 150 °C	-	1.19	1.62	Ω
		V_{GS} = 4.5 V; I_D = 1 A; T_j = 25 °C	-	555	805	mΩ
9 _{fs}	forward transconductance	V _{DS} = 10 V; I _D = 1.1 A; T _j = 25 °C	-	3.5	-	S
R _G	gate resistance	f = 1 MHz	-	7.6	-	Ω
Dynamic ch	aracteristics					
Q _{G(tot)}	total gate charge	V_{DS} = 50 V; I _D = 1.1 A; V _{GS} = 10 V;	-	2.9	4.4	nC
Q _{GS}	gate-source charge	T _j = 25 °C	-	0.3	-	nC
Q _{GD}	gate-drain charge		-	0.7	-	nC
C _{iss}	input capacitance	V_{DS} = 50 V; f = 1 MHz; V_{GS} = 0 V;	-	112	-	pF
C _{oss}	output capacitance	T _j = 25 °C	-	9	-	pF
C _{rss}	reverse transfer capacitance		-	7	-	pF
t _{d(on)}	turn-on delay time	V_{DS} = 50 V; I _D = 1.1 A; V _{GS} = 10 V;	-	6	-	ns
t _r	rise time	R _{G(ext)} = 6 Ω; T _j = 25 °C	-	8	-	ns
t _{d(off)}	turn-off delay time		-	10	-	ns
t _f	fall time		-	5	-	ns
Source-drai	n diode	1	I	1	1	
V _{SD}	source-drain voltage	I _S = 1.1 A; V _{GS} = 0 V; T _i = 25 °C	-	0.9	1.2	V

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PMT560ENEA

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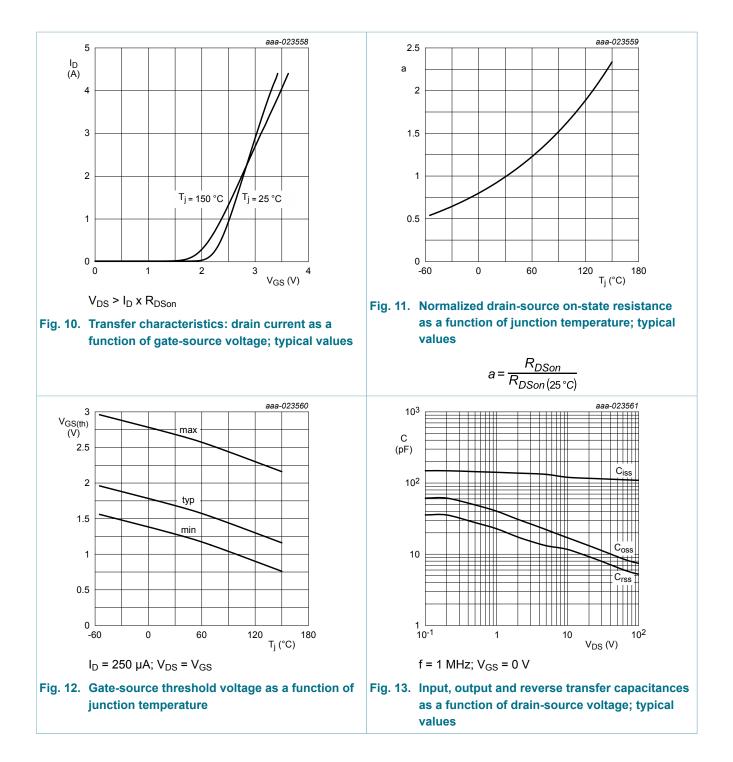


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PMT560ENEA

100 V N-channel Trench MOSFET



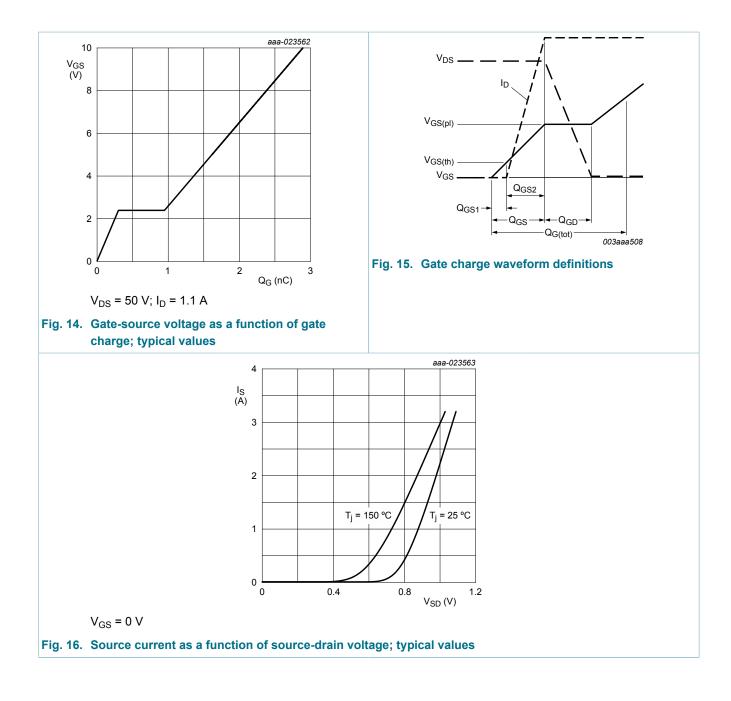
PMT560ENEA

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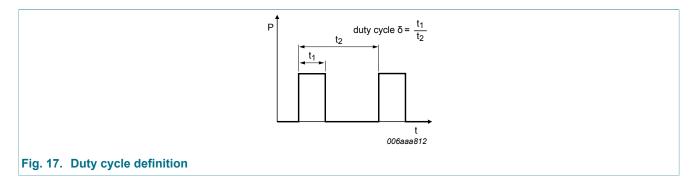
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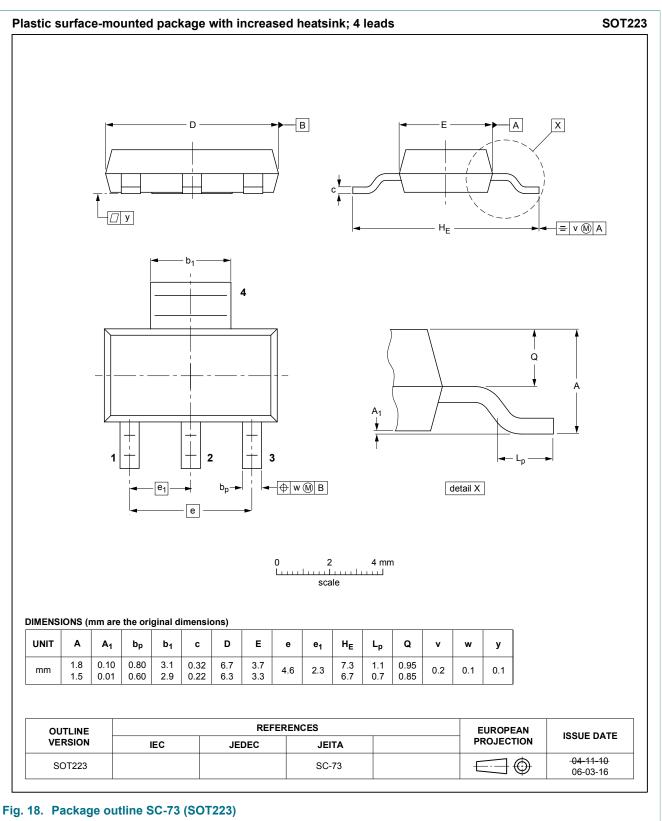
11. Test information



11.1 Quality information

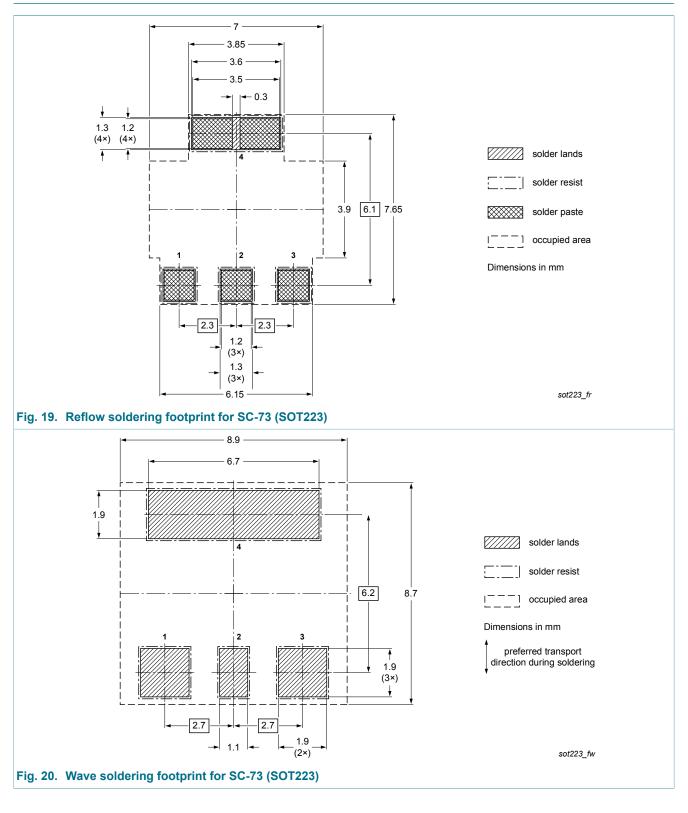
This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

12. Package outline



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13. Soldering



PMT560ENEA

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14. Revision history

Table 8. Revision history							
Data sheet ID	Release date	Data sheet status	Change notice	Supersedes			
PMT560ENEA v.1	20160714	Product data sheet	-	-			

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15. Legal information

15.1 Data sheet status

Document status [1][2]	Product status [<u>3]</u>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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