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FCH47N60 N-Channel SuperFET[®] MOSFET 600 V, 47 A, 70 mΩ

Features

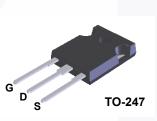
- 650 V @ T_J = 150°C
- Typ. R_{DS(on)} = 58 mΩ
- Ultra Low Gate Charge (Typ. Q_g = 210 nC)
- Low Effective Output Capacitance (Typ. Coss(eff.) = 420 pF)
- 100% Avalanche Tested
- RoHS Compliant

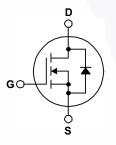
Applications

- Solar Inverter
- AC-DC Power Supply

Description

SuperFET[®] MOSFET is Fairchild Semiconductor's first generation of high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low onresistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.





MOSFET Maximum Ratings T_C = 25°C unless otherwise noted.

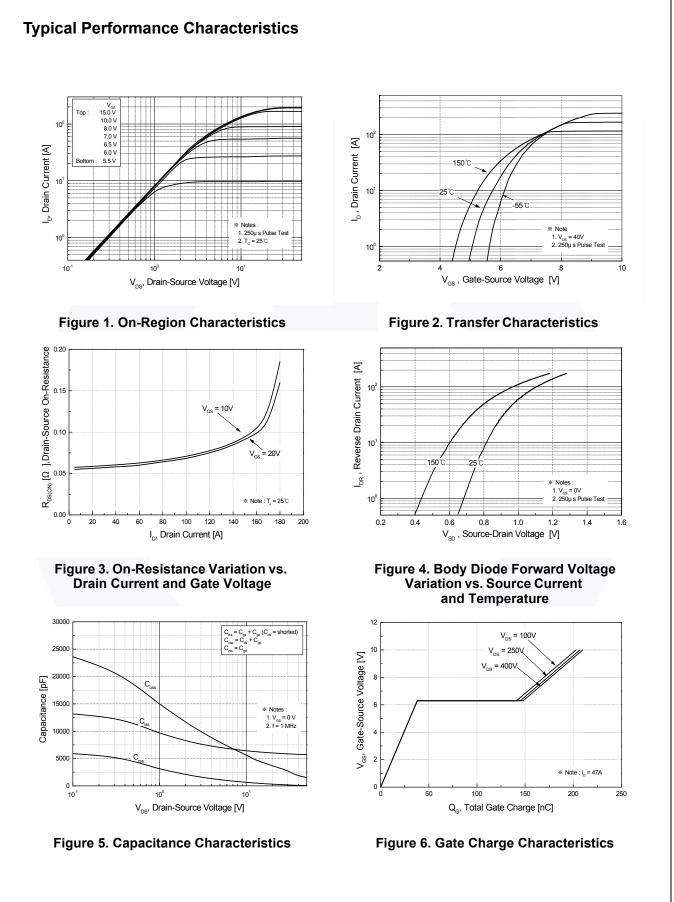
Symbol		FCH47N60_F133	Unit	
V _{DSS}	Drain to Source Voltage		600	V
	Drain Current	Continuous (T _C = 25°C)	47	^
ID	Drain Current	Continuous (T _C = 100°C)	29.7	- A
I _{DM}	Drain Current	Pulsed (Note 1)	141	А
V _{GSS}	Gate to Source Voltage		±30	V
E _{AS}	Single Pulsed Avalanche Energy (Note 2)		1800	mJ
I _{AR}	Avalanche Current (Note 1)		47	А
E _{AR}	Repetitive Avalanche Energy	41.7	mJ	
dv/dt	Peak Diode Recovery dv/dt (Note 3)		4.5	V/ns
P _D	Dower Dissinction	$(T_{C} = 25^{\circ}C)$	417	W
	Power Dissipation	Derate Above 25°C	3.33	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +150	°C
TL	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	°C

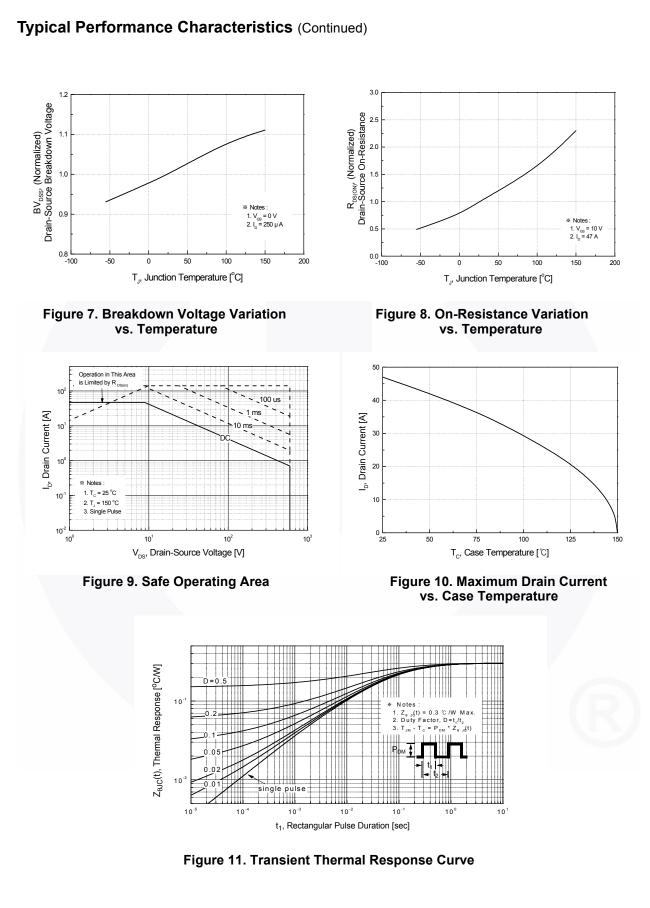
Thermal Characteristics

Symbol	Parameter	FCH47N60_F133	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Case-to-Sink, Typ.	0.24	°C/W
$R_{ extsf{ heta}JA}$	Thermal Resistance, Junction to Ambient, Max.	41.7	°C/W

0 — N-Channel SuperFET [®] MO	FCH47N6	
rFET [®] MC	0 — N-Chanr	
T [®] MC	ĥ	
SFE	T [®] MOSF	

Part Nu	nber	Top Mark	Package	Packing Meth	od Reel Si	ze	Tape Width	n Qu	antity
FCH47N6)_F133	FCH47N60	TO-247	Tube	N/A		N/A	30 units	
Electrica	Chara	cteristics T _c = 25°		there is noted					
Symbol		Parameter		Test Conc	litions	Min.	Тур.	Max.	Unit
Off Chara	teristics			1001 0011			.,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	maxi	•
			V	/ _{GS} = 0 V, I _D = 250	μΑ, Τ _C = 25°C	600	-	-	V
BV _{DSS}	Drain-to-8	Source Breakdown Voltag	ge ∖	$V_{\rm GS} = 0 \text{ V}, \text{ I}_{\rm D} = 250$	μΑ, Τ _C = 150°C	; -	650	-	V
ΔΒV _{DSS} / ΔΤ _J	Breakdow Coefficier	vn Voltage Temperature nt	I	_D = 250 μA, Refere	nced to 25°C	-	0.6	-	V/°C
BV _{DS}	Drain to S Voltage	Source Avalanche Breako	V	/ _{GS} = 0 V, I _D = 47 /		-	700	-	V
D 00	Zero Gate	Zero Gate Voltage Drain Current		/ _{DS} = 600 V, V _{GS} =		-	-	1	μA
DSS				/ _{DS} = 480 V, T _C = 1		-	-	10	μΛ
GSS	Gate-to-B	ody Leakage Current	V	V _{GS} = ±30 V, V _{DS} =	0 V	-	-	±100	nA
On Charao	teristics								
V _{GS(th)}	Gate Threshold Voltage			/ _{GS} = V _{DS} , I _D = 250	Ο μΑ	3.0	-	5.0	V
R _{DS(on)}	Static Drain-to-Source On Resistance $V_{GS} = 10 \text{ V}, I_D = 23.5 \text{ A}$				-	0.058	0.070	Ω	
JFS	Forward Transconductance			/ _{DS} = 40 V, I _D = 23	.5 A	-	40	-	S
Dynamic (Character	ristics							
C _{iss}	Input Capacitance					-	5900	8000	pF
C _{oss}		Output Capacitance		$V_{\rm DS} = 25 \text{ V}, \text{ V}_{\rm GS} = 1.0 \text{ MHz}$	0 V,	-	3200	4200	pF
Crss	Reverse Transfer Capacitance f = 1.0 MHz		-	250	-	pF			
C _{oss}	Output Capacitance			V _{DS} = 480 V, V _{GS} = 0 V, f = 1.0 MHz			160	-	pF
C _{oss(eff.)}	Effective Output Capacitance		١	$V_{\rm DS}$ = 0 V to 400 V,	V_{GS} = 0 V	-	420	-	pF
Switching	Characte	eristics							
d(on)	Turn-On E					-	185	430	ns
·	Turn-On Rise Time Turn-Off Delay		1	V_{DD} = 300 V, I _D = 47 A, V _{GS} = 10 V, R _G = 25 Ω		-	210	450	ns
d(off)						-	520	1100	ns
t	Turn-Off F			(Note 4)		-	75	160	ns
Q _{g(tot)}		e Charge at 10 V	1	$V_{\rm DS} = 480 \text{ V}, \text{ I}_{\rm D} = 47 \text{ A},$		-	210	270	nC
2 _{gs}	Gate to Source Gate Charge Gate to Drain "Miller" Charge		\	$V_{GS} = 10 V$ (Note 4)		-	38	-	nC
ୁ ପୁ _{gd}						-	110	-	nC
	rce Diode	e Characteristics	I				-		
s	-	Continuous Drain-to-Sou	urce Diode	Forward Current		-	-	47	Α
SM	Maximum Pulsed Drain-to-Source Diode F		Diode Forv			-	-	141	Α
V _{SD}	Drain-to-Source Diode Forward Voltage		ltage \	$V_{GS} = 0 \text{ V}, \text{ I}_{SD} = 47 \text{ A}$		-	-	1.4	V
	Reverse-F	Recovery Time		$V_{GS} = 0 V, I_{SD} = 47 A,$		-	590	-	ns
Q _{rr}	Reverse-F	Recovery Charge	d	$II_F/dt = 100 \text{ A/}\mu\text{s}$		-	25	-	μC



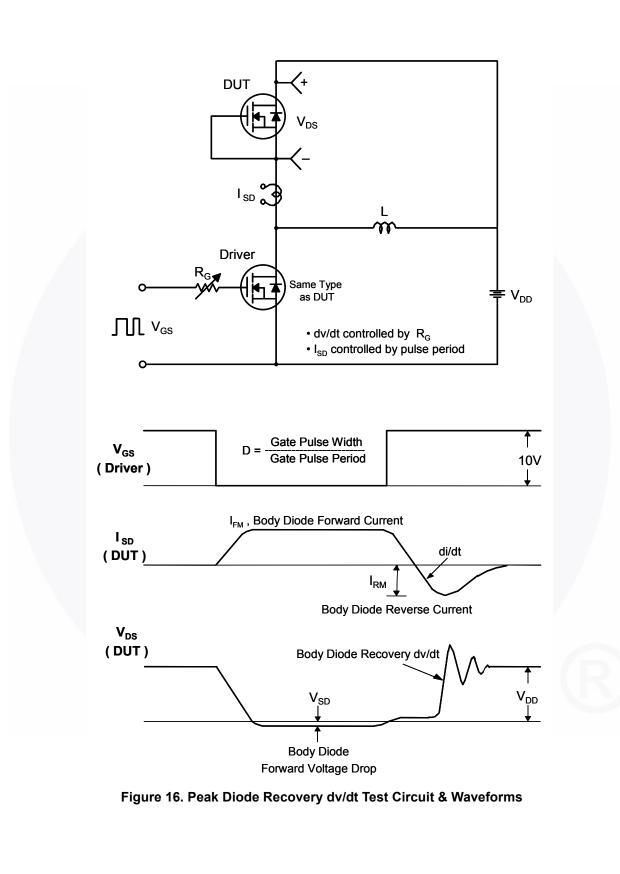


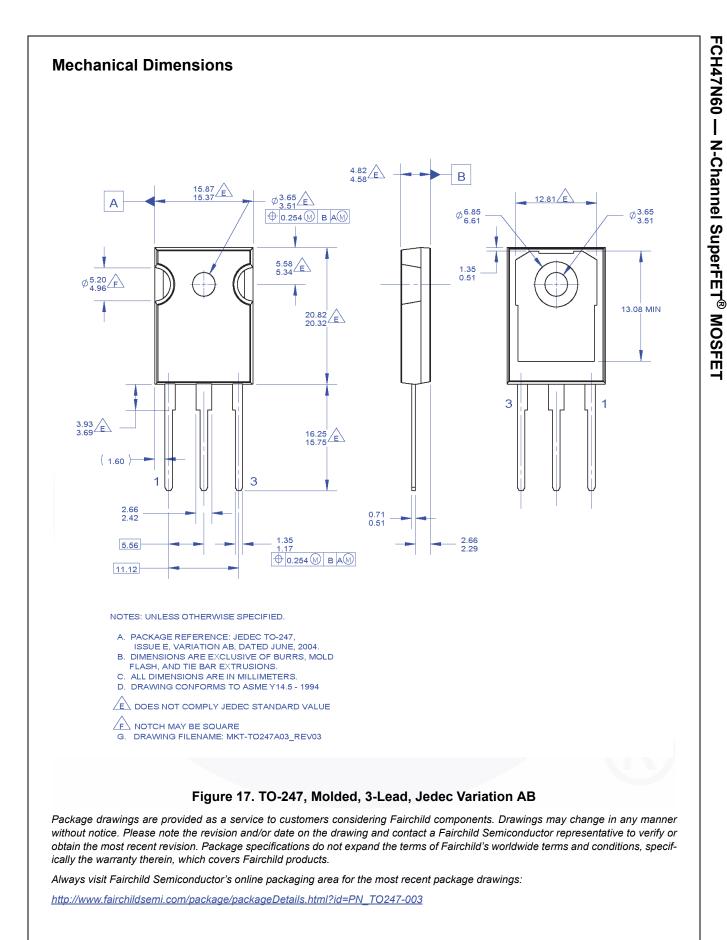
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 V_{GS} ≶ R Q_g FV_{DS} Q_{gd} Q_{gs} • DUT I_G = const. Charge Figure 13. Gate Charge Test Circuit & Waveform R VDS V_{DS} 90% 0 V_{DD} R_{G} 10% V_{GS} DUT V_{GS} ∏ 0 Figure 14. Resistive Switching Test Circuit & Waveforms BV_{DSS} BV_{DSS} - V_{DD} L $E_{AS} = \frac{1}{2} L I_{AS}^{2}$ $\mathsf{BV}_{\mathsf{DSS}}$ I_D I_{AS} R_G $\mathsf{V}_{\mathsf{D}\mathsf{D}}$ $I_{D}(t)$ V_{GS} $V_{DS}(t)$ V_{DD} DUT Time t_n Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

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