

Features

- Temperature ranges
 - Industrial: -40 °C to 85 °C
- Very high speed: 55 ns
- Wide voltage range: 2.2 V to 3.6 V
- Pin compatible with CY62127BV
- Ultra-low active power
 - Typical active current: 0.85 mA at f = 1 MHz
 - Typical active current: 5 mA at f = f_{MAX}
- Ultra-low standby power
- Easy memory expansion with \overline{CE} and \overline{OE} features
- Automatic power-down when deselected
- Available in Pb-free 48-ball FBGA and 44-pin TSOP Type II packages

Functional Description

The CY62127DV30 is a high-performance CMOS static RAM organized as 64K words by 16-bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable

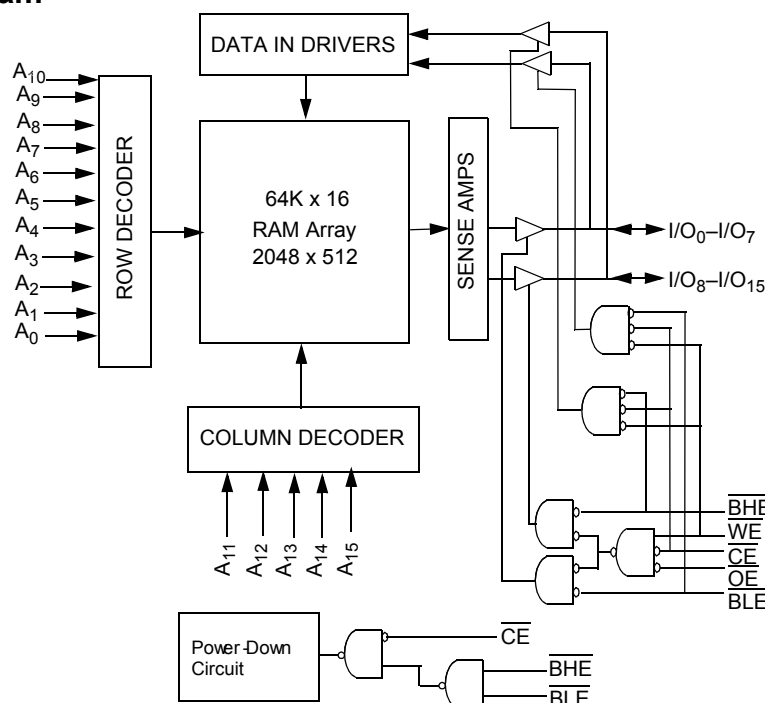
applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 90% when addresses are not toggling. The device can be put into standby mode reducing power consumption by more than 99% when deselected (\overline{CE} HIGH or both BHE and BLE are HIGH). The input/output pins (I/O₀ through I/O₁₅) are placed in a high-impedance state when: deselected (\overline{CE} HIGH), outputs are disabled (\overline{OE} HIGH), both byte high enable and byte low enable are disabled (BHE, BLE HIGH) or during a write operation (\overline{CE} LOW and \overline{WE} LOW).

Writing to the device is accomplished by taking chip enable (\overline{CE}) and write enable (\overline{WE}) inputs LOW. If byte low enable (BLE) is LOW, then data from I/O pins (I/O₀ through I/O₇), is written into the location specified on the address pins (A₀ through A₁₅). If byte high enable (BHE) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₅).

Reading from the device is accomplished by taking chip enable (\overline{CE}) and output enable (\overline{OE}) LOW while forcing the write enable (\overline{WE}) HIGH. If byte low enable (BLE) is LOW, then data from the memory location specified by the address pins appear on I/O₀ to I/O₇. If byte high enable (BHE) is LOW, then data from memory appear on I/O₈ to I/O₁₅. See the truth table at the back of this datasheet for a complete description of read and write modes.

For a complete list of related documentation, [click here](#).

Logic Block Diagram



Contents

Product Portfolio	3	Ordering Information	12
Pin Configurations	3	Ordering Code Definitions	12
Maximum Ratings	4	Package Diagrams	13
Operating Range	4	Acronyms	14
DC Electrical Characteristics	4	Document Conventions	14
Capacitance	5	Units of Measure	14
Thermal Resistance	5	Document History Page	15
AC Test Loads and Waveforms	5	Sales, Solutions, and Legal Information	17
Data Retention Characteristics	6	Worldwide Sales and Design Support	17
Data Retention Waveform	6	Products	17
Switching Characteristics	7	PSoC@Solutions	17
Switching Waveforms	8	Cypress Developer Community	17
Truth Table	11	Technical Support	17

Product Portfolio

Product	V _{CC} Range (V)			Speed (ns)	Power Dissipation						
					Operating, I _{CC} (mA)					Standby I _{SB2} (μA)	
	f = 1 MHz		f = f _{MAX}								
	Min	Typ	Max		Typ ^[1]	Max	Typ ^[1]	Max	Range	Typ ^[1]	Max
CY62127DV30LL	2.2	3.0	3.6	55	0.85	1.5	5	10	Industrial	1.5	4

Pin Configurations

Figure 1. 48-ball FBGA pinout [2, 3]

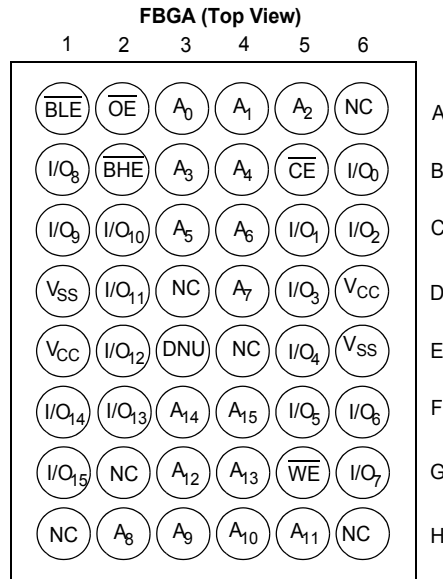
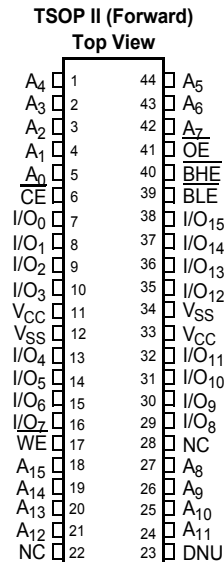


Figure 2. 44-pin TSOP Type II pinout [2, 3]



Notes

1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.
2. NC pins are not connected to the die. Expansion pins on FBGA Package: E4 - 2M, D3 - 4M, H1 - 8M, G2 - 16M, H6 - 32M
3. Pin #23 of TSOP-II and E3 ball of FBGA are DNU, which have to be left floating or tied to V_{ss} to ensure proper application.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature	-65 °C to +150 °C
Ambient temperature with power applied	-55 °C to +125 °C
Supply voltage to ground potential	-0.3 V to 3.9 V
DC voltage applied to outputs in high Z State ^[4]	-0.3 V to V _{CC} + 0.3 V

DC input voltage ^[4]	-0.3 V to V _{CC} + 0.3 V
Output current into outputs (LOW)	20 mA
Static discharge voltage (per MIL-STD-883, method 3015)	> 2001 V
Latch-up current	> 200 mA

Operating Range

Range	Ambient Temperature (T _A)	V _{CC} ^[5]
Industrial	-40 °C to +85 °C	2.2 V to 3.6 V

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-55			Unit	
			Min	Typ ^[6]	Max		
V _{OH}	Output HIGH voltage	2.2 ≤ V _{CC} ≤ 2.7	I _{OH} = -0.1 mA	2.0	-	-	V
		2.7 ≤ V _{CC} ≤ 3.6	I _{OH} = -1.0 mA	2.4	-	-	
V _{OL}	Output LOW voltage	2.2 ≤ V _{CC} ≤ 2.7	I _{OL} = 0.1 mA	-	-	0.4	V
		2.7 ≤ V _{CC} ≤ 3.6	I _{OL} = 2.1 mA	-	-	0.4	
V _{IH}	Input HIGH voltage	2.2 ≤ V _{CC} ≤ 2.7		1.8	-	V _{CC} + 0.3	V
		2.7 ≤ V _{CC} ≤ 3.6		2.2	-	V _{CC} + 0.3	
V _{IL}	Input LOW voltage	2.2 ≤ V _{CC} ≤ 2.7		-0.3	-	0.6	V
		2.7 ≤ V _{CC} ≤ 3.6		-0.3	-	0.8	
I _{IX}	Input leakage current	GND ≤ V _I ≤ V _{CC}		-1	-	+1	μA
I _{OZ}	Output leakage current	GND ≤ V _O ≤ V _{CC} , Output disabled		-1	-	+1	μA
I _{CC}	V _{CC} operating supply current	f = f _{MAX} = 1/t _{RC}	V _{CC} = 3.6 V, I _{OUT} = 0 mA, CMOS level	-	5	10	mA
		f = 1 MHz		-	0.85	1.5	
I _{SB1}	Automatic CE power-down current – CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2 \text{ V},$ $V_{IN} \geq V_{CC} - 0.2 \text{ V}, V_{IN} \leq 0.2 \text{ V},$ $f = f_{MAX}$ (Address and data only), $f = 0$ (\overline{OE} , \overline{WE} , \overline{BHE} and \overline{BLE})		-	1.5	4	μA
I _{SB2}	Automatic CE power-down current – CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2 \text{ V},$ $V_{IN} \geq V_{CC} - 0.2 \text{ V or } V_{IN} \leq 0.2 \text{ V},$ $f = 0, V_{CC} = 3.6 \text{ V}$		-	1.5	4	μA

Notes

- V_{IL(min)} = -2.0 V for pulse durations less than 20 ns., V_{IH(max)} = V_{CC} + 0.75 V for pulse durations less than 20 ns.
- Full device operation requires linear ramp of V_{CC} from 0 V to V_{CC(min)} and V_{CC} must be stable at V_{CC(min)} for 500 μs.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.

Capacitance

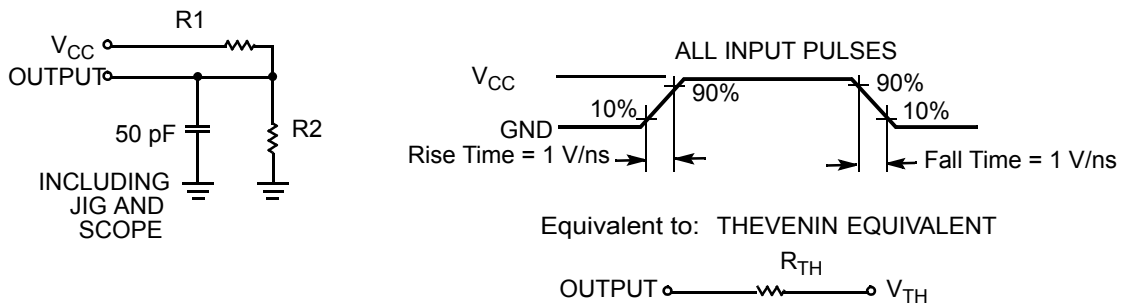
Parameter ^[7]	Description	Test Conditions	Max	Unit
C _{IN}	Input capacitance	T _A = 25 °C, f = 1 MHz, V _{CC} = V _{CC(typ)}	8	pF
C _{OUT}	Output capacitance		8	pF

Thermal Resistance

Parameter ^[8]	Description	Test Conditions	FBGA	TSOP-II	Unit
θ _{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	52.02	62.01	°C/W
θ _{JC}	Thermal resistance (junction to case)		10.98	22.08	°C/W

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms



Parameters	2.5 V (2.2 V–2.7 V)	3.0 V (2.7 V–3.6 V)	Unit
R ₁	16600	1103	Ω
R ₂	15400	1554	Ω
R _{TH}	8000	645	Ω
V _{TH}	1.20	1.75	V

Note

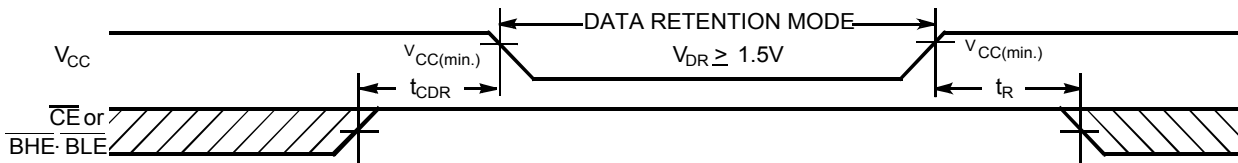
7. Tested initially and after any design or process changes that may affect these parameters.

Data Retention Characteristics

Parameter	Description	Conditions	Min	Typ ^[9]	Max	Unit
V _{DR}	V _{CC} for data retention		1.5	–	–	V
I _{CCDR}	Data retention current	V _{CC} = 1.5 V, $\overline{CE} \geq V_{CC} - 0.2$ V, V _{IN} ≥ V _{CC} - 0.2 V or V _{IN} ≤ 0.2 V		–	3	μA
t _{CDR}	Chip deselect to data retention time		0	–	–	ns
t _R ^[10]	Operation recovery time		55	–	–	ns

Data Retention Waveform

Figure 4. Data Retention Waveform ^[11]



Notes

- 8. Tested initially and after any design or process changes that may affect these parameters.
- 9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.
- 10. Full device operation requires linear V_{CC} ramp from V_{DR} to V_{CC(min)} > 200 μs.

Switching Characteristics

Over the Operating Range

Parameter ^[12]	Description	CY62127DV30-55		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	55	–	ns
t_{AA}	Address to data valid	–	55	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	\overline{CE} LOW to data valid	–	55	ns
t_{DOE}	\overline{OE} LOW to data valid	–	25	ns
t_{LZOE}	\overline{OE} LOW to low Z ^[13]	5	–	ns
t_{HZOE}	\overline{OE} HIGH to high Z ^[13, 14]	–	20	ns
t_{LZCE}	\overline{CE} LOW to low Z ^[13]	10	–	ns
t_{HZCE}	\overline{CE} HIGH to high Z ^[13, 14]	–	20	ns
t_{PU}	\overline{CE} LOW to power-up	0	–	ns
t_{PD}	\overline{CE} HIGH to power-down	–	55	ns
t_{DBE}	$\overline{BLE}/\overline{BHE}$ LOW to data valid	–	55	ns
t_{LZBE} ^[15]	$\overline{BLE}/\overline{BHE}$ LOW to low Z ^[13]	5	–	ns
t_{HZBE}	$\overline{BLE}/\overline{BHE}$ HIGH to high Z ^[13, 14]	–	20	ns
Write Cycle^[16, 17]				
t_{WC}	Write cycle time	55	–	ns
t_{SCE}	\overline{CE} LOW to write end	40	–	ns
t_{AW}	Address setup to write end	40	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	\overline{WE} pulse width	40	–	ns
t_{BW}	$\overline{BLE}/\overline{BHE}$ LOW to write end	40	–	ns
t_{SD}	Data setup to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	\overline{WE} LOW to high Z ^[13, 14]	–	20	ns
t_{LZWE}	\overline{WE} HIGH to low Z ^[13]	10	–	ns

Notes

11. $\overline{BHE}.\overline{BLE}$ is the AND of both \overline{BHE} and \overline{BLE} . Chip can be deselected by either disabling the Chip Enable signals or by disabling both byte enable pins.
12. Test conditions assume signal transition time of 1V/ns or less, timing reference levels of $V_{CC(typ.)}/2$, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL} .
13. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any device.
14. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
15. If both byte enables are toggled together, this value is 10 ns.
16. The internal Write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE} = V_{IL}$, \overline{BHE} and/or $\overline{BLE} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
17. The minimum write pulse width for WRITE Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW) should be sum of t_{HZWE} and t_{SD} .

Switching Waveforms

Figure 5. Read Cycle No. 1 (Address Transition Controlled) [18, 19]

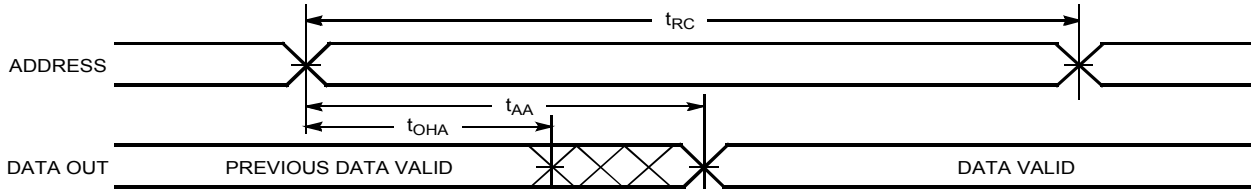
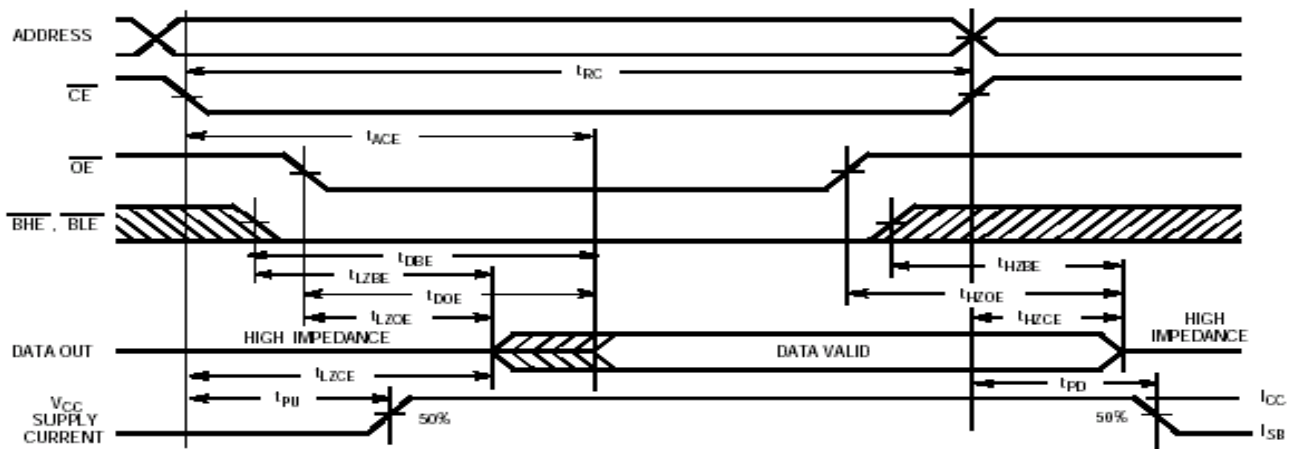


Figure 6. Read Cycle No. 2 (\overline{OE} Controlled) [18, 19, 20]



Notes

- 18. Device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$, \overline{BHE} , $\overline{BLE} = V_{IL}$.
- 19. \overline{WE} is HIGH for Read cycle.
- 20. Address valid prior to or coincident with \overline{CE} , \overline{BHE} , \overline{BLE} transition LOW.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 1 (\overline{WE} Controlled) [21, 22, 23, 24, 25]

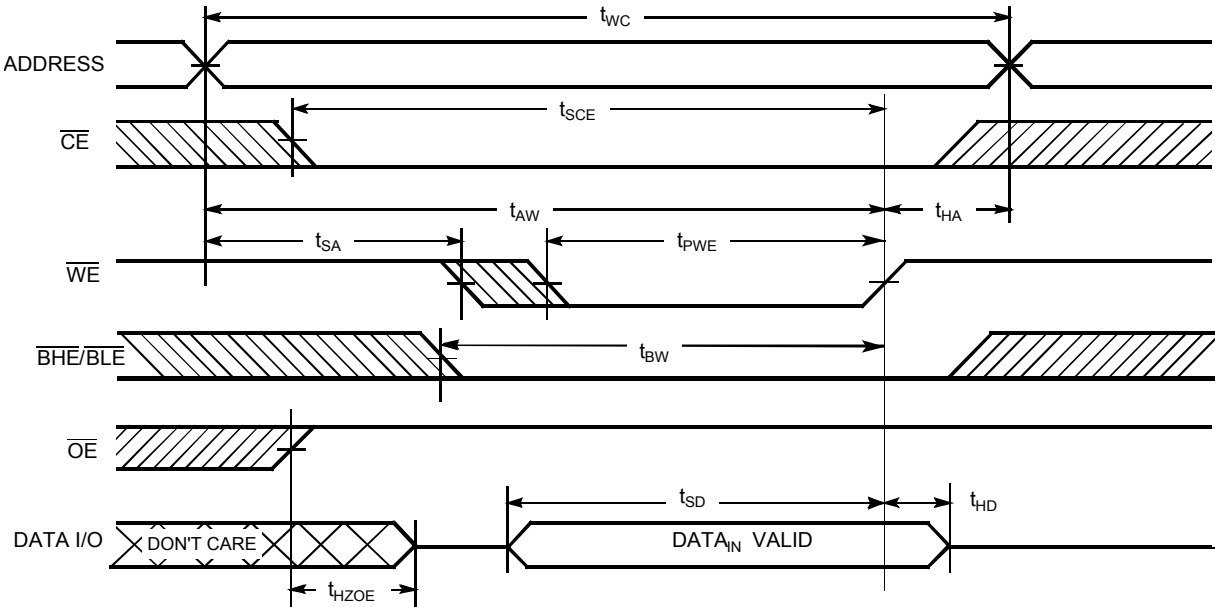
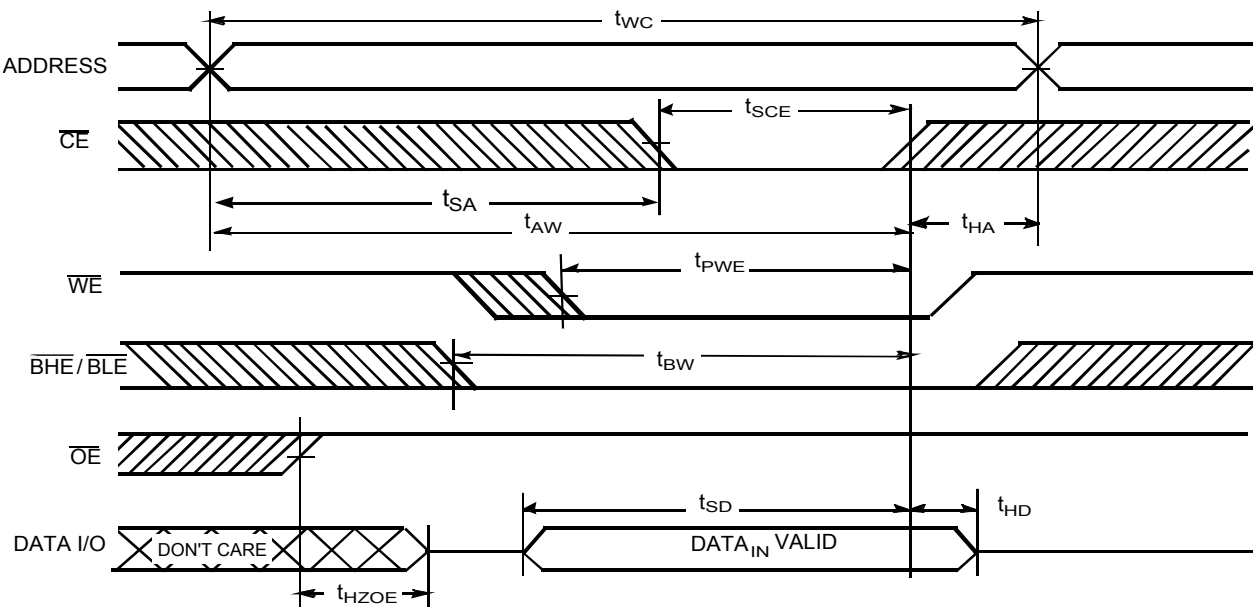


Figure 8. Write Cycle No. 2 (\overline{CE} Controlled) [21, 22, 23, 24, 25]



Notes

21. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
22. The internal Write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE} = V_{IL}$, BHE and/or BLE = V_{IL} . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
23. Data I/O is high-impedance if $\overline{OE} = V_{IH}$.
24. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.
25. During the DON'T CARE period in the DATA I/O waveform, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW) [26, 27, 28]

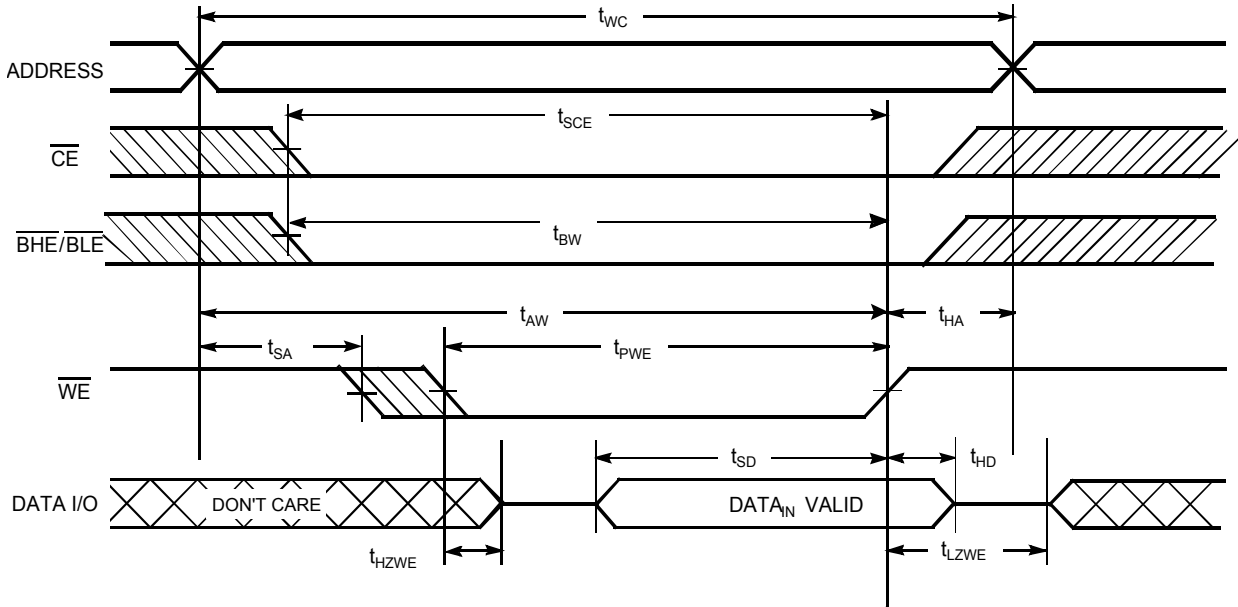
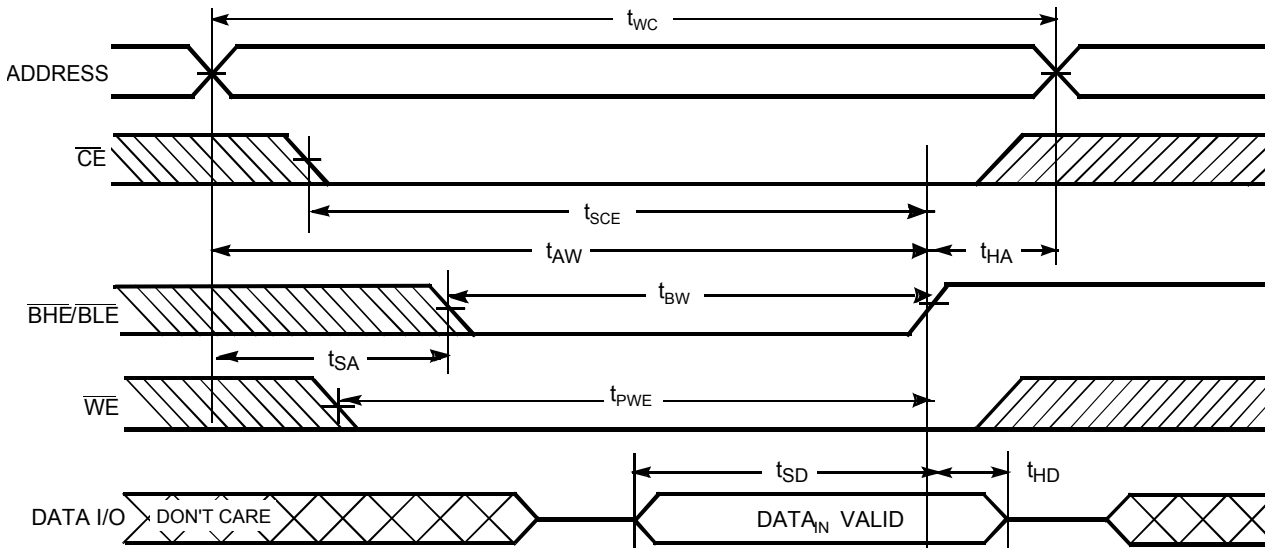


Figure 10. Write Cycle No. 4 (\overline{BHE} / \overline{BLE} Controlled) [26, 27]



Notes

- 26. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.
- 27. During the DON'T CARE period in the DATA I/O waveform, the I/Os are in output state and input signals should not be applied.
- 28. The minimum write pulse width for WRITE Cycle No.3 (\overline{WE} Controlled, \overline{OE} LOW) should be sum of t_{HZWE} and t_{SD} .

Truth Table

$\overline{\text{CE}}$ [29, 30]	$\overline{\text{WE}}$	$\overline{\text{OE}}$	$\overline{\text{BHE}}$	$\overline{\text{BLE}}$	I/O ₀ –I/O ₇	I/O ₈ –I/O ₁₅	Mode	Power
H	X	X	X	X	High Z	High Z	Deselect/Power-down	Standby (I _{SB})
L	X	X	H	H	High Z	High Z	Deselect/Power-down	Standby (I _{SB})
L	H	L	L	L	Data Out	Data Out	Read All Bits	Active (I _{CC})
L	H	L	H	L	Data Out	High Z	Read Lower Byte Only	Active (I _{CC})
L	H	L	L	H	High Z	Data Out	Read Upper Byte Only	Active (I _{CC})
L	H	H	L	L	High Z	High Z	Output Disabled	Active (I _{CC})
L	H	H	H	L	High Z	High Z	Output Disabled	Active (I _{CC})
L	H	H	L	H	High Z	High Z	Output Disabled	Active (I _{CC})
L	L	X	L	L	Data in	Data in	Write	Active (I _{CC})
L	L	X	H	L	Data in	High Z	Write Lower Byte Only	Active (I _{CC})
L	L	X	L	H	High Z	Data in	Write Upper Byte Only	Active (I _{CC})

Notes

29. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ HIGH, the output remains in a high-impedance state.

30. During the DON'T CARE period in the DATA I/O waveform, the I/Os are in output state and input signals should not be applied.

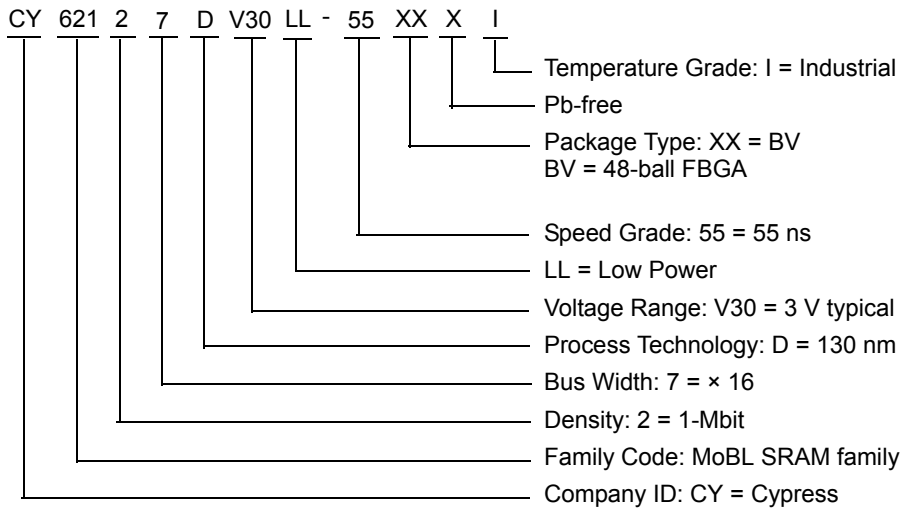
Ordering Information

Cypress offers other versions of this type of product in many different configurations and features. The below table contains only the list of parts that are currently available. For a complete listing of all options, visit the Cypress website at www.cypress.com and see product summary page at <http://www.cypress.com/products> or contact your local sales representative.

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives and distributors. To find the office closest to you, visit us at <http://www.cypress.com/go/datasheet/offices>.

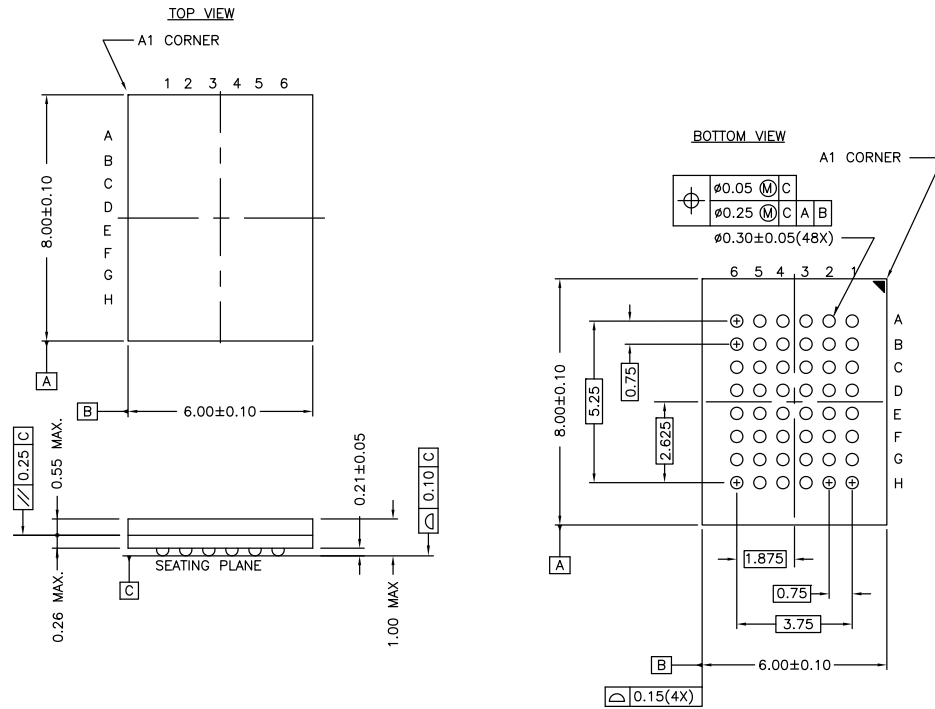
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62127DV30LL-55BVXI	51-85150	48-ball FBGA (6 mm × 8 mm × 1 mm) (Pb-free)	Industrial

Ordering Code Definitions



Package Diagrams

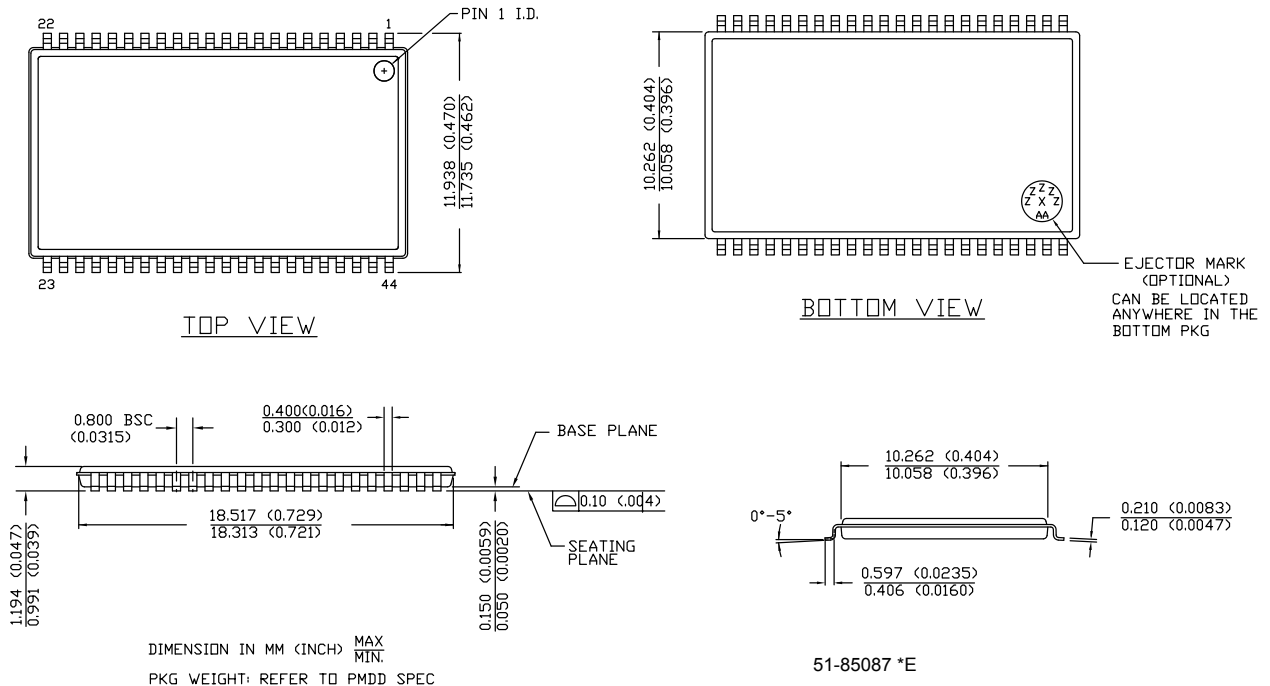
Figure 11. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150



NOTE:
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 *H

Figure 12. 44-pin TSOP Z44-II Package Outline, 51-85087



51-85087 *E

Acronyms

Acronym	Description
$\overline{\text{BHE}}$	Byte High Enable
$\overline{\text{BLE}}$	Byte Low Enable
CMOS	Complementary Metal Oxide Semiconductor
$\overline{\text{CE}}$	Chip Enable
FBGA	Fine-Pitch Ball Grid Array
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
$\overline{\text{WE}}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
μA	microampere
mA	milliampere
ns	nanosecond
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62127DV30 MoBL [®] , 1-Mbit (64K × 16) Static RAM Document Number: 38-05229				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	117690	JUI	08/27/02	New data sheet
*A	127311	MPR	06/13/03	Changed status from Advanced to Preliminary. Updated DC Electrical Characteristics : Changed maximum value of I _{SB2} parameter from 4 μA to 5 μA corresponding to Test Condition "L". Changed maximum value of I _{SB2} parameter from 3 μA to 4 μA corresponding to Test Condition "LL". Updated Capacitance : Changed value of C _{IN} parameter from 6 pF to 8 pF. Updated Data Retention Characteristics : Changed maximum value of I _{CCDR} parameter from 1.2 μA to 4 μA corresponding to Test Condition "L". Changed maximum value of I _{CCDR} parameter from 0.8 μA to 3 μA corresponding to Test Condition "LL".
*B	128341	JUI	07/22/03	Changed status from Preliminary to Final. Add 70 ns speed related information in all instances across the document. Updated Ordering Information .
*C	129000	CDY	08/29/03	Updated DC Electrical Characteristics : Changed typical value of I _{CC} parameter corresponding to Test Condition "f = 1 MHz" from 0.5 mA to 0.85 mA.
*D	316039	PCI	See ECN	Added 45 ns speed bin related information in all instances across the document. Updated AC Test Loads and Waveforms : Added Note "Test condition for the 45-ns part is a load capacitance of 30 pF." and referred the same note in Figure 3 . Updated Ordering Information : Updated part numbers. Changed name of 44-lead TSOP-II package from Z44 to ZS44 in "Package Name" column.
*E	346982	AJU	See ECN	Added 56-pin QFN package related information in all instances across the document. Updated Ordering Information .
*F	369955	SYT	See ECN	Added Automotive related information in all instances across the document. Updated Features : Added Temperature Ranges. Updated Ordering Information : Added Pb-free Automotive parts for 55 ns Speed bin.
*G	457685	NXR	See ECN	Removed 56-pin QFN package related information in all instances across the document. Updated Ordering Information .
*H	470383	NXR	See ECN	Updated Pin Configurations : Updated Figure 2 (Changed pin 23 of TSOP II from NC to DNU). Updated Note 3.
*I	2897885	RAME / NIKM	03/22/10	Updated Ordering Information (Removed inactive parts). Updated Package Diagrams .

Document History Page *(continued)*

Document Title: CY62127DV30 MoBL®, 1-Mbit (64K × 16) Static RAM				
Document Number: 38-05229				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
*J	3010373	AJU	08/20/2010	Updated Features . Updated Product Portfolio . Updated Operating Range . Updated DC Electrical Characteristics . Updated Data Retention Characteristics . Updated Switching Characteristics . Updated Ordering Information and added Ordering Code Definitions . Minor edits. Updated to new template.
*K	3329789	RAME	07/27/11	Updated Functional Description : Removed the Note "For best practice recommendations, refer to the Cypress application note "System Design Guidelines" at http://www.cypress.com website." and its reference. Updated to new template.
*L	3393183	RAME	10/03/11	Post to web.
*M	3861271	TAVA	01/08/2013	Updated Ordering Information (Updated part numbers). Updated Package Diagrams : spec 51-85150 – Changed revision from *G to *H. spec 51-85087 – Changed revision from *D to *E.
*N	4499469	MEMJ	09/11/2014	Updated Switching Characteristics : Added Note 17 and referred the same note in "Write Cycle". Updated Switching Waveforms : Added Note 28 and referred the same note in Figure 9 . Updated to new template. Completing Sunset Review.
*O	4576478	MEMJ	11/21/2014	Updated Functional Description : Added "For a complete list of related documentation, click here ." at the end.
*P	4920942	VINI	09/15/2015	Updated to new template. Completing Sunset Review.
*Q	5444200	VINI	09/21/2016	Updated Thermal Resistance : Replaced "two-layer" with "four-layer" in "Test Conditions" column. Updated all values of θ_{JA} and θ_{JC} parameters. Updated to new template. Completing Sunset Review.
*R	5997966	AESATMP9	12/21/2017	Updated logo and copyright.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Arm [®] Cortex [®] Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC[®] Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6 MCU](#)

Cypress Developer Community

[Community](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2002-2017. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. No computing device can be absolutely secure. Therefore, despite security measures implemented in Cypress hardware or software products, Cypress does not assume any liability arising out of any security breach, such as unauthorized access to or use of a Cypress product. In addition, the products described in these materials may contain design defects or errors known as errata which may cause the product to deviate from published specifications. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.



Стандарт Электрон Связь

Мы молодая и активно развивающаяся компания в области поставок электронных компонентов. Мы поставляем электронные компоненты отечественного и импортного производства напрямую от производителей и с крупнейших складов мира.

Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию .

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России , а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

Минимальные сроки поставки, гибкие цены, неограниченный ассортимент и индивидуальный подход к клиентам являются основой для выстраивания долгосрочного и эффективного сотрудничества с предприятиями радиоэлектронной промышленности, предприятиями ВПК и научно-исследовательскими институтами России.

С нами вы становитесь еще успешнее!

Наши контакты:

Телефон: +7 812 627 14 35

Электронная почта: sales@st-electron.ru

Адрес: 198099, Санкт-Петербург,
Промышленная ул, дом № 19, литера Н,
помещение 100-Н Офис 331