ADVANCE

CYW4390

WICED™ Wi-Fi IEEE 802.11 b/g/n SoC with Embedded Application Processor

The Cypress CYW4390 is a single-chip device that provides the highest level of integration for applications targeting the Internet of Things and provides a complete embedded wireless system solution included in a system-on-a-chip (SOC). The CYW4390 device supports all the rates specified in the IEEE 802.11 b/g/n specifications. Included on-chip are an ARM Cortex-based applications processor, single stream IEEE 802.11n MAC/baseband/radio, a 2.4 GHz transmit power amplifier (PA), and a receive low-noise amplifier (LNA). It also supports optional antenna diversity for improved RF performance in difficult environments.

CYW4390 is an optimized SoC targeting embedded applications in the industrial and medical sensor, home appliances and, generally, internet-of-things space.

Using advanced design techniques and process technology to reduce active and idle power, the CYW4390 is designed to address the needs of embedded devices that require minimal power consumption and compact size.

It includes a power management unit which simplifies the system power topology and allows for direct operation from a battery for battery powered applications while maximizing battery life.

Cypress Part Numbering Scheme

Cypress is converting the acquired IoT part numbers from Broadcom to the Cypress part numbering scheme. Due to this conversion, there is no change in form, fit, or function as a result of offering the device with Cypress part number marking. The table provides Cypress ordering part number that matches an existing IoT part number.

Table 1. Mapping Table for Part Number between Broadcom and Cypress

Broadcom Part Number	Cypress Part Number
BCM4390	CYW4390
BCM4390DKWBG	CYW4390DKWBG
BCM4390DKWBGT	CYW4390DKWBGT

Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use.

For a comprehensive list of acronyms and other terms used in Cypress documents, go to http://www.cypress.com/glossary.

Features

General Features

- Supports battery voltage range from 3.0V to 5.25V supplies with internal switching regulator.
- Programmable dynamic power management
- 6k-bit OTP for storing board parameters
- Package options: 286 bump WLCSP (4.87 mm x 5.413 mm; 0.2 mm pitch)

Key IEEE 802.11x Features

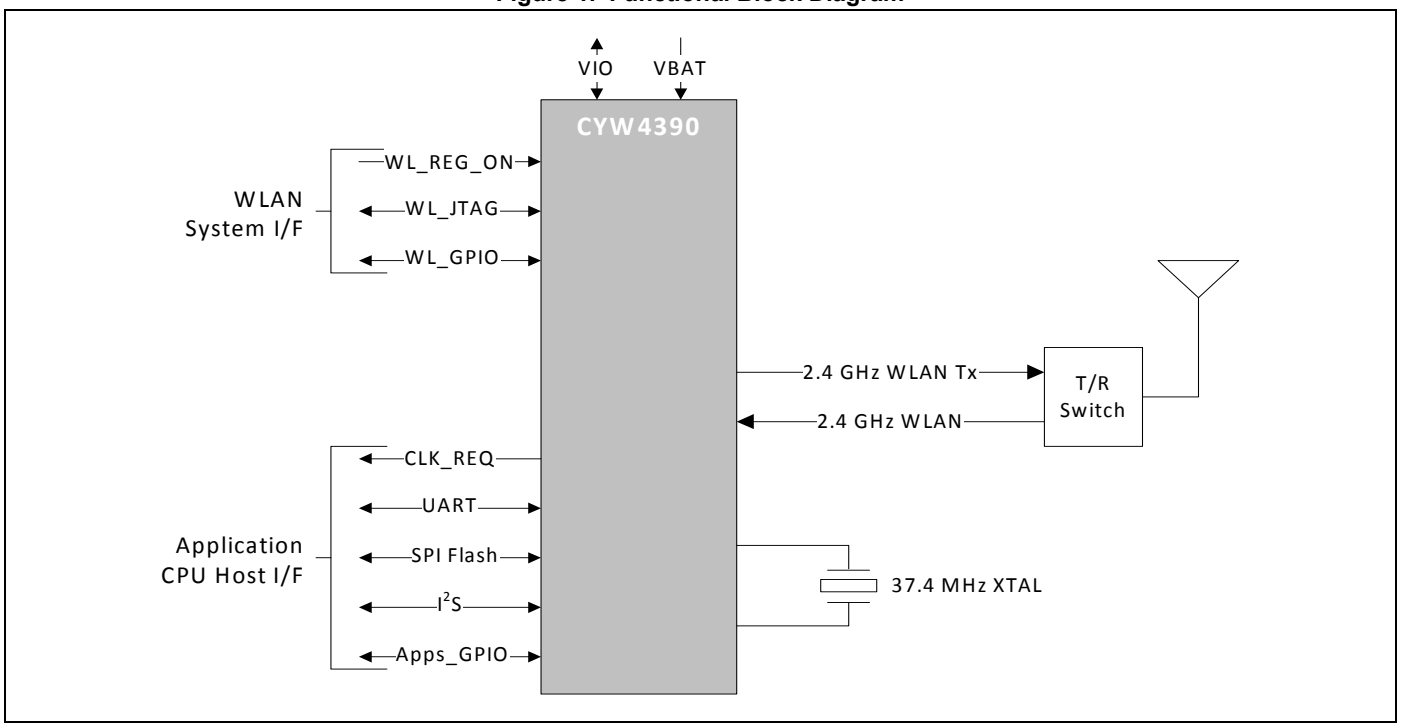
- IEEE 802.11n compliant
- Single-stream spatial multiplexing up to 72 Mbps data rate
- Supports 20 MHz channels with optional SGI.
- Full IEEE 802.11 b/g legacy compatibility with enhanced performance
- Tx and Rx low-density parity check (LDPC) support for improved range and power efficiency
- On-chip power and low-noise amplifiers.
- Internal fractional nPLL allows support for a wide range of reference clock frequencies.
- Supports IEEE 802.15.2 external coexistence interface to optimize bandwidth utilization with other co-located wireless technologies such as Bluetooth, LTE, GPS, or WiMAX.
- Integrated ARMCR4™ processor with tightly coupled memory for complete WLAN subsystem functionality, minimizing the need to wake up the applications processor for standard WLAN functions (to further minimize power consumption while maintaining the ability to upgrade to future features in the field)
- Software architecture supported by standard WICED SDK to allow easy migration from existing discrete MCU designs and to future devices

- Security support:
  - WPA™ and WPA2™ (Personal) support for powerful encryption and authentication
  - AES and TKIP in hardware for faster data encryption and IEEE 802.11i compatibility
  - Reference WLAN subsystem provides Cisco® Compatible Extensions (CCX, CCX 2.0, CCX 3.0, CCX 4.0, CCX 5.0)
  - Supports Wi-Fi Protected Setup and Wi-Fi Easy-Setup
- Worldwide regulatory support: Global products supported with worldwide homologated design

Application Processor Features

- ARM Cortex-M3 32-bit RISC processor
- 448 KB RAM for application code and data execution

Figure 1. Functional Block Diagram



IoT Resources

Cypress provides a wealth of data at http://www.cypress.com/internet-things-iot to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. Cypress provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the Cypress Support Community website (http://community.cypress.com/).

Contents

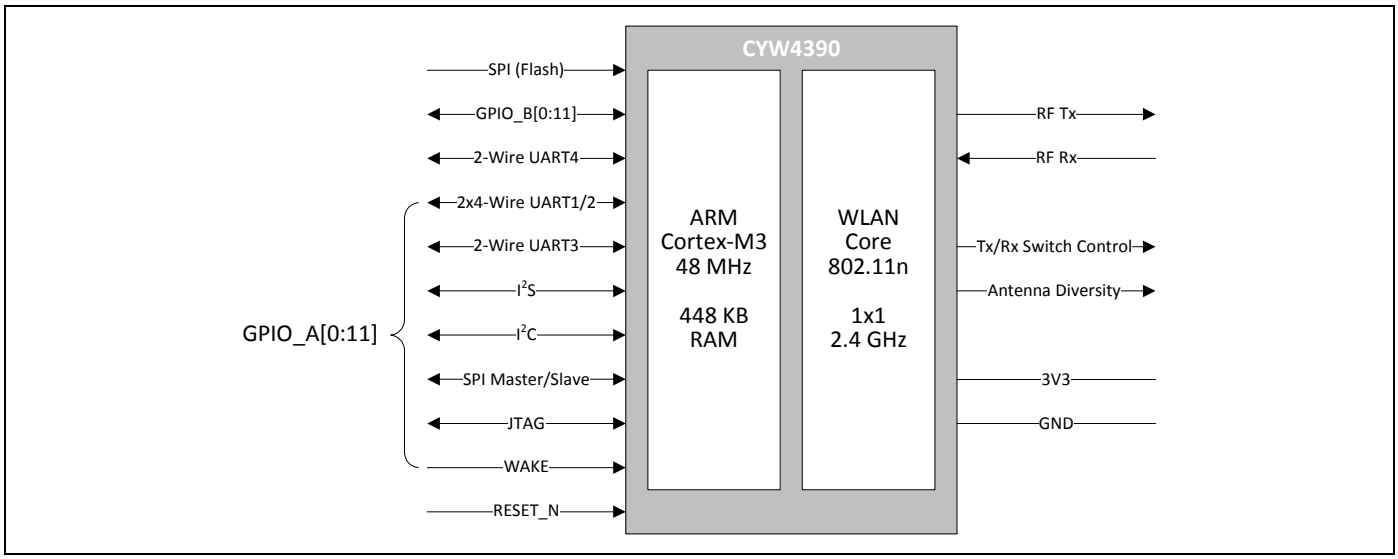
1. Overview

1.1 Overview

The Cypress CYW4390 is a single-chip device that provides the highest level of integration for an embedded system-on-a-chip with integrated IEEE 802.11 b/g/n MAC/baseband/radio and a separate ARM-Cortex M3 applications processor. It provides a small form-factor solution with minimal external components to drive down cost for mass volumes and allows for an embedded system with flexibility in size, form, and function. Comprehensive power management circuitry and software ensure the system can meet the needs of highly embedded systems that require minimal power consumption and reliable operation.

Figure 2 shows the interconnect of all the major physical blocks in the CYW4390 and their associated external interfaces, which are described in greater detail in the following sections.

Figure 2. Block Diagram and IO



1.2 Features

The CYW4390 supports the following features:

- ARM Cortex-M3 clocked at 48 MHz
- 448 KB of SRAM available for the applications processor
- Two high-speed 4-wire UART interfaces with operation up to 4 Mbps
- Two low-speed 2-wire UART interfaces
- One generic SPI master/slave interface with operation up to 24 MHz
- One SPI master interface for serial flash
- One I^2C interface
- One I^2S interface
- 24 x GPIOs (12 dedicated,12 with alternate functions)
- IEEE 802.11 b/g/n 1x1 2.4 GHz radio
- Single- and dual-antenna support

1.3 Standards Compliance

The CYW4390 supports the following standards:

- IEEE 802.11n
- IEEE 802.11b
- IEEE 802.11g
- IEEE 802.11d
- IEEE 802.11h
- IEEE 802.11i
- Security:
  - WEP
  - WPA™ Personal
  - WPA2™ Personal
  - WMM
  - WMM-PS (U-APSD)
  - WMM-SA
  - AES (hardware accelerator)
  - TKIP (hardware accelerator)
  - CKIP (software support)
- Proprietary Protocols:
  - CCXv2
  - CCXv3
  - CCXv4
  - CCXv5
  - WFAEC

The CYW4390 supports the following additional standards:

- IEEE 802.11r—fast roaming (between APs)
- IEEE 802.11w—secure management frames
- IEEE 802.11 Extensions:
  - IEEE 802.11e QoS enhancements (as per the WMM® specification is already supported)
  - IEEE 802.11i MAC enhancements
  - IEEE 802.11k radio resource measurement

2. Power Supplies and Power Management

2.1 CYW4390 PMU Features

- VBAT to 1.35Vout (275 mA nominal, 600 mA maximum) Core-Buck (CBUCK) switching regulator
- VBAT to 3.3Vout (200 mA nominal, 450 mA maximum) LDO3P3
- 1.35V to 1.2Vout (100 mA nominal, 150 mA maximum) LNLDO
- 1.35V to 1.2out (175 mA nominal, 300 mA maximum) CLDO with bypass mode for deep sleep
- Additional internal LDOs (not externally accessible)

2.2 Power Supply Topology

One buck regulator, multiple LDO regulators, and a power management unit (PMU) are integrated into the CYW4390. All regulators are programmable via the PMU. These blocks simplify power supply design for embedded designs.

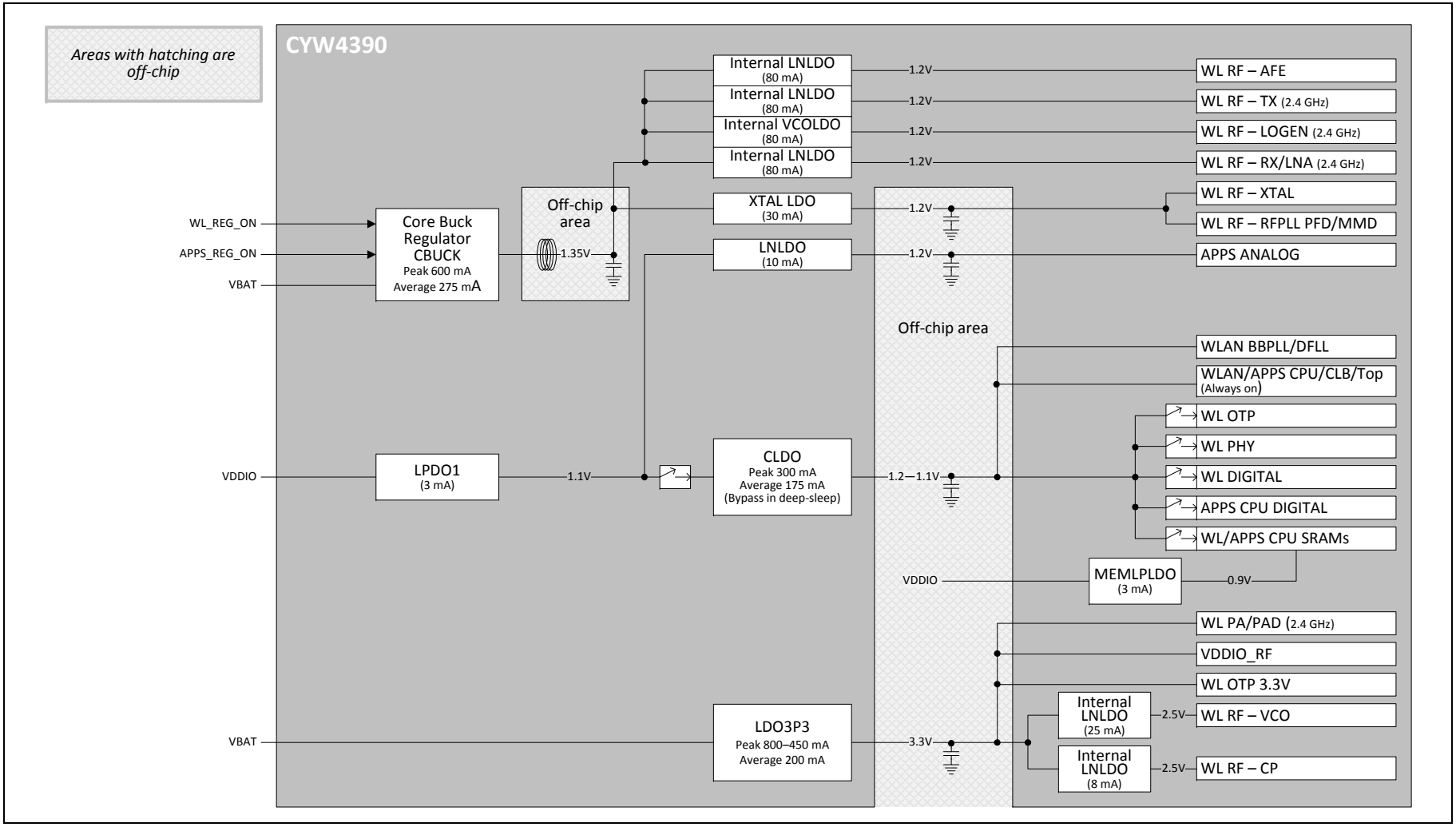
A single VBAT (3.0V to 5.25V DC max) and VIO supply (1.8V to 3.3V) can be used, with all additional voltages being provided by the regulators in the CYW4390.

Two control signals, APPS_REG_ON and WL_REG_ON, are used to power-up the regulators and take the respective core out of reset. The CBUCK CLDO and LNLDO power up when any of the reset signals are deasserted. All regulators are powered down only when both APPS_REG_ON and WL_REG_ON are deasserted. The applications processor can drive WL_REG_ON internally when the pin is externally tied to ground. The CLDO and LNLDO may be turned off/on based on the dynamic demands of the application.

The CYW4390 allows for an extremely low power-consumption mode by completely shutting down the CBUCK, CLDO, and LNLDO regulators. When in this state, LPLDO1 and LPLDO2 (which are low-power linear regulators that are supplied by the system VIO supply) provide the CYW4390 with all the voltages it requires, further reducing leakage currents.

Figure 3 shows the regulators and a typical power topology.

Figure 3. Typical Power Topology



2.3 Power Management

The CYW4390 has been designed with the stringent power consumption requirements of embedded devices in mind. All areas of the chip design are optimized to minimize power consumption. Silicon processes and cell libraries were chosen to reduce leakage current and supply voltages. Additionally, the CYW4390 integrated RAM is a high Vt memory with dynamic clock control. The dominant supply current consumed by the RAM is leakage current only. The CYW4390 also includes an advanced WLAN power management unit (PMU) sequencer. The PMU sequencer provides significant power savings by putting the CYW4390 into various power management states appropriate to the current environment and activities that are being performed. The power management unit enables and disables internal regulators, switches, and other blocks based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them. Power up sequences are fully programmable. Configurable, free-running counters (running at 32.768 kHz LPO clock) in the PMU sequencer are used to turn on/turn off individual regulators and power switches. Clock speeds are dynamically changed (or gated altogether) for the current mode. Slower clock speeds are used wherever possible.

The CYW4390 WLAN-specific power states are described as follows:

- Active mode—All WLAN blocks in the CYW4390 are powered up and fully functional with active carrier sensing and frame transmission and receiving. All required regulators are enabled and put in the most efficient mode based on the load current. Clock speeds are dynamically adjusted by the PMU sequencer.
- Doze mode—The radio, analog domains, and most of the linear regulators are powered down. The rest of the WLAN portion of the CYW4390 remains powered up in an IDLE state. All main clocks (PLL, crystal oscillator or TCXO) are shut down to reduce active power to the minimum. The 32.768 kHz LPO clock is available only for the PMU sequencer. This condition is necessary to allow the PMU sequencer to wake up the chip and transition to Active mode. In Doze mode, the primary power consumed by the WLAN core is due to leakage current.
- Deep-sleep mode—Most of the chip including both analog and digital domains and most of the regulators are powered off. Logic states in the digital core are saved and preserved into a retention memory in the always-ON domain before the digital core is powered off. Upon a wake-up event triggered by the PMU timers or an external interrupt, logic states in the digital core are restored to their pre-deep-sleep settings to avoid lengthy HW reinitialization.
- Power-down mode—The CYW4390 is effectively powered off by shutting down all internal regulators. The chip is brought out of this mode by external logic re-enabling the internal regulators.

The CYW4390 application processor subsystem can be independently powered on or off at the system level in the power-down mode. In addition it is also possible to keep the application processor in active mode while the WLAN blocks are in Doze or Deep-Sleep.

2.4 PMU Sequencing

The PMU sequencer is responsible for minimizing system power consumption. It enables and disables various system resources based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them.

Resource requests may come from several sources: clock requests from cores, the minimum resources defined in the ResourceMin register, and the resources requested by any active resource request timers. The PMU sequencer maps clock requests into a set of resources required to produce the requested clocks.

Each resource is in one of four states: enabled, disabled, transition_on, and transition_off and has a timer that contains 0 when the resource is enabled or disabled and a non-zero value in the transition states. The timer is loaded with the time_on or time_off value of the resource when the PMU determines that the resource must be enabled or disabled. That timer decrements on each 32.768 kHz PMU clock. When it reaches 0, the state changes from transition_off to disabled or transition_on to enabled. If the time_on value is 0, the resource can go immediately from disabled to enabled. Similarly, a time_off value of 0 indicates that the resource can go immediately from enabled to disabled. The terms enable sequence and disable sequence refer to either the immediate transition or the timer load-decrement sequence.

During each clock cycle, the PMU sequencer performs the following actions:

- Computes the required resource set based on requests and the resource dependency table.
- Decrements all timers whose values are non zero. If a timer reaches 0, the PMU clears the ResourcePending bit for the resource and inverts the ResourceState bit.
- Compares the request with the current resource status and determines which resources must be enabled or disabled.
- Initiates a disable sequence for each resource that is enabled, no longer being requested, and has no powered up dependents.
- Initiates an enable sequence for each resource that is disabled, is being requested, and has all of its dependencies enabled.

2.5 Power-Off Shutdown

The CYW4390 provides a low-power shutdown feature that allows the device to be turned off. When the CYW4390 is not needed in the system, VDDIO_RF and VDDC are shut down while VDDIO remains powered. This allows the CYW4390 to be effectively off while keeping the I/O pins powered so that they do not draw extra current from any other devices connected to the I/O.

During a low-power shut-down state, provided VDDIO remains applied to the CYW4390, all outputs are tristated, and most inputs signals are disabled. Input voltages must remain within the limits defined for normal operation. This is done to prevent current paths or create loading on any digital signals in the system, and enables the CYW4390 to be fully integrated in an embedded device and take full advantage of the lowest power-savings modes.

When the CYW4390 is powered on from this state, it is the same as a normal power-up and the device does not retain any information about its state from before it was powered down.

2.6 Power-Up/Power-Down/Reset Circuits

The CYW4390 has two signals (see Table 2) that enable or disable the application CPU and WLAN subsystems and the internal regulator blocks, allowing external system circuitry to control power consumption. For timing diagrams of these signals and the required power-up sequences, see Power-Up Sequence and Timing on page 56.

Table 2. Power-Up/Power-Down/Reset Control Signals

Signal	Description
WL_REG_ON	This signal is used by the PMU (with APPS_REG_ON) to power up the WLAN section. It is also OR-gated with the APPS_REG_ON input to control the internal CYW4390 regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low, the WLAN section is in reset. If APPS_REG_ON and WL_REG_ON are both low, the regulators are disabled. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
APPS_REG_ON	This signal is used by the PMU (with WL_REG_ON) to decide whether or not to power down the internal CYW4390 regulators. If APPS_REG_ON and WL_REG_ON are low, the regulators will be disabled. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.

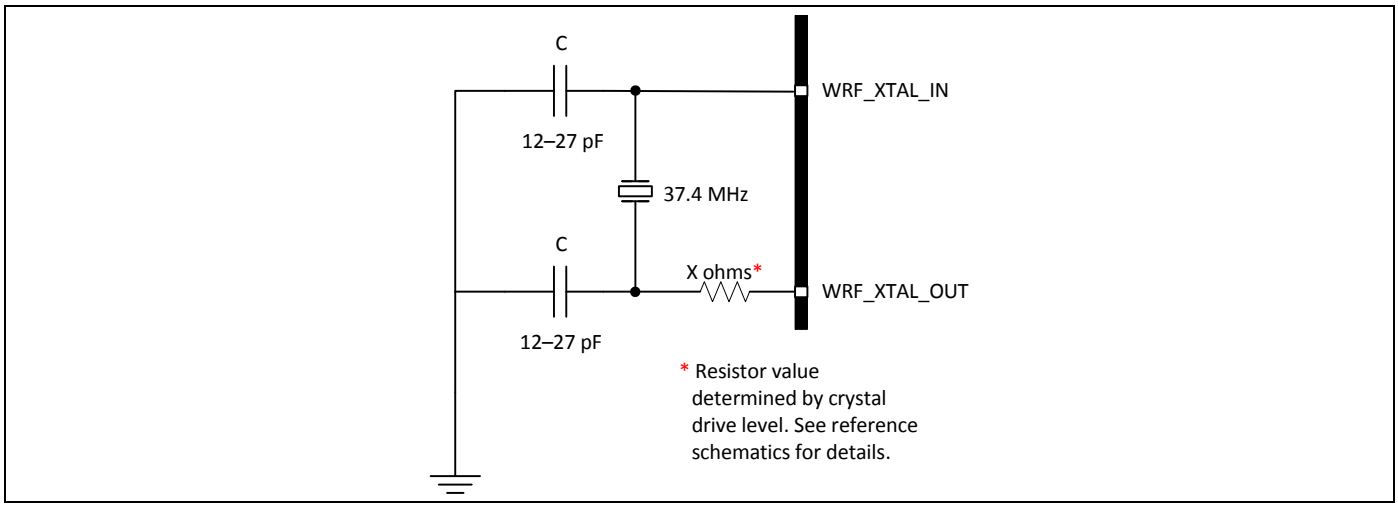
3. Frequency References

An external crystal is used for generating all radio frequencies and normal operation clocking. As an alternative, an external frequency reference may be used. In addition, a low-power oscillator (LPO) is provided for lower power mode timing.

3.1 Crystal Interface and Clock Generation

The CYW4390 can use an external crystal to provide a frequency reference. The recommended configuration for the crystal oscillator including all external components is shown in Figure 4. Consult the reference schematics for the latest configuration.

Figure 4. Recommended Oscillator Configuration



A fractional-N synthesizer in the CYW4390 generates the radio frequencies, clocks, and data/packet timing, enabling it to operate using a wide selection of frequency references.

The recommended default frequency reference is a 37.4 MHz crystal. The signal characteristics for the crystal interface are listed in Table 3 on page 11.

Note: Although the fractional-N synthesizer can support alternative reference frequencies, frequencies other than the default require support to be added in the driver, plus additional extensive system testing. Contact Cypress for further details.

3.2 External Frequency Reference

As an alternative to a crystal, an external precision frequency reference can be used, provided that it meets the Phase Noise requirements listed in Table 3.

If used, the external clock should be connected to the WRF_XTAL_IN pin through an external 1000 pF coupling capacitor, as shown in Figure 5. The internal clock buffer connected to this pin will be turned OFF when the CYW4390 goes into sleep mode. When the clock buffer turns ON and OFF there will be a small impedance variation. Power must be supplied to the WRF_XTAL_BUCK_VDD1P5 pin.

Figure 5. Recommended Circuit to Use with an External Reference Clock

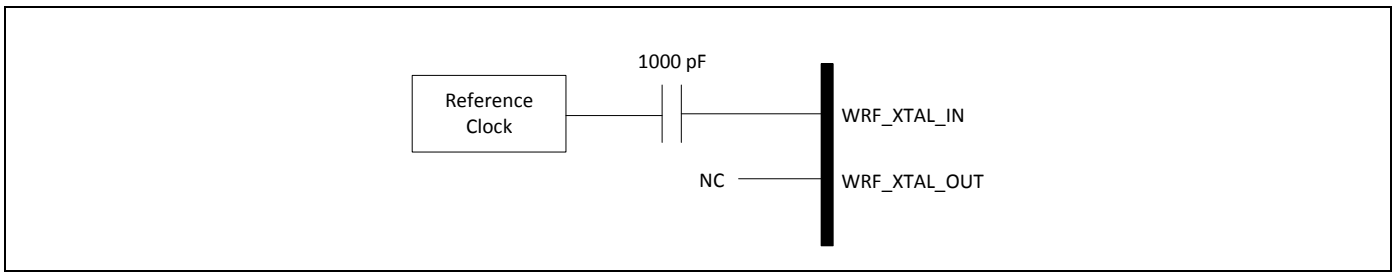


Table 3. Crystal Oscillator and External Clock – Requirements and Performance

Parameter	Conditions/Notes	Crystal[a]			External Frequency Reference[b c]			
		Min	Typ	Max	Min	Typ	Max	Units
Frequency	IEEE 802.11 b/g/n operation	Between 19 MHz and 52 MHz[d]						
Frequency tolerance over the lifetime of the equipment, including temperature[e]	Without trimming	–20	–	20	–20	–	20	ppm
Crystal load capacitance	–	–	12	–	–	–	–	pF
ESR	–	–	–	60	–	–	–	Ω
Drive level	External crystal must be able to tolerate this drive level.	200	–	–	–	–	–	µW
Input impedance (WRF_XTAL_IN)	Resistive	–	–	–	30K	100K	–	Ω
	Capacitive	–	–	7.5	–	–	7.5	pF
WRF_XTAL_IN Input low level	DC-coupled digital signal	–	–	–	0	–	0.2	V
WRF_XTAL_IN Input high level	DC-coupled digital signal	–	–	–	1.0	–	1.26	V
WRF_XTAL_IN input voltage (see Figure 5)	AC-coupled analog signal	–	–	–	400	–	1200	mV_{p-p}
Duty cycle	37.4 MHz clock	–	–	–	40	50	60	%
Phase Noise[f] (IEEE 802.11b/g)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–129	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–	–	–	–136	dBc/Hz
Phase Noise[f] (IEEE 802.11n, 2.4 GHz)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–134	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–	–	–	–141	dBc/Hz

a. (Crystal) Use WRF_XTAL_IN and WRF_XTAL_OUT.
b. See External Frequency Reference on page 10 for alternative connection methods.
c. For a clock reference other than 37.4 MHz, 20 × log10(f/ 37.4) dB should be added to the limits, where f = the reference clock frequency in MHz.
d. The frequency step size is approximately 80 Hz resolution.
e. It is the responsibility of the equipment designer to select oscillator components that comply with these specifications.
f. Assumes that external clock has a flat phase noise response above 100 kHz.

3.3 External 32.768 KHz Low-Power Oscillator

The CYW4390 uses a secondary low frequency clock for low-power-mode timing. Either the internal low-precision LPO or an external 32.768 kHz precision oscillator is required. The internal LPO frequency range is approximately 33 kHz ± 30% over process, voltage, and temperature, which is adequate for some applications. However, one trade-off caused by this wide LPO tolerance is a small current consumption increase during power save mode that is incurred by the need to wake up earlier to avoid missing beacons.

Whenever possible, the preferred approach is to use a precision external 32.768 kHz clock that meets the requirements listed in Figure 4 on page 12.

The external 32.768 kHz crystal provides:

- A real-time clock for the apps core
- Accurate timing for the WLAN power-save modes

Table 4. External 32.768 kHz Sleep Clock Specifications

Parameter	LPO Clock	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	±100	ppm
Duty cycle	30–70	%
Input signal amplitude	200–1800	mV, p-p
Signal type	Square-wave or sine-wave	–
Input impedance[a]	>100K <5	Ω pF
Clock jitter (during initial start-up)	<10,000	ppm

a. When power is applied or switched off.

4. Applications Microprocessor and Memory Unit

The applications microprocessor core is based on the ARM® Cortex-M3™ 32-bit RISC processor with embedded ICE-RT debug and JTAG interface units.

The applications processor boots from an internal ROM-based bootloader. The ROM bootloader copies a configurable boot application from serial-flash to RAM, then passes execution to the boot application. The applications processor is responsible for running the entirety of the WICED software stack, including the optional RTOS, WLAN driver, various libraries to implement WLAN, networking features, and the end-user application.

The 48 MHz processor operates efficiently in both power and performance with tightly-coupled SRAM of 448 KB to provide space for code execution and system resource and variable storage.

The application processor controls the peripheral I/O of the CYW4390, including a dedicated SPI flash interface, SPI master/slave interface, GPIOs, I^2C, I_2S, and four UARTs. The application processor is also responsible for bootstrapping the WLAN core, including downloading the WLAN firmware from external serial flash storage.

The CYW4390 does not have internal flash storage: all code is stored and loaded from external serial flash.

In addition to the dedicated SPI interface to serial flash, the CYW4390 provides a secondary master/slave SPI interface to allow expansion with other devices.

To reduce overall system power consumption, the application processor can be powered down independently of the WLAN core. During powerdown, the state of the entire 448 KB of Applications RAM is retained.

4.1 Reset

The CYW4390 has an integrated power-on reset circuit that resets all circuits to a known power-on state. The power-on reset (POR) circuit is out of reset after APPS_REG_ON goes High. If APPS_REG_ON is low, then the POR circuit is held in reset.

5. Applications Microprocessor Subsystem External Interfaces

5.1 Introduction

The CYW4390 provides a large variety of IO interfaces to enable flexible system design:

- A SPI master for flash access
- A SPI master/slave
- Two high-speed 4-wire UARTs
- Two 2-wire UART available for use by the Apps core (and WLAN core for debugging)
- An I^2C interface
- An I^2S interface
- Up to 24 GPIOs organized in two separate banks of 12. GPIOs in Bank A have alternate functions (see Table 5 on page 15), GPIOs in Bank B are dedicated.

Table 5. GPIO Port A Alternate Functions

Name	Alternate Functions							
	UART1	UART2	UART3	SPI	I^2C	I^2S	GPIO	DEBUG
APPS_I2S_DO	–	UART2_CTS_N	UART3_TX/RX	–	–	I2S_DO	GPIO_A8	–
APPS_I2S_DI	–	UART2_RTS_N	UART3_TX/RX	–	–	I2S_DI	GPIO_A6	–
APPS_I2S_CLK	–	UART2_RXD	UART3_TX/RX	–	–	I2S_CLK	GPIO_A9	–
APPS_I2S_WS	–	UART2_TXD	UART3_TX/RX	–	–	I2S_WS	GPIO_A7	–
APPS_UART1_CTS_N	UART1_CTS_N	–	UART3_TX/RX	SPI_CLK	–	–	GPIO_A1	–
APPS_UART1_RTS_N	UART1_RTS_N	–	UART3_TX/RX	SPI_CS_N	–	–	GPIO_A0	–
APPS_UART1_RXD	UART1_RXD	–	UART3_TX/RX	SPI_MISO	I2C_SDA	–	GPIO_A5	–
APPS_UART1_TXD	UART1_TXD	–	UART3_TX/RX	SPI_MOSI	I2C_SCL	–	GPIO_A4	–
APPS_WAKE	–	–	UART3_TX/RX	–	–	–	GPIO_A10	–
APPS_SPI_IRQ	–	–	UART3_TX/RX	SPI_IRQ	–	–	GPIO_A11	–
APPS_JTAG_TMS	–	–	UART3_TX/RX	–	–	I2S_DO	GPIO_A2	JTAG_TMS
APPS_JTAG_TCK	–	–	UART3_TX/RX	–	–	I2S_DI	GPIO_A3	JTAG_TCK
APPS_JTAG_TDI	–	–	UART3_TX/RX	–	–	I2S_CLK	GPIO_A4	JTAG_TDI
APPS_JTAG_TDO	–	–	UART3_TX/RX	–	–	I2S_WS	GPIO_A5	JTAG_TDO

5.2 SPI Flash Interface

The CYW4390 provides a dedicated SPI interface that connects to an external serial flash with a maximum clock speed of 24 MHz. Use of the SPI flash interface is mandatory for self-hosted systems booting an application that runs on the Application processor.

5.2.1 SPI Master/Slave Interface

In addition to the SPI flash interface the CYW4390 supports a secondary SPI interface with a clock frequency of up to 24 MHz to support external SPI peripherals. This interface can be configured either as a master or a slave interface. The SPI interface has various configuration options including support for active-low or active-high operation for the chip-select, active-low or active-high operation for the interrupt line and bit ordering on the MISO/MOSI lines to be either big endian or little endian.

5.3 UART Interfaces

UART1 and UART2 have standard 4-wire interfaces (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps.

UART1 has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support high data throughput. UART2 has a smaller FIFO that is only 256-bytes. Access to the FIFOs is available to the application processor through the AHB interface and supports either DMA or CPU driven data transfer.

The CYW4390 UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

The CYW4390 UARTs can operate correctly with other devices as long as the combined baud rate error of the two devices is within ±2%.

Table 6. Example of Common Baud Rates

Desired Rate	Actual Rate	Error (%)
4000000	4000000	0.00
3692000	3692308	0.01
3000000	3000000	0.00
2000000	2000000	0.00
1500000	1500000	0.00
1444444	1454544	0.70
921600	923077	0.16
460800	461538	0.16
230400	230796	0.17
115200	115385	0.16
57600	57692	0.16
38400	38400	0.00
28800	28846	0.16
19200	19200	0.00
14400	14423	0.16
9600	9600	0.00

The UART timing is shown by the combination of Figure 6 and Table 7.

Figure 6. UART Timing

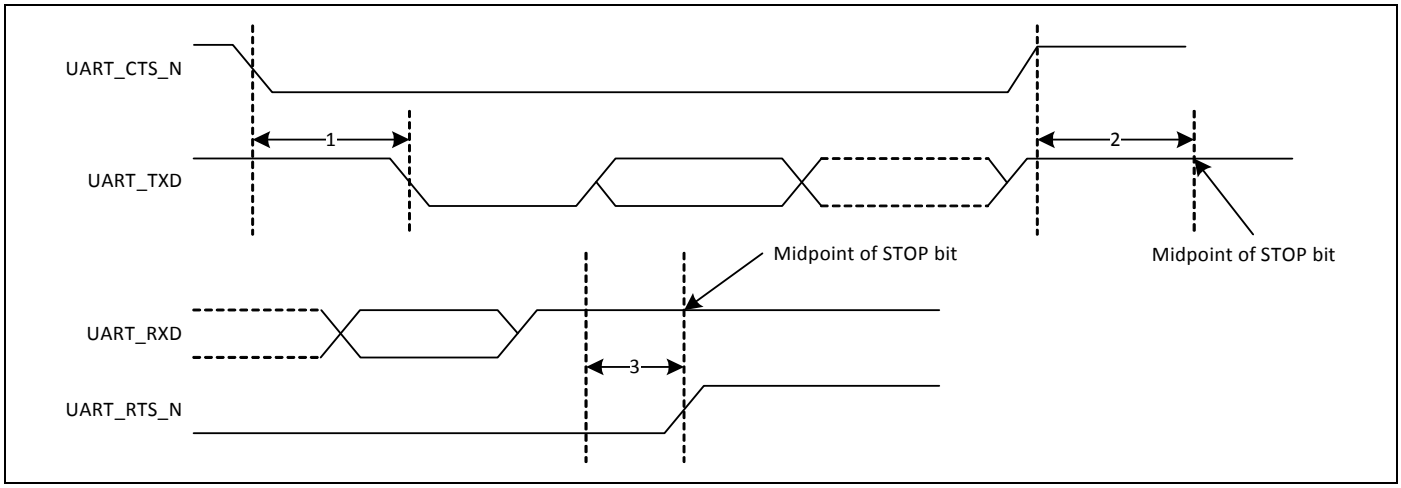


Table 7. UART Timing Specifications

Ref No.	Characteristics	Min.	Typ.	Max.	Unit
1	Delay time, UART_CTS_N low to UART_TXD valid	–	–	1.5	Bit periods
2	Setup time, UART_CTS_N high before midpoint of stop bit	–	–	0.5	Bit periods
3	Delay time, midpoint of stop bit to UART_RTS_N high	–	–	0.5	Bit periods

5.4 I^2S Interface

The CYW4390 has one I^2S digital audio port, which supports both master and slave modes.

The I^2S SCK and I^2S WS (clock and word select) become outputs in master mode and inputs in slave mode, while the I2S SDO is always output.

The channel word length is 16 bits and the data is justified so that the MSB of the left-channel data is aligned with the MSB of the I^2S, per the I^2S specification. The MSB of each data word is transmitted one-bit clock cycle after the I^2S WS transition, synchronous with the falling edge of the bit clock.

Left-channel data is transmitted when I^2S WS is low: right-channel data is transmitted when I^2S WS is high.

Data bits sent by the CYW4390 are synchronized with the falling edge of I2S_SCLK and should be sampled by the receiver on the rising edge of I2S_SCK.

In master mode, the clock rate is: 48 KHz x 32 bits per frame = 1.536 MHz.

The master clock is generated from the input reference clock using an N/M clock divider.

In the slave mode, any clock rate up to 3.072 MHz is supported.

5.5 General Purpose Input and Output

The CYW4390 has 24 general purpose IO (GPIO) pins that can be configured as input or output. Each IO can be configured to have internal pull-up or pull-down resistors. At power-on reset all IOs are configured as input with no pull. Software can configure the IOs appropriately. In power-down modes, the IOs are configured as high-Z with no pull.

GPIOs are grouped into two banks of twelve GPIOs:

- Bank A GPIOs have alternate functions (seeTable 5 on page 15).
- Bank B GPIOs are dedicated GPIOs, except during test (see Table 8).

Table 8. Bank B GPIO Test Functions

GPIO	Test Function
GPIO_B0	–
GPIO_B1	–
GPIO_B2	WL_JTAG_TCK
GPIO_B3	WL_JTAG_TMS
GPIO_B4	WL_JTAG_TDI
GPIO_B5	WL_JTAG_TDO
GPIO_B6	WL_JTAG_TDO
GPIO_B7	–
GPIO_B8	–
GPIO_B9	–
GPIO_B10	–
GPIO_B11	–

5.6 I^2C

TBD

6. WLAN Global Functions

6.1 WLAN CPU and Memory Subsystem

The CYW4390 WLAN section includes an independent integrated ARM Cortex-R4™ 32-bit processor with internal RAM and ROM. The ARM Cortex-R4 is a low-power processor that features low gate count, low interrupt latency, and low-cost debug capabilities. It runs all WLAN firmware and provides support for the standards-compliant WLAN implementation running independent of the applications processor. The Cortex-R4 processor is not available to customers for general purpose applications processing.

At 0.19 µW/MHz, the Cortex-R4 is the most power efficient general-purpose microprocessor available, outperforming 8- and 16-bit devices on MIPS/µW. It supports integrated sleep modes.

6.2 One-Time Programmable Memory

Various hardware configuration parameters may be stored in an internal 6 Kbit one-time programmable (OTP) memory, which is read by WICED bootstrap system software after a device reset. In addition, customer-specific parameters, including the system vendor ID and the MAC address can be stored, depending on the specific board design.

The initial state of all bits in an unprogrammed OTP device is 0. After any bit is programmed to a 1, it cannot be reprogrammed to 0. The entire OTP array can be programmed in a single write cycle using a utility provided with the Cypress WLAN manufacturing test tools. Alternatively, multiple write cycles can be used to selectively program specific bytes, but only bits which are still in the 0 state can be altered during each programming cycle.

Prior to OTP programming, all values should be verified using the appropriate editable nvram.txt file, which is provided with the reference board design package.

6.3 UART Interface

One 2-wire UART interface can be enabled by software as an alternate function on GPIO pins. Provided primarily for debugging during WLAN development, this UART enables the CYW4390 to operate as RS-232 data termination equipment (DTE) for exchanging and managing data with other serial devices. It is compatible with the industry standard 16550 UART, and provides a FIFO size of 64 × 8 in each direction.

6.4 JTAG Interfaces

The CYW4390 applications core and WLAN core have independent support for the IEEE 1149.1 JTAG boundary scan standard for performing application firmware debugging and device package and PCB assembly testing during manufacturing.

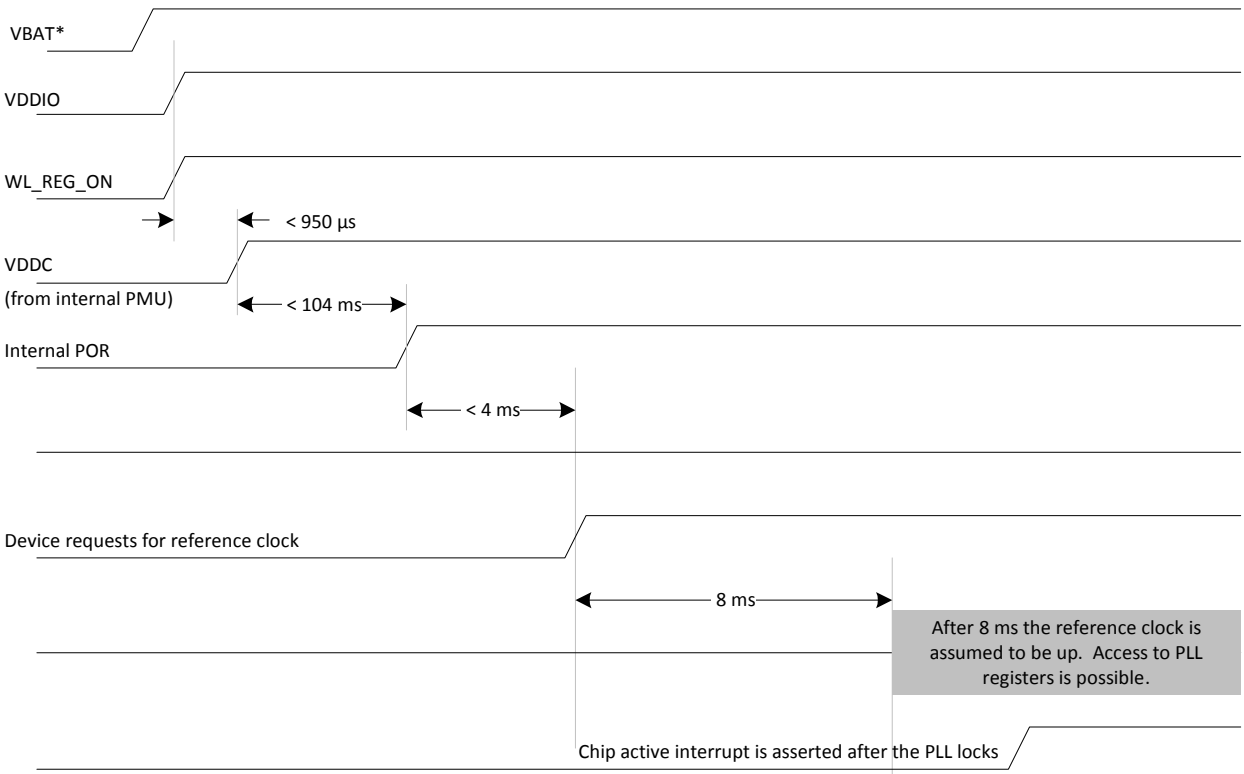
The applications core JTAG port provides developers with single-step thread-aware and memory inspection debugging capability using the Cypress WICED development system.

The WLAN core JTAG interface allows Cypress to assist customers by using proprietary debug and characterization test tools during board bring-up. Therefore it is highly recommended to provide access to the JTAG pins by means of test points or a header on all PCB designs.

6.5 Boot Sequence

Figure 7 shows the boot sequence from power-up to firmware download.

Figure 7. Boot Sequence



***Notes:**

1. VBAT should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

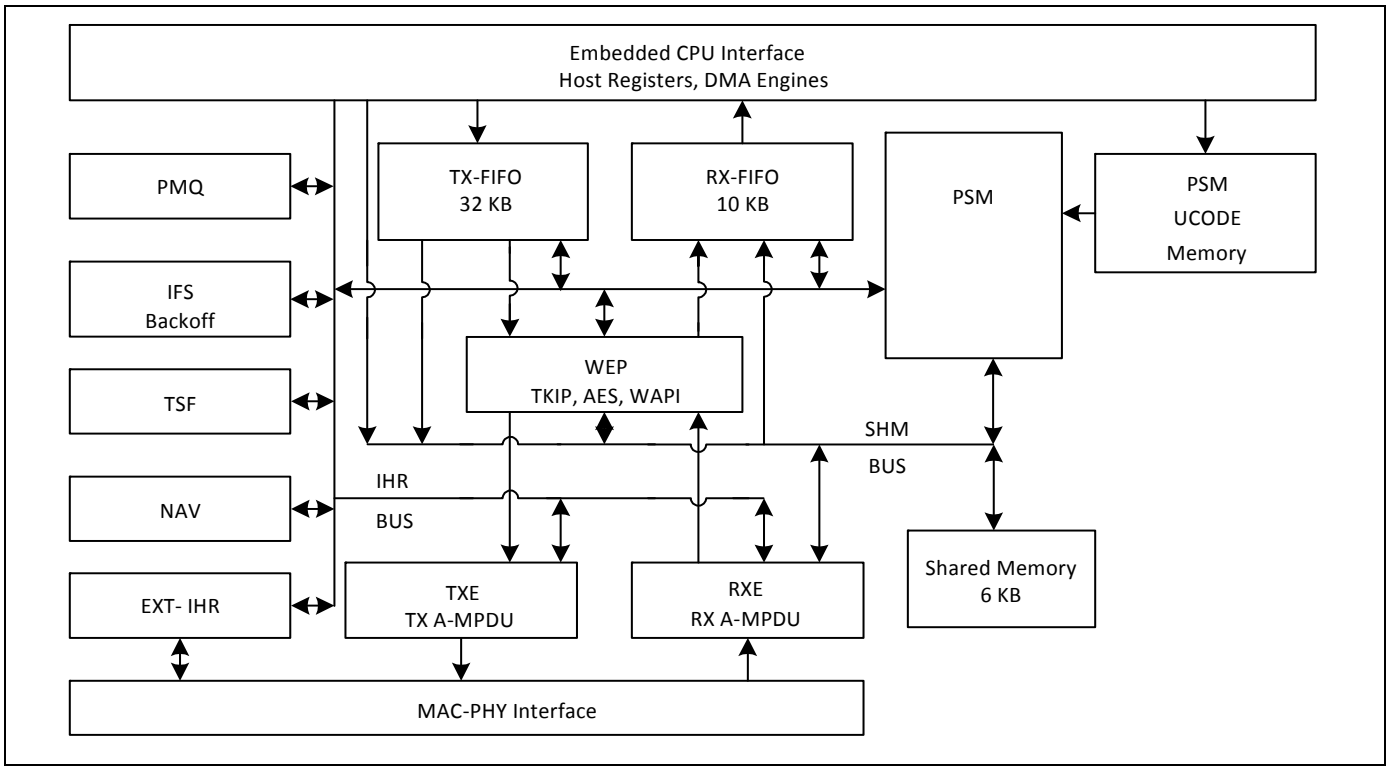
7. Wireless LAN MAC and PHY

7.1 IEEE 802.11n MAC

The CYW4390 WLAN MAC is designed to support high-throughput operation with low-power consumption. Several power saving modes have been implemented that allow the MAC to consume very little power while maintaining network-wide timing synchronization. The architecture diagram of the MAC is shown in Figure 8.

The following sections provide an overview of the important modules in the MAC.

Figure 8. WLAN MAC Architecture



The CYW4390 WLAN media access controller (MAC) supports features specified in the IEEE 802.11 base standard, and amended by IEEE 802.11n. The key MAC features include:

- Enhanced MAC for supporting IEEE 802.11n features
- Transmission and reception of aggregated MPDUs (A-MPDU) for high throughput (HT)
- Support for power management schemes, including WMM power-save, power-save multi-poll (PSMP) and multiphase PSMP operation
- Support for immediate ACK and Block-ACK policies
- Interframe space timing support, including RIFS
- Support for RTS/CTS and CTS-to-self frame sequences for protecting frame exchanges
- Back-off counters in hardware for supporting multiple priorities as specified in the WMM specification
- Timing synchronization function (TSF), network allocation vector (NAV) maintenance, and target beacon transmission time (TBTT) generation in hardware
- Hardware offload for AES-CCMP, legacy WPA TKIP, legacy WEP ciphers, WAPI, and support for key management
- Programmable independent basic service set (IBSS) or infrastructure basic service set functionality
- Statistics counters for MIB support

Programmable State Machine

The programmable state machine (PSM) is a microcoded engine, which provides most of the low-level control to the hardware, to implement the IEEE 802.11 specification. It is a microcontroller that is highly optimized for flow control operations, which are predominant in implementations of communication protocols. The instruction set and fundamental operations are simple and general, which allows algorithms to be optimized until very late in the design process. It also allows for changes to the algorithms to track evolving IEEE 802.11 specifications.

The PSM fetches instructions from the microcode memory. It uses the shared memory to obtain operands for instructions, as a data store, and to exchange data between both the host and the MAC data pipeline (via the SHM bus). The PSM also uses a scratch-pad memory (similar to a register bank) to store frequently accessed and temporary variables.

The PSM exercises fine-grained control over the hardware engines, by programming internal hardware registers (IHR). These IHRs are co-located with the hardware functions they control, and are accessed by the PSM via the IHR bus.

The PSM fetches instructions from the microcode memory using an address determined by the program counter, instruction literal, or a program stack. For ALU operations the operands are obtained from shared memory, scratch pad, IHRs, or instruction literals, and the results are written into the shared memory, scratch pad, or IHRs.

There are two basic branch instructions: conditional branches and ALU based branches. To better support the many decision points in the IEEE 802.11 algorithms, branches can depend on either a readily available signals from the hardware modules (branch condition signals are available to the PSM without polling the IHRs), or on the results of ALU operations.

Wired Equivalent Privacy

The wired equivalent privacy (WEP) engine encapsulates all the hardware accelerators to perform the encryption and decryption, and MIC computation and verification. The accelerators implement the following cipher algorithms: legacy WEP, WPA TKIP, and WPA2 AES-CCMP.

The PSM determines, based on the frame type and association information, the appropriate cipher algorithm to be used. It supplies the keys to the hardware engines from an on-chip key table. The WEP interfaces with the TXE to encrypt and compute the MIC on transmit frames, and the RXE to decrypt and verify the MIC on receive frames.

Transmit Engine

The transmit engine (TXE) constitutes the transmit data path of the MAC. It coordinates the DMA engines to store the transmit frames in the TXFIFO. It interfaces with WEP module to encrypt frames, and transfers the frames across the MAC-PHY interface at the appropriate time determined by the channel access mechanisms.

The data received from the DMA engines are stored in transmit FIFOs. The MAC supports multiple logical queues to support traffic streams that have different QoS priority requirements. The PSM uses the channel access information from the IFS module to schedule a queue from which the next frame is transmitted. Once the frame is scheduled, the TXE hardware transmits the frame based on a precise timing trigger received from the IFS module.

The TXE module also contains the hardware that allows the rapid assembly of MPDUs into an A-MPDU for transmission. The hardware module aggregates the encrypted MPDUs by adding appropriate headers and pad delimiters as needed.

Receive Engine

The receive engine (RXE) constitutes the receive data path of the MAC. It interfaces with the DMA engine to drain the received frames from the RXFIFO. It transfers bytes across the MAC-PHY interface and interfaces with the WEP module to decrypt frames. The decrypted data is stored in the RXFIFO.

The RXE module contains programmable filters that are programmed by the PSM to accept or filter frames based on several criteria such as receiver address, BSSID, and certain frame types.

The RXE module also contains the hardware required to detect A-MPDUs, parse the headers of the containers, and disaggregate them into component MPDUS.

Interframe Space

The interframe space (IFS) module contains the timers required to determine interframe space timing including RIFS timing. It also contains multiple backoff engines required to support prioritized access to the medium as specified by WMM.

The interframe spacing timers are triggered by the cessation of channel activity on the medium, as indicated by the PHY. These timers provide precise timing to the TXE to begin frame transmission. The TXE uses this information to send response frames or perform transmit frame-bursting (RIFS or SIFS separated, as within a TXOP).

The backoff engines (for each access category) monitor channel activity, in each slot duration, to determine whether to continue or pause the backoff counters. When the backoff counters reach 0, the TXE gets notified, so that it may commence frame transmission. In the event of multiple backoff counters decrementing to 0 at the same time, the hardware resolves the conflict based on policies provided by the PSM.

The IFS module also incorporates hardware that allows the MAC to enter a low-power state when operating under the IEEE power save mode. In this mode, the MAC is in a suspended state with its clock turned off. A sleep timer, whose count value is initialized by the PSM, runs on a slow clock and determines the duration over which the MAC remains in this suspended state. Once the timer expires the MAC is restored to its functional state. The PSM updates the TSF timer based on the sleep duration ensuring that the TSF is synchronized to the network.

Timing Synchronization Function

The timing synchronization function (TSF) module maintains the TSF timer of the MAC. It also maintains the target beacon transmission time (TBTT). The TSF timer hardware, under the control of the PSM, is capable of adopting timestamps received from beacon and probe response frames in order to maintain synchronization with the network.

The TSF module also generates trigger signals for events that are specified as offsets from the TSF timer, such as uplink and downlink transmission times used in PSMP.

Network Allocation Vector

The network allocation vector (NAV) timer module is responsible for maintaining the NAV information conveyed through the duration field of MAC frames. This ensures that the MAC complies with the protection mechanisms specified in the standard.

The hardware, under the control of the PSM, maintains the NAV timer and updates the timer appropriately based on received frames. This timing information is provided to the IFS module, which uses it as a virtual carrier-sense indication.

MAC-PHY Interface

The MAC-PHY interface consists of a data path interface to exchange RX/TX data from/to the PHY. In addition, there is an programming interface, which can be controlled either by the host or the PSM to configure and control the PHY.

7.2 IEEE 802.11n PHY

The CYW4390 WLAN Digital PHY is designed to comply with IEEE 802.11 b/g/n single-stream specifications to provide wireless LAN connectivity supporting data rates from 1 Mbps to 72 Mbps for low-power, high-performance embedded applications.

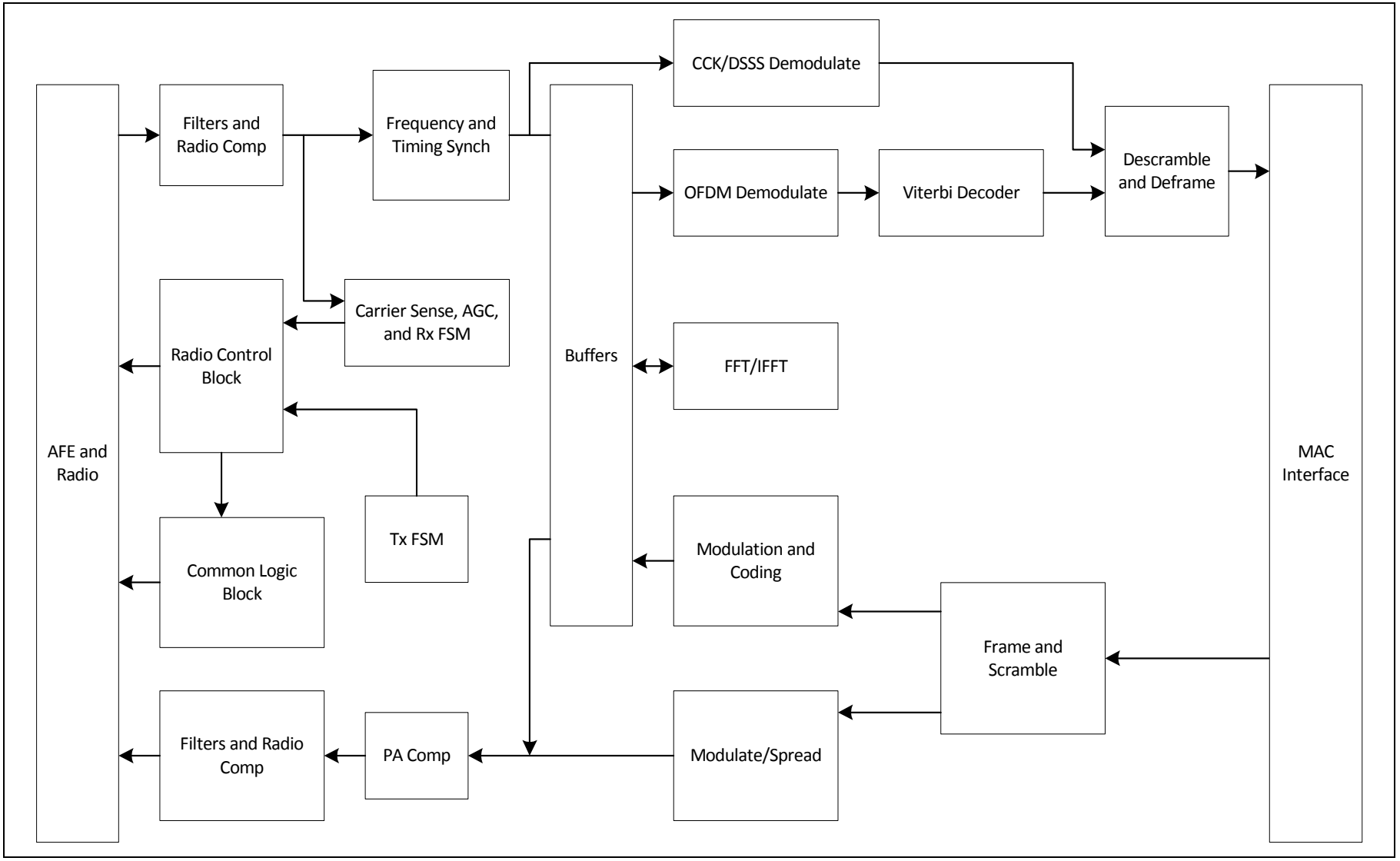
The PHY has been designed to work in the presence of interference, radio nonlinearity, and various other impairments. It incorporates optimized implementations of the filters, FFT and Viterbi decoder algorithms. Efficient algorithms have been designed to achieve maximum throughput and reliability, including algorithms for carrier sense/rejection, frequency/phase/timing acquisition and tracking, channel estimation and tracking. The PHY receiver also contains a robust IEEE 802.11b demodulator. The PHY carrier sense has been tuned to provide high throughput for IEEE 802.11g/11b hybrid networks.

The key PHY features include:

- Programmable data rates in 20 MHz channels, as specified in IEEE 802.11n
- Supports Optional Short GI and Green Field modes in Tx and Rx
- Tx and Rx LDPC for improved range and power efficiency
- All scrambling, encoding, forward error correction, and modulation in the transmit direction and inverse operations in the receive direction.
- Supports IEEE 802.11h/k for worldwide operation
- Advanced algorithms for low power, enhanced sensitivity, range, and reliability
- Automatic gain control scheme for blocking and non blocking application scenario for cellular applications
- Closed loop transmit power control
- Digital RF chip calibration algorithms to handle CMOS RF chip non-idealities
- On-the-fly channel frequency and transmit power selection
- Supports per packet Rx antenna diversity
- Available per-packet channel quality and signal strength measurements
- Designed to meet FCC and other worldwide regulatory requirements

Figure 9 on page 25 is a block diagram of the WLAN PHY.

Figure 9. WLAN PHY Block Diagram

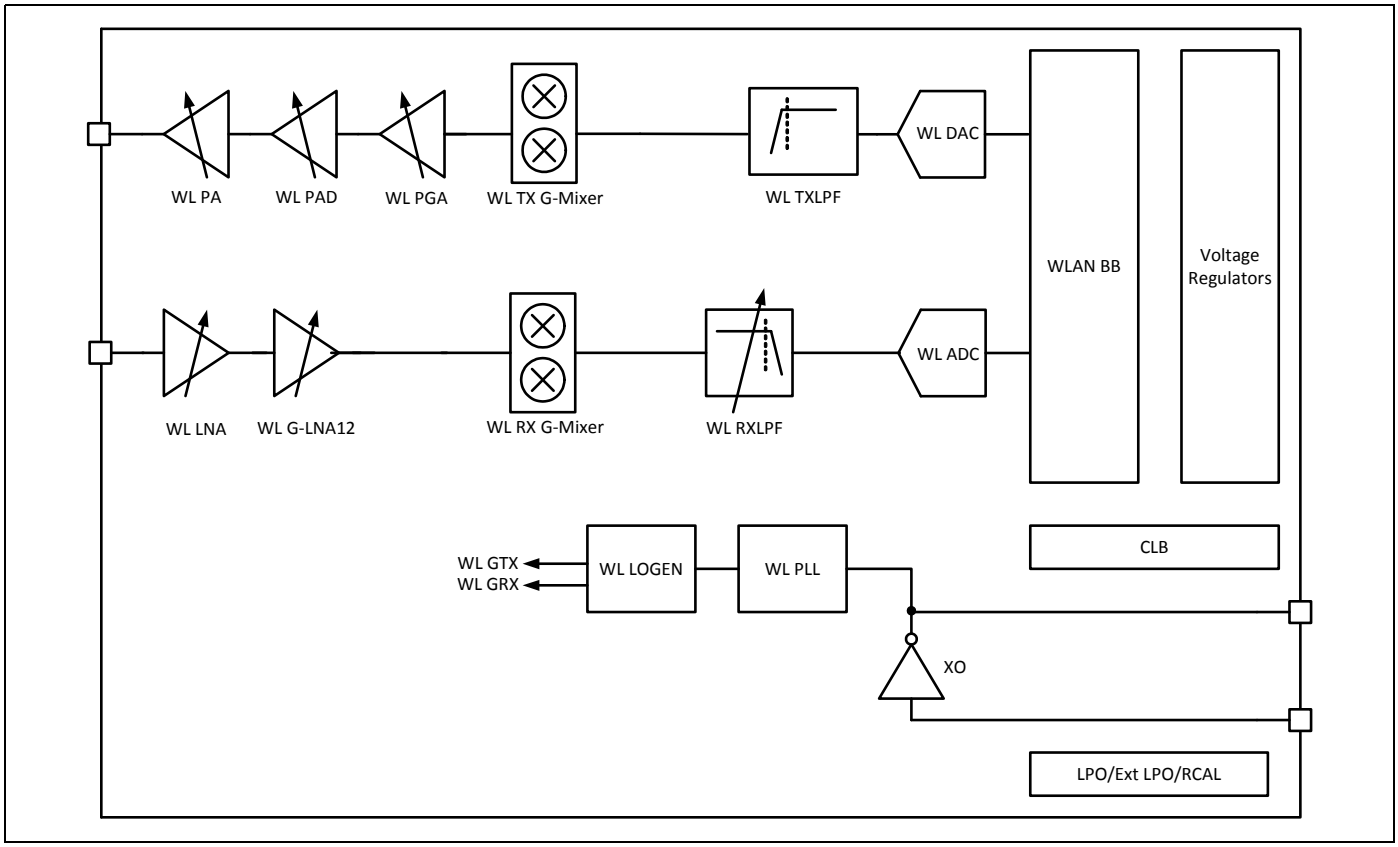


8. WLAN Radio Subsystem

The CYW4390 includes an integrated single-band WLAN RF transceiver that has been optimized for use in 2.4 GHz WLAN systems. It has been designed to provide low-power, low-cost, and robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM band. The transmit and receive sections include all on-chip filtering, mixing, and gain control functions.

A block diagram of the radio subsystem is shown in Figure 10. Note that integrated on-chip baluns (not shown) convert the fully differential transmit and receive paths to single-ended signal pins.

Figure 10. Radio Functional Block Diagram



8.1 Receiver Path

The CYW4390 has a wide dynamic range, direct conversion receiver that employs high order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band. The 2.4 GHz receive path has a dedicated on-chip low-noise amplifier (LNA).

8.2 Transmit Path

Baseband data is modulated and upconverted to the 2.4 GHz ISM band, respectively. Linear on-chip power amplifiers are included, which are capable of delivering high output powers while meeting IEEE 802.11 b/g/n specifications without the need for external PAs. When using the internal PAs, closed-loop output power control is completely integrated.

8.3 Calibration

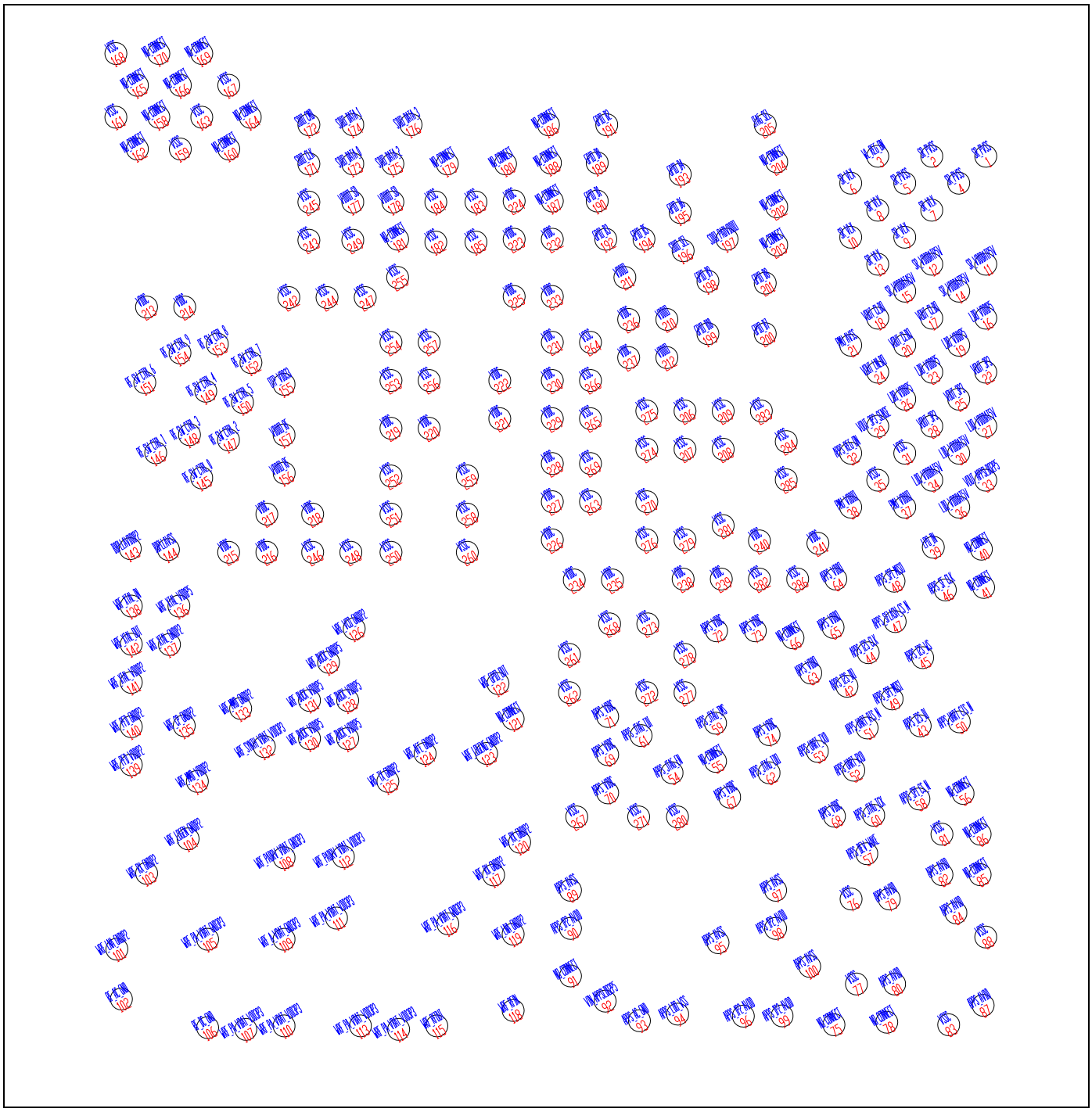
The CYW4390 features dynamic and automatic on-chip calibration to continually compensate for temperature and process variations across components. These calibration routines are performed periodically in the course of normal radio operation. Examples of some of the automatic calibration algorithms are baseband filter calibration for optimum transmit and receive performance, and LOFT calibration for carrier leakage reduction. In addition, I/Q Calibration, R Calibration, and VCO Calibration are performed on-chip. No per-board calibration is required in manufacturing test, which helps to minimize the test time and cost in large volume production.

9. Pinout and Signal Descriptions

9.1 Ball Maps

Figure 11 shows the WLCSP bump map.

Figure 11. 286-Bump WLCSP (Bottom View, Bumps Facing Up)



9.2 Pin Lists

Table 9 contains the 286-bump WLCSP coordinates.

Table 9. 286-Bump WLCSP Coordinates

Bump#	NET_NAME	Package Bump Side View (0,0 center of die)		Package Top Side View (0,0 center of die)	
		X	Y	X	Y
1	SR_PVSS_1	2275.005	2003.355	–2275.005	2003.355
2	SR_PVSS_2	1992.162	2003.355	–1992.162	2003.355
3	WL_REG_ON	1709.319	2003.355	–1709.319	2003.355
4	SR_PVSS_4	2133.584	1861.934	–2133.584	1861.934
5	SR_PVSS_5	1850.741	1861.934	–1850.741	1861.934
6	SR_VLX_6	1567.898	1861.934	–1567.898	1861.934
7	SR_VLX_7	1992.162	1720.512	–1992.162	1720.512
8	SR_VLX_8	1709.319	1720.512	–1709.319	1720.512
9	SR_VLX_9	1850.741	1579.091	–1850.741	1579.091
10	SR_VLX_10	1567.898	1579.091	–1567.898	1579.091
11	SR_VDDBATP5V_11	2275.005	1437.669	–2275.005	1437.669
12	SR_VDDBATP5V_12	1992.162	1437.669	–1992.162	1437.669
13	SR_VLX_13	1709.319	1437.669	–1709.319	1437.669
14	SR_VDDBATP5V_14	2133.584	1296.248	–2133.584	1296.248
15	SR_VDDBATA5V	1850.741	1296.248	–1850.741	1296.248
16	LDO_VDD1P5_16	2275.005	1154.826	–2275.005	1154.826
17	VOUT_CLDO_17	1992.162	1154.826	–1992.162	1154.826
18	VOUT_CLDO_18	1709.319	1154.826	–1709.319	1154.826
19	LDO_VDD1P5_19	2133.584	1013.405	–2133.584	1013.405
20	VOUT_CLDO_20	1850.741	1013.405	–1850.741	1013.405
21	PMU_AVSS	1567.898	1013.405	–1567.898	1013.405
22	VOUT_3P3_22	2275.005	871.983	–2275.005	871.983
23	LDO_VDD1P5_23	1992.162	871.983	–1992.162	871.983
24	VOUT_LNLDO_24	1709.319	871.983	–1709.319	871.983
25	VOUT_3P3_25	2133.584	730.562	–2133.584	730.562
26	LDO_VDD1P5_26	1850.741	730.562	–1850.741	730.562
27	LDO_VDDBAT5V_27	2275.005	589.140	–2275.005	589.140
28	VOUT_3P3_28	1992.162	589.140	–1992.162	589.140
29	VOUT_3P3_SENSE_29	1709.319	589.140	–1709.319	589.140
30	LDO_VDDBAT5V	2133.584	447.719	–2133.584	447.719
31	VSSC_31	1850.741	447.719	–1850.741	447.719
32	APPS_REG_ON_32	1567.898	447.719	–1567.898	447.719
33	NC_33	2275.005	306.297	–2275.005	306.297
34	LDO_VDDBAT5V_34	1992.162	306.297	–1992.162	306.297
35	VSSC_35	1709.319	306.297	–1709.319	306.297
36	LDO_VDDBAT5V_36	2133.584	164.876	–2133.584	164.876

Table 9. 286-Bump WLCSP Coordinates (Cont.)

Bump#	NET_NAME	Package Bump Side View (0,0 center of die)		Package Top Side View (0,0 center of die)	
		X	Y	X	Y
37	PMU_VDDIO_37	1850.741	164.876	–1850.741	164.876
38	PMU_VDDIO_38	1567.898	164.876	–1567.898	164.876
39	LPO_IN	2000.397	–45.054	–2000.397	–45.054
40	NC_40	2252.010	–55.251	–2252.010	–55.251
41	NC_41	2264.169	–255.429	–2264.169	–255.429
42	APPS_I2S_DO	1548.201	–773.253	–1548.201	–773.253
43	APPS_I2S_DI	1931.412	–980.847	–1931.412	–980.847
44	APPS_I2S_CLK	1659.396	–597.546	–1659.396	–597.546
45	APPS_I2S_WS	1944.471	–623.367	–1944.471	–623.367
46	APPS_SFLASH_CLK	2063.397	–268.848	–2063.397	–268.848
47	APPS_SFLASH_CS_N	1800.498	–434.448	–1800.498	–434.448
48	APPS_SFLASH_MISO	1794.801	–223.146	–1794.801	–223.146
49	APPS_SFLASH_MOSI	1784.397	–839.853	–1784.397	–839.853
50	APPS_UART_1_CTS_N	2136.414	–959.733	–2136.414	–959.733
51	APPS_UART1_RTS_N	1653.744	–991.854	–1653.744	–991.854
52	APPS_UART1_RXD	1583.904	–1213.488	–1583.904	–1213.488
53	APPS_UART1_TXD	1393.104	–1114.101	–1393.104	–1114.101
54	APPS_JTAG_EN	632.001	–1226.646	–632.001	–1226.646
55	NC_55	859.998	–1166.652	–859.998	–1166.652
56	NC_56	2156.196	–1334.853	–2156.196	–1334.853
57	APPS_WAKE	1652.097	–1650.546	–1652.097	–1650.546
58	APPS_SPI_IRQ	1925.202	–1363.752	–1925.202	–1363.752
59	APPS_JTAG_TMS	859.998	–966.654	–859.998	–966.654
60	APPS_JTAG_TCK	1688.097	–1449.099	–1688.097	–1449.099
61	APPS_JTAG_TDI	470.001	–1031.652	–470.001	–1031.652
62	APPS_JTAG_TDO	1139.997	–1226.646	–1139.997	–1226.646
63	APPS_VDDO_63	1358.481	–704.151	–1358.481	–704.151
64	APPS_VDDO_64	1489.998	–211.653	–1489.998	–211.653
65	APPS_VDDO_65	1475.499	–464.652	–1475.499	–464.652
66	NC_66	1265.574	–519.930	–1265.574	–519.930
67	APPS_VDDC_67	933.699	–1354.050	–933.699	–1354.050
68	APPS_VDDC_68	1482.501	–1453.950	–1482.501	–1453.950
69	APPS_VDDC_69	294.996	–1131.651	–294.996	–1131.651
70	APPS_VDDC_70	294.996	–1331.649	–294.996	–1331.649
71	APPS_VDDC_71	294.996	–931.653	–294.996	–931.653
72	APPS_VDDC_72	864.903	–482.949	–864.903	–482.949
73	APPS_VDDC_73	1067.997	–482.949	–1067.997	–482.949
74	APPS_VDDC_74	1139.997	–1026.648	–1139.997	–1026.648

Table 9. 286-Bump WLCSP Coordinates (Cont.)

Bump#	NET_NAME	Package Bump Side View (0,0 center of die)		Package Top Side View (0,0 center of die)	
		X	Y	X	Y
75	NC_75	1479.864	–2546.550	–1479.864	–2546.550
76	VSSC_76	1569.797	–1888.101	–1569.797	–1888.101
77	VSSC_77	1597.593	–2333.169	–1597.593	–2333.169
78	NC_78	1756.686	–2533.167	–1756.686	–2533.167
79	APPS_AVDD_79	1769.795	–1888.101	–1769.795	–1888.101
80	APPS_AVDD_80	1797.591	–2333.169	–1797.591	–2333.169
81	VSSC_81	2045.451	–1548.549	–2045.451	–1548.549
82	APPS_AVDD_82	2045.451	–1760.319	–2045.451	–1760.319
83	VSSC_83	2080.781	–2546.550	–2080.781	–2546.550
84	APPS_AVDD_84	2118.860	–1960.317	–2118.860	–1960.317
85	NC_85	2245.449	–1760.319	–2245.449	–1760.319
86	NC_86	2245.449	–1548.549	–2245.449	–1548.549
87	APPS_AVDD_87	2261.469	–2444.675	–2261.469	–2444.675
88	VSSC_88	2274.852	–2086.889	–2274.852	–2086.889
89	APPS_AVSS_89	99.975	–1842.066	–99.975	–1842.066
90	APPS_1P2_AVDD_90	99.975	–2042.064	–99.975	–2042.064
91	NC_91	99.975	–2291.099	–99.975	–2291.099
92	VOUT_LNDO_SENSE	281.861	–2422.625	–281.861	–2422.625
93	APPS_AC_GND	461.505	–2525.544	–461.505	–2525.544
94	APPS_LDO_VSS	661.503	–2491.097	–661.503	–2491.097
95	APPS_AVSS_95	873.183	–2116.746	–873.183	–2116.746
96	APPS_1P2_AVDD_96	1005.281	–2501.330	–1005.281	–2501.330
97	APPS_AVSS_97	1174.454	–1842.066	–1174.454	–1842.066
98	APPS_1P2_AVDD_98	1174.454	–2042.064	–1174.454	–2042.064
99	APPS_1P2_AVDD_99	1208.352	–2500.155	–1208.352	–2500.155
100	APPS_AVSS_100	1352.595	–2240.766	–1352.595	–2240.766
101	WRF_LNA_GND1P2_101	–2275.490	–2150.537	2275.490	–2150.537
102	RF_AC_GND	–2251.986	–2411.789	2251.986	–2411.789
103	WRF_RX_GND1P2_103	–2119.686	–1753.146	2119.686	–1753.146
104	WRF_LOGEN_GND1P2	–1902.494	–1572.417	1902.494	–1572.417
105	WRF_PA_VBAT_GND3P3_105	–1800.006	–2098.656	1800.006	–2098.656
106	RF_DC_GND_106	–1800.006	–2561.652	1800.006	–2561.652
107	WRF_PA_VBAT_GND3P3_107	–1600.008	–2570.652	1600.008	–2570.652
108	WRF_PADRV_VBAT_GND3P3_108	–1400.010	–1671.660	1400.010	–1671.660
109	WRF_PA_VBAT_GND3P3_109	–1400.010	–2098.656	1400.010	–2098.656
110	WRF_PA_VBAT_GND3P3_110	–1400.010	–2552.652	1400.010	–2552.652
111	WRF_PA_VBAT_GND3P3_111	–1125.249	–1987.776	1125.249	–1987.776
112	WRF_PADRV_VBAT_VDD3P3	–1089.249	–1666.260	1089.249	–1666.260

Table 9. 286-Bump WLCSP Coordinates (Cont.)

Bump#	NET_NAME	Package Bump Side View (0,0 center of die)		Package Top Side View (0,0 center of die)	
		X	Y	X	Y
113	WRF_PA_VBAT_VDD3P3_113	–1000.014	–2552.652	1000.014	–2552.652
114	WRF_PA_VBAT_VDD3P3_114	–800.016	–2570.652	800.016	–2570.652
115	WRF_RFOUT	–600.018	–2552.652	600.018	–2552.652
116	WRF_PA_VBAT_GND3P3_116	–542.225	–2017.656	542.225	–2017.656
117	WRF_RX_GND1P2_117	–302.510	–1761.939	302.510	–1761.939
118	WRF_RFIN	–200.022	–2471.652	200.022	–2471.652
119	WRF_LNA_GND1P2_119	–200.022	–2071.656	200.022	–2071.656
120	WRF_RX_GND1P2_120	–165.822	–1590.174	165.822	–1590.174
121	NC_121	–200.022	–943.668	200.022	–943.668
122	WRF_GPIO_OUT	–279.173	–759.168	279.173	–759.168
123	WRF_LOGENG_GND1P2	–338.919	–1125.594	338.919	–1125.594
124	WRF_AFE_GND1P2	–661.308	–1125.594	661.308	–1125.594
125	WRF_TX_GND1P2	–856.014	–1271.664	856.014	–1271.664
126	WRF_VCO_GND1P2	–1032.414	–471.672	1032.414	–471.672
127	WRF_BUCK_VDD1P5_127	–1066.853	–1047.744	1066.853	–1047.744
128	WRF_BUCK_VDD1P5_128	–1066.853	–847.746	1066.853	–847.746
129	WRF_BUCK_GND1P5	–1166.852	–647.748	1166.852	–647.748
130	WRF_BUCK_VDD1P5_130	–1266.851	–1047.744	1266.851	–1047.744
131	WRF_BUCK_VDD1P5_131	–1266.851	–847.746	1266.851	–847.746
132	WRF_SYNTH_VBAT_VDD3P3	–1503.344	–1089.662	1503.344	–1089.662
133	WRF_MMD_GND1P2	–1627.031	–889.668	1627.031	–889.668
134	WRF_MMD_VDD1P2	–1854.006	–1271.664	1854.006	–1271.664
135	WRF_CP_GND1P2	–1922.892	–980.154	1922.892	–980.154
136	WRF_XTAL_VDD1P5	–1950.522	–353.066	1950.522	–353.066
137	WRF_XTAL_GND1P2	–2000.004	–554.598	2000.004	–554.598
138	WRF_XTAL_IN	–2199.998	–353.066	2199.998	–353.066
139	WRF_PFD_VDD1P2	–2200.002	–1185.062	2200.002	–1185.062
140	WRF_PFD_GND1P2	–2200.002	–985.064	2200.002	–985.064
141	WRF_XTAL_VDD1P2	–2200.002	–753.062	2200.002	–753.062
142	WRF_XTAL_OUT	–2200.002	–553.064	2200.002	–553.064
143	BBPLLAVDD1P2	–2205.429	–52.326	2205.429	–52.326
144	BBPLLAVSS	–2005.431	–57.348	2005.431	–57.348
145	RF_SW_CTRL_0	–1831.200	318.141	1831.200	318.141
146	RF_SW_CTRL_1	–2072.022	449.946	2072.022	449.946
147	RF_SW_CTRL_2	–1691.052	517.221	1691.052	517.221
148	RF_SW_CTRL_3	–1895.118	544.410	1895.118	544.410
149	RF_SW_CTRL_4	–1809.960	772.110	1809.960	772.110
150	RF_SW_CTRL_5	–1617.639	713.790	1617.639	713.790

Table 9. 286-Bump WLCSP Coordinates (Cont.)

Bump#	NET_NAME	Package Bump Side View (0,0 center of die)		Package Top Side View (0,0 center of die)	
		X	Y	X	Y
151	RF_SW_CTRL_6	–2129.154	817.452	2129.154	817.452
152	RF_SW_CTRL_7	–1573.278	922.392	1573.278	922.392
153	RF_SW_CTRL_8	–1749.264	1019.259	1749.264	1019.259
154	RF_SW_CTRL_9	–1944.888	972.936	1944.888	972.936
155	OTP_VDD33	–1400.001	808.353	1400.001	808.353
156	VDDIO_RF_156	–1399.398	343.350	1399.398	343.350
157	VDDIO_RF_157	–1400.001	543.348	1400.001	543.348
158	NC_158	–2055.795	2207.556	2055.795	2207.556
159	NC_159	–1943.295	2041.056	1943.295	2041.056
160	NC_160	–1689.455	2041.056	1689.455	2041.056
161	VSSC_161	–2280.795	2207.556	2280.795	2207.556
162	NC_162	–2168.295	2041.056	2168.295	2041.056
163	VSSC_163	–1830.795	2207.556	1830.795	2207.556
164	NC_164	–1576.959	2207.556	1576.959	2207.556
165	NC_165	–2168.295	2374.758	2168.295	2374.758
166	NC_166	–1943.295	2374.758	1943.295	2374.758
167	NC_167	–1689.455	2374.758	1689.455	2374.758
168	VSSC_168	–2280.795	2541.258	2280.795	2541.258
169	NC_169	–1830.795	2541.258	1830.795	2541.258
170	NC_170	–2055.795	2541.258	2055.795	2541.258
171	SDIO_CLK	–1269.996	1963.350	1269.996	1963.350
172	SDIO_CMD	–1269.996	2168.352	1269.996	2168.352
173	SDIO_DATA_0	–1040.001	1963.350	1040.001	1963.350
174	SDIO_DATA_1	–1040.001	2168.352	1040.001	2168.352
175	SDIO_DATA_2	–830.004	1963.350	830.004	1963.350
176	SDIO_DATA_3	–735.000	2168.352	735.000	2168.352
177	VDDIO_SD_177	–1040.001	1763.352	1040.001	1763.352
178	VDDIO_SD_178	–830.004	1763.352	830.004	1763.352
179	NC_179	–545.001	1963.350	545.001	1963.350
180	NC_180	–240.000	1963.350	240.000	1963.350
181	NC_181	–805.002	1568.349	805.002	1568.349
182	VSSC_182	–605.004	1553.346	605.004	1553.346
183	VSSC_183	–394.998	1763.352	394.998	1763.352
184	VSSC_184	–605.004	1763.352	605.004	1763.352
185	VSSC_185	–394.998	1553.346	394.998	1553.346
186	NC_186	–15.000	2168.352	15.000	2168.352
187	NC_187	4.998	1768.347	–4.998	1768.347
188	NC_188	–5.001	1968.354	5.001	1968.354

Table 9. 286-Bump WLCSP Coordinates (Cont.)

Bump#	NET_NAME	Package Bump Side View (0,0 center of die)		Package Top Side View (0,0 center of die)	
		X	Y	X	Y
189	GPIO_B0	239.997	1968.354	–239.997	1968.354
190	GPIO_B1	239.997	1768.347	–239.997	1768.347
191	GPIO_B2	290.001	2168.352	–290.001	2168.352
192	GPIO_B3	284.997	1568.349	–284.997	1568.349
193	GPIO_B4	675.003	1908.351	–675.003	1908.351
194	GPIO_B5	485.004	1568.349	–485.004	1568.349
195	GPIO_B6	675.003	1708.353	–675.003	1708.353
196	SDIO_SEL	689.997	1508.346	–689.997	1508.346
197	SDIO_PADVDDIO	920.001	1568.349	–920.001	1568.349
198	GPIO_B9	820.002	1348.353	–820.002	1348.353
199	GPIO_B10	820.002	1073.349	–820.002	1073.349
200	GPIO_B7	1119.999	1073.349	–1119.999	1073.349
201	GPIO_B8	1119.999	1338.354	–1119.999	1338.354
202	DEBUG_EN	1180.002	1738.350	–1180.002	1738.350
203	GPIO_B11	1180.002	1538.352	–1180.002	1538.352
204	NC_204	1180.002	1973.349	–1180.002	1973.349
205	JTAG_SEL	1119.999	2168.352	–1119.999	2168.352
206	VSSC_206	699.996	668.349	–699.996	668.349
207	VSSC_207	699.996	468.351	–699.996	468.351
208	VSSC_208	900.003	468.351	–900.003	468.351
209	VSSC_209	900.003	668.349	–900.003	668.349
210	VDDIO_210	605.001	1148.346	–605.001	1148.346
211	VDDIO_211	384.996	1368.351	–384.996	1368.351
212	VDDIO_212	605.001	948.348	–605.001	948.348
213	VDDC_213	–2120.001	1213.353	2120.001	1213.353
214	VDDC_214	–1920.003	1213.353	1920.003	1213.353
215	VDDC_215	–1689.999	–71.649	1689.999	–71.649
216	VDDC_216	–1490.001	–71.649	1490.001	–71.649
217	VDDC_217	–1490.001	128.349	1490.001	128.349
218	VDDC_218	–1249.998	128.349	1249.998	128.349
219	VDDC_219	–840.003	578.349	840.003	578.349
220	VDDC_220	–639.996	578.349	639.996	578.349
221	VDDC_221	–269.997	628.353	269.997	628.353
222	VDDC_222	–269.997	828.351	269.997	828.351
223	VDDC_223	–195.000	1568.349	195.000	1568.349
224	VDDC_224	–195.000	1768.347	195.000	1768.347
225	VDDC_225	–195.000	1268.352	195.000	1268.352
226	VDDC_226	4.998	–6.651	–4.998	–6.651

Table 9. 286-Bump WLCSP Coordinates (Cont.)

Bump#	NET_NAME	Package Bump Side View (0,0 center of die)		Package Top Side View (0,0 center of die)	
		X	Y	X	Y
227	VDDC_227	4.998	193.347	–4.998	193.347
228	VDDC_228	4.998	393.354	–4.998	393.354
229	VDDC_229	4.998	628.353	–4.998	628.353
230	VDDC_230	4.998	828.351	–4.998	828.351
231	VDDC_231	4.998	1028.349	–4.998	1028.349
232	VDDC_232	4.998	1568.349	–4.998	1568.349
233	VDDC_233	4.998	1268.352	–4.998	1268.352
234	VDDC_234	120.000	–216.648	–120.000	–216.648
235	VDDC_235	319.998	–216.648	–319.998	–216.648
236	VDDC_236	405.003	1148.346	–405.003	1148.346
237	VDDC_237	405.003	948.348	–405.003	948.348
238	VDDC_238	689.997	–211.653	–689.997	–211.653
239	VDDC_239	890.004	–211.653	–890.004	–211.653
240	VDDC_240	1090.002	–11.646	–1090.002	–11.646
241	VDDC_241	1396.119	–24.588	–1396.119	–24.588
242	VSSC_242	–1374.999	1263.348	1374.999	1263.348
243	VSSC_243	–1269.996	1563.354	1269.996	1563.354
244	VSSC_244	–1175.001	1263.348	1175.001	1263.348
245	VSSC_245	–1269.996	1763.352	1269.996	1763.352
246	VSSC_246	–1249.998	–71.649	1249.998	–71.649
247	VSSC_247	–975.003	1263.348	975.003	1263.348
248	VSSC_248	–1050.000	–71.649	1050.000	–71.649
249	VSSC_249	–1040.001	1563.354	1040.001	1563.354
250	VSSC_250	–840.003	–71.649	840.003	–71.649
251	VSSC_251	–840.003	128.349	840.003	128.349
252	VSSC_252	–840.003	328.347	840.003	328.347
253	VSSC_253	–840.003	828.351	840.003	828.351
254	VSSC_254	–840.003	1028.349	840.003	1028.349
255	VSSC_255	–805.002	1368.351	805.002	1368.351
256	VSSC_256	–639.996	828.351	639.996	828.351
257	VSSC_257	–639.996	1028.349	639.996	1028.349
258	VSSC_258	–439.998	128.349	439.998	128.349
259	VSSC_259	–439.998	328.734	439.998	328.734
260	VSSC_260	–439.998	–71.649	439.998	–71.649
261	VSSC_261	94.998	–606.654	–94.998	–606.654
262	VSSC_262	94.998	–806.652	–94.998	–806.652
263	VSSC_263	204.996	193.347	–204.996	193.347
264	VSSC_264	204.996	1028.349	–204.996	1028.349

Table 9. 286-Bump WLCSP Coordinates (Cont.)

Bump#	NET_NAME	Package Bump Side View (0,0 center of die)		Package Top Side View (0,0 center of die)	
		X	Y	X	Y
265	VSSC_265	204.996	628.353	–204.996	628.353
266	VSSC_266	204.996	828.351	–204.996	828.351
267	VSSC_267	133.104	–1457.550	–133.104	–1457.550
268	VSSC_268	305.004	–446.652	–305.004	–446.652
269	VSSC_269	204.996	393.354	–204.996	393.354
270	VSSC_270	499.998	193.347	–499.998	193.347
271	VSSC_271	457.401	–1457.550	–457.401	–1457.550
272	VSSC_272	499.998	–806.652	–499.998	–806.652
273	VSSC_273	505.002	–446.652	–505.002	–446.652
274	VSSC_274	499.998	468.351	–499.998	468.351
275	VSSC_275	499.998	668.349	–499.998	668.349
276	VSSC_276	499.998	–6.651	–499.998	–6.651
277	VSSC_277	699.996	–806.652	–699.996	–806.652
278	VSSC_278	699.996	–606.654	–699.996	–606.654
279	VSSC_279	699.996	–6.651	–699.996	–6.651
280	VSSC_280	660.603	–1457.550	–660.603	–1457.550
281	VSSC_281	900.003	68.346	–900.003	68.346
282	VSSC_282	1090.002	–211.653	–1090.002	–211.653
283	VSSC_283	1100.001	668.349	–1100.001	668.349
284	VSSC_284	1229.997	508.347	–1229.997	508.347
285	VSSC_285	1229.997	308.349	–1229.997	308.349
286	VSSC_286	1290.000	–211.653	–1290.000	–211.653

9.3 Signal Descriptions

The signal name, type, and description of each pin in the CYW4390 are listed in Table 10. The symbol listed in the Type column indicates the pin direction (I/O = bidirectional, I = input, O = output) and the internal pull-up/pull-down characteristics, if any (PU = weak internal pull-up resistor and PD = weak internal pull-down resistor).

Table 10. WLCSP and FCFBGA Pin Descriptions

Signal Name	WLCSP Bump #	Type	Description
APPS_1P2_AVDD	90, 96, 98, 99	PWR	Power supply.
APPS_AC_GND	93	GND	Connect to ground to reduce system RF noise.
APPS_AVDD	79, 80, 82, 84, 87	PWR	APPS CPU domain power supply. Connect to 1.2V
APPS_AVSS	89, 95, 97, 100	GND	Ground. Connect to VSSC for ESD mitigation.
APPS_WAKE	57	I/O	Application CPU subsystem. Device wakes from sleep signal.
APPS_I2S_CLK	44	I/O	I^2S clock. Can be master (output) or slave (input)
APPS_I2S_DI	43	I/O	I^2S data input.
APPS_I2S_DO	42	I/O	I^2S data output.
APPS_I2S_WS	45	I/O	I^2S word select (WS).
APPS_JTAG_EN	54	I/O	Application CPU subsystem: JTAG enable.
APPS_JTAG_TCK	60	I/O	Application CPU subsystem: JTAG interface.
APPS_JTAG_TDI	61	I/O	
APPS_JTAG_TDO	62	I/O	
APPS_JTAG_TMS	59	I/O	
APPS_LDO_VSS	94	GND	Connect to VSSC for ESD.
APPS_REG_ON	32	I	Used by the PMU to power up or power down the on-chip regulators that supply power to the Application CPU subsystem. Also, when deasserted, the Application CPU will be held in reset.
APPS_SFLASH_CLK	46	I/O	SPI serial flash interface SPI clock output.
APPS_SFLASH_CS_N	47	I/O	External serial flash interface chip-select (functionality cannot be remapped to another purpose).
APPS_SPI_IRQ	58	I/O	SPI interface interrupt input.
APPS_SFLASH_MISO	48	I	Serial flash SPI MISO input.
APPS_SFLASH_MOSI	49	O	Serial flash SPI MOSI output.
APPS_UART1_CTS_N	50	I	UART1 clear-to-send. Active-low, clear-to-send signal for the HCI UART interface.
APPS_UART1_RTS_N	51	O	UART1 request-to-send. Active-low request-to-send signal for the UART1 interface.
APPS_UART1_RXD	52	I	UART1 serial input. Serial data input for the UART1 interface.
APPS_UART1_TXD	53	O	UART1 serial output. Serial data output for the UART1 interface.
APPS_VDDC	67, 68, 69, 70, 71, 72, 73, 74	PWR	1.2V core supply for APPS CPU.
APPS_VDDO	63, 64, 65	PWR	Connect to 3.3V.
BBPLLAVDD	143	PWR	Connect to 1.2V

Table 10. WLCSP and FCFBGA Pin Descriptions (Cont.)

Signal Name	WLCSP Bump #	Type	Description
BBPLLAVSS	144	GND	Connect to VSSC for ESD.
GPIO_B0	189	I/O	Programmable Bank B GPIO pins.
GPIO_B1	190		
GPIO_B2	191		
GPIO_B3	192		
GPIO_B4	193		
GPIO_B5	194		
GPIO_B6	195		
GPIO_B7	200		
GPIO_B8	201		
GPIO_B9	198		
GPIO_B10	199		
GPIO_B10	230		
DEBUG_EN	202	–	Externally drives the 4390 JTAG enable pins high/low under software control for debug security purposes.
JTAG_SEL	205	I/O	WLAN JTAG enable. This pin must be connected to ground if the JTAG interface is not used.
LDO_VDD1P5	16, 19, 23, 26	I	LNLDO input.
LDO_VDDBAT5V	27, 30, 34, 36	I	LDO VBAT.
LPO_IN	39	I	External sleep clock input (32.768 KHz).
NC	40, 41, 55, 56, 66, 75, 85, 86, 91, 121, 158, 160, 162, 164–166, 169, 170, 179–181, 186–188, 202, 204	–	No connect.
OTP_VDD33	155	PWR	OTP 3.3V supply.
PMU_AVSS	21	GND	Quiet ground. Connect to VSSC for ESD.
PMU_VDDIO	37, 38	PWR	1.8V–3.3V supply for PMU controls. Must be directly connected to VDDIO on the PCB.
RF_AC_GND	102	GND	Connect to Ground to reduce system RF noise.
RF_DC_GND	106	GND	Connect to Ground to reduce system RF noise.
RF_SW_CTRL_0	145	O	Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.
RF_SW_CTRL_1	146		
RF_SW_CTRL_2	147		
RF_SW_CTRL_3	148		
RF_SW_CTRL_4	149		
RF_SW_CTRL_5	150		
RF_SW_CTRL_6	151		
RF_SW_CTRL_7	152		
RF_SW_CTRL_8	153		
RF_SW_CTRL_9	154		
SDIO_CLK	171	I	SDIO clock input.

Table 10. WLCSP and FCFBGA Pin Descriptions (Cont.)

Signal Name	WLCSP Bump #	Type	Description
SDIO_CMD	172	I/O	SDIO command line.
SDIO_DATA_0	173	I/O	SDIO data line 0.
SDIO_DATA_1	174	I/O	SDIO data line 1.
SDIO_DATA_2	175	I/O	SDIO data line 2.
SDIO_DATA_3	176	I/O	SDIO data line 3.
SDIO_PADVDDIO	197	I/O	Connect to the same VDD supply rail as SDIO interface.
SDIO_SEL	196	I/O	Connect to ground.
SR_PVSS	1, 2, 4, 5	GND	Power ground.
SR_VDDBATA5V	15	I	Quiet VBAT.
SR_VDDBATP5V	11, 12, 14	I	Power VBAT.
SR_VLX	6, 7, 8, 9, 10, 13	O	Cbuck switching regulator output. Refer to Table 20 on page 50 for recommendations of the inductor and capacitor for this supply.
VDDC	213–241	PWR	1.2V core supply for WLAN.
VDDIO	210–212	PWR	1.8V–3.3V supply for WLAN. Must be directly connected to PMU_VDDIO and APPS_VDDO on the PCB.
VDDIO_RF	156, 157	PWR	IO supply for RF switch control pads (3.3V).
VDDIO_SD	177, 178	PWR	1.8V–3.3V supply for SDIO pads.
VOUT_3P3	22, 25, 28	O	LDO 3.3V output.
VOUT_3P3_SENSE	29	O	Voltage sense pin for LDO 3.3V output.
VOUT_CLDO	17, 18, 20	O	Output of core LDO.
VOUT_LNLDO	24	O	Output of LNLDO.
VSSC	31, 35, 76, 77, 78, 81, 83, 88, 159, 161, 163, 167, 168, 182–185 206 –209, 242–286	GND	Core ground.
WL_REG_ON	3	I	Used by the PMU to power up/power down the on-chip regulators that supply power to the WLAN subsystem. This pin may be internally driven by the apps core even if the pin is externally connected to GND.
WL_VDDC	–	PWR	1.2V core supply for WLAN.
WRF_AFE_GND1P2	124	GND	AFE ground. Connect to VSSC for ESD.
WRF_BUCK_GND1P5	129	GND	Internal capacitor-less LDO ground. Connect to VSSC for ESD.
WRF_BUCK_VDD1P5	127, 128, 130, 131	PWR	Internal capacitor-less LDO supply.
WRF_CP_GND1P2	135	GND	Ground. Connect to VSSC for ESD.
WRF_GPIO_OUT	122	I/O	GPIO
WRF_LNA_GND1P2	101, 119	GND	Internal LNA ground.
WRF_LOGEN_GND1P2	104	GND	LOGEN ground. Connect to VSSC for ESD.
WRF_LOGENG_GND1P2	123	GND	LOGEN ground. Connect to VSSC for ESD.
WRF_MMD_GND1P2	133	GND	Ground. Connect to VSSC for ESD

Table 10. WLCSP and FCFBGA Pin Descriptions (Cont.)

Signal Name	WLCSP Bump #	Type	Description
WRF_MMD_VDD1P2	134	PWR	1.2V supply
WRF_PA_VBAT_GND3P3	105, 107, 109, 110, 111,116	GND	Connect to VSSC for ESD
WRF_PA_VBAT_VDD3P3	113, 114	PWR	PA 3.3V VBAT supply
WRF_PADRV_VBAT_GND3P3	108	GND	PAD ground. Connect to VSSC for ESD.
WRF_PADRV_VBAT_VDD3P3	112	PWR	PA Driver VBAT supply.
WRF_PFD_GND1P2	140	GND	Ground. Connect to VSSC for ESD.
WRF_PFD_VDD1P2	139	PWR	1.2V supply.
WRF_RFIN	118	I	2.4 GHz WLAN Receiver input.
WRF_RFOUT	115	O	2.4 GHz WLAN PA output.
WRF_RX_GND1P2	103, 117, 120	GND	RX 2 GHz ground. Connect to VSSC for ESD.
WRF_SYNTH_VBAT_VDD3P3	132	PWR	Synth VDD 3.3V supply.
WRF_TX_GND1P2	125	GND	TX ground. Connect to VSSC for ESD.
WRF_VCO_GND1P2	126	GND	VCO/LOGEN ground. Connect to VSSC for ESD.
WRF_XTAL_GND1P2	137	GND	XTAL ground. Connect to VSSC for ESD.
WRF_XTAL_IN	138	I	Crystal oscillator input.
WRF_XTAL_OUT	142	O	Crystal oscillator output.
WRF_XTAL_VDD1P2	141	I	Crystal LDO input (1.35V).
WRF_XTAL_VDD1P5	136	O	Crystal LDO output (1.2V).

9.4 I/O States

The following notations are used in Table 11:

- I: Input signal
- O: Output signal
- I/O: Input/Output signal
- PU = Pulled up
- PD = Pulled down
- NoPull = Neither pulled up nor pulled down

Table 11. I/O States

Name	I/O	Keeper[a]	Active Mode	Low Power State/ Sleep (All Power Present)	Power-down[b] (APPS_REG_ON and WL_REG_ON Held Low)	Out-of-Reset; Before SW Download (APPS_RST_N High; WL_REG_ON High)	(WL_REG_ON High and APPS_RST_N=0) and VDDIOs Are Present	Power Rail
APPS_WAKE	I/O	Y	Input/Output; PU, PD, NoPull (programmable)	Input; PU, PD, NoPull (programmable)	High-Z, NoPull	Input, PD	Input, PD	APPS_VDDO
APPS_REG_ON	I	N	Input; PD (pull down can be disabled)	Input; PD (pull down can be disabled)	Input; PD (of 200K)	Input; PD (of 200K)	Input; PD (of 200K)	–
APPS_UART1_CTS_N	I	Y	Input; NoPull	Input; NoPull	High-Z, NoPull	Input; PU	Input; PU	APPS_VDDO
APPS_UART1_RTS_N	O	Y	Output; NoPull	Output; NoPull	High-Z, NoPull	Input; PU	Input; PU	APPS_VDDO
APPS_UART1_RXD	I	Y	Input; PU	Input; NoPull	High-Z, NoPull	Input; PU	Input; PU	APPS_VDDO
APPS_UART1_TXD	O	Y	Output; NoPull	Output; NoPull	High-Z, NoPull	Input; PU	Input; PU	APPS_VDDO
SDIO_CMD	I/O	N	Input/Output; PU (SDIO Mode),	Input; PU (SDIO Mode)	High-Z, NoPull	Input; PU (SDIO Mode)	Input; PU (SDIO Mode)	WL_VDDIO
SDIO_DATA[0:3]	I/O	N	Input/Output; PU (SDIO Mode)	Input; PU (SDIO Mode)	High-Z, NoPull	Input; PU (SDIO Mode)	Input; PU (SDIO Mode)	WL_VDDIO
SDIO_CLK	I	N	Input; NoPull	Input; noPull	High-Z, NoPull	Input; noPull	Input; noPull	WL_VDDIO
GPIO_B0	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: PD])	Input/Output; PU, PD, NoPull (programmable [Default: PD])	High-Z, NoPull	Input; PD	Input; PD	WL_VDDIO
GPIO_B1	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	Input; NoPull	WL_VDDIO
GPIO_B10	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	Input; NoPull	WL_VDDIO

Table 11. I/O States (Cont.)

Name	I/O	Keeper[a]	Active Mode	Low Power State/ Sleep (All Power Present)	Power-down[b] (APPS_REG_ON and WL_REG_ON Held Low)	Out-of-Reset; Before SW Download (APPS_RST_N High; WL_REG_ON High)	(WL_REG_ON High and APPS_RST_N=0) and VDDIOs Are Present	Power Rail
GPIO_B11	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: PD])	Input/Output; PU, PD, NoPull (programmable [Default: PD])	High-Z, NoPull	Input; PD	Input; PD	WL_VDDIO
GPIO_B2	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	Input; NoPull	WL_VDDIO
GPIO_B3	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: PD])	Input/Output; PU, PD, NoPull (programmable [Default: PD])	High-Z, NoPull	Input; PD	Input; PD	WL_VDDIO
GPIO_B4	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	Input; NoPull	WL_VDDIO
GPIO_B5	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: PD])	Input/Output; PU, PD, NoPull (programmable [Default: PD])	High-Z, NoPull	Input; PD	Input; PD	WL_VDDIO
GPIO_B6	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	Input; NoPull	WL_VDDIO
GPIO_B7	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	Input; NoPull	WL_VDDIO
GPIO_B8	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: PD])	Input/Output; PU, PD, NoPull (programmable [Default: PD])	High-Z, NoPull	Input; PD	Input; PD	WL_VDDIO
GPIO_B9	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: PD])	Input/Output; PU, PD, NoPull (programmable [Default: PD])	High-Z, NoPull	Input; PD	Input; PD	WL_VDDIO
WL_REG_ON	I	N	Input; PD (pull-down can be disabled)	Input; PD (pull-down can be disabled)	Input; PD (of 200K)	Input; PD (of 200K)	Input; PD (of 200K)	–

a. Keeper column: N = pad has no keeper. Y = pad has a keeper. Keeper is always active except in Power-down state. If there is no keeper, and it is an input and there is Nopull, then the pad should be driven to prevent leakage due to floating pad (SDIO_CLK, for example).
b. In the Power-down state (xx_REG_ON=0): High-Z; NoPull => the pad is disabled because power is not supplied.

10. DC Characteristics

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

10.1 Absolute Maximum Ratings

Caution: The absolute maximum ratings in Table 12 indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Table 12. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
DC supply for VBAT and PA driver supply	VBAT	–0.5 to +6.0	V
DC supply voltage for digital I/O	VDDIO	–0.5 to 3.9	V
DC supply voltage for RF switch I/Os	VDDIO_RF	–0.5 to 3.9	V
DC input supply voltage for CLDO and LNLDO	–	–0.5 to 1.575	V
DC supply voltage for RF analog	VDDRF	–0.5 to 1.32	V
DC supply voltage for core	VDDC	–0.5 to 1.32	V
WRF_TCXO_VDD	–	–0.5 to 3.63	V
Maximum undershoot voltage for I/O	$V_{undershoot}$	–0.5	V
Maximum junction temperature	T_j	125	°C

10.2 Environmental Ratings

The environmental ratings are shown in Table 13.

Table 13. Environmental Ratings

Characteristic	Value	Units	Conditions/Comments
Ambient Temperature (T_A)	–30 to +85	°C	Functional operation[a]
Storage Temperature	–40 to +125	°C	–
Relative Humidity	Less than 60	%	Storage
	Less than 85	%	Operation

a. Functionality is guaranteed but specifications require derating at extreme temperatures; see the specification tables for details.

10.3 Electrostatic Discharge Specifications

Extreme caution must be exercised to prevent electrostatic discharge (ESD) damage. Proper use of wrist and heel grounding straps to discharge static electricity is required when handling these devices. Always store unused material in its antistatic packaging.

Table 14. ESD Specifications

Pin Type	Symbol	Condition	ESD Rating	Unit
ESD, Handling Reference: NQY00083, Section 3.4, Group D9, Table B	ESD_HAND_HBM	Human body model contact discharge per JEDEC EID/JESD22-A114	TBD	V
Machine Model (MM)	ESD_HAND_MM	Machine model contact	TBD	V
CDM	ESD_HAND_CDM	Charged device model contact discharge per JEDEC EIA/JESD22-C101	TBD	V

10.4 Recommended Operating Conditions and DC Characteristics

Caution: Functional operation is not guaranteed outside of the limits shown in Table 15 on page 44 and operation outside these limits for extended periods can adversely affect long-term reliability of the device.

Table 15. Recommended Operating Conditions and DC Characteristics

Parameter	Symbol	Value			Unit
		Minimum	Typical	Maximum	
DC supply voltage for VBAT	VBAT	3.0[a]	–	5.25[b]	V
DC supply voltage for core	VDD	1.14	1.2	1.26	V
DC supply voltage for RF blocks in chip	VDDRF	1.14	1.2	1.26	V
DC supply voltage for TCXO input buffer	WRF_TCXO_VDD	1.62	1.8	1.98	V
DC supply voltage for digital I/O	VDDIO, VDDIO_SD	1.71	–	3.63	V
DC supply voltage for RF switch I/Os	VDDIO_RF	3.13	3.3	3.46	V
Internal POR threshold	Vth_POR	0.4	–	0.7	V
Other Digital I/O Pins					
For VDDIO = 1.8V:					
Input high voltage	VIH	0.65 × VDDIO	–	–	V
Input low voltage	VIL	–	–	0.35 × VDDIO	V
Output high voltage @ 2 mA	VOH	VDDIO – 0.45	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.45	V
For VDDIO = 3.3V:					
Input high voltage	VIH	2.00	–	–	V
Input low voltage	VIL	–	–	0.80	V
Output high voltage @ 2 mA	VOH	VDDIO – 0.4	–	–	V
Output low Voltage @ 2 mA	VOL	–	–	0.40	V
RF Switch Control Output Pins[c]					
For VDDIO_RF = 3.3V:					
Output high voltage @ 2 mA	VOH	VDDIO – 0.4	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.40	V
Input capacitance	C_{IN}	–	–	5	pF

a. The CYW4390 is functional across this range of voltages. Optimal RF performance specified in the data sheet, however, is guaranteed only for 3.13V < VBAT < 4.8V.
b. The maximum continuous voltage is 5.25V. Voltages up to 6.0V for up to 10 seconds, cumulative duration over the lifetime of the device are allowed. Voltages as high as 5.5V for up to 250 seconds, cumulative duration over the lifetime of the device are allowed.
c. Programmable 2 mA to 16 mA drive strength. Default is 10 mA.

11. WLAN RF Specifications

11.1 Introduction

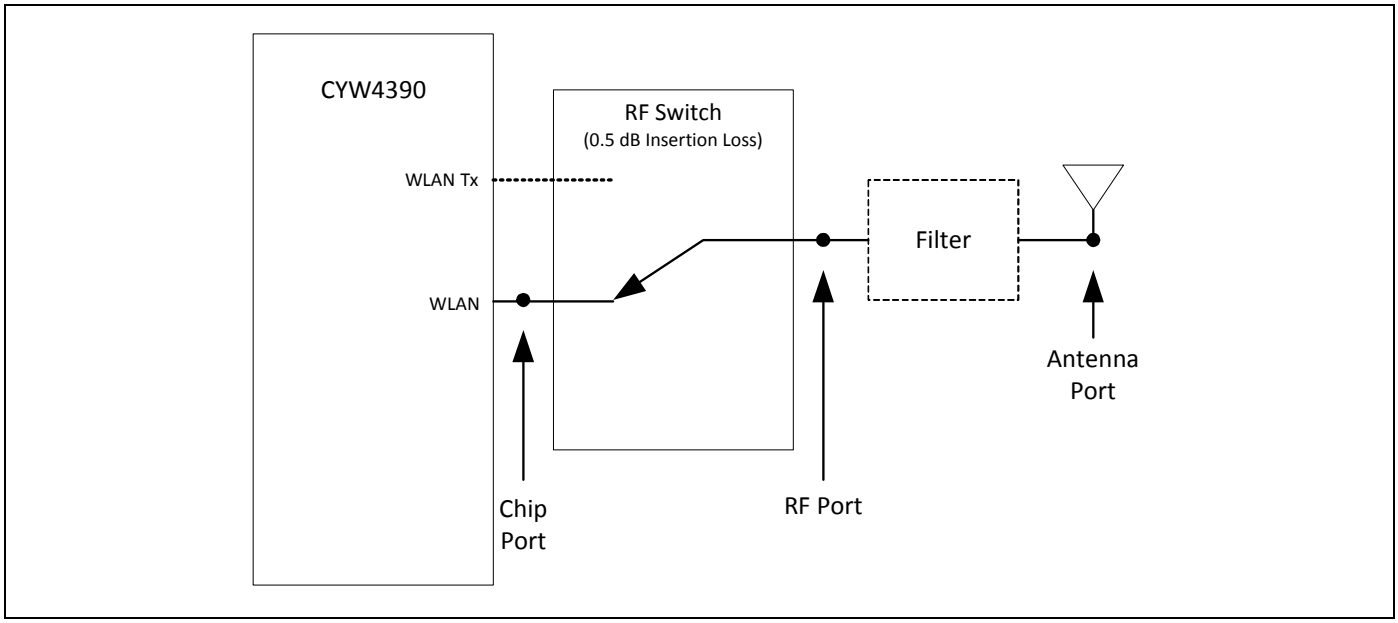
The CYW4390 includes an integrated single-band direct conversion radio that supports the 2.4 GHz band. This section describes the RF characteristics of the 2.4 GHz radio.

Note: Values in this section of the data sheet are design goals and are subject to change based on the results of device characterization.

Unless otherwise stated, limit values apply for the conditions specified inTable 13 on page 42 and Table 15 on page 44. Typical values apply for the following conditions:

- VBAT = 3.6V
- Ambient temperature +25°C

Figure 12. Port Locations



Note: All WLAN specifications are specified at the chip port, unless otherwise specified.

11.2 2.4 GHz Band General RF Specifications

Table 16. 2.4 GHz Band General RF Specifications

Item	Condition	Minimum	Typical	Maximum	Unit
Tx/Rx switch time	Including TX ramp down	–	–	5	µs
Rx/Tx switch time	Including TX ramp up	–	–	2	µs
Power-up and power-down ramp time	DSSS/CCK modulations	–	–	< 2	µs

11.3 WLAN 2.4 GHz Receiver Performance Specifications

Note: The specifications in Table 17 are specified at the chip port, unless otherwise specified.

Table 17. WLAN 2.4 GHz Receiver Performance Specifications

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Frequency range	–		2400	–	2500	MHz
RX sensitivity IEEE 802.11b (8% PER for 1024 octet PSDU)[a]	1 Mbps DSSS		–	–98.4	–	dBm
	2 Mbps DSSS		–	–96.5	–	dBm
	5.5 Mbps DSSS		–	–93.7	–	dBm
	11 Mbps DSSS		–	–91.4	–	dBm
RX sensitivity IEEE 802.11g (10% PER for 1024 octet PSDU)[a]	6 Mbps OFDM		–	–95.5	–	dBm
	9 Mbps OFDM		–	–94.1	–	dBm
	12 Mbps OFDM		–	–93.2	–	dBm
	18 Mbps OFDM		–	–90.6	–	dBm
	24 Mbps OFDM		–	–87.3	–	dBm
	36 Mbps OFDM		–	–84	–	dBm
	48 Mbps OFDM		–	–79.3	–	dBm
	54 Mbps OFDM		–	–77.8	–	dBm
RX sensitivity IEEE 802.11n (10% PER for 4096 octet PSDU)[a,b.] Defined for default parameters: GF, 800 ns GI, and non-STBC.	20 MHz channel spacing for all MCS rates					
	MCS0		–	–95	–	dBm
	MCS1		–	–92.7	–	dBm
	MCS2		–	–90.2	–	dBm
	MCS3		–	–87.1	–	dBm
	MCS4		–	–83.5	–	dBm
	MCS5		–	–78.9	–	dBm
	MCS6		–	–77.3	–	dBm
	MCS7		–	–75.7	–	dBm
Blocking level for 1dB Rx sensitivity degradation (without external filtering)[c]	776–794 MHz	CDMA2000	–	–24	–	dBm
	824–849 MHz[d]	cdmaOne	–	–25	–	dBm
	824–849 MHz	GSM850	–	–15	–	dBm
	880–915 MHz	E-GSM	–	–16	–	dBm
	1710–1785 MHz	GSM1800	–	–18	–	dBm
	1850–1910 MHz	GSM1800	–	–19	–	dBm
	1850–1910 MHz	cdmaOne	–	–26	–	dBm
	1850–1910 MHz	WCDMA	–	–26	–	dBm
	1920–1980 MHz	WCDMA	–	–28.5	–	dBm
	2500–2570 MHz	Band 7	–	–45	–	dBm
	2300–2400 MHz	Band 40	–	–50	–	dBm
	2570–2620 MHz	Band 38	–	–45	–	dBm
	2545–2575 MHz	XGP Band	–	–45	–	dBm

Table 17. WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
In-band static CW jammer immunity (fc – 8 MHz < fcw < + 8 MHz)	Rx PER < 1%, 54 Mbps OFDM, 1000 octet PSDU for: (RxSens + 23 dB < Rxlevel < max input level)		–80	–	–	dBm
Input In-Band IP3[a]	Maximum LNA gain		–	–15.5	–	dBm
	Minimum LNA gain		–	–1.5	–	dBm
Maximum Receive Level @ 2.4 GHz	@ 1, 2 Mbps (8% PER, 1024 octets)		–3.5	–	–	dBm
	@ 5.5, 11 Mbps (8% PER, 1024 octets)		–9.5	–	–	dBm
	@ 6–54 Mbps (10% PER, 1024 octets)		–9.5	–	–	dBm
	@ MCS0–7 rates (10% PER, 4095 octets)		–9.5	–	–	dBm
LPF 3 dB Bandwidth	–		9	–	12	MHz
Adjacent channel rejection-DSSS (Difference between interfering and desired signal at 8% PER for 1024 octet PSDU with desired signal level as specified in Condition/Notes)	**Desired and interfering signal 30 MHz apart**					
	1 Mbps DSSS	–74 dBm	35	–	–	dB
	2 Mbps DSSS	–74 dBm	35	–	–	dB
	Desired and interfering signal 25 MHz apart					
	5.5 Mbps DSSS	–70 dBm	35	–	–	dB
	11 Mbps DSSS	–70 dBm	35	–	–	dB
Adjacent channel rejection-OFDM (Difference between interfering and desired signal (25 MHz apart) at 10% PER for 1024 octet PSDU with desired signal level as specified in Condition/Notes)	6 Mbps OFDM	–79 dBm	16	–	–	dB
	9 Mbps OFDM	–78 dBm	15	–	–	dB
	12 Mbps OFDM	–76 dBm	13	–	–	dB
	18 Mbps OFDM	–74 dBm	11	–	–	dB
	24 Mbps OFDM	–71 dBm	8	–	–	dB
	36 Mbps OFDM	–67 dBm	4	–	–	dB
	48 Mbps OFDM	–63 dBm	0	–	–	dB
	54 Mbps OFDM	–62 dBm	–1	–	–	dB
Adjacent channel rejection MCS0– 7 (Difference between interfering and desired signal (25 MHz apart) at 10% PER for 4096 octet PSDU with desired signal level as specified in Condition/Notes)	MCS0	–79 dBm	16	–	–	dB
	MCS1	–76 dBm	13	–	–	dB
	MCS2	–74 dBm	11	–	–	dB
	MCS3	–71 dBm	8	–	–	dB
	MCS4	–67 dBm	4	–	–	dB
	MCS5	–63 dBm	0	–	–	dB
	MCS6	–62 dBm	–1	–	–	dB
	MCS7	–61 dBm	–2	–	–	dB
Maximum receiver gain	–	–	–	95	–	dB
Gain control step	–	–	–	3	–	dB
RSSI accuracy[e]	Range –98 dBm to –30 dBm		–5	–	5	dB
	Range above –30 dBm		–8	–	8	dB
Return loss	Z_o = 50Ω, across the dynamic range		10	11.5	13	dB
Receiver cascaded noise figure	At maximum gain		–	4	–	dB

a. Derate by 1.5 dB for –30°C to –10°C and 55°C to 85°C.
b. Sensitivity degradations for alternate settings in MCS modes. MM: 0.5 dB drop, and SGI: 2 dB drop.

c. The cellular standard listed for each band indicates the type of modulation used to generate the interfering signal in that band for the purpose of this test. It is not intended to indicate any specific usage of each band in any specific country.
d. The blocking levels are valid for channels 1 to 11. (For higher channels, the performance may be lower due to third harmonic signals (3 × 824 MHz) falling within band.)
e. The minimum and maximum values shown have a 95% confidence level.

11.4 WLAN 2.4 GHz Transmitter Performance Specifications

Note: The specifications in Table 18 are specified at the chip port output, unless otherwise specified.

Table 18. WLAN 2.4 GHz Transmitter Performance Specifications

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Frequency range	–		2400	–	2500	MHz
Harmonic level (at 18 dBm with 100% duty cycle)	4.8–5.0 GHz	2nd harmonic	–	–8	–	dBm/1 MHz
	7.2–7.5 GHz	3rd harmonic	–	–18	–	dBm/1 MHz
EVM Does Not Exceed						
Tx power at RF port for highest power level setting at 25°C and VBAT = 3.6V with spectral mask and EVM compliance[a, b]	802.11b (DSSS/CCK)	–9 dB	19	20.5	–	dBm
	OFDM, BPSK	–8 dB	19	20	–	dBm
	OFDM, QPSK	–13 dB	19	20	–	dBm
	OFDM, 16-QAM	–19 dB	17.5	19	–	dBm
	OFDM, 64-QAM (R = 3/4)	–25 dB	16.5	18	–	dBm
	OFDM, 64-QAM (R = 5/6)	–28 dB	15.5	17	–	dBm
Phase noise	37.4 MHz Crystal, Integrated from 10 kHz to 10 MHz		–	0.45	–	Degrees
Tx power control dynamic range	–		10	–	–	dB
Closed-loop Tx power variation at highest power level setting	Across full temperature and voltage range. Applies across 10 dBm to 20 dBm output power range.		–	–	±1.5	dB
Carrier suppression	–		15	–	–	dBc
Gain control step	–		–	0.25	–	dB
Return loss at Chip port Tx	Z_o = 50Ω		–	6	–	dB

a. Derate by 1.5 dB for temperatures less than –10°C or more than 55°C, or voltages less than 3.0V. Derate by 3.0 dB for voltages of less than 2.7V, or voltages of less than 3.0V at temperatures less than –10°C or greater than 55°C. Derate by 4.5 dB for –40°C to –30°C.
b. Tx power for Channel 1 and Channel 11 is specified by non-volatile memory parameters.

11.5 General Spurious Emissions Specifications

Table 19. General Spurious Emissions Specifications

Parameter	Condition/Notes		Min	Typ	Max	Unit
Frequency range	–		2400	–	2500	MHz
General Spurious Emissions						
Tx Emissions	30 MHz < f < 1 GHz	RBW = 100 kHz	–	–93	–	dBm
	1 GHz < f < 12.75 GHz	RBW = 1 MHz	–	–45.5	–	dBm
	1.8 GHz < f < 1.9 GHz	RBW = 1 MHz	–	–72	–	dBm
	5.15 GHz < f < 5.3 GHz	RBW = 1 MHz	–	–87	–	dBm
Rx/standby Emissions	30 MHz < f < 1 GHz	RBW = 100 kHz	–	–107	–	dBm
	1 GHz < f < 12.75 GHz	RBW = 1 MHz	–	–65[a]	–	dBm
	1.8 GHz < f < 1.9 GHz	RBW = 1 MHz	–	–87	–	dBm
	5.15 GHz < f < 5.3 GHz	RBW = 1 MHz	–	–100	–	dBm

a. For frequencies other than 3.2 GHz, the emissions value is –96 dBm. The value presented in table is the result of LO leakage at 3.2 GHz.

12. Internal Regulator Electrical Specifications

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Functional operation is not guaranteed outside of the specification limits provided in this section.

12.1 Core Buck Switching Regulator

Table 20. Core Buck Switching Regulator (CBUCK) Specifications

Specification	Notes	Min	Typ	Max	Units
Input supply voltage (DC)	DC voltage range inclusive of disturbances.	3.0	3.6	5.25[a]	V
PWM mode switching frequency	CCM, Load > 100 mA VBAT = 3.6V	2.8	4	5.2	MHz
PWM output current	–	–	–	600	mA
Output current limit	–	–	1400		mA
Output voltage range	Programmable, 30 mV steps Default = 1.35V	1.2	1.35	1.5	V
PWM output voltage DC accuracy	Includes load and line regulation. Forced PWM mode	–4	–	4	%
PWM ripple voltage, static	Measure with 20 MHz bandwidth limit. Static Load. Max Ripple based on VBAT = 3.6V, Vout = 1.35V, Fsw = 4 MHz, 2.2 µH inductor L > 1.05 µH, Cap + Board total-ESR < 20 mΩ, C_{out} > 1.9 µF, ESL<200pH	–	7	20	mVpp
PWM mode peak efficiency	Peak Efficiency at 200 mA load	78	86	–	%
PFM mode efficiency	10 mA load current	70	81	–	%
Start-up time from power down	VIO already ON and steady. Time from REG_ON rising edge to CLDO reaching 1.2V	–	–	850	µs
External inductor	0806 size, ± 30%, 0.11 ± 25% Ohms	–	2.2	–	µH
External output capacitor	Ceramic, X5R, 0402, ESR <30 mΩ at 4 MHz, ± 20%, 6.3V	2.0[b]	4.7	10[c]	µF
External input capacitor	For SR_VDDBATP5V pin, ceramic, X5R, 0603, ESR < 30 mΩ at 4 MHz, ± 20%, 6.3V, 4.7 µF	0.67[b]	4.7	–	µF
Input supply voltage ramp-up time	0 to 4.3V	40	–	–	µs

a. The maximum continuous voltage is 5.25V. Voltages up to 6.0V for up to 10 seconds, cumulative duration, over the lifetime of the device are allowed. Voltages as high as 5.5V for up to 250 seconds, cumulative duration, over the lifetime of the device are allowed.
b. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.
c. Total capacitance includes those connected at the far end of the active load.

12.2 3.3V LDO (LDO3P3)

Table 21. LDO3P3 Specifications

Specification	Notes	Min	Typ	Max	Units
Input supply voltage, V_{in}	Min = V_o + 0.2V = 3.5V dropout voltage requirement must be met under maximum load for performance specifications.	3.0	3.6	5.25[a]	V
Output current	–	0.001	–	450	mA
Nominal output voltage, V_o	Default = 3.3V	–	3.3	–	V
Dropout voltage	At max load.	–	–	200	mV
Output voltage DC accuracy	Includes line/load regulation.	–5	–	+5	%
Quiescent current	No load	–	–	100	µA
Line regulation	V_{in} from (V_o + 0.2V) to 4.8V, max load	–	–	3.5	mV/V
Load regulation	load from 1 mA to 450 mA	–	–	0.3	mV/mA
PSRR	$V_{in} \geq V_o$ + 0.2V, V_o = 3.3V, C_o = 4.7 µF, Max load, 100 Hz to 100 kHz	20	–	–	dB
LDO turn-on time	Chip already powered up.	–	160	250	µs
External output capacitor, C_o	Ceramic, X5R, 0402, (ESR: 5 mΩ–240 mΩ), ± 10%, 10V	1.0[b]	4.7	10	µF
External input capacitor	For SR_VDDBATA5V pin (shared with Bandgap) Ceramic, X5R, 0402, (ESR: 30m–200 mΩ), ± 10%, 10V. Not needed if sharing VBAT capacitor 4.7 µF with SR_VDDBATP5V.	–	4.7	–	µF

a. The maximum continuous voltage is 5.25V. Voltages up to 6.0V for up to 10 seconds, cumulative duration, over the lifetime of the device are allowed. Voltages as high as 5.5V for up to 250 seconds, cumulative duration, over the lifetime of the device are allowed.
b. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

12.3 CLDO

Table 22. CLDO Specifications

Specification	Notes	Min	Typ	Max	Units
Input supply voltage, V_{in}	Min = 1.2 + 0.15V = 1.35V dropout voltage requirement must be met under maximum load.	1.3	1.35	1.5	V
Output current	–	0.2	–	300	mA
Output voltage, V_o	Programmable in 25 mV steps. Default = 1.2.V	1.1	1.2	1.275	V
Dropout voltage	At max load	–	–	150	mV
Output voltage DC accuracy	Includes line/load regulation	–4	–	+4	%
Quiescent current	No load	–	24	–	µA
	300 mA load	–	2.1	–	mA
Line Regulation	V_{in} from (V_o + 0.15V) to 1.5V, maximum load	–	–	5	mV/V
Load Regulation	Load from 1 mA to 300 mA	–	0.02	0.05	mV/mA
Leakage Current	Power down	–	–	20	µA
	Bypass mode	–	1	3	µA
PSRR	@1 kHz, V_{in} ≥ 1.35V, C_o = 4.7 µF	20	–		dB
Start-up Time of PMU	VIO up and steady. Time from the REG_ON rising edge to the CLDO reaching 1.2V.	–	–	700	µs
LDO Turn-on Time	LDO turn-on time when rest of the chip is up	–	140	180	µs
External Output Capacitor, C_o	Total ESR: 5 mΩ–240 mΩ	1.32[a]	4.7	–	µF
External Input Capacitor	Only use an external input capacitor at the VDD_LDO pin if it is not supplied from CBUCK output.	–	1	2.2	µF

a. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

12.4 LNLDO

Table 23. LNLDO Specifications

Specification	Notes	Min	Typ	Max	Units
Input supply voltage, V_{in}	Min = $1.2V_o$ + 0.15V = 1.35V dropout voltage requirement must be met under maximum load.	1.3	1.35	1.5	V
Output Current	–	0.1	–	150	mA
Output Voltage, V_o	Programmable in 25 mV steps. Default = 1.2V	1.1	1.2	1.275	V
Dropout Voltage	At maximum load	–	–	150	mV
Output Voltage DC Accuracy	Includes line/load regulation	–4	–	+4	%
Quiescent current	No load	–	44	–	µA
	Max load	–	970	990	µA
Line Regulation	V_{in} from (V_o + 0.1V) to 1.5V, max load	–	–	5	mV/V
Load Regulation	Load from 1 mA to 150 mA	–	0.02	0.05	mV/mA
Leakage Current	Power-down	–	–	10	µA
Output Noise	@30 kHz, 60–150 mA load C_o = 2.2 µF @100 kHz, 60–150 mA load C_o = 2.2 µF	–	–	60 35	nV/rt Hz nV/rt Hz
PSRR	@ 1kHz, Input > 1.35V, C_o= 2.2 µF, V_o = 1.2V	20	–	–	dB
LDO Turn-on Time	LDO turn-on time when rest of chip is up	–	140	180	µs
External Output Capacitor, C_o	Total ESR (trace/capacitor): 5 mΩ–240 mΩ	0.5[a]	2.2	4.7	µF
External Input Capacitor	Only use an external input capacitor at the VDD_LDO pin if it is not supplied from CBUCK output. Total ESR (trace/capacitor): 30 mΩ–200 mΩ	–	1	2.2	µF

a. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

13. System Power Consumption

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Note: Unless otherwise stated, these values apply for the conditions specified in Table 15 on page 44.

Table 24. Application Processor Current Consumption

Mode	Bandwidth (MHz)	Band (GHz)	Vbat = 3.6V, VDDIO = 1.8V, T(A) = 25°C		Notes
			Vbat, mA	Vio, µA	
Sleep Modes					
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD

13.1 WLAN Current Consumption

The WLAN current consumption measurements are shown in Table 25.

Table 25. Typical WLAN Power Consumption[a]

Mode	Bandwidth (MHz)	Band (GHz)	Vbat = 3.6V, VDDIO = 1.8V, T(A) = 25°C		Notes
			Vbat, mA	Vio, µA	
Sleep Modes					
Off			0.005	3	Note[b]
Sleep			0.1	200	Note[c]
IEEE Power Save, DTIM 1			1.2	60	Note[d]
IEEE Power Save, DTIM 3			0.4	60	Note[d]
Active Modes					
Transmit, CCK	20	2.4	88	60	Notes[e, f]
Transmit, MCS7	20	2.4	111	60	Notes[e, f]
Transmit, CCK (@20 dBm)	20	2.4	342	60	Notes[f, g]
Transmit, MCS7 (@18.5 dBm)	20	2.4	295	60	Notes[f, g]
Receive	20	2.4	61	60	Notes[f, h, i]
CRS	20	2.4	56	60	Note[j]

a. Vio is specified with all pins idle (not switching) and not driving any loads.
b. WL_REG_ON and APPS_REG_ON are low.
c. Idle, not associated or inter-beacon.
d. Beacon interval is 102.4 ms and beacon duration is 1 ms @ 1 Mbps. Average current is over three DTIM intervals.
e. Duty cycle is 100%.
f. Measured using packet engine test mode.
g. Duty cycle is 100%. It includes internal PA contribution.
h. Duty cycle is 100%. Carrier sense (CS) detect/packet receive.
i. MCS7 and HT20.
j. Carrier Sense (CCA) when no carrier is present.

13.2 JTAG Timing

Table 26. JTAG Timing Characteristics

Signal Name	Period	Output Maximum	Output Minimum	Setup	Hold
TCK	125 ns	–	–	–	–
TDI	–	–	–	20 ns	0 ns
TMS	–	–	–	20 ns	0 ns
TDO	–	100 ns	0 ns	–	–
$\overline{\text{JTAG\_TRST}}$	250 ns	–	–	–	–

14. Power-Up Sequence and Timing

14.1 Sequencing of Reset and Regulator Control Signals

The CYW4390 has two signals that allow the host to control power consumption by enabling or disabling the APPS CPU, WLAN, and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states (see Figure 13 and Figure 14 on page 57, and Figure 15 and Figure 16 on page 58). The timing values indicated are minimum required values; longer delays are also acceptable.

14.1.1 Description of Control Signals

- **WL_REG_ON**: Used by the PMU to power up the WLAN section. It is also OR-gated with the APPS_REG_ON input to control the internal CYW4390 regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset. If both the APPS_REG_ON and WL_REG_ON pins are low, the regulators are disabled.
- **APPS_REG_ON**: Used by the PMU (OR-gated with WL_REG_ON) to power up the internal CYW4390 regulators. If both the APPS_REG_ON and WL_REG_ON pins are low, the regulators are disabled. When this pin is low and WL_REG_ON is high, the APPS CPU section is in reset.

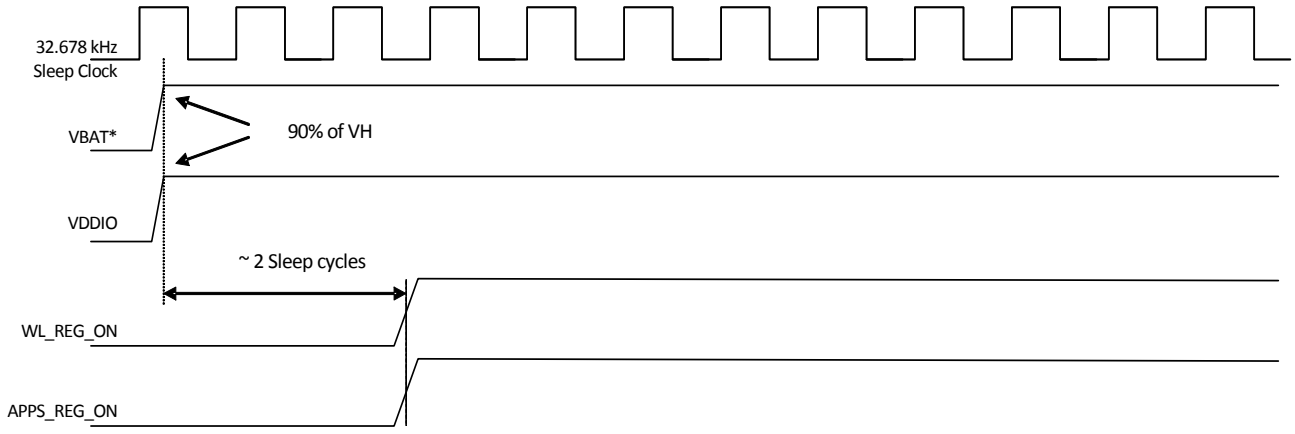
Note: For both the WL_REG_ON and APPS_REG_ON pins, there should be at least a 10 ms time delay between consecutive toggles (where both signals have been driven low). This is to allow time for the CBUCK regulator to discharge. If this delay is not followed, then there may be a VDDIO in-rush current on the order of 36 mA during the next PMU cold start.

Note: The CYW4390 has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after VDDC and VDDIO have both passed the POR threshold.

Note: VBAT should not rise 10%–90% faster than 40 microseconds. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

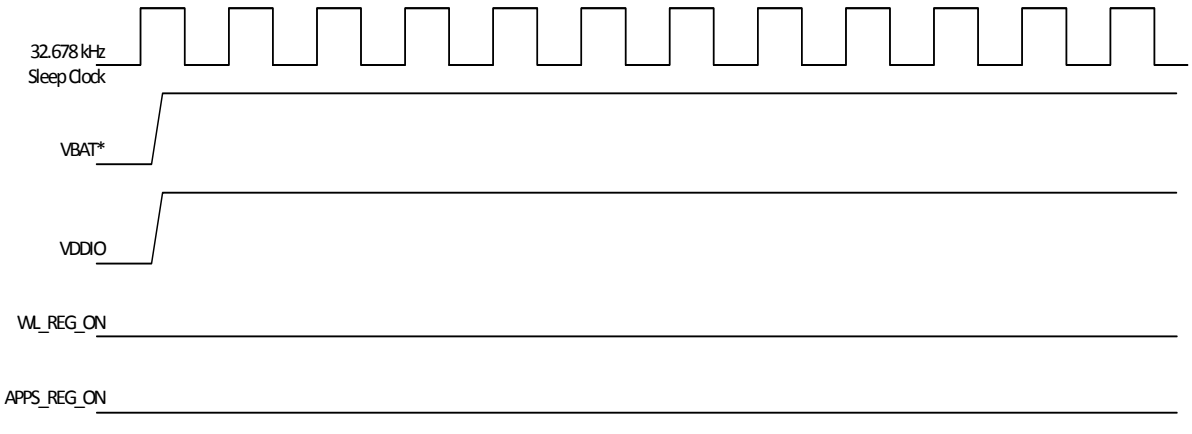
14.1.2 Control Signal Timing Diagrams

Figure 13. WLAN = ON, APPS CPU = ON



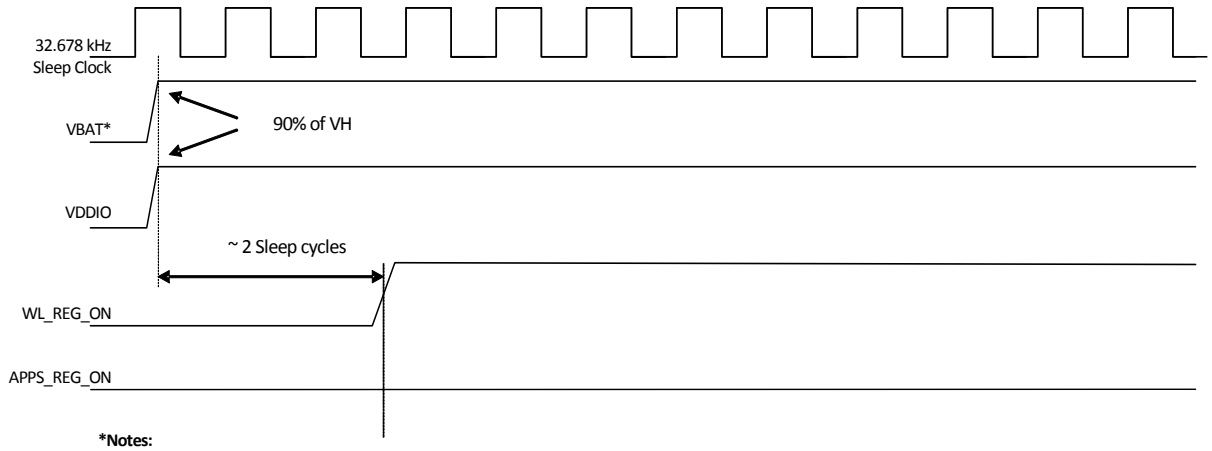
***Notes:**
1. VBAT should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

Figure 14. WLAN = OFF, APPS CPU = OFF



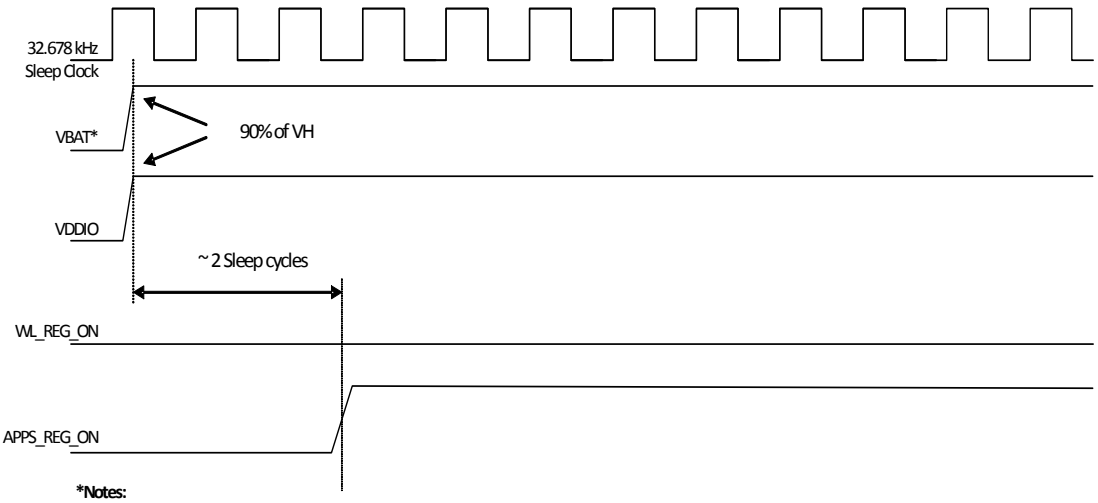
***Notes:**
1. VBAT should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

Figure 15. WLAN = ON, APPS CPU = OFF



***Notes:**
1. VBAT should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

Figure 16. WLAN = OFF, APPS CPU= ON



***Notes:**
1. VBAT should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

15. Package Information

15.1 Package Thermal Characteristics

Table 27. Package Thermal Characteristics[a]

Characteristic	WLCSP
θ_{JA} (°C/W) (value in still air)	33.45
θ_{JB} (°C/W)	3.45
θ_{JC} (°C/W)	1.00
Ψ_{JT} (°C/W)	3.45
Ψ_{JB} (°C/W)	10.64
Maximum Junction Temperature T_j (°C)	125
Maximum Power Dissipation (W)	1.119

a. No heat sink, TA = 70°C. This is an estimate, based on a 4-layer PCB that conforms to EIA/JESD51–7 (101.6 mm × 101.6 mm × 1.6 mm) and P = 1.119W continuous dissipation.

15.2 Junction Temperature Estimation and PSI$_{JT}$ Versus THETA$_{JC}$

Package thermal characterization parameter PSI–J_T (Ψ_{JT}) yields a better estimation of actual junction temperature (T_J) versus using the junction-to-case thermal resistance parameter Theta–J_C (θ_{JC}). The reason for this is that θ_{JC} assumes that all the power is dissipated through the top surface of the package case. In actual applications, some of the power is dissipated through the bottom and sides of the package. Ψ_{JT} takes into account power dissipated through the top, bottom, and sides of the package. The equation for calculating the device junction temperature is:

$$T_J = T_T + P \times \Psi_{JT}$$

Where:

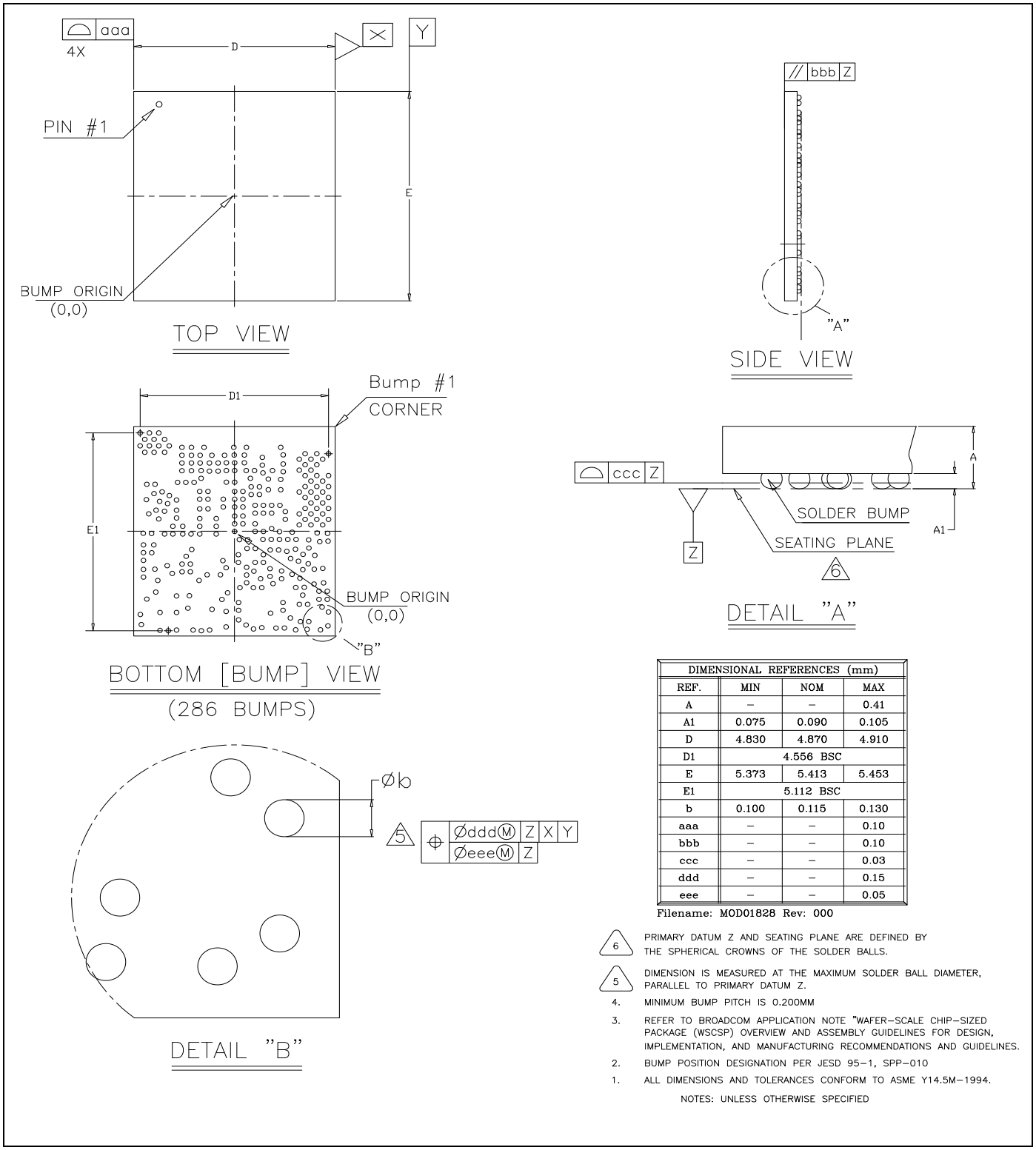
- T_J = Junction temperature at steady-state condition (°C)
- T_T = Package case top center temperature at steady-state condition (°C)
- P = Device power dissipation (Watts)
- Ψ_{JT} = Package thermal characteristics; no airflow (°C/W)

15.3 Environmental Characteristics

For environmental characteristics data, see Table 13 on page 42.

16. Mechanical Information

Figure 17. 286-Bump WLCSP Package Bump Map



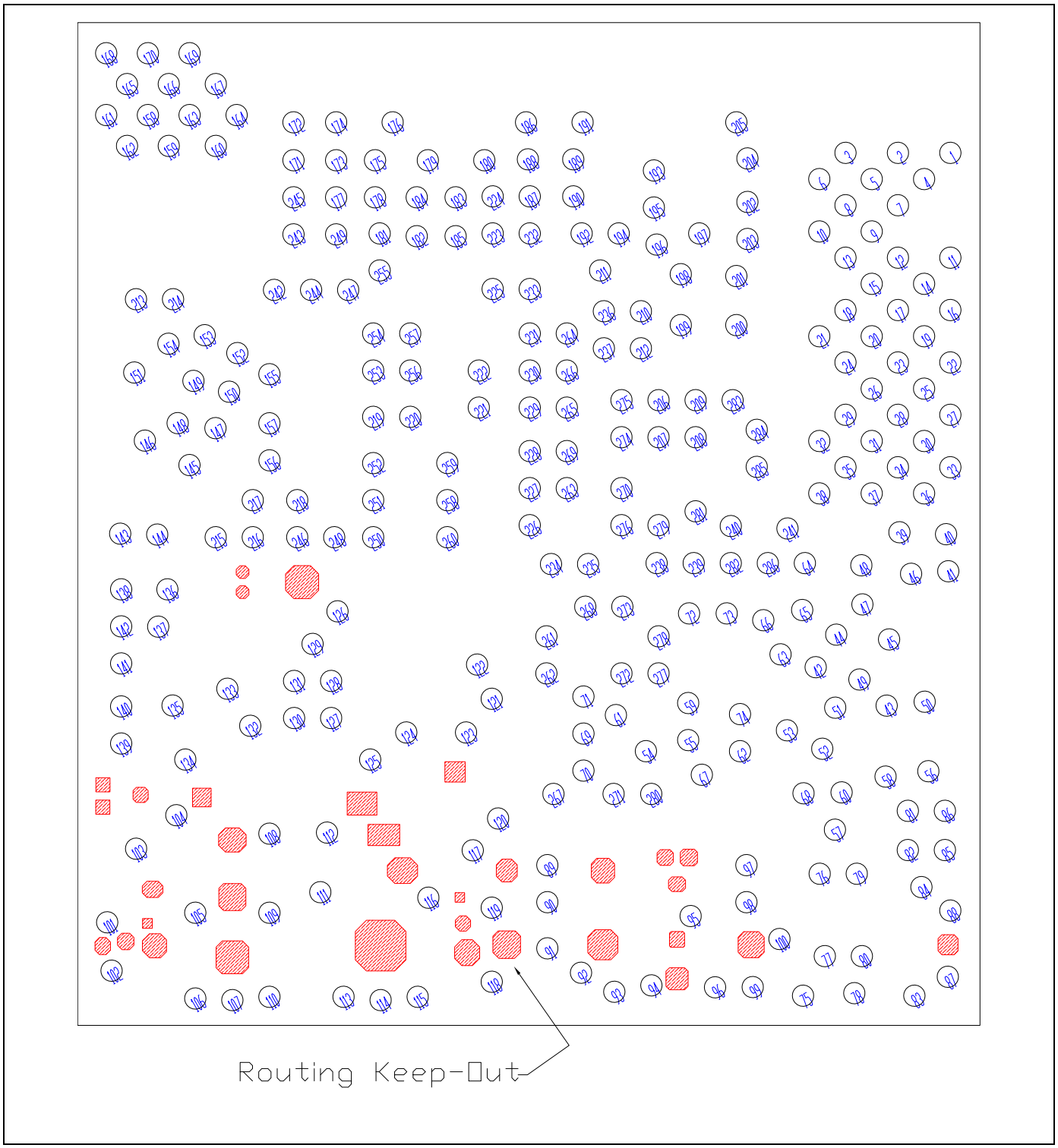
DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	–	–	0.41
A1	0.075	0.090	0.105
D	4.830	4.870	4.910
D1		4.556 BSC	
E	5.373	5.413	5.453
E1		5.112 BSC	
b	0.100	0.115	0.130
aaa	–	–	0.10
bbb	–	–	0.10
ccc	–	–	0.03
ddd	–	–	0.15
eee	–	–	0.05

Filename: MOD01828 Rev: 000

6. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.
4. MINIMUM BUMP PITCH IS 0.200MM
3. REFER TO BROADCOM APPLICATION NOTE "WAFER–SCALE CHIP–SIZED PACKAGE (WSCSP) OVERVIEW AND ASSEMBLY GUIDELINES FOR DESIGN, IMPLEMENTATION, AND MANUFACTURING RECOMMENDATIONS AND GUIDELINES.
2. BUMP POSITION DESIGNATION PER JESD 95–1, SPP–010
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.

NOTES: UNLESS OTHERWISE SPECIFIED

Figure 18. WLCSP Keep-Out Areas for PCB Layout—Bottom View, Bumps Facing Up



Note: Top-layer metal is not allowed in the keep-out areas.

17. Ordering Information

Part Number	Package	Description	Ambient Operating Temperature
CYW4390DKWBG	286-bump WLCSP (4.87 mm × 5.413 mm, 0.2 mm pitch)	Single-band 2.4 GHz WLAN	–30°C to +85°C

Document History

Document Title: CYW4390 WICED™ Wi-Fi IEEE 802.11 b/g/n SoC with Embedded Application Processor Document Number: 002-15055				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	–	05/15/2013	4390-DS100-R: Initial release
*A	–	–	12/05/2013	4390-DS101-R: Updated: • Significant changes throughout the document.
*B	–	–	12/11/2013	4390-DS102-R: Updated: • Figure 1 on page 1 • “General Features” on page 2 • “Power Supply Topology” on page 12 • Figure 3: “Typical Power Topology,” on page 13 • “External 32.768 KHz Low-Power Oscillator” on page 20 • Table 4: “GPIO Port A Alternate Functions,” on page 23 • Figure 9: “WLAN PHY Block Diagram,” on page 35 • Figure 10: “Radio Functional Block Diagram,” on page 36 • “Receiver Path” on page 36 • Table 8: “WLAN MAC Architecture,” on page 30 • Table 9: “WLCSP and FCFBGA Pin Descriptions,” on page 48 • Table 14: “Recommended Operating Conditions and DC Characteristics,” on page 57 • Table 16: “WLAN 2.4 GHz Receiver Performance Specifications,” on page 60 • Table 19: “Core Buck Switching Regulator (CBUCK) Specifications,” on page 65 • Table 20: “LDO3P3 Specifications,” on page 66 • Table 24: “Typical WLAN Power Consumption,” on page 69 • Figure 14: “WLAN = OFF, APPS CPU = OFF,” on page 72 • Figure 15: “WLAN = ON, APPS CPU = OFF,” on page 73 • Figure 16: “WLAN = OFF, APPS CPU= ON,” on page 73 • Figure 18: “WLCSP Keep-Out Areas for PCB Layout —Bottom View, Bumps Facing Up,” on page 76
*C	–	–	02/05/2014	4390-DS103-R: Updated: • “Features” on page 1
*D	5524606	UTSV	11/17/2016	Updated to Cypress template
*E	5705750	AESATMP7	04/21/2017	Updated Cypress Logo and Copyright.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC®Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP | PSoC 6

Cypress Developer Community

Forums | WICED IoT Forums | Projects | Video | Blogs | Training | Components

Technical Support

cypress.com/support

Стандарт Электрон Связь

Мы молодая и активно развивающаяся компания в области поставок электронных компонентов. Мы поставляем электронные компоненты отечественного и импортного производства напрямую от производителей и с крупнейших складов мира.

Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию .

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России , а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

Минимальные сроки поставки, гибкие цены, неограниченный ассортимент и индивидуальный подход к клиентам являются основой для выстраивания долгосрочного и эффективного сотрудничества с предприятиями радиоэлектронной промышленности, предприятиями ВПК и научно-исследовательскими институтами России.

С нами вы становитесь еще успешнее!

Наши контакты:

Телефон: +7 812 627 14 35

Электронная почта: sales@st-electron.ru

Адрес: 198099, Санкт-Петербург, Промышленная ул, дом № 19, литера Н, помещение 100-Н Офис 331