

# XMC4000 Application Kit

For XMC4000 Family

## CPU\_45A-V3

CPU Board XMC4500 General Purpose

## Board User's Manual

Revision 1.0, 2014-01-10

Microcontroller

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## Table of Contents

<b>Introduction</b> .....	<b>7</b>
<b>1 Overview</b> .....	<b>7</b>
1.1 Key Features .....	7
1.2 Block Diagram .....	8
<b>2 Hardware Description</b> .....	<b>9</b>
2.1 Power Supply .....	10
2.2 Reset .....	12
2.3 Clock Generation.....	12
2.4 Boot Option .....	13
2.5 Debug Interface.....	14
2.5.1 On-board USB Debugger.....	14
2.5.2 Cortex Debug Connector (10-pin).....	15
2.5.3 Cortex Debug+ETM Connector (20-pin) .....	16
2.6 Serial Flash Memory .....	18
2.7 USB .....	19
2.8 RTC .....	21
2.9 User LEDs and User Buttons .....	22
2.10 Potentiometer .....	22
2.11 Satellite Connectors .....	23
2.11.1 COM Connector .....	24
2.11.2 HMI Connector .....	25
2.11.3 ACT Satellite Connector.....	26
<b>3 Differences to Board Version V2</b> .....	<b>27</b>
<b>4 Production Data</b> .....	<b>27</b>
4.1 Schematics.....	27
4.2 Component Placement and Geometry.....	32
4.3 Bill of Material (BOM) .....	33

## List of Figures

Figure 1	CPU_45A-V3 Board Block Diagram.....	8
Figure 2	CPU Board XMC4500 General Purpose (CPU_45A-V3).....	9
Figure 3	Powering option through USB interface (5 V).....	10
Figure 4	CPU_45A-V3 Board Power.....	11
Figure 5	Battery (VBAT Supply).....	11
Figure 6	Reset.....	12
Figure 7	Reset LED and Reset Switch.....	12
Figure 8	Clock Generation.....	13
Figure 9	Boot Options Switch.....	13
Figure 10	On-Board USB Debugger.....	14
Figure 11	Cortex Debug Connector (10-pin).....	15
Figure 12	Cortex Debug Connector (10-pin) Layout.....	15
Figure 13	Cortex Debug+ETM Connector (20-pin).....	16
Figure 14	Cortex Debug+ETM Connector (20-pin) Layout.....	17
Figure 15	Quad SPI Flash Interface Circuit.....	18
Figure 16	Quad SPI Flash.....	18
Figure 17	USB Connector Schematic.....	19
Figure 18	USB power generation - Host/OTG mode.....	19
Figure 19	Battery Holder for Coin Cell.....	21
Figure 20	RTC.....	21
Figure 21	GPIO LED.....	22
Figure 22	Satellite Connectors.....	23
Figure 23	Satellite Connector Type COM.....	24
Figure 24	Satellite Connector Type HMI.....	25
Figure 25	Satellite Connector Type ACT.....	26
Figure 26	Schematic of Satellite Connectors, USB-OTG.....	28
Figure 27	Schematic of XMC4500.....	29
Figure 28	Schematic of Power Supply, Debug Connectors, Reset Circuit.....	30
Figure 29	Schematic of On-board Debugger.....	31
Figure 30	Component Placement and Geometry.....	32

## List of Tables

Table 1	Power status LED's .....	10
Table 2	Power Measurement .....	11
Table 3	Boot Options Settings .....	13
Table 4	Cortex Debug Connector (10 Pin) .....	15
Table 5	Cortex Debug+ETM Connector (20 Pin) .....	16
Table 6	Quad SPI Signals .....	18
Table 7	USB micro AB connector Pinout .....	19
Table 8	GPIO LED .....	22
Table 9	User Button .....	22
Table 10	Potentiometer .....	22
Table 11	Differences to older board versions .....	27
Table 12	BOM of CPU_45A-V3 Board .....	33

## Introduction

This document describes the features and hardware details of the CPU Board XMC4500 General Purpose (CPU\_45A-V3) designed to work with Infineon's XMC4500 Microcontroller. This board is part of Infineon's XMC4000 Application Kits.

## 1 Overview

The CPU board CPU\_45A-V3 houses the XMC4500 Microcontroller and three satellite connectors (HMI, COM, ACT) for application expansion. The board along with satellite cards (e.g. HMI\_OLED-V1, COM\_ETH-V1, AUT\_ISO-V1, MOT\_GPDV-V boards) demonstrates the capabilities of XMC4500. The main use case for this board is to demonstrate the generic features of XMC4500 device including tool chain. The focus is safe operation under evaluation conditions. The board is neither cost nor size optimized and does not serve as a reference design.

### 1.1 Key Features

The CPU\_45A-V3 board is equipped with the following features

- XMC4500 (ARM<sup>®</sup> Cortex™-M4-based) Microcontroller, 120 MHz CPU clock, 1 MByte on-chip Flash, 160 kByte RAM, LQFP-144,
- Connection to XMC4500 satellite cards via satellite connectors COM, HMI and ACT
- USB OTG Host/Device support via micro USB connector
- Debug options
  - On-board Debugger via Debug USB connector
  - Cortex Debug connector 10-pin (0.05")
  - Cortex Debug+ETM connector 20-pin (0.05")
- Reset push button
- 32 MBit quad SPI flash memory
- Boot option switch
- PowerScale Connector: Ready for MCU power consumption analysis
- 5 LED's
  - 3 Power indicating LED's
  - 1 User LEDs (P3.9)
  - 1 RESET LED
  - 1 Debug LED
- User Button connected to P2.15
- Potentiometer, connected to analog input P14.1
- Power supply
  - Via Micro-USB connector in USB device mode
  - Via satellite connector pins (COM/ACT satellites cards can supply power to CPU board)
  - Via Debug USB connector
  - RTC backup battery

## 1.2 Block Diagram

Figure 1 shows the functional block diagram of the CPU\_45A-V3 board. For more information about the power supply please refer to chapter 2.1.

The CPU board has got the following building blocks:

- 3 Satellite Connectors (COM, HMI ACT)
- On-board Debugger via Debug USB connector (Micro-USB)
- User LED connected to P3.9
- User Button connected to P2.15
- Quad SPI flash memory (EE) connected to USIC1 Channel1 with Chip-Select1
- 2 Cortex Debug Connectors
- Variable resistor (POTI) connected to GPIO P14.1
- USB On-The-Go Connector (Micro-USB)

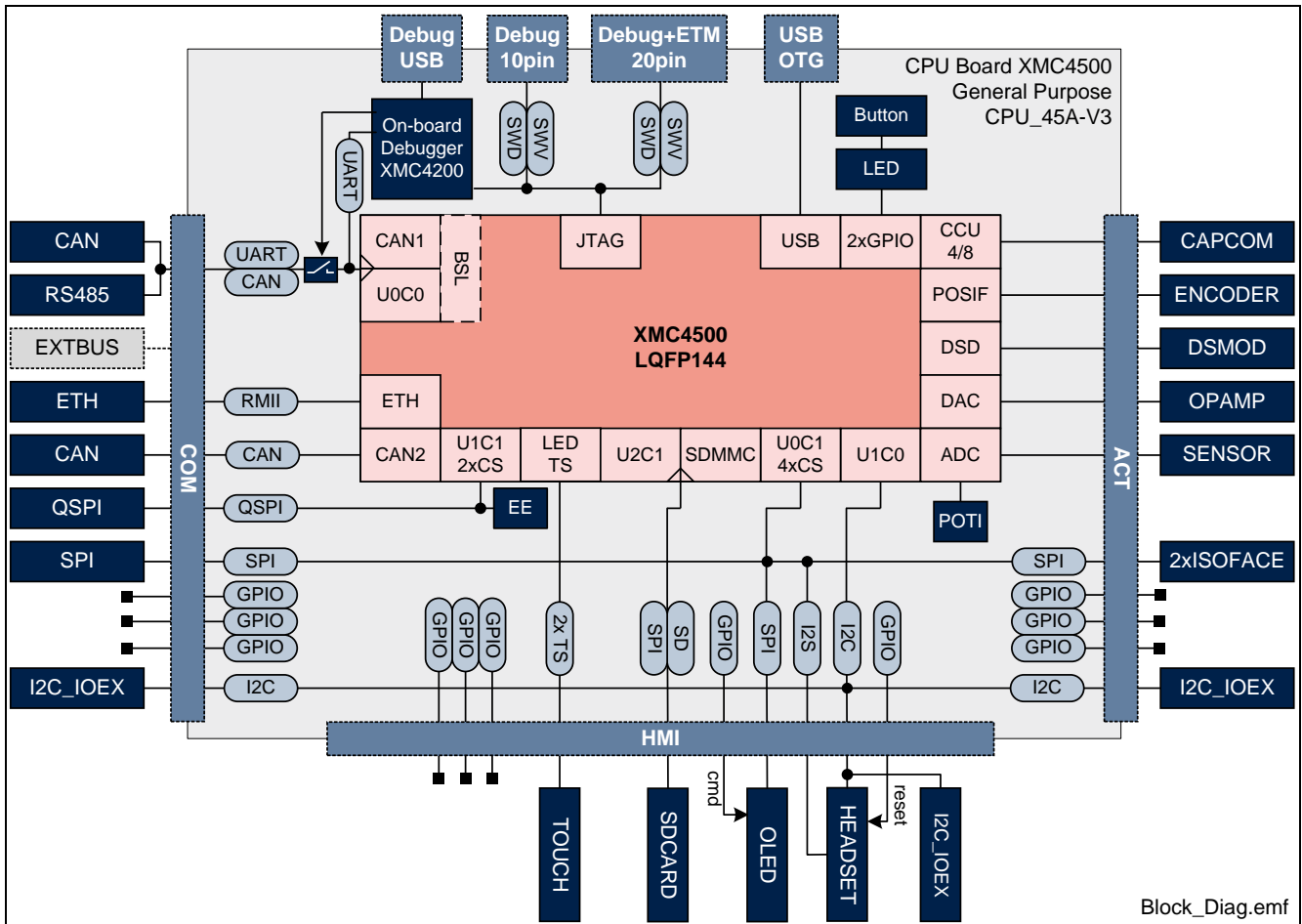


Figure 1 CPU\_45A-V3 Board Block Diagram



## 2 Hardware Description

The following sections give a detailed description of the hardware and how it can be used.

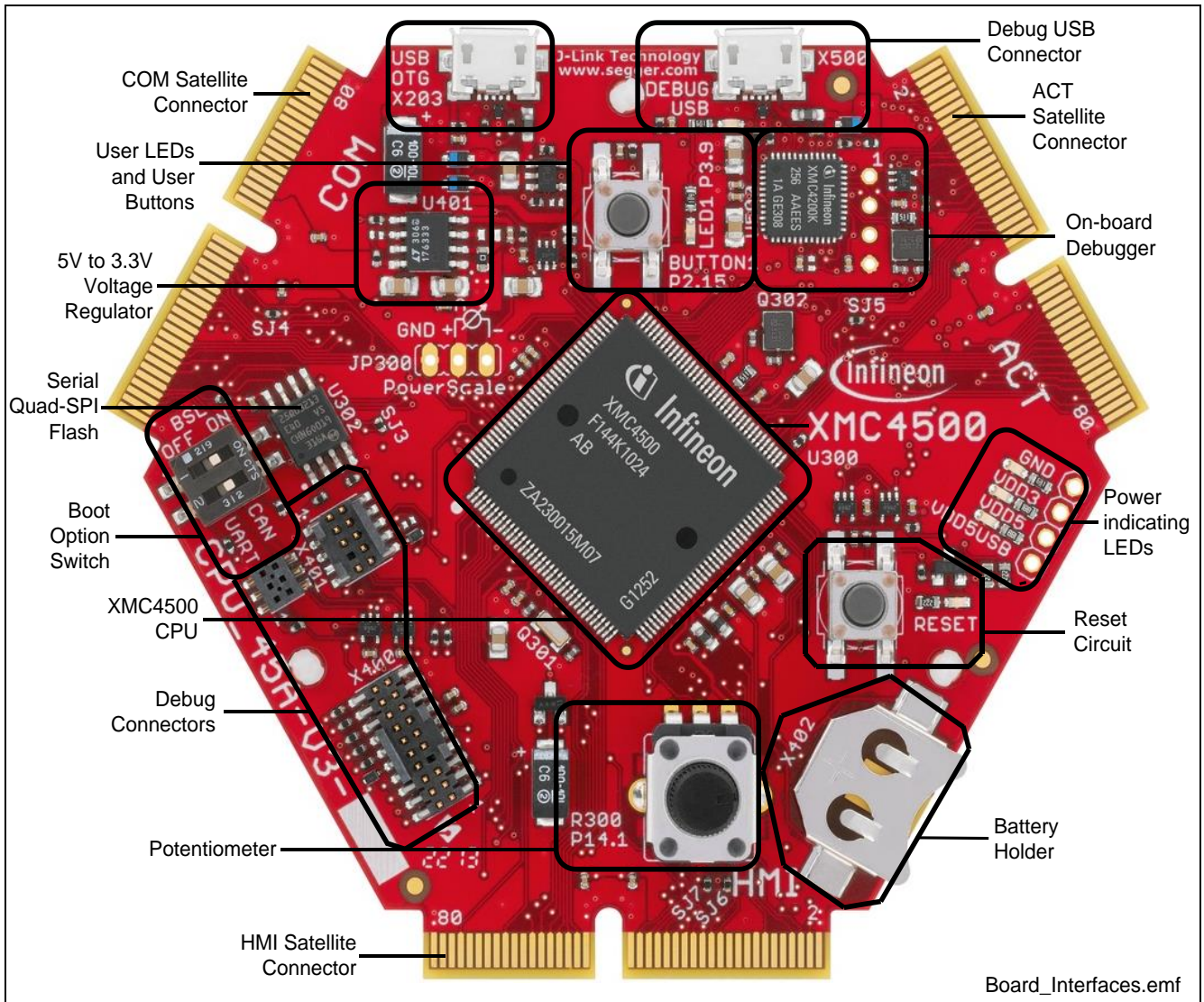


Figure 2 CPU Board XMC4500 General Purpose (CPU\_45A-V3)

## 2.1 Power Supply

The CPU\_45A-V3 board can be powered via the USB plug (5 V); however, there is a current limit that can be drawn from the host PC through USB. If the CPU\_45A-V3 board is used to drive other satellite cards (e.g. AUT\_ISO-V1 or MOT\_GPDLV-V2) and the total current required exceeds 500 mA, then the board needs to be powered by either an external power supply connected to USB or by a satellite card, which supports external power supply like e.g. AUT\_ISO-V1, MOT\_GPDLV-V2, COM\_ETH-V1.

For powering the board through USB interface, connect the USB cable provided with the kit to the Micro-USB connector on board.

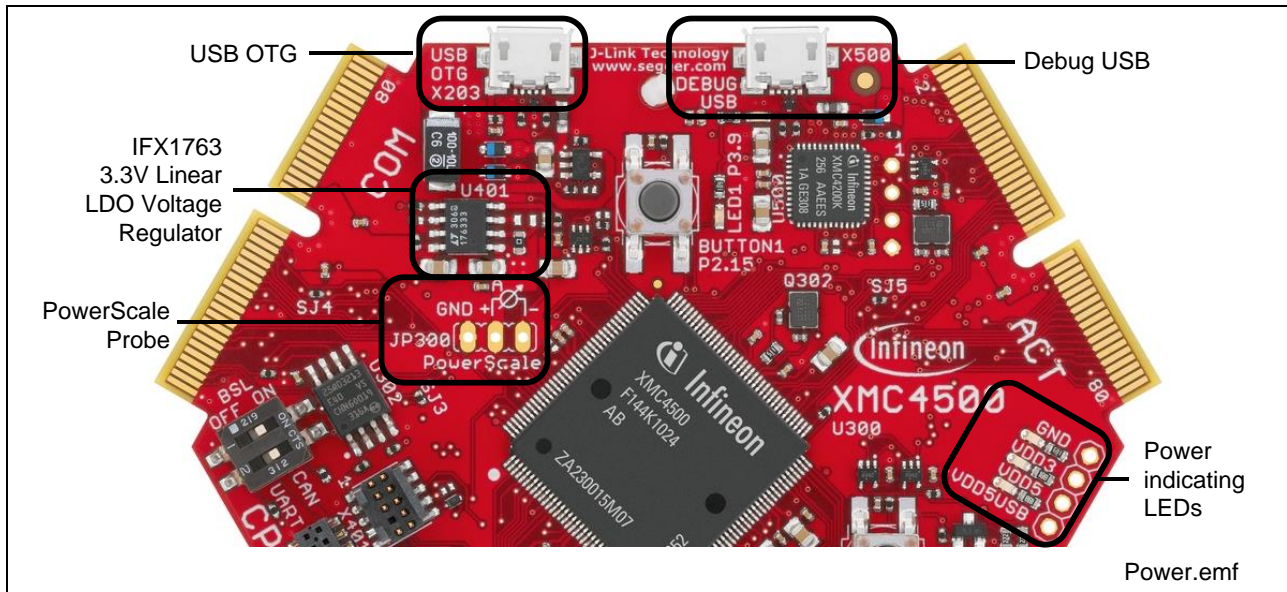


Figure 3 Powering option through USB interface (5 V)

To indicate the power status of CPU\_45A-V3 board three LED's are provided on board (See Figure 3). The LED will be "ON" when the corresponding rail is powered.

Table 1 Power status LED's

LED Reference	Power Rail	Voltage	Note
V401	VDD5	5 V	Must always be "ON"
V402	VDD5USB	5 V	"ON" if powered by USB plug
V403	VDD3.3	3.3 V	Must always be "ON"

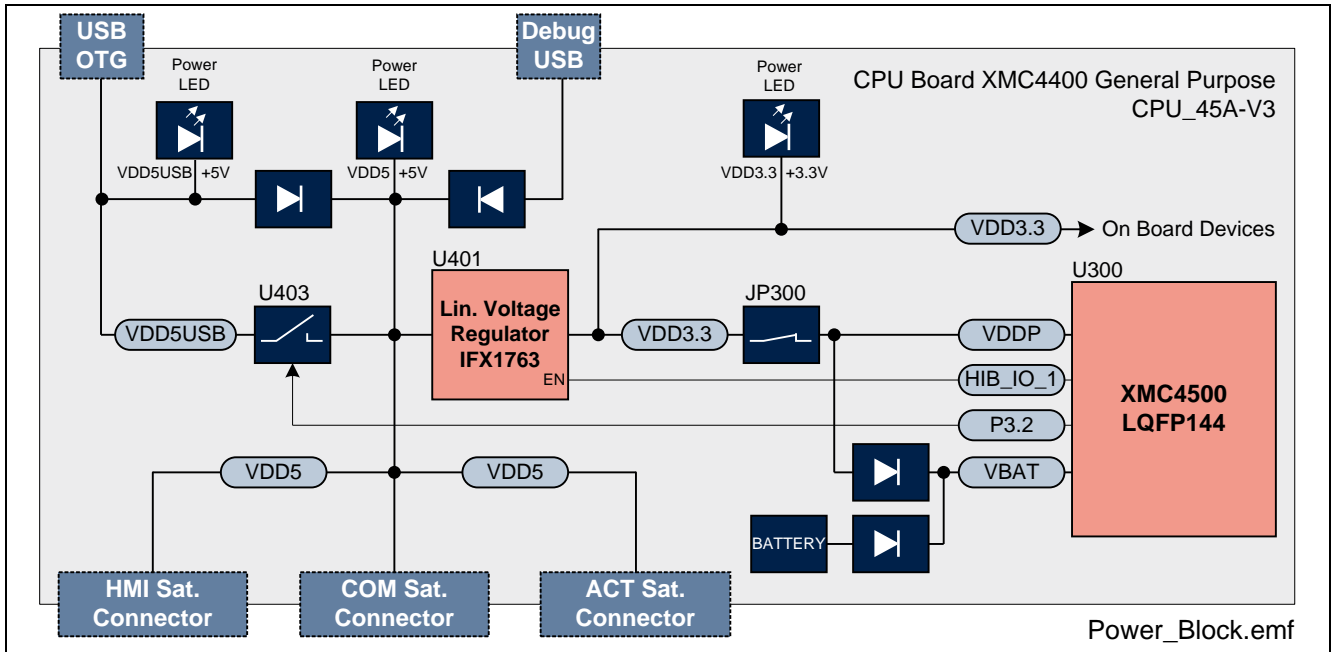


Figure 4 CPU\_45A-V3 Board Power



Figure 5 Battery (VBAT Supply)

Hitex PowerScale probe is provided on the CPU\_45A-V3 board to measure the power consumption.

Table 2 Power Measurement

Jumper	Function	Description
JP300	PowerScale	A Hitex PowerScale probe can be connected for current sensing the VDD3.3 (CPU power source). Default: pos. 1-2 (closed) <i>Note: On the PCB there is a shorting trace between pin 1-2. This trace has to be cut first, before using PowerScale. Pin 3 is GND.</i>

The maximum current drawn by the CPU board without any satellite cards connected is about 150 mA.

## 2.2 Reset

The reset pin (PORST#) of the XMC45000 is a bi-directional pin. An internal pull-up resistor will keep the PORST# pin high during normal operation. A low level at this pin will force a hardware reset. In case of an internal reset the PORST# pin will drive a low signal. An internal circuit of the XMC4500 ensures a save Power-on-Reset. XMC4500 does not require any additional external components to generate a reset signal during power-up. An on-board reset button (SW400, RESET) supports a hardware reset of the CPU during operation. The reset signal is also routed to all satellite connectors. The reset state is indicated by a red LED (V407). The LED will be “ON” during reset state and will be “OFF” during normal operation conditions.

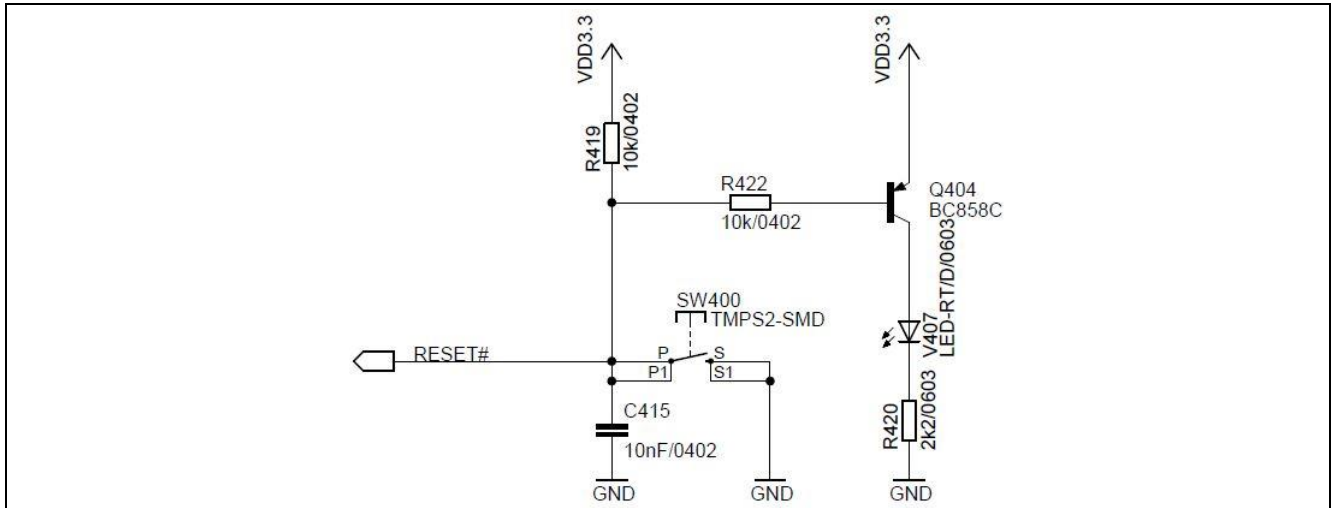


Figure 6 Reset

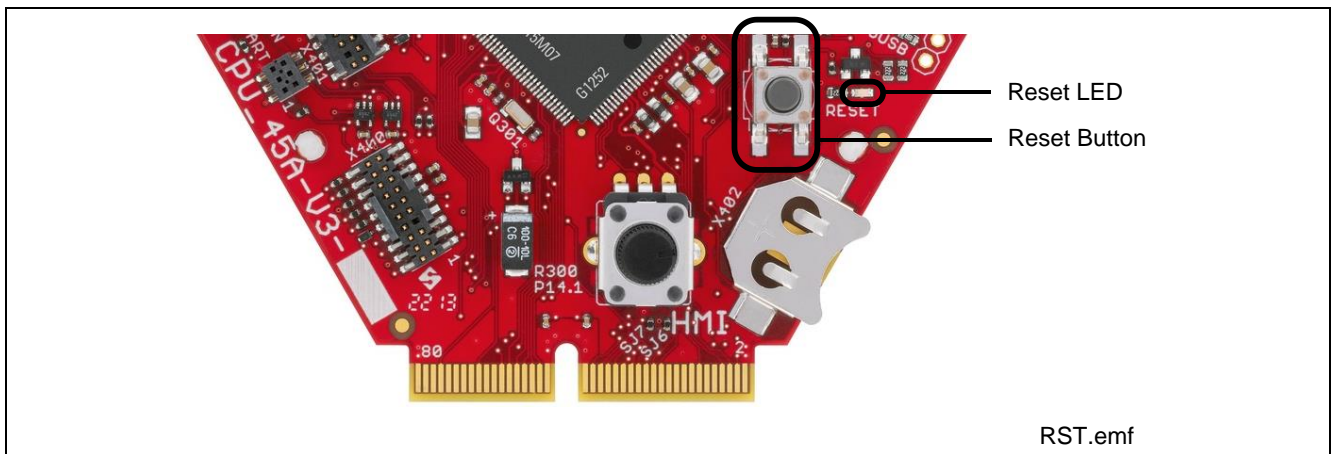


Figure 7 Reset LED and Reset Switch

## 2.3 Clock Generation

An external 12 MHz crystal provides the clock signal to the XMC4500 microcontroller. The drive strength of the oscillator is set to maximum by software, in order to ensure a safe start-up of the oscillator even under worst case conditions. A serial 510 Ohm resistor will attenuate the oscillations during operations.

For the RTC clock a separate external 32.768 kHz crystal is used on board.

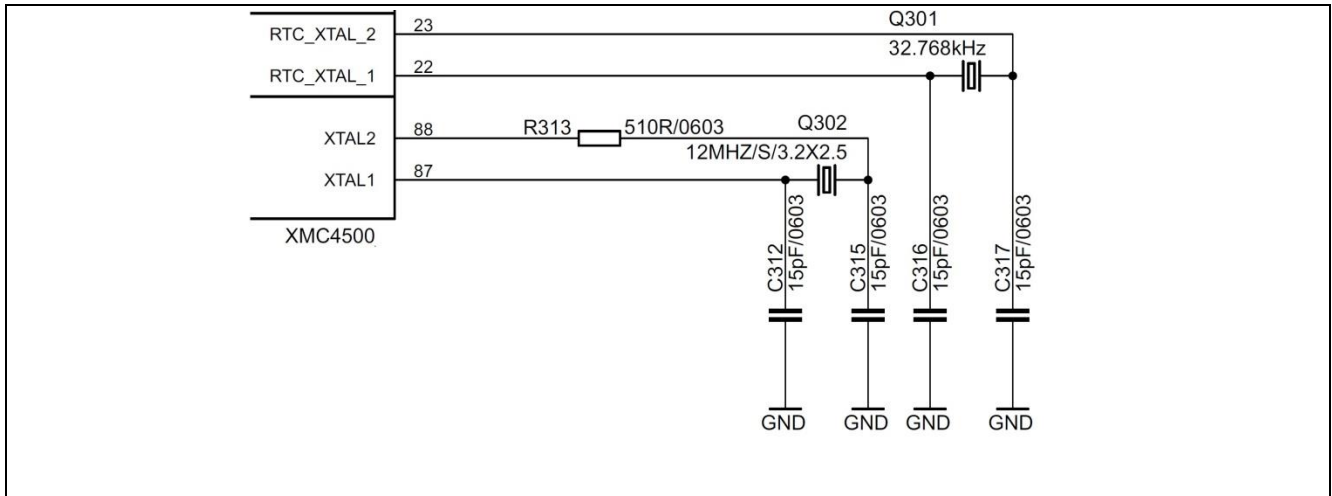


Figure 8 Clock Generation

## 2.4 Boot Option

During power-on-reset the XMC4500 latches the dip switch SW300 settings via the TCK and the TMS pin. Based on the values latched different boot options are possible.

Table 3 Boot Options Settings

BSL (TMS)	CAN/UART (TCK)	Boot Option
OFF (1)	UART (0)	Normal Mode (Boot from flash)
ON (0)	UART (0)	ASC BSL Enabled (Boot from UART)
OFF (1)	CAN (1)	BMI Customized Boot Enabled
ON (0)	CAN (1)	CAN BSL Enabled (Boot from CAN)

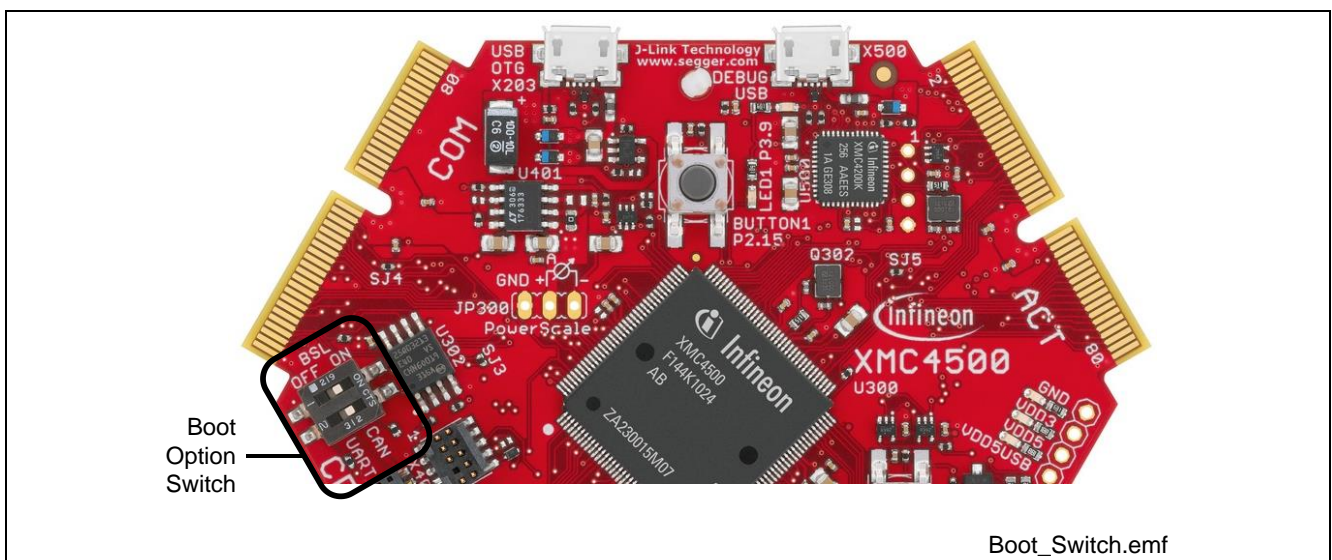


Figure 9 Boot Options Switch

## 2.5 Debug Interface

The CPU\_45A-V3 board supports JTAG debug via 3 different connectors.

- On-board Debugger
- Cortex Debug Connector (10-pin)
- Cortex Debug+ETM Connector (20-pin)

The Hexagon Application Boards are designed to use “Serial Wire Debug” as debug interface. JTAG is not supported by default because the GPIO P0.7 (TDI), where the required TDI function is mapped to, is used by various Actuator boards connected to the ACT satellite connector.

*Note: It is strongly recommended not to use JTAG debug mode, especially if satellites boards are connected, which uses the GPIO 0.7. For the same reason also do not use the on-board debugger in JTAG mode.*

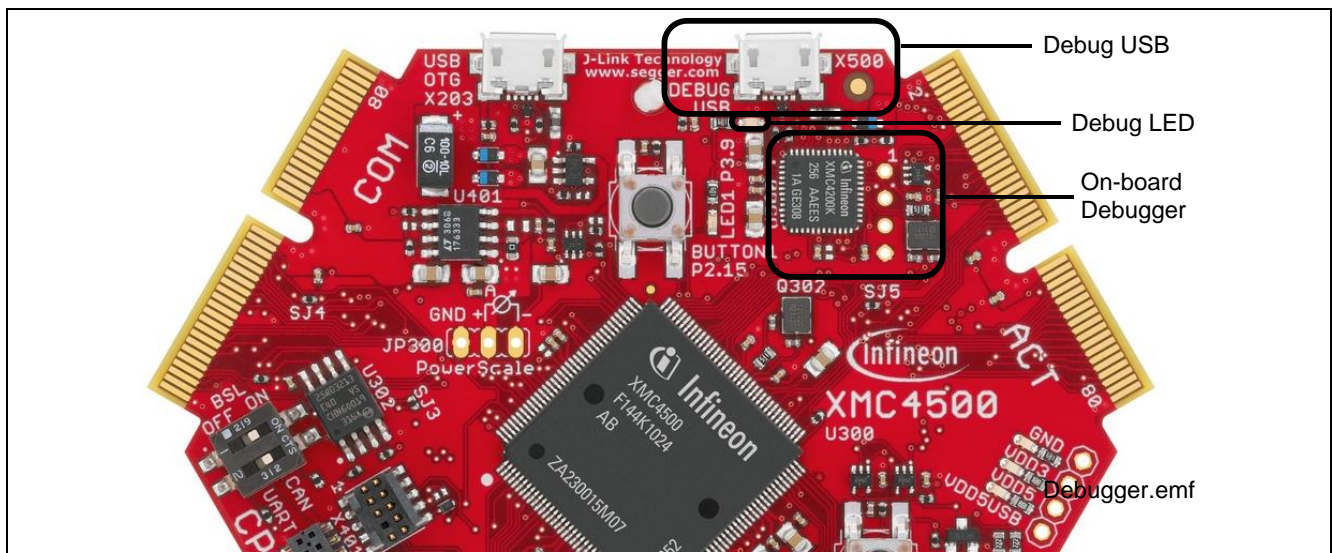
If you want to use the JTAG debug mode through the cortex debug connectors (X400, X401) anyway, enable the JTAG interface of the XMC device by assembling the pull-up resistor R427 (4k7 Ohm) and the resistor R410 (0 - 33 Ohm).

### 2.5.1 On-board USB Debugger

The on-board debugger supports

- Serial Wire Debug
- Serial Wire Viewer
- Full Duplex UART communication via a USB Virtual COM

The on-board debugger can be accessed through the Debug USB connector shown in Figure 10. The Debug LED V502 shows the status during debugging.



**Figure 10 On-Board USB Debugger**

When using an external debugger connected to the 10-pin/20-pin Cortex Debug Connector, the on-board debugger is switched off.

When using the USB virtual COM port function of the on-board debugger the UART interface to the COM satellite is disabled through the switches U301 and U303.

### 2.5.2 Cortex Debug Connector (10-pin)

The CPU\_45A-V3 board supports Serial Wire debug operation and Serial Wire viewer operation (via the SWO signal when Serial Wire debug mode is used) through the 10-pin Cortex Debug Connector.

When using an external debugger connected to the 10-pin Cortex Debug Connector, the on-board debugger is switched off.

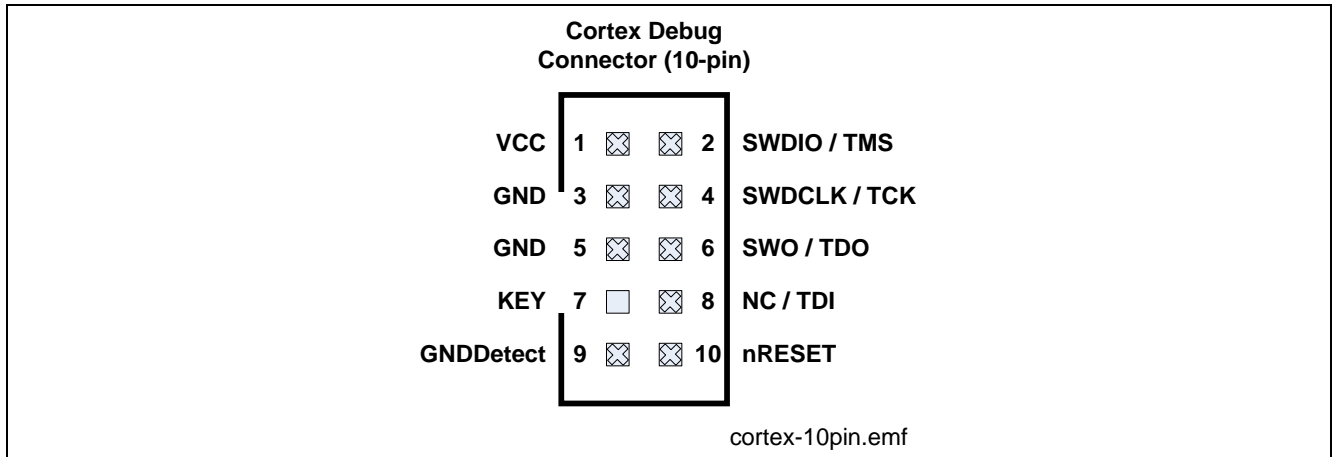


Figure 11 Cortex Debug Connector (10-pin)

Table 4 Cortex Debug Connector (10 Pin)

Pin No.	Signal Name	Serial Wire Debug	JTAG Debug
1	VCC	+3.3 V	+3.3 V
2	SWDIO / TMS	Serial Wire Data I/O	Test Mode Select
3	GND	Ground	Ground
4	SWDCLK / TCK	Serial Wire Clock	Test Clock
5	GND	Ground	Ground
6	SWO / TDO	Trace Data OUT	Test Data OUT
7	KEY	KEY	KEY
8	NC / TDI	Not connected	Test Data IN
9	GNDDetect	Ground Detect	Ground Detect
10	nRESET	Reset (Active Low)	Reset (Active Low)

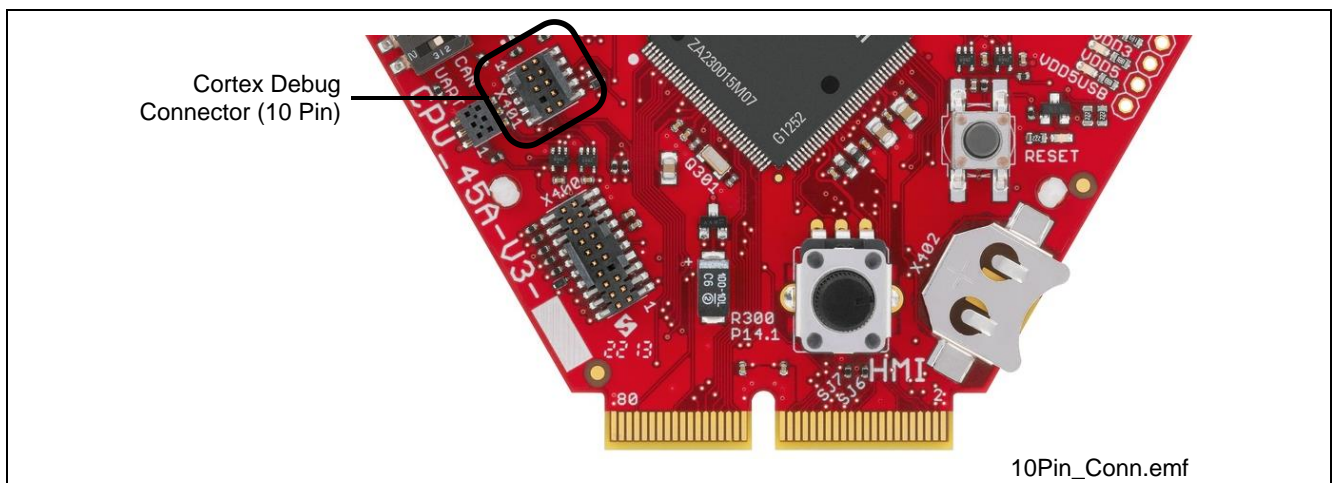


Figure 12 Cortex Debug Connector (10-pin) Layout

### 2.5.3 Cortex Debug+ETM Connector (20-pin)

The CPU\_45A-V3 board supports Serial Wire debug operation, Serial Wire viewer operation (via SWO connection when Serial Wire debug mode is used) and Instruction Trace operation through the 20-pin Cortex Debug+ETM Connector.

JTAG operation additionally would require the TDI (P0.7) signal. By default the TDI signal is disconnected from the Cortex Debug Connectors by a not assembled resistor R410, because the pin P0.7 is used by the Actuator boards connected to the ACT satellite connector.

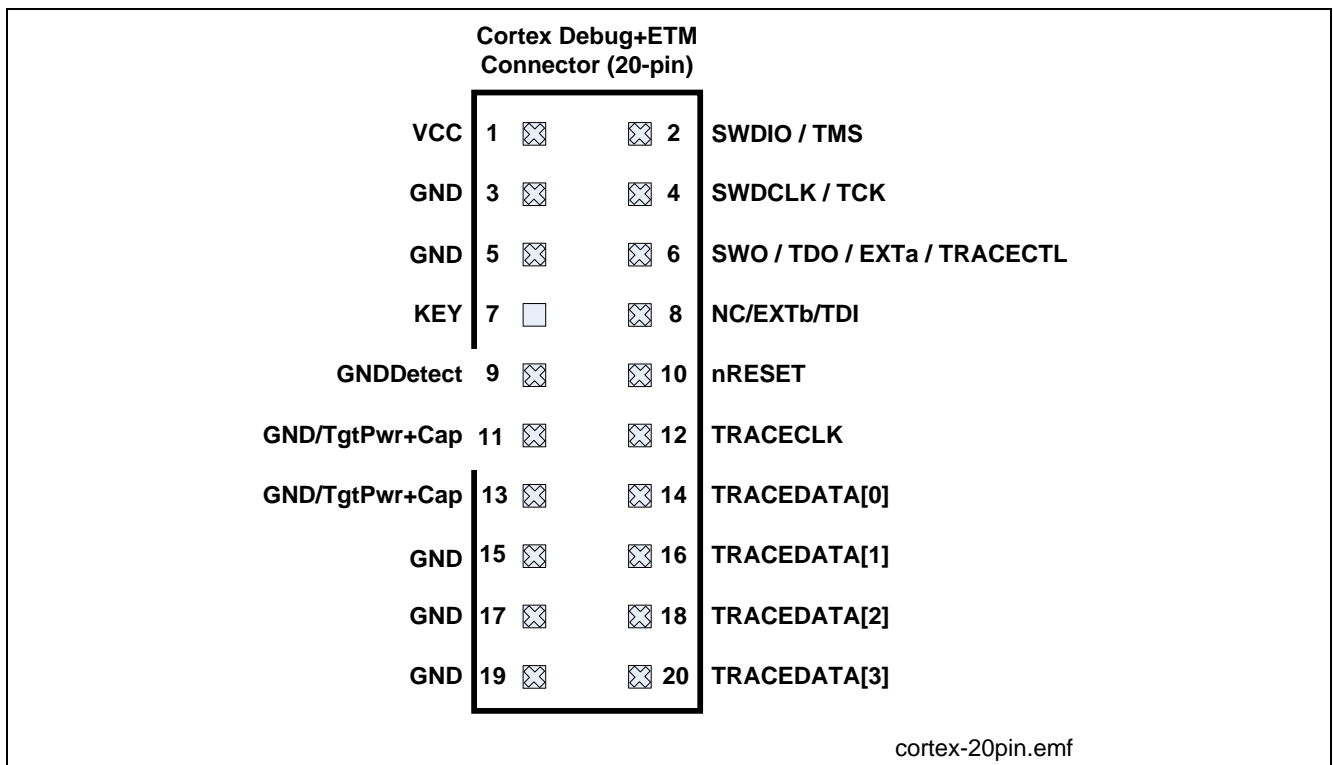


Figure 13 Cortex Debug+ETM Connector (20-pin)

Table 5 Cortex Debug+ETM Connector (20 Pin)

Pin No.	Signal Name	Serial Wire Debug	JTAG Debug
1	VCC	+3.3 V	+3.3 V
2	SWDIO / TMS	Serial Wire Data I/O	Test Mode Select
3	GND	Ground	Ground
4	SWDCLK / TCK	Serial Wire Clock	Test Clock
5	GND	Ground	Ground
6	SWO / TDO	Trace Data OUT	Test Data OUT
7	KEY	KEY	KEY
8	NC / TDI	Not connected	Test Data IN
9	GNDDetect	Ground Detect	Ground Detect
10	nRESET	Reset (Active Low)	Reset (Active Low)
11	GND/TgtPwr+Cap	Ground	Ground
12	TRACECLK	Trace Clock	Trace Clock
13	GND/TgtPwr+Cap	Ground	Ground
14	TRACEDATA[0]	Trace Data 0	Trace Data 0
15	GND	Ground	Ground



**Table 5 Cortex Debug+ETM Connector (20 Pin)**

Pin No.	Signal Name	Serial Wire Debug	JTAG Debug
16	TRACEDATA[1]	Trace Data 1	Trace Data 1
17	GND	Ground	Ground
18	TRACEDATA[2]	Trace Data 2	Trace Data 2
19	GND	Ground	Ground
20	TRACEDATA[3]	Trace Data 3	Trace Data 3



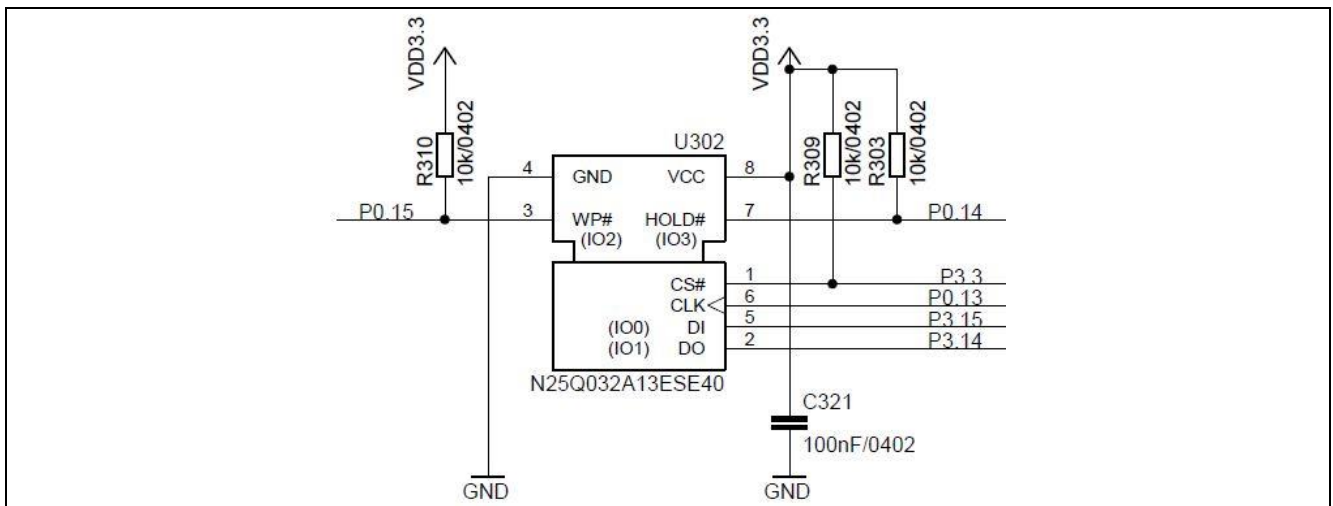
**Figure 14 Cortex Debug+ETM Connector (20-pin) Layout**

## 2.6 Serial Flash Memory

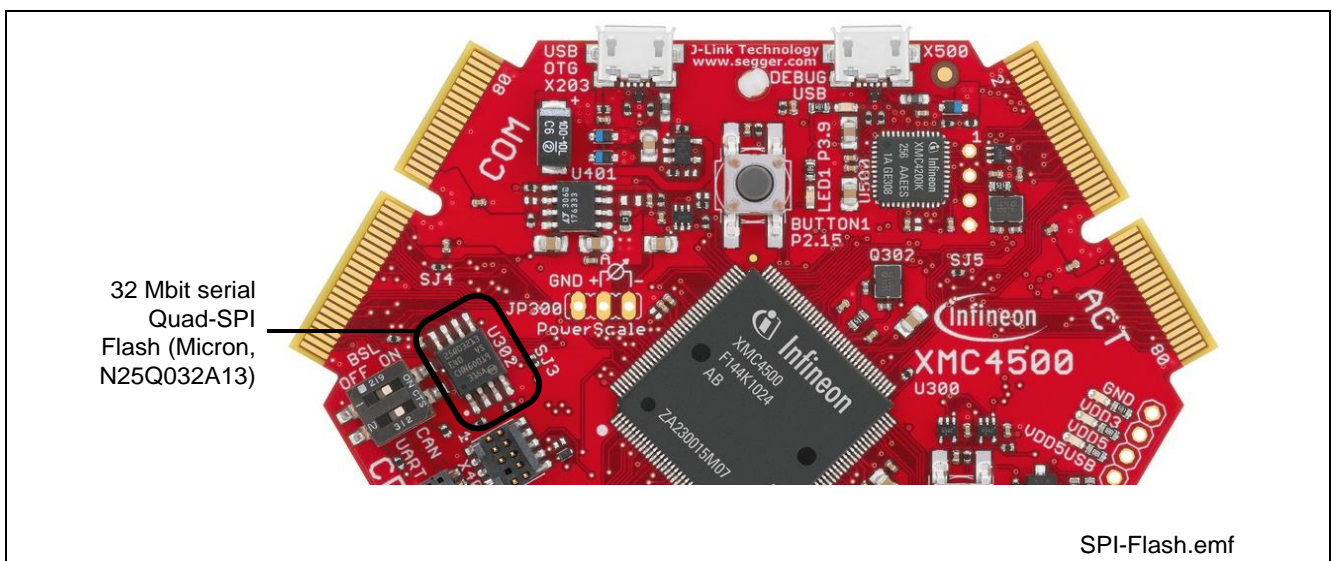
The CPU\_45A-V3 board provides a 32 Mbit serial flash memory from Micron (type: N25Q03) interfaced to XMC4500 through a SPI interface. The SPI interface can be configured as single, dual or quad SPI.

**Table 6 Quad SPI Signals**

Pin No.	Pin Description	Signal Name	Signal Description
P0.13	U1C1_SCLKOUT	CLK	Clock
P3.3	U1C1_SELO1	CS#	Active Low Chip Select
P3.15	U1C1_DOUT0	DI (IO0)	Data Input/Output of Flash (MTRST/MOSI)
P3.14	U1C1_DX0B	DO (IO1)	Data Input/Output of Flash (MRST/MISO )
P0.14	U1C1_HOUT3/DWIN3	HOLD# (IO3)	Data Input/Output
P0.15	U1C1_HOUT2/DWIN2	WP# (IO2)	Data Input/Output



**Figure 15 Quad SPI Flash Interface Circuit**



**Figure 16 Quad SPI Flash**

## 2.7 USB

The XMC4500 supports USB interface in host only mode, device only mode or as an OTG Dual Role Device (DRD). In USB device mode, power is expected through VBUS (pin 1) from an external host (e.g. PC). When the current is more than 500 mA power from an external source through satellite cards shall be used.

*Note: Some PCs, notebooks or hubs have a weak USB supply which is not sufficient for proper supply. In this case use an external 5 Volt power supply or a powered USB hub.*

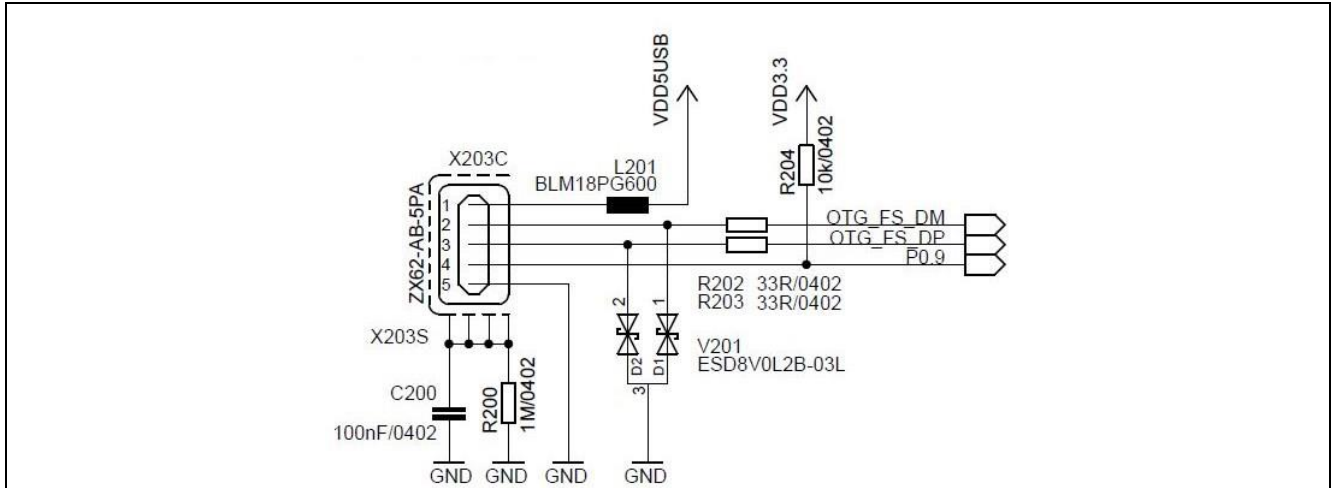


Figure 17 USB Connector Schematic

Port P0.9 of XMC4500 is connected to the USB ID pin (pin 4). An OTG device will detect whether a USB 3.0 Micro-A or Micro-B plug is inserted by checking the ID pin. When the ID = FALSE, Micro-A connector is plugged and when ID = TRUE a Micro-B connector is plugged in. When ID is true the XMC4500 acts as USB host else as USB device.

Table 7 USB micro AB connector Pinout

Pin No.	Pin Name	Pin Description
1	VBUS	5 V
2	D-	Data Minus
3	D+	Data Plus
4	ID	Identification
5	GND	Ground

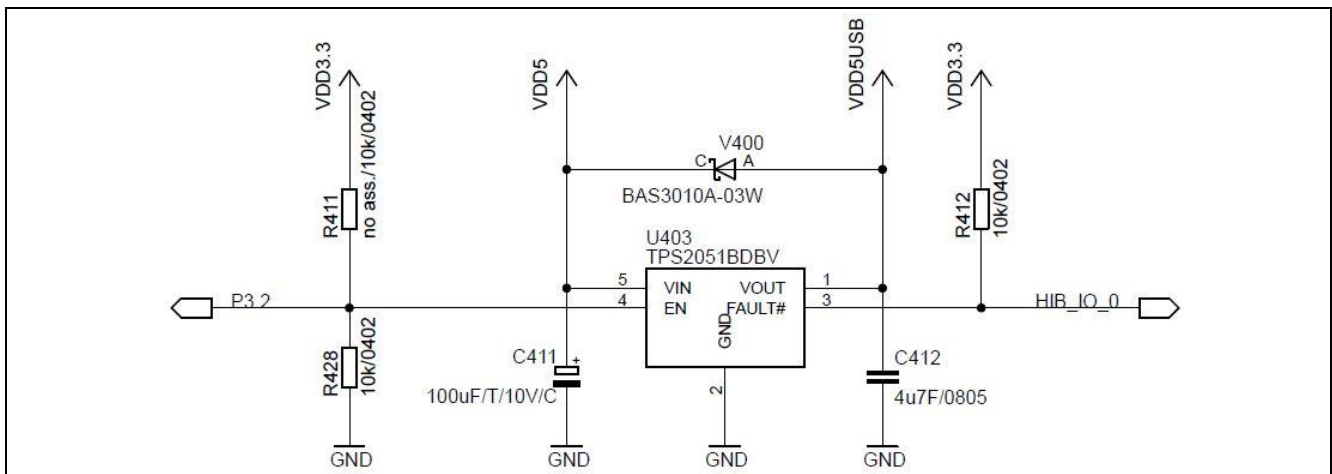


Figure 18 USB power generation - Host/OTG mode

**Hardware Description**

In the host only mode and OTG mode the CPU\_45A-V3 board is capable of supplying power to the connected device (e.g. USB mouse). The board has a power-switch which is controlled by the XMC4500. Port P3.2 (active high) is used for this purpose. In the Host/OTG mode a low active FAULT signal indicates to XMC4500 via HIB\_IO\_0 signal, if more than 500 mA current is drawn by the external device. HIB\_IO\_0 signal is used as general purpose input pin for this implementation.

Diode V400 will allow powering the board through USB in all USB modes via e.g. a PC.

## 2.8 RTC

The XMC4400 CPU has two power domains, the Core Domain and Hibernate Domain. The Core Domain (VDDP pins) is connected to the VDD3.3 rail. An on-board LDO voltage regulator generates VDD3.3 (3.3 V) from VDD5 (5 V).

The Hibernate Domain is powered via the auxiliary supply pin VBAT, which is supplied by either a 3 V coin cell (size 1216, 1220, 1225) plugged into the battery holder (see Figure 19) or 3.3 V (VDD3.3) generated by the on-board voltage regulator.



Figure 19 Battery Holder for Coin Cell

The Real Time Clock (RTC) is located in the hibernate domain. The XMC4500 uses the HIB\_IO\_1 signal (active low) to shut down the external LDO voltage regulator which generates the VDD3.3 (Core Domain). Even if the Core Domain is not powered the Hibernate Domain will operate if VBAT is available. The RTC keeps running as long as the Hibernate Domain is powered via the auxiliary supply VBAT. The RTC is capable to wake-up the whole system from Hibernate mode by setting HIB\_IO\_1 to high.

With VDD3.3 power supply switched off and no coin cell supply the power in the capacitor connected to VBAT will provide power to the hibernate domain for about 10 seconds (depending on which features in the hibernate domain are enabled).

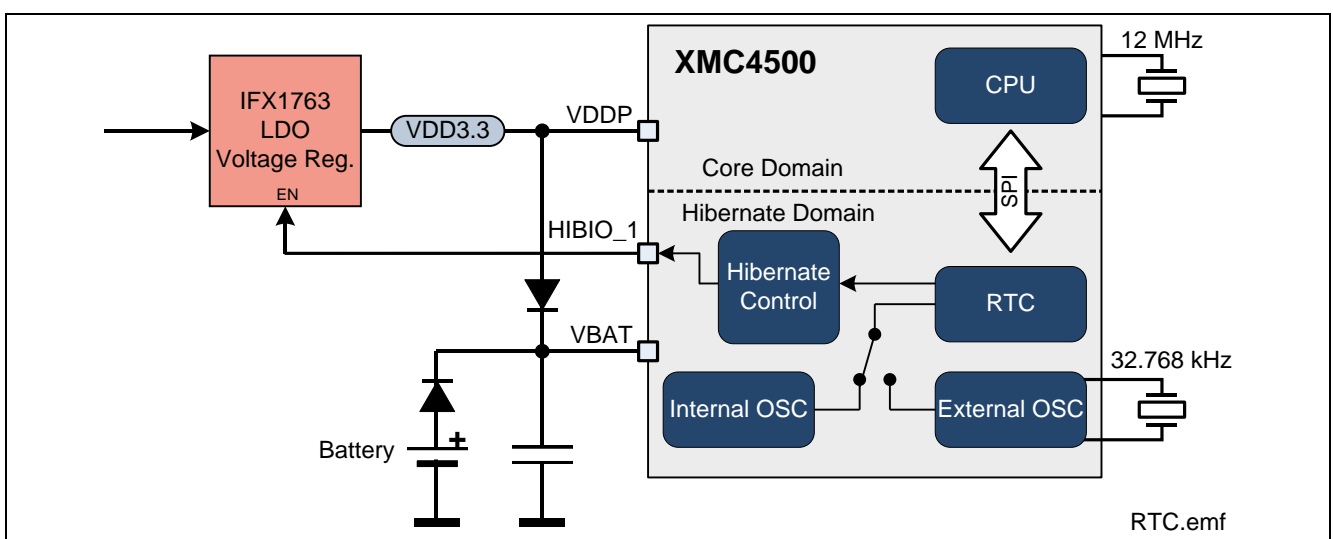


Figure 20 RTC

## 2.9 User LEDs and User Buttons

The port pin P3.9 of XMC4500 is connected to a LED V300. More user LED's are available through I2C GPIO expander on most of the satellite cards.

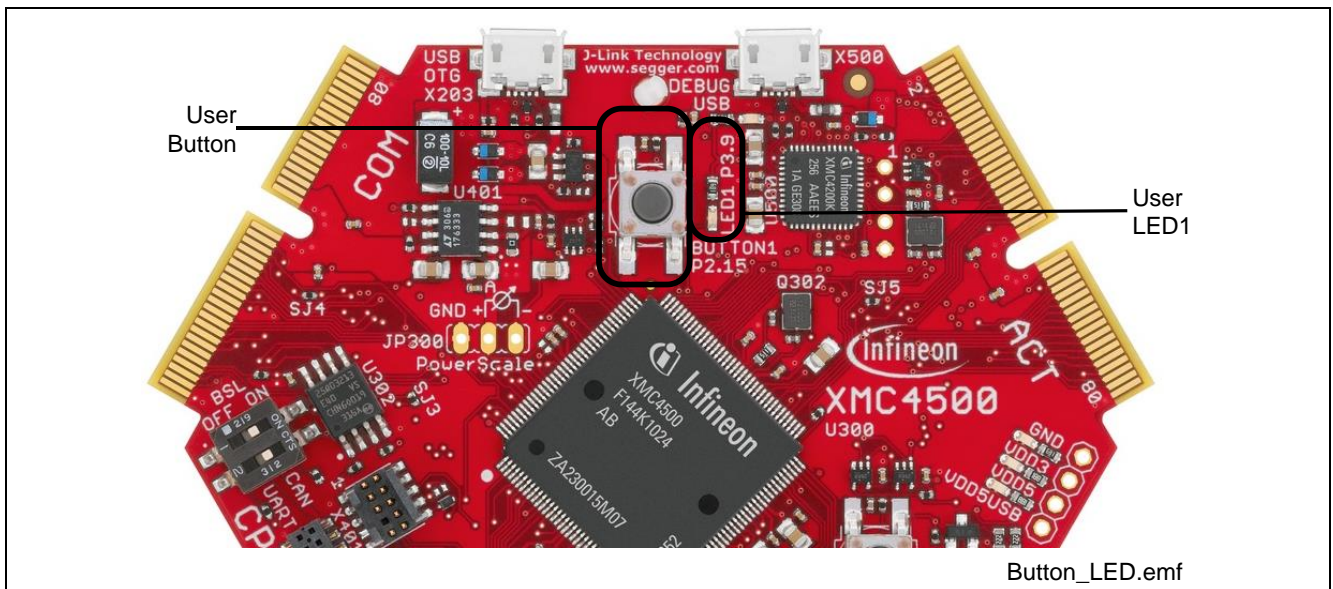
**Table 8 GPIO LED**

LED	Connected to Port Pin
V300	GPIO P3.9

The User Button is connected to port pin P2.15 of the XMC4500.

**Table 9 User Button**

Button	Connected to Port Pin
BUTTON1	P2.15



**Figure 21 GPIO LED**

## 2.10 Potentiometer

The CPU\_45A-V3 board provides a potentiometer POT1 for ease of use and testing of the on-chip analog to digital converter. The potentiometer is connected to the analog input G0\_CH1 (P14.1). The analog output of the potentiometer ranges from 0 V to 3.3 V.

**Table 10 Potentiometer**

R300	P14.1 / G0_CH1 (Group 0, Channel 1)
------	-------------------------------------

## 2.11 Satellite Connectors

The CPU\_45A-V3 board provides three satellite connectors for application extension by satellite cards:

- COM satellite connector (Communication)
- HMI satellite connector (Human Machine Interface)
- ACT satellite connector (Actuator)

*Note: Satellite cards shall be connected to their matching satellite connectors only. (For e.g. COM satellite cards shall be connected to COM satellite connector only)*

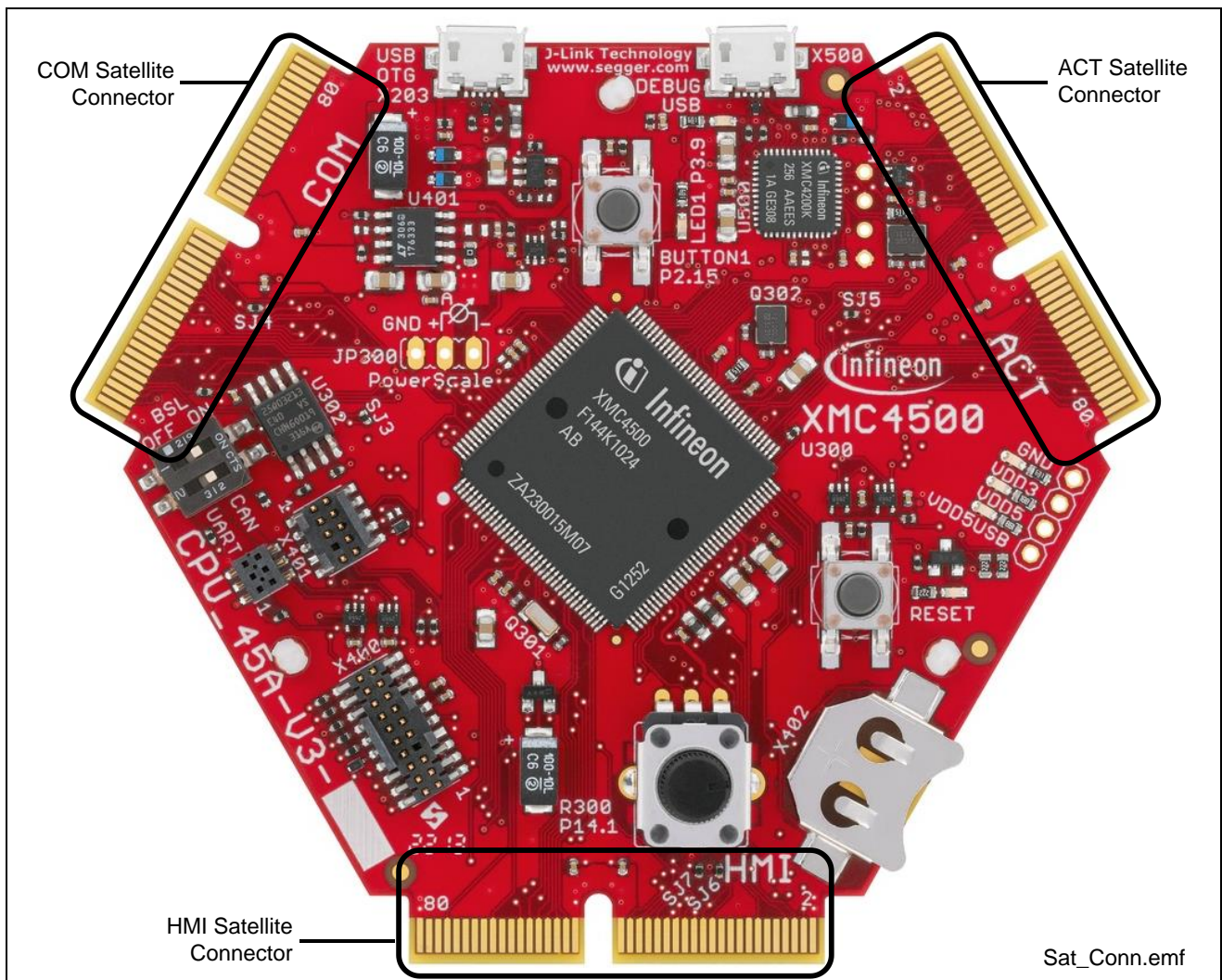


Figure 22 Satellite Connectors

### 2.11.1 COM Connector

The COM satellite connector on the CPU\_45A-V3 board allows interface expansion through COM satellite cards (e.g. COM\_ETH-V1)

CPU_45A-V3		Satellite Connector		CPU_45A-V3	
XMC Pin	XMC Function	Pin	Function	XMC Pin	XMC Function
VSS	GND	COM	GND	VSS	GND
P0.13	U1C1_SCLKOUT	2	qSPI_D0	P3.15	P3.15
P0.12	U1C1_SELO0	3	qSPI_D1	P3.14	P3.14
P3.3	U1C1_SELO1	5	qSPI_D2	P0.15	P0.15
nc	nc	7	qSPI_D3	P0.14	P0.14
nc	nc	9	RSVD	nc	nc
nc	nc	11	RSVD	nc	nc
P2.3	ETH0_RXD1A	12	ETH_RMII	ETH0_TXD1	P2.9
P2.2	ETH0_RXD0A	13	ETH_RMII	ETH0_TXD0	P2.8
P2.0	ETH0_MDO	14	ETH_RMII	ETH0_CRS_DVC	P15.9
P2.7	ETH0_MDC	15	ETH_RMII	ETH0_RXERD	P5.3
P5.9	ETH0_TX_EN	16	ETH_RMII	ETH0_CLK_RMIIC	P15.8
nc	nc	17	ETH_RMII	GND	VSS
P3.10	P3.10	18	RSVD	nc	nc
P1.4 (β)	U0C0_DX0B	19	ASC_DIR	CAN_N2_TXD	P1.9
P1.5 (β)	U0C0_DOUT0	20	ASC_RXD	CAN_N2_RXDA	P1.8
P5.5	P5.5	21	ASC_TXD	U0C1_DOUT0	P3.13
P3.1	U0C1_SELO0	22	SPI_CSC0	U0C1_DX0B	P2.5
nc	nc	23	SPI_CSC1	U0C1_SCLKOUT	P3.0
P2.14	U1C0_DOUT0/DX0B	24	SPI_CSC2	U1C0_SCLKOUT	P5.8
P14.13	P14.13	25	I2C_SDA	P0.6	P0.6
P3.7	P3.7	26	COM_GPIO1	RESET#	PORST
		27	COM_GPIO0		
		28	VDD5		
		29	VDD5		
		30	VDD5		
		31	VDD5		
		32	VDD5		
		33	VDD5		
		34	VDD5		
		35	VDD5		
		36	VDD5		
		37	VDD5		
		38	VDD5		
		39	VDD5		
		40	VDD5		
		41	VDD5		
		42	VDD5		
		43	VDD5		
		44	VDD5		
		45	VDD5		
		46	VDD5		
		47	EBU_ADV	nc	nc
		48	EBU_WR	nc	nc
		49	EBU_RD	nc	nc
		50	EBU_BC	nc	nc
		51	EBU_CS	nc	nc
		52	EBU_CS	nc	nc
		53	EBU_CS	nc	nc
		54	EBU_CS	nc	nc
		55	EBU_CS	nc	nc
		56	EBU_CS	nc	nc
		57	EBU_CS	nc	nc
		58	EBU_CS	nc	nc
		59	EBU_CS	nc	nc
		60	EBU_CS	nc	nc
		61	GND	nc	nc
		62	EBU_A	nc	nc
		63	EBU_A	nc	nc
		64	EBU_A	nc	nc
		65	EBU_A	nc	nc
		66	EBU_A	nc	nc
		67	EBU_A	nc	nc
		68	EBU_A	nc	nc
		69	EBU_A	nc	nc
		70	EBU_A	nc	nc
		71	EBU_A	nc	nc
		72	EBU_A	nc	nc
		73	EBU_A	nc	nc
		74	EBU_A	nc	nc
		75	EBU_A	nc	nc
		76	EBU_A	nc	nc
		77	EBU_A	nc	nc
		78	EBU_A	nc	nc
		79	GND	GND	VSS
		80	GND		
		COM	GND		

Figure 23 Satellite Connector Type COM

(3) This pin is connected with the satellite connector via an analog switch



### 2.11.2 HMI Connector

The HMI satellite connector on the CPU\_45A-V3 board allows interface expansion through HMI satellite cards.

CPU_45A-V3		Satellite Connector		CPU_45A-V3	
XMC Pin	XMC Function	Function	Pin	Function	XMC Pin
VSS	GND	GND	1	GND	VSS
P3.6	MMC_CLK_OUT	MMC_CLK	2	MMC_nRST	P0.11
P1.6	MMC_DATA1_OUT	MMC_DATA1	4	MMC_DATA0	P4.0
P4.1	MMC_DATA3_OUT	MMC_DATA3	8	MMC_DATA2	P1.7
nc	nc	MMC_DATA5	10	MMC_DATA4	nc
nc	nc	MMC_DATA7	12	MMC_DATA6	nc
VSS	GND	MMC_BUSPOW	13	MMC_CMD	P3.5
nc	nc	MMC_nSDCD	15	MMC_LED	VSS
nc	nc	RSVD	17	MMC_SDWC	nc
nc	nc	RSVD	19	RSVD	nc
nc	nc	RSVD	21	RSVD	nc
P2.10	P2.10	AudioRST	23	OLED_CMD	P5.11
P3.1	U0C1_SELO0	I2S_WA	25	I2S_MTSR	U0C1_DOUT0
nc	nc	I2S_MCLK	27	I2S_MIRST	U0C1_DX0B
nc	nc	I2S_SYNCCLK	29	I2S_SCLK	U0C1_SCLKOUT
P3.12	U0C1_SELO1	SPI_CSH0	31	SPI_MTSR	U0C1_DOUT0
P3.1	U0C1_SELO0	SPI_CSH1	33	SPI_MIRST	U0C1_DX0B
P3.8	U0C1_SELO3	SPI_CSH2	35	SPI_SCLK	U0C1_SCLKOUT
P2.14	U1C0_DX0D/DOUT0	I2C_SDA	37	I2C_SCL	U1C0_SCLKOUT
P15.5	P15.5 Input	HMI_GPIO1	39	GPIO	P0.6
P5.6	P5.6	HMI_GPIO0	41	RESET	PORST
		VDD5	43	VDD5	
		VDD5	45	VDD5	
VAGND	AGND	AGND	46	VDD5	VAREF
P14.9	VADC_G1CH1	DAC1/ADC1	47	AREF	VAREF
P14.6	VADC_G0CH6	ADC3/ORC0	49	DAC0/ADC0	VADC_G1CH0
P14.12	VADC_G1CH4	ADC15	51	ADC2/DACREF	VADC_G0CH4
P15.13	VADC_G3CH5	ADC17	53	ADC14	VADC_G0CH4
P15.12	VADC_G3CH4	ADC19	55	ADC16	VADC_G0CH3
nc	nc	RSVD	57	ADC18	VADC_G2CH2
nc	nc	RSVD	59	RSVD	nc
nc	nc	RSVD	61	RSVD	nc
nc	nc	RSVD	63	RSVD	nc
nc	nc	TPx1	65	TP7	LEDTS0_TSIN7A
nc	nc	TPx0	67	TP6	nc
nc	nc	COL3	69	TP5	nc
nc	nc	COL2	71	TP4	nc
nc	nc	COL1	73	TP3	nc
P0.10	LEDTS0_COL1	COL0	75	TP2	nc
P5.7	LEDTS0_COLA	COLA	77	TP1	LEDTS0_TSIN2A
VSS	GND	GND	79	TP0	nc
		GND	80	GND	VSS

Figure 24 Satellite Connector Type HMI

### 2.11.3 ACT Satellite Connector

The ACT satellite connector on the CPU\_45A-V3 board allows interface expansion through ACT satellite cards.

CPU_45A-V3		XMC Function		XMC Pin	
Satellite Connector		Function	Pin	Function	
CPU_45A-V3		XMC Function		XMC Pin	
<b>ACT</b>					
VSS	GND	GND	1	GND	VSS
nc	nc	PIF1INO	2	PIF0IN1	P1.3
nc	nc	PIF1INI1	3	PIF0IN2	P1.2
nc	nc	PIF1IN2	4	PIF0IN3	P1.1
P1.0	DSD_PWMN	PWMN	5	DSDINO	P0.8 (2)
P5.1	DSD_PWMN	PWMP	6	DSDINI1	P2.6
P1.7	DSD_MCLK2A	DSDCLK0	7	DSDIN2	P1.6
P3.4	DSD_MCLK3B	DSDCLK1	8	DSDIN3	P6.5 (3)
nc	nc	RSVD	9	RSVD	nc
P4.3	CCU43_IN3A	CC_IN3	10	CC_IN0	P4.6
P5.2	CCU81_IN1B	CC_IN4	11	CC_IN1	P4.5
P5.4	CCU81_IN3B	CC_IN5	12	CC_IN2	P4.4
P0.7 (1)	CCU80_IN0A	TRAP_A	13	ENA_A	P2.13
P5.0	CCU81_IN0A/1A/2A/3A	TRAP_B	14	ENA_B	P2.12
P4.7	CCU43_IN0C	TRAP_X	15	ENA_X	P6.4
P3.11	U0C1_SELO2	SPL_CSA0	16	SPL_MTRST	P3.13
P3.8	U0C1_SELO3	SPL_CSA1	17	SPL_MTRST	P2.5
nc	nc	SPL_CSA2	18	SPL_SCLK	P3.0
P2.14	U1CO_DX0D/DOUT0	I2C_SDA	19	I2C_SCL	P5.8
P15.4	P15.4 Input	ACT_GPI01	20	GPI0	P0.6
P4.2	P4.2	ACT_GPI00	21	RESET	PORST
		VDD5	22	VDD5	
		VDD5	23	VDD5	
<b>ACT</b>					
VAGND	AGND	VDD5	46	VDD5	VAREF
P14.9	VADC_G1CH1	AGND	47	AREF	VAREF
P14.6	VADC_G0CH6	DAC1/ADC1	48	DAC0/ADCO	P14.8
P14.7	VADC_G0CH7	ADC3/ORCO	49	ADC2/DACREF	P14.4
P14.0	VADC_G0CH0	ADC5/ORC2	50	ADC4/ORC1	P14.4
P14.5	VADC_G2CH1	ADC7	51	ADC6/ORC3	P14.15
P15.14	VADC_G3CH6	ADC9	52	ADC8	P14.2
P15.15	VADC_G3CH7	ADC11	53	ADC10	P15.6
P1.15	CCU81_OUT00	PWMB0_H	54	ADCI2	P15.7
P1.12	CCU81_OUT01	PWMB0_L	55	PWMMA0_H	P0.5
P1.14	CCU81_OUT10	PWMB1_H	56	PWMMA0_L	P0.2
P1.11	CCU81_OUT11	PWMB1_L	57	PWMMA1_H	P0.4
P1.13	CCU81_OUT20	PWMB2_H	58	PWMMA1_L	P0.1
P1.10	CCU81_OUT21	PWMB2_L	59	PWMMA2_H	P0.3
P6.0 (3)	CCU81_OUT31	PWMX2	60	PWMMA2_L	P0.0
P6.1 (3)	CCU81_OUT30	PWMX3	61	PWMX0	P6.3
VSS	GND	GND	76	PWMX1	P6.2
		VDD5	77	GND	VSS
		VDD5	78	VDD5	
		VDD5	79	VDD5	
		VDD5	80	VDD5	
		VDD5	81	VDD5	
		VDD5	82	VDD5	
		VDD5	83	VDD5	
		VDD5	84	VDD5	
		VDD5	85	VDD5	
		VDD5	86	VDD5	
		VDD5	87	VDD5	
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		VDD5	89	VDD5	
		VDD5	90	VDD5	
		VDD5	91	VDD5	
		VDD5	92	VDD5	
		VDD5	93	VDD5	
		VDD5	94	VDD5	
		VDD5	95	VDD5	
		VDD5	96	VDD5	
		VDD5	97	VDD5	
		VDD5	98	VDD5	
		VDD5	99	VDD5	
		VDD5	100	VDD5	

Figure 25 Satellite Connector Type ACT

- (1) P0.7 can also be used for JTAG Debugging (TDI)
- (2) P0.8 is used as TRST in order to enable JTAG Debug
- (3) This pin is connected with the satellite connector via an analog switch

### 3 Differences to Board Version V2

**Table 11 Differences to older board versions**

Topic of Change	Description
Debugger	An on-board debugger has been added. The debugger has an USB interface (X500). An external debugger can still be used via X400 / X401.
User Push Button	A user button as been added. The user button is connected to P2.15. In V2 versions P2.15 was connected to P2.14.
I2C Connection	The SDA signal of the I2C is connected to P2.14 only. In V2 versions the SDA signal was connected to P2.14 and P2.15.
USB Shielding	The USB shield has been connected to ground through a 1 MOhm resistor and a 100 nF capacitor

## 4 Production Data

### 4.1 Schematics

This chapter contains the schematics for the CPU board:

- Schematic of Satellite Connectors, USB-OTG
- Schematic of XMC4500
- Schematic of Power Supply, Debug Connectors, Reset Circuit
- Schematic of On-board Debugger

The board has been designed with Eagle. The PCB design data of this board can be downloaded from [www.infineon.com/xmc-dev](http://www.infineon.com/xmc-dev).

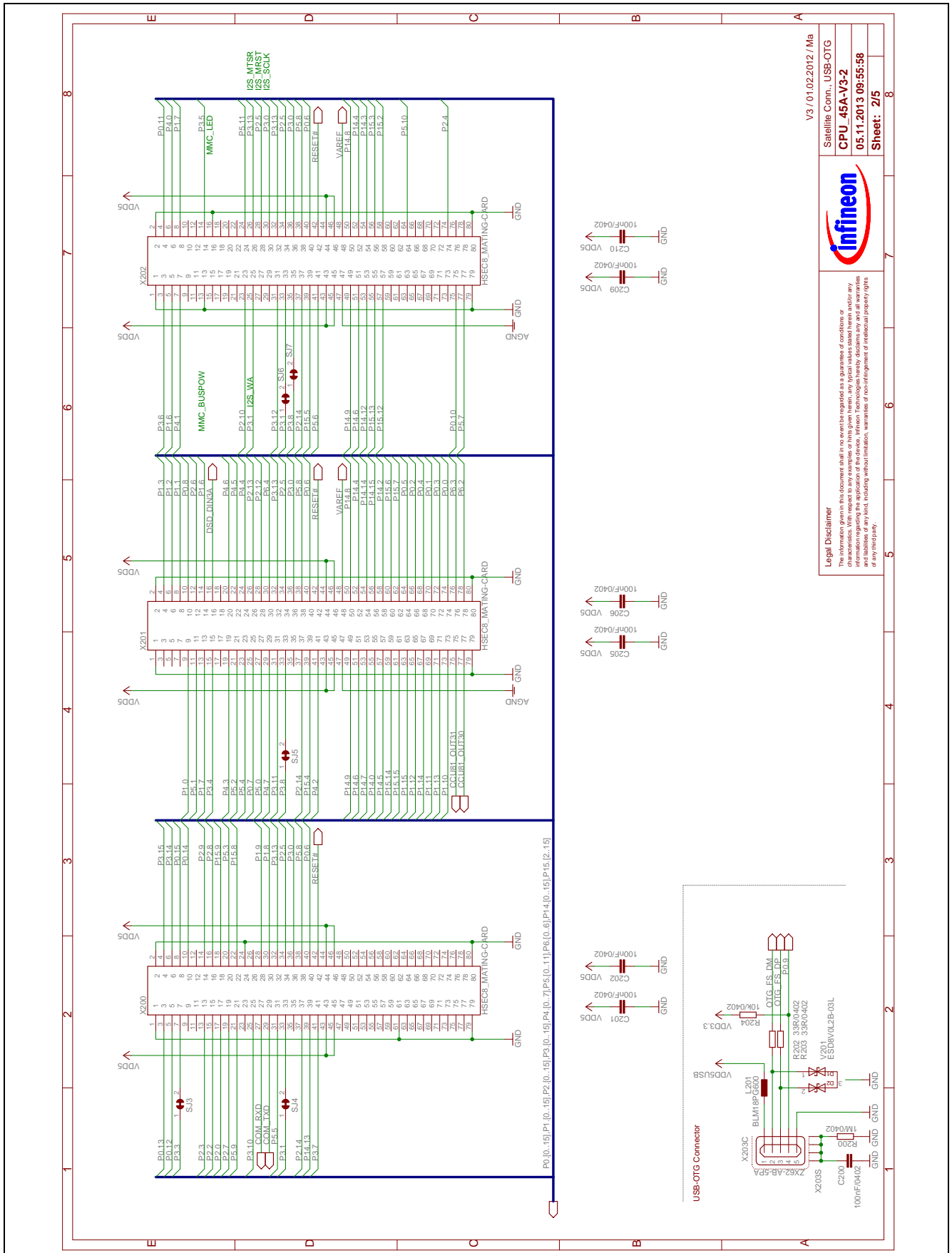
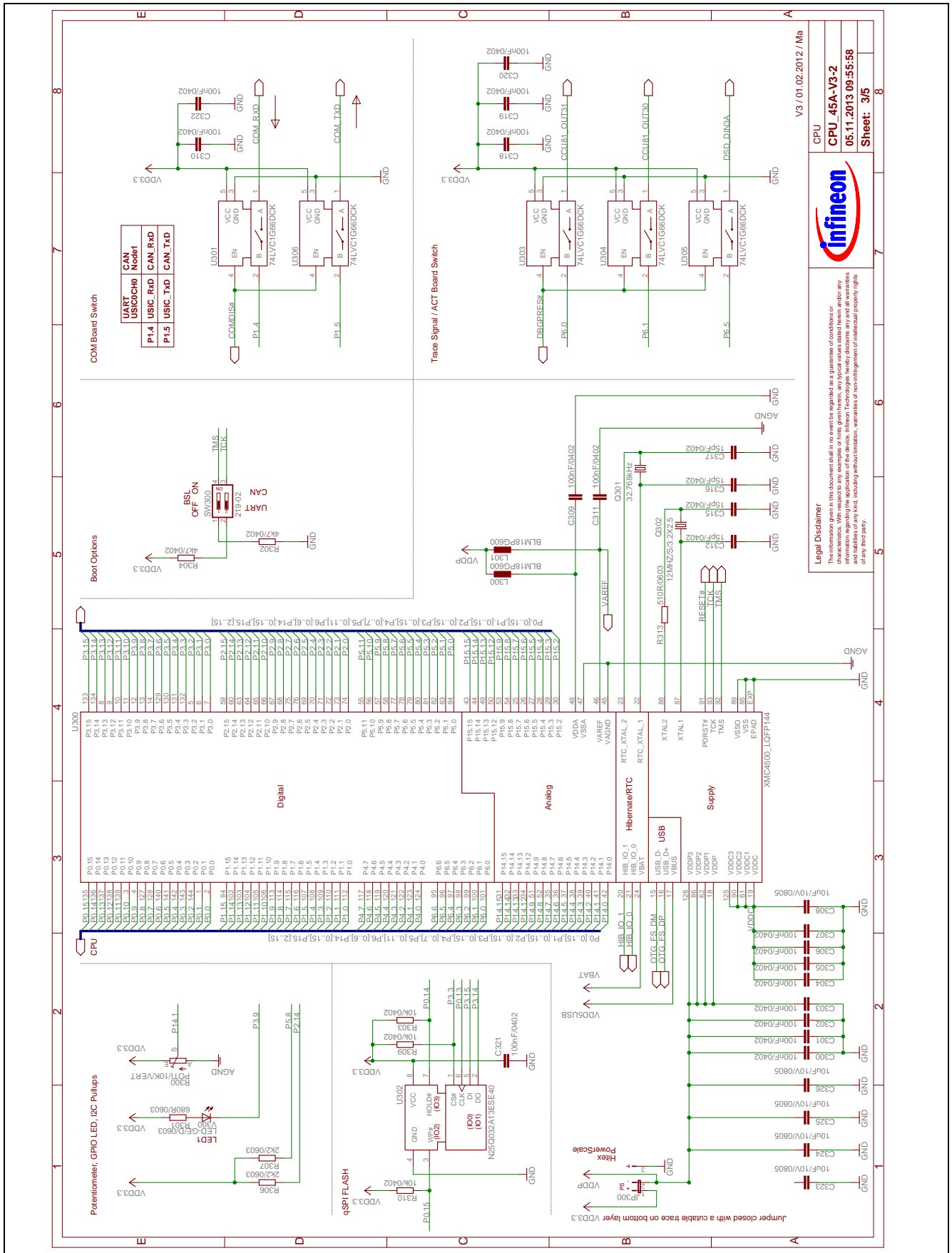
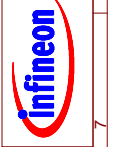


Figure 26 Schematic of Satellite Connectors, USB-OTG



V3 / 01.02.2012 / Ma  
CPU  
CPU 45A-V3-2  
05.11.2013 09:55:58  
Sheet: 3/5



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Figure 27 Schematic of XMC4500



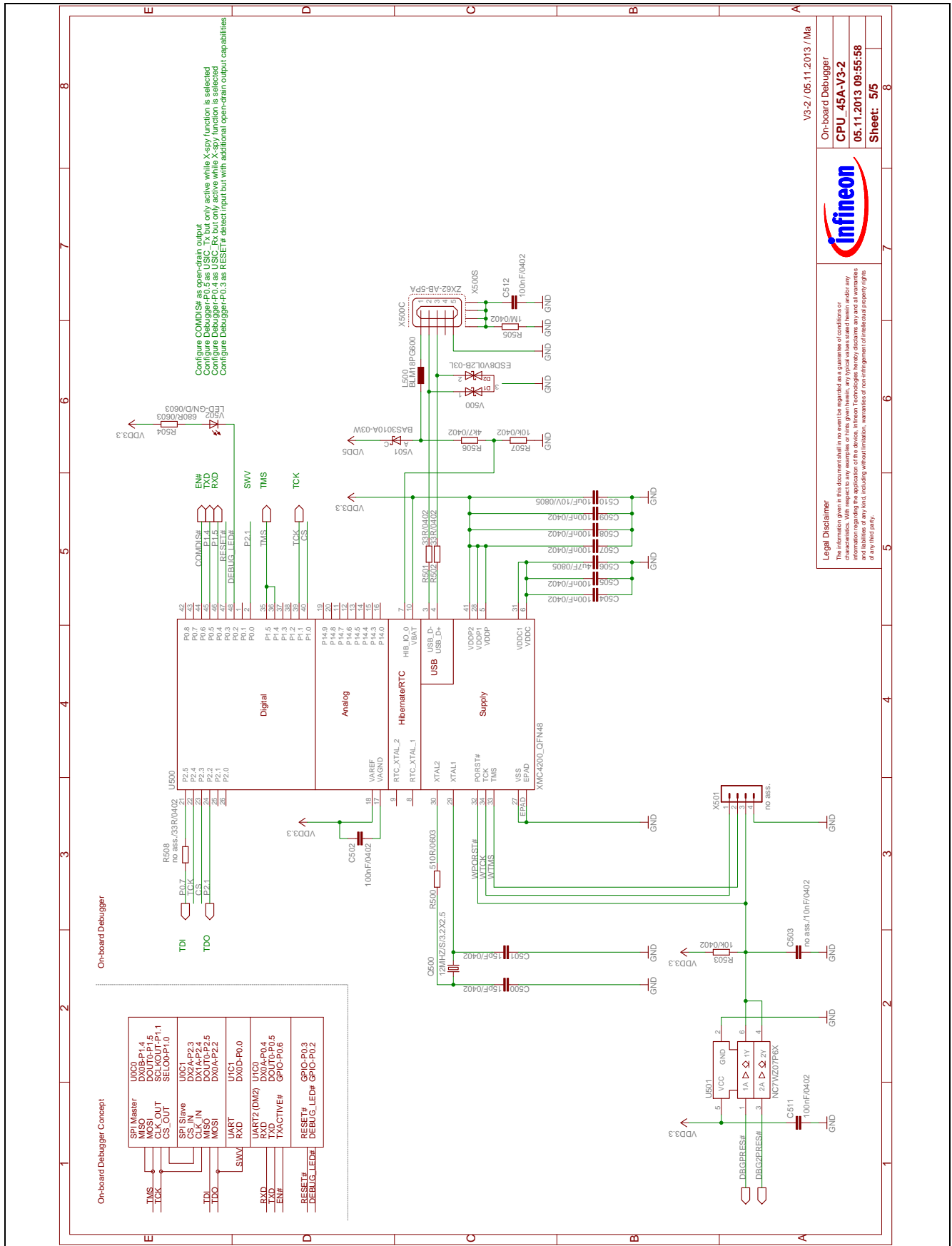


Figure 29 Schematic of On-board Debugger

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On-board Debugger  
CPU\_45A-V3-2  
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## 4.2 Component Placement and Geometry

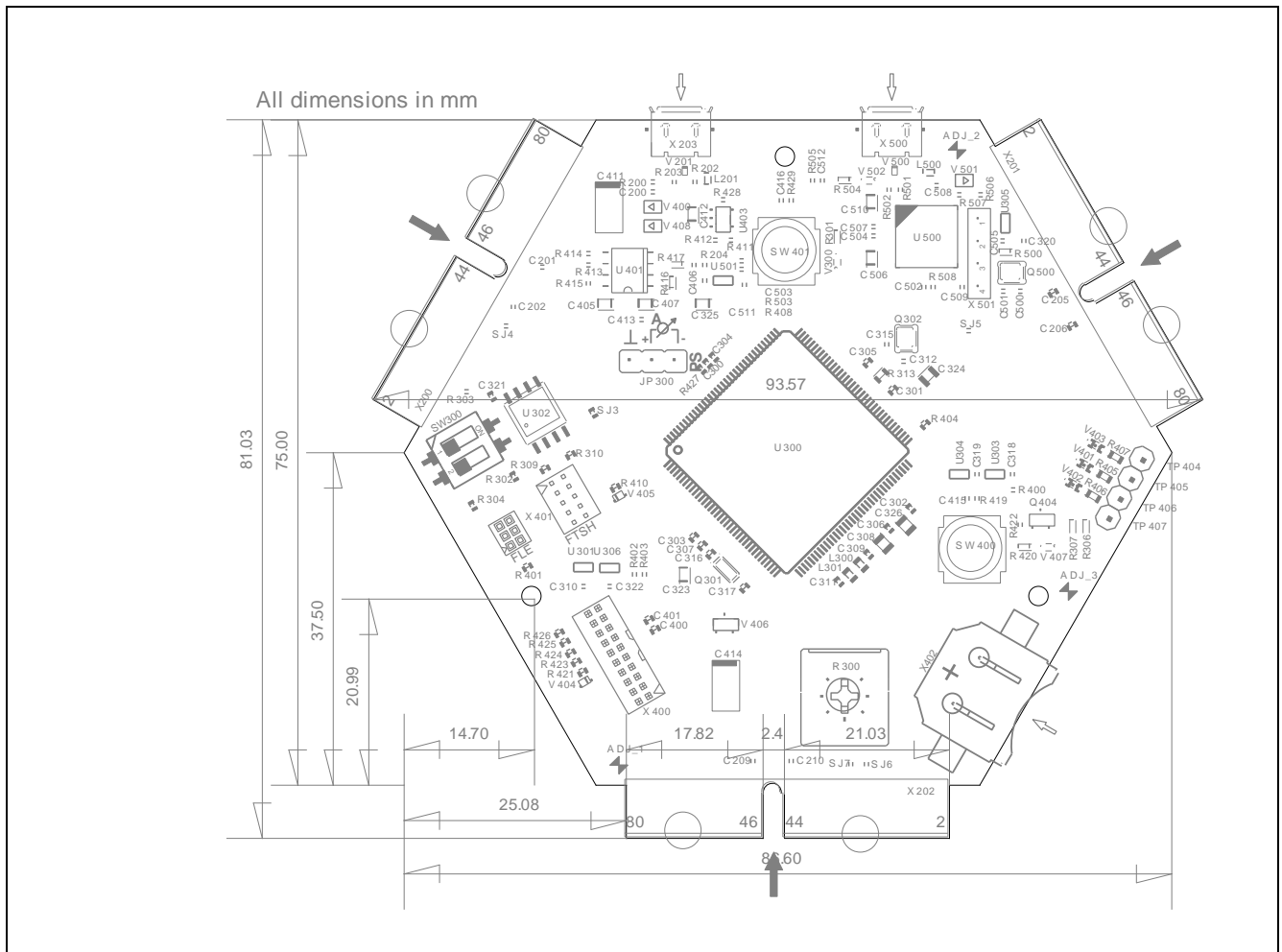


Figure 30 Component Placement and Geometry



### 4.3 Bill of Material (BOM)

**Table 12 BOM of CPU\_45A-V3 Board**

Pos. No.	Qty	Value	Device	Reference Des.
1	1	0R/0603	Resistor	R416
2	2	1M/0402	Resistor	R200, R505
3	2	1k5/0603	Resistor	R405, R406
4	3	2k2/0603	Resistor	R306, R307, R420
5	3	4k7/0402	Resistor	R302, R304, R506
6	1	4u7F/0805	Capacitor, ceramic 10% X7R	C412, C506
7	15	10k/0402	Resistor	R204, R303, R309, R310, R400, R401, R408, R412, R414, R419, R422, R428, R429, R503, R507
8	2	10nF/0402	Capacitor	C406, C415
9	9	10uF/10V/0805	Capacitor ceramic	C308, C323, C324, C325, C326, C405, C407, C510
10	2	12MHZ/S/3.2X2.5	Crystal, NX3225GD, NDK	Q302, Q500
11	6	15pF/0402	Capacitor, ceramic 10% NP0	C312, C315, C316, C317, C500, C501
12	1	32.768kHz	Crystal, NX3215SA, NDK	Q301
13	12	33R/0402	Resistor	R202, R203, R402, R403, R404, R421, R423, R424, R425, R426, R501, R502
14	5	74LVC1G66DCK	IC, Single Analog Switch	U301, U303, U304, U305, U306
15	35	100nF/0402	Capacitor	C200, C201, C202, C205, C206, C209, C210, C300, C301, C302, C303, C304, C305, C306, C307, C309, C310, C311, C318, C319, C320, C321, C322, C400, C401, C413, C416, C502, C504, C505, C507, C508, C509, C511, C512
16	2	100uF/T/10V/C	Capacitor, bipolar	C411, C414
17	1	219-02	Dual DIP-Switch, 0.1" SMD	SW300
18	1	270k/0402	Resistor	R415
19	2	510R/0603	Resistor	R313, R500
20	3	680R/0603	Resistor	R301, R407, R504
21	3	BAS3010A-03W	Diode, SOD323, Infineon	V400, V408, V501
22	2	BAT54-02V	Diode, SC79, Infineon	V404, V405
23	1	BAV70	Diode, SOT23-3, Infineon	V406
24	1	BC858C	Transistor, SOT23-3, Infineon	Q404
25	1	BK-885	Battery Holder, 12mm Coin Cell	X402
26	4	BLM18PG600	Ferrite Bead, 0603, Murata	L201, L300, L301, L500
27	2	ESD8V0L2B-03L	Diode, TSLP-3-1, Infineon	V201, V500
28	3	FIDUCIAL	FIDUCIAL	ADJ_1, ADJ_2, ADJ_3
29	3	HSEC8_MATING-CARD	Connector, 80-pin Edgecard, Samtec	X200, X201, X202
30	1	IFX1763_PADNOP	Voltage Regulator, 3.3V LDO, Infineon	U401
31	1	LED-GE/D/0603	LED, yellow	V300

**Table 12 BOM of CPU\_45A-V3 Board**

Pos. No.	Qty	Value	Device	Reference Des.
32	4	LED-GN/D/0603	LED, green	V401, V402, V403, V502
33	1	LED-RT/D/0603	LED, red	V407
34	1	NC7WZ07P6X	NC7WZ07_2P6X	U501
35	1	POTI/10K/VERT	Potentiometer, K09K1130A8G, ALPS	R300
36	1	S2*10/1.27SO	Connector, FTSH-110-01-L-DVK-P, Samtec	X400
37	1	N25Q032A13ESE40	IC, Serial SPI Flash, 32Mb	U302
38	2	TMPS2-SMD	Switch, tactile	SW400, SW401
39	1	TPS2051BDBV	IC, Power Switch	U403
40	1	XE3K_DM2+CTX	Connector, FTSH-105-01-LM-DVK, without pin 7, Samtec Connector, FLE-103-01-G-DV, Samtec	X401
41	1	XMC4200_QFN48	IC, XMC4200, QFN48, Infineon	U500
42	1	XMC4500_LQFP144	IC, XMC4500, LQFP144, Infineon	U300
43	2	ZX62-AB-5PA	Connector, Micro-USB, Hirose	X203, X500
44	1	no ass.	Pinheader, 4-pin, 0.1" TH	X501
45	4	no ass.	Pinheader, 1-pin, 0.1" TH	TP404, TP405, TP406, TP407
46	1	no ass./0R/0603	Resistor	R417
47	1	no ass./4k7/0402	Resistor	R427
48	2	no ass./10k/0402	Resistor	R411, R413
49	1	no ass./10nF/0402	Resistor	C503
50	2	no ass./33R/0402	Resistor	R410, R508
51	1	no ass.	Pinheader, 3-pin, 0.1" TH, Hitex PowerScale	JP300
52	5	0R/0402	Solder Jumper (0 Ohm)	SJ3, SJ4, SJ5, SJ6, SJ7

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