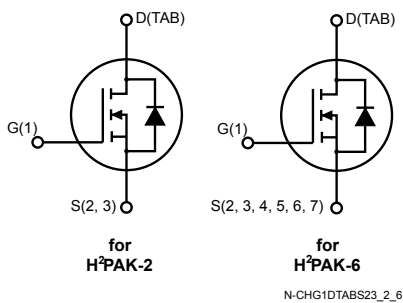
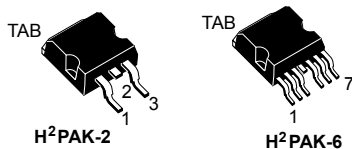


## N-channel 100 V, 2 mΩ typ., 180 A STripFET™ F7 Power MOSFETs in an H<sup>2</sup>PAK-2 and H<sup>2</sup>PAK-6 packages



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STH240N10F7-2	100 V	2.5 mΩ	180 A
STH240N10F7-6			

- Among the lowest R<sub>DS(on)</sub> on the market
- Excellent FoM (figure of merit)
- Low C<sub>rss</sub>/C<sub>iss</sub> ratio for EMI immunity
- High avalanche ruggedness

### Description

These N-channel Power MOSFETs utilize STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Product status	
STH240N10F7-2	
STH240N10F7-6	
Product summary	
Order code	STH240N10F7-2
Marking	240N10F7
Package	H <sup>2</sup> PAK-2
Packing	Tape and reel
Order code	STH240N10F7-6
Marking	240N10F7
Package	H <sup>2</sup> PAK-6
Packing	Tape and reel

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	100	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	180	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	120	A
$I_{DM}^{(2)}$	Drain current (pulsed)	720	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	300	W
$E_{AS}^{(3)}$	Single pulse avalanche energy	500	mJ
$T_j$	Operating junction temperature range	-55 to 175	$^\circ\text{C}$
$T_{stg}$	Storage temperature range		

1. Current limited by package.
2. Pulse width limited by safe operating area.
3. Starting  $T_j=25\text{ }^\circ\text{C}$ ,  $I_D=45\text{ A}$ ,  $V_{DD}=50\text{ V}$

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.5	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	35	$^\circ\text{C/W}$

1. When mounted on 1 inch<sup>2</sup> FR-4, 2 Oz copper board.

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 3. On/Off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$ , $V_{GS} = 0\ \text{V}$	100			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\ \text{V}$ , $V_{DS} = 100\ \text{V}$			1	$\mu\text{A}$
		$V_{GS} = 0\ \text{V}$ , $V_{DS} = 100\ \text{V}$ , $T_C = 125\text{ °C}$ <sup>(1)</sup>			100	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{GS} = \pm 20\ \text{V}$ , $V_{DS} = 0\ \text{V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\ \mu\text{A}$	2.5		4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\ \text{V}$ , $I_D = 60\ \text{A}$		2	2.5	m $\Omega$

1. Defined by design, not subject to production test.

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\ \text{V}$ , $f = 1\ \text{MHz}$ , $V_{GS} = 0\ \text{V}$	-	11550	-	pF
$C_{oss}$	Output capacitance		-	2950	-	pF
$C_{riss}$	Reverse transfer capacitance		-	217	-	pF
$Q_g$	Total gate charge	$V_{DD} = 50\ \text{V}$ , $I_D = 180\ \text{A}$ ,	-	160	-	nC
$Q_{gs}$	Gate-source charge	$V_{GS} = 0$ to $10\ \text{V}$	-	48	-	nC
$Q_{gd}$	Gate-drain charge	(see Figure 15. Test circuit for gate charge behavior)	-	38	-	nC

**Table 5. Switching times**

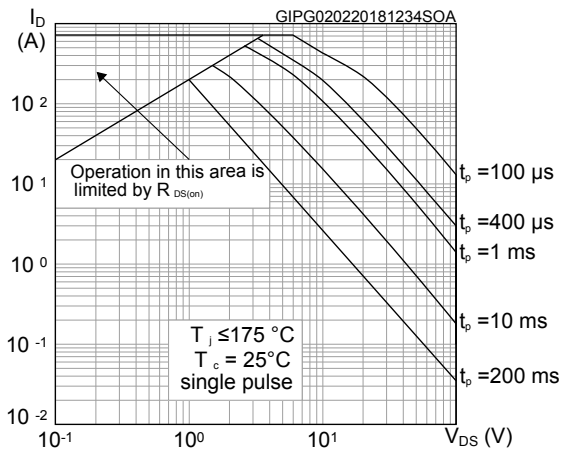
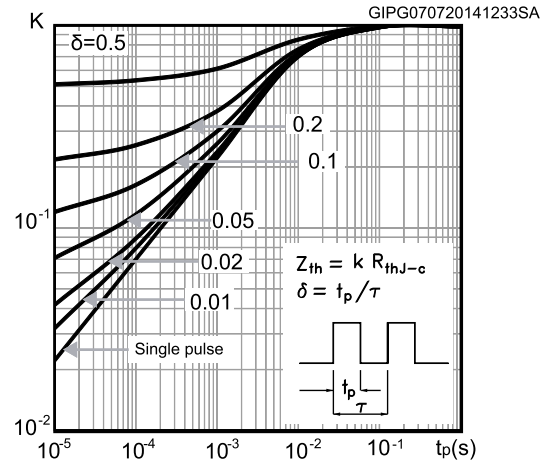
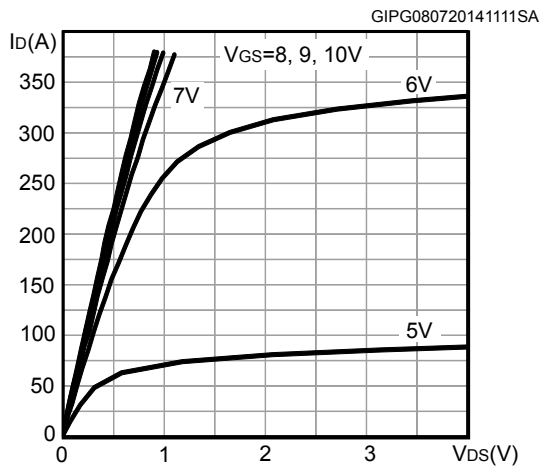
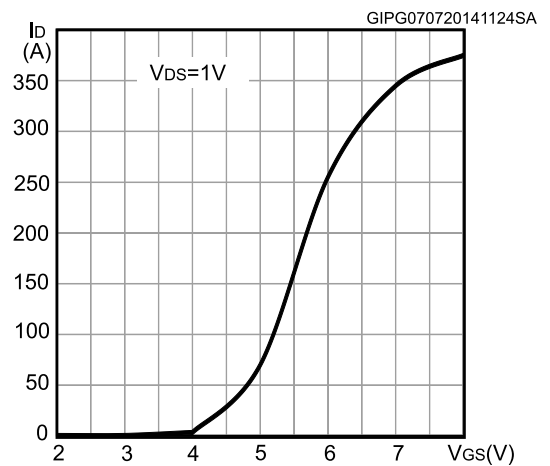
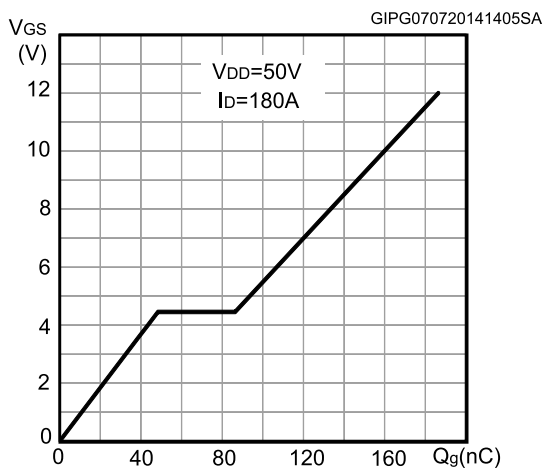
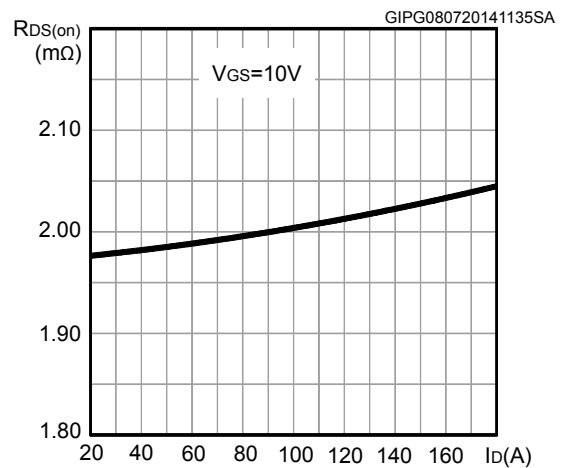
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 50\ \text{V}$ , $I_D = 90\ \text{A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\ \text{V}$ (see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	49	-	ns
$t_r$	Rise time		-	139	-	ns
$t_{d(off)}$	Turn-off delay time		-	110	-	ns
$t_f$	Fall time		-	112	-	ns

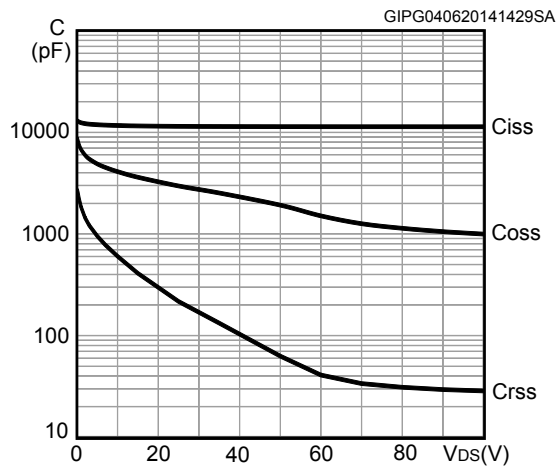
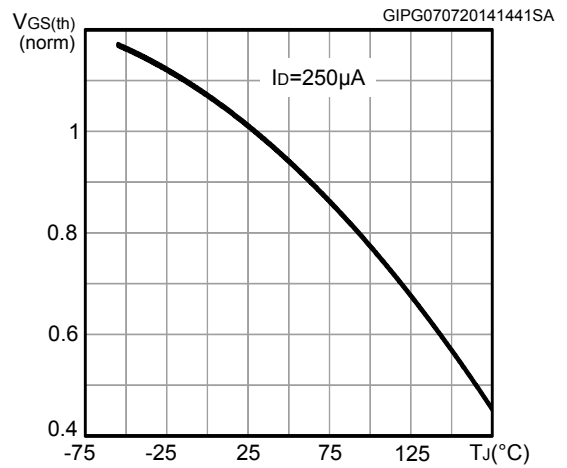
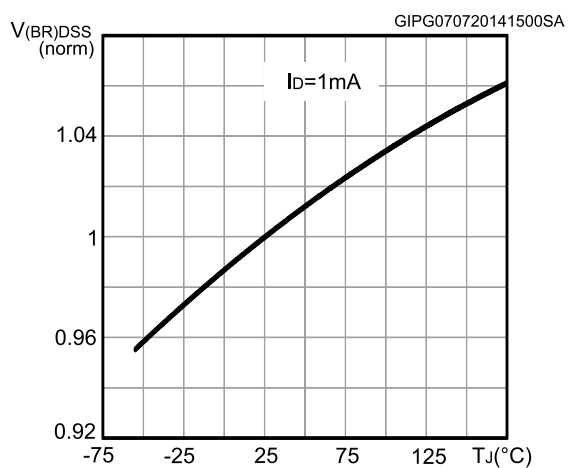
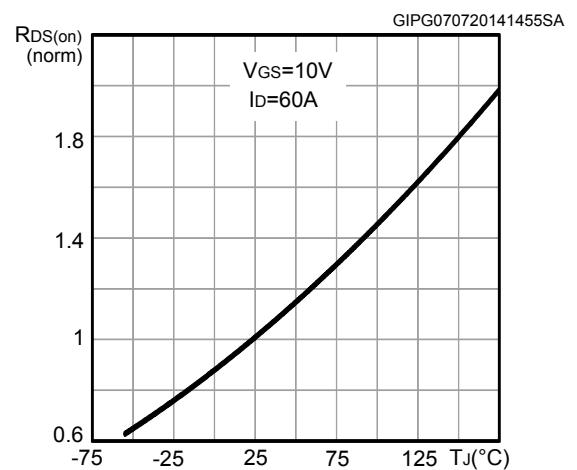
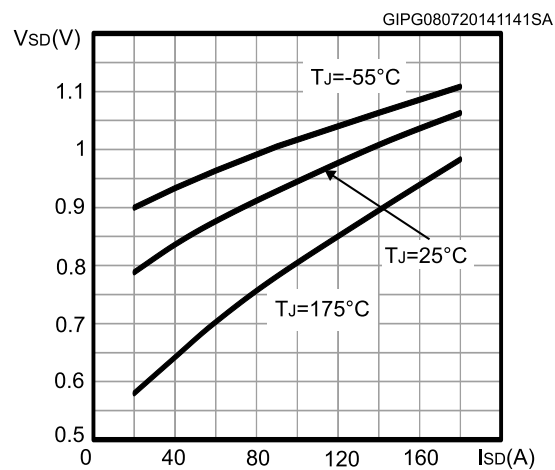
**Table 6. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		180	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		720	A

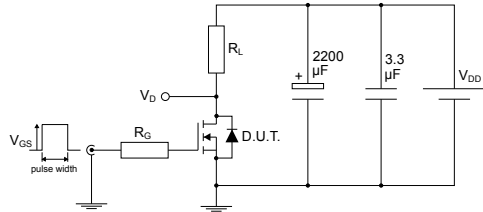
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(2)}$	Source-drain curren	$I_{SD} = 180 \text{ A}$ , $V_{GS} = 0 \text{ V}$	-		1.2	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 180 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$	-	108		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 64 \text{ V}$ , $T_J = 150 \text{ }^\circ\text{C}$ (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	315		nC
$I_{RRM}$	Reverse recovery current		-	5.8		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration=300  $\mu\text{s}$ , duty cycle 1.5%.

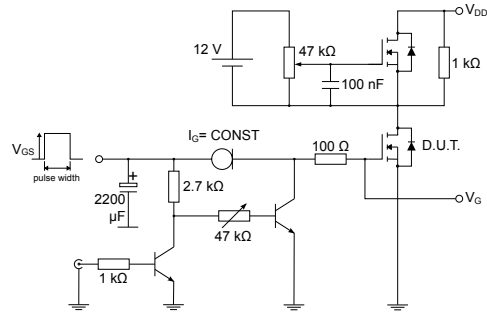
**2.1 Electrical characteristics (curves)**
**Figure 3. Safe operating area**

**Figure 4. Thermal impedance**

**Figure 5. Output characteristics**

**Figure 6. Transfer characteristics**

**Figure 7. Gate charge vs gate-source voltage**

**Figure 8. Static drain-source on-resistance**


**Figure 9. Capacitance variations**

**Figure 10. Normalized gate threshold voltage vs. temperature**

**Figure 11. Normalized V<sub>(BR)DSS</sub> vs. temperature**

**Figure 12. Normalized on-resistance vs. temperature**

**Figure 13. Source-drain diode forward characteristics**


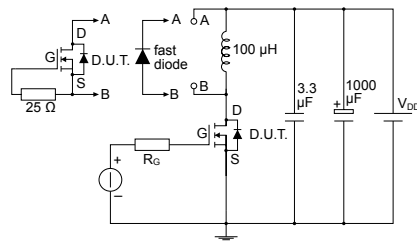
### 3 Test circuits

**Figure 14. Test circuit for resistive load switching times**


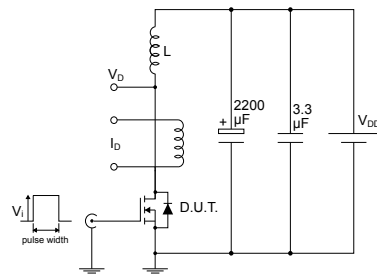
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**Figure 15. Test circuit for gate charge behavior**


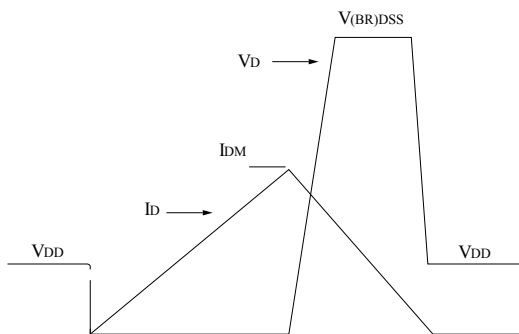
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**Figure 16. Test circuit for inductive load switching and diode recovery times**


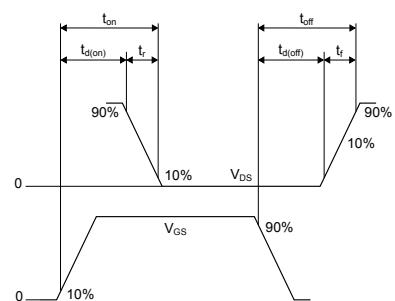
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**Figure 17. Unclamped inductive load test circuit**


AM01471v1

**Figure 18. Unclamped inductive waveform**


AM01472v1

**Figure 19. Switching time waveform**


AM01473v1

## 4 Package information

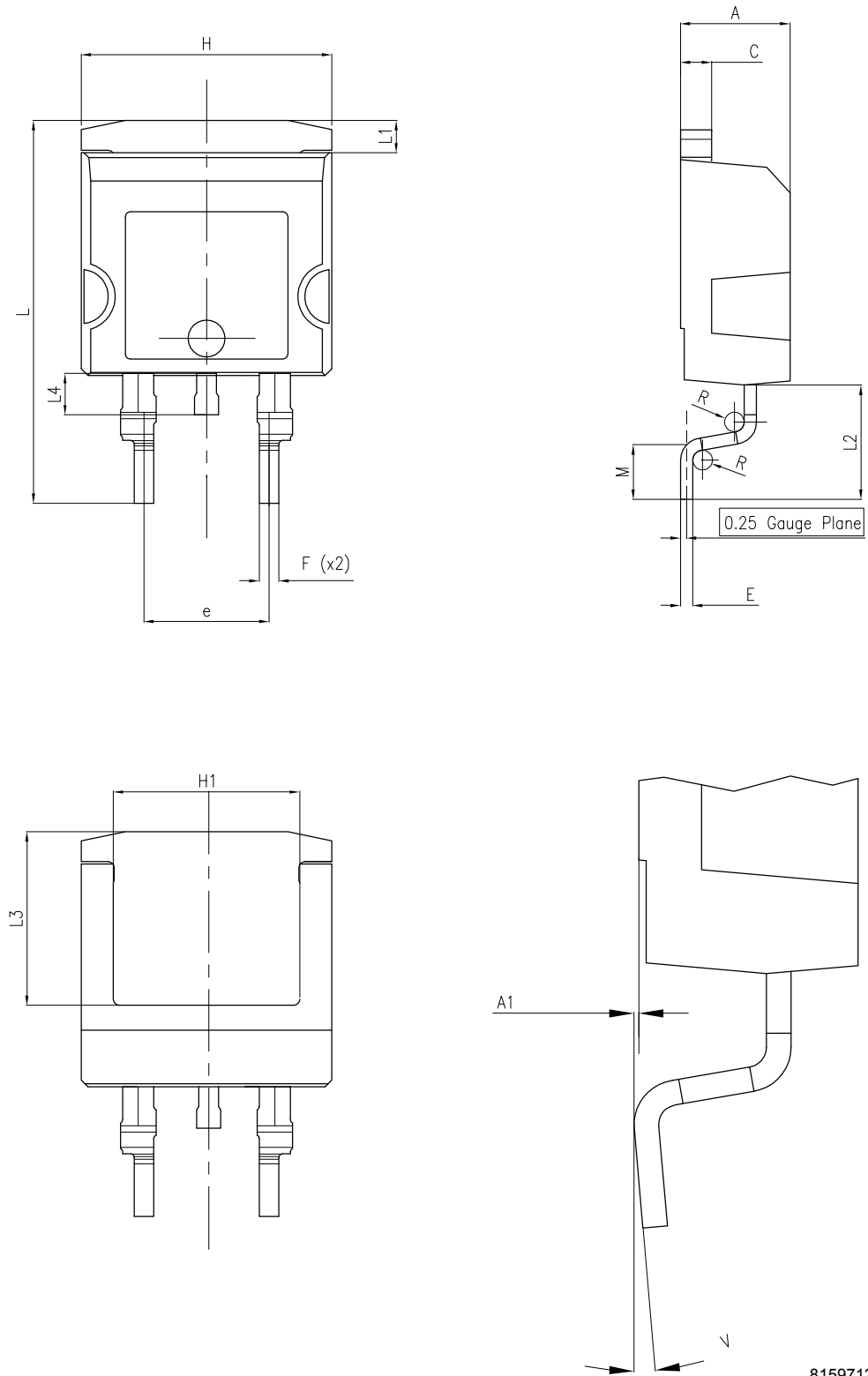
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### 4.1 H<sup>2</sup>PAK-2 package information

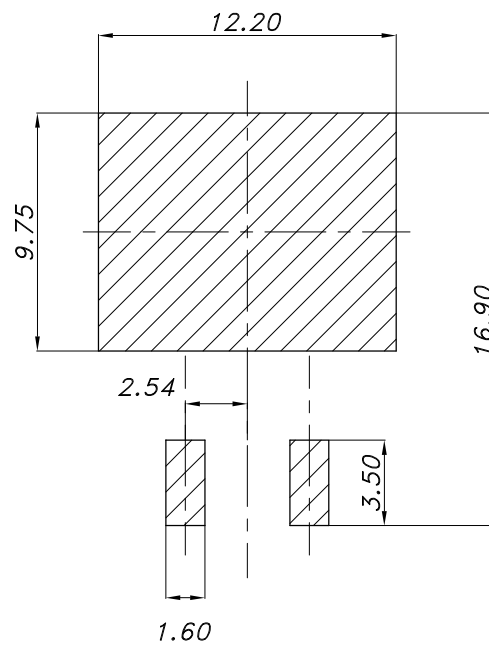
Figure 20. H<sup>2</sup>PAK-2 package outline



8159712\_6

**Table 7. H<sup>2</sup>PAK-2 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.70
A1	0.03		0.20
C	1.17		1.37
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
H	10.00		10.40
H1	7.40		7.80
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	6.85		7.25
L4	1.5		1.7
M	2.6		2.9
R	0.20		0.60
V	0°		8°

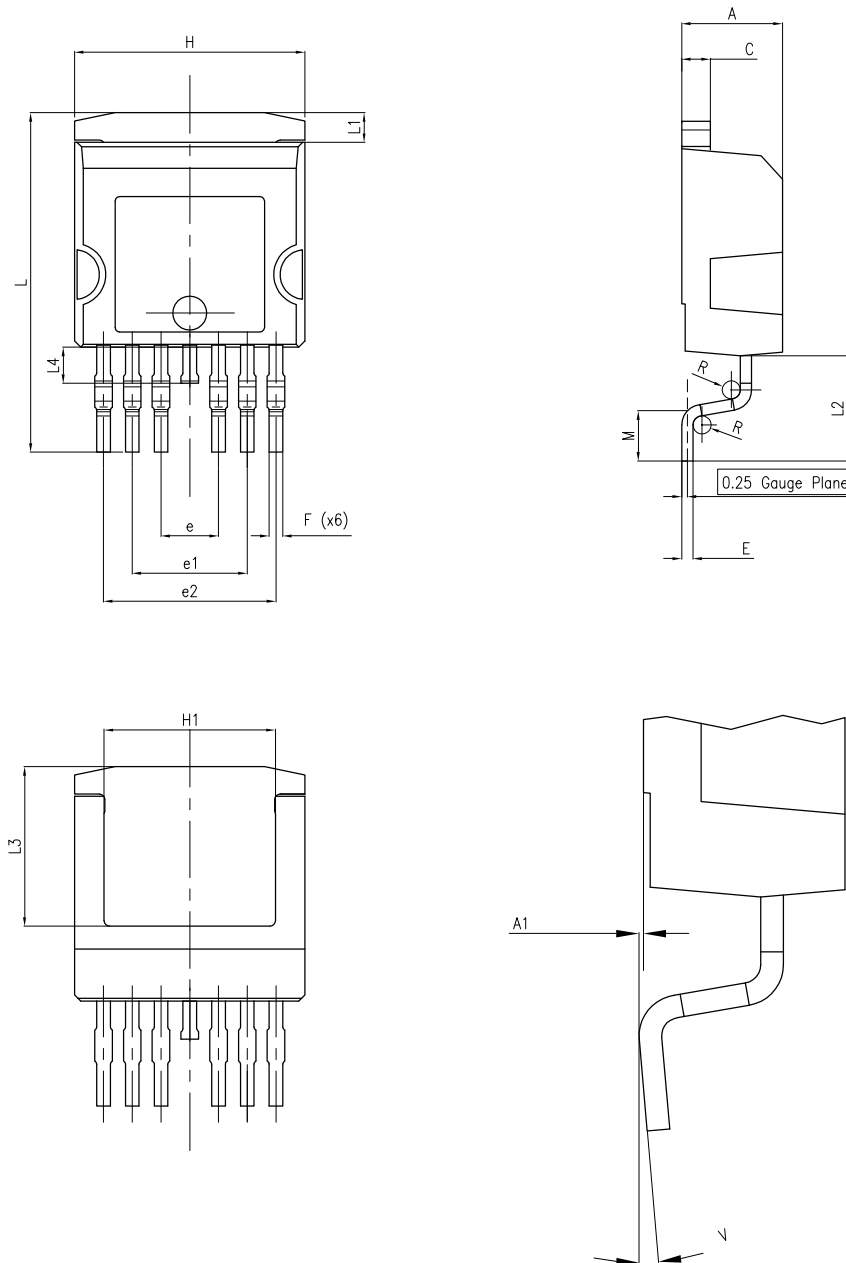
**Figure 21. H<sup>2</sup>PAK-2 recommended footprint**


8159712\_6

Note: Dimensions are in mm.

## 4.2 H<sup>2</sup>PAK-6 package information

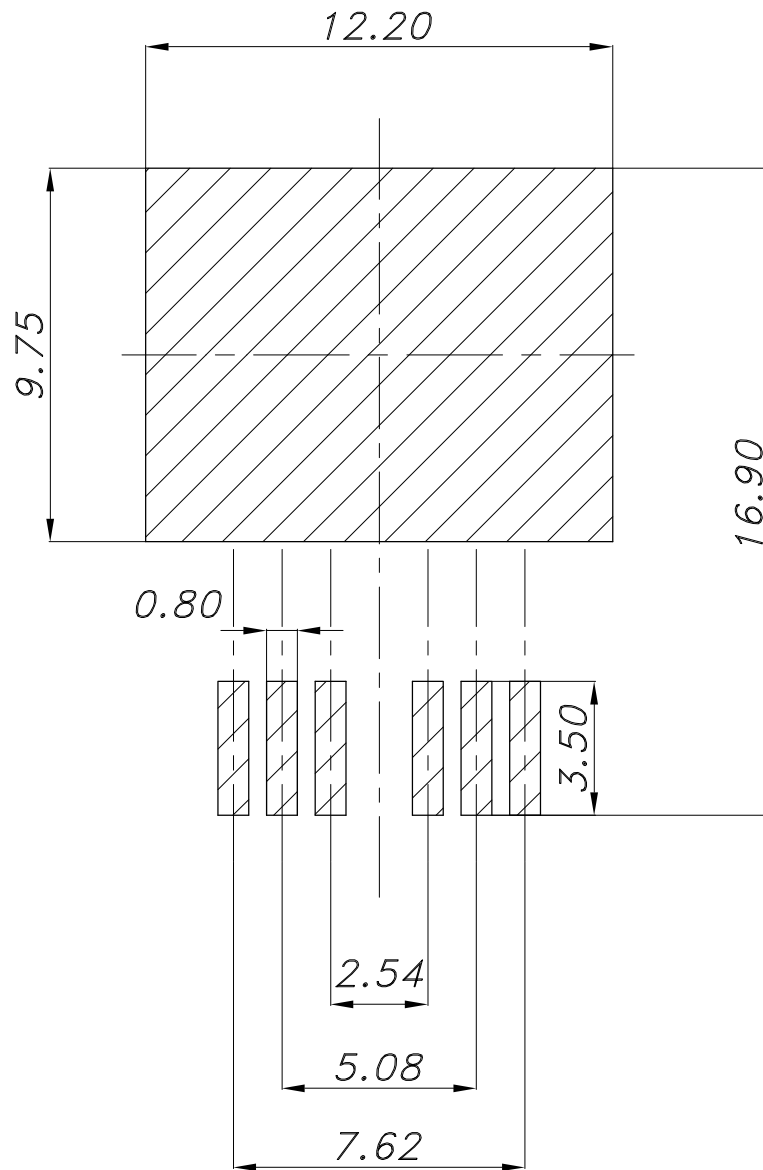
Figure 22. H<sup>2</sup>PAK-6 package outline



**Table 8. H<sup>2</sup>PAK-6 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.70
A1	0.03		0.20
C	1.17		1.37
e	2.34	2.54	2.74
e1	4.88		5.28
e2	7.42		7.82
E	0.45		0.60
F	0.50		0.70
H	10.00		10.40
H1	7.40		7.80
L	14.75		15.25
L1	1.27		1.40
L2	4.35		4.95
L3	6.85		7.25
L4	1.50		1.75
M	1.90		2.50
R	0.20		0.60
V	0°		8°

Figure 23. H<sup>2</sup>PAK-6 recommended footprint

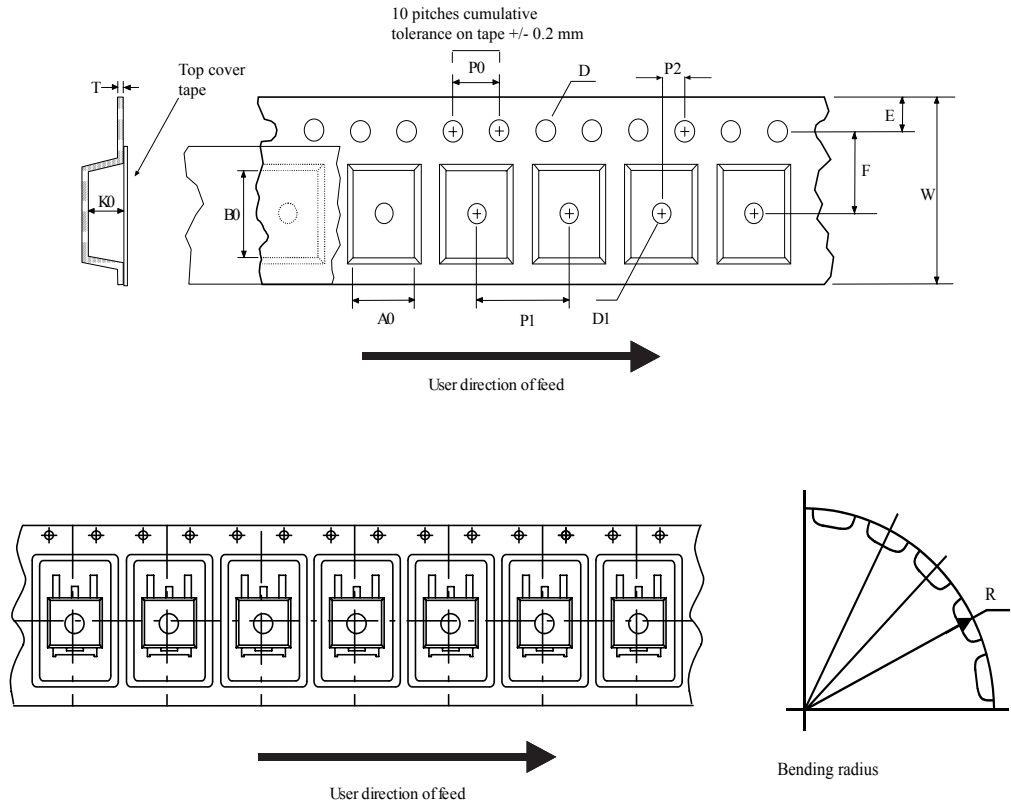


footprint\_Rev\_8

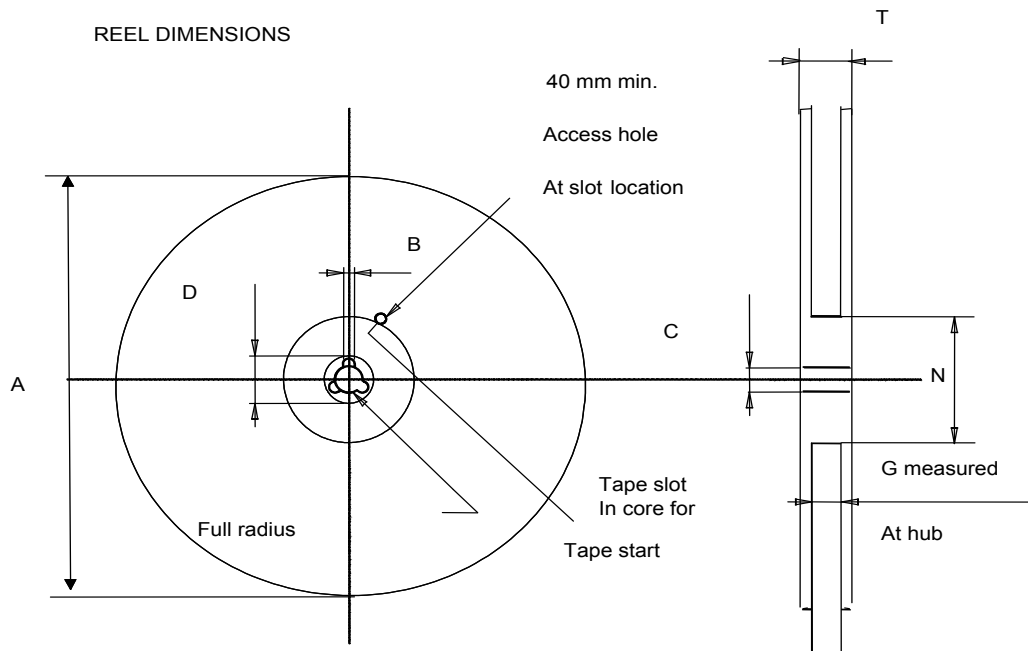
Note: Dimensions are in mm.

### 4.3 Packing information

Figure 24. Tape outline



AM08852v2

**Figure 25. Reel outline**

**Table 9. Tape and reel mechanical data**

Dim.	Tape		Dim.	Reel	
	mm			mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

## Revision history

**Table 10. Document revision history**

Date	Version	Changes
07-May-2014	1	Initial release.
23-Jul-2014	2	<ul style="list-style-type: none"> <li>– Modified: title and description</li> <li>– Added: <i>Section 2.1: Electrical characteristics (curves)</i></li> <li>– Minor text changes</li> </ul>
06-Feb-2018	3	<ul style="list-style-type: none"> <li>Removed maturity status indication from cover page. Production data.</li> <li>Modified <a href="#">Figure 3. Safe operating area.</a></li> <li>Minor text changes.</li> </ul>



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