

NL17SH126

Noninverting 3-State Buffer

The NL17SH126 is an advanced high speed CMOS noninverting 3-state buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffered 3-state output which provides high noise immunity and stable output.

The NL17SH126 input structure provides protection when voltages up to 7 V are applied, regardless of the supply voltage. This allows the NL17SH126 to be used to interface 5 V circuits to 3 V circuits.

Features

- High Speed: $t_{PD} = 3.5$ ns (Typ) at $V_{CC} = 5$ V
- Low Power Dissipation: $I_{CC} = 1$ μ A (Max) at $T_A = 25^\circ\text{C}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- These are Pb-Free Devices

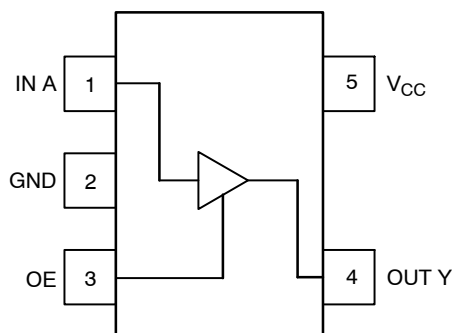


Figure 1. Pinout (Top View)

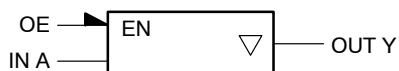


Figure 2. Logic Symbol



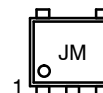
ON Semiconductor®

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MARKING DIAGRAM



SOT-953
CASE 527AE



J = Specific Device Code
M = Month Code

PIN ASSIGNMENT

1	IN A
2	GND
3	OE
4	OUT Y
5	V_{CC}

FUNCTION TABLE

A Input	OE Input	Y Output
L	H	L
H	H	H
X	L	Z

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

MAXIMUM RATINGS

Symbol	Characteristics	Value	Unit
V_{CC}	DC Supply Voltage	-0.5 to +7.0	V
V_{IN}	DC Input Voltage	-0.5 to +7.0	V
V_{OUT}	DC Output Voltage $V_{CC} = 0$ High or Low State	-0.5 to 7.0 -0.5 to $V_{CC} + 0.5$	V
I_{IK}	Input Diode Current	-20	mA
I_{OK}	Output Diode Current $V_{OUT} < GND; V_{OUT} > V_{CC}$	± 20	mA
I_{OUT}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND	50	mA
P_D	Power dissipation in still air	50	mW
T_L	Lead temperature, 1 mm from case for 10 secs	260	°C
T_J	Junction temperature under bias	+150	°C
T_{stg}	Storage temperature	-65 to +150	°C
$I_{Latchup}$	Latchup Performance Above V_{CC} and Below GND at 125°C (Note 1)	± 100	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	5.5	V
V_{IN}	DC Input Voltage	0.0	5.5	V
V_{OUT}	DC Output Voltage	0.0	V_{CC}	V
T_A	Operating Temperature Range	-55	+125	°C
t_r, t_f	Input Rise and Fall Time $V_{CC} = 3.3 V \pm 0.3 V$ $V_{CC} = 5.0 V \pm 0.5 V$	0 0	100 20	ns/V

Device Junction Temperature versus Time to 0.1% Bond Failures

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

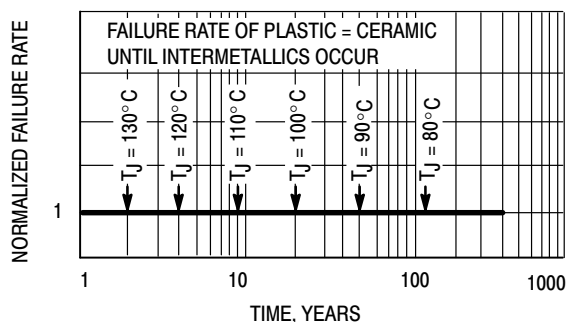


Figure 3. Failure Rate vs. Time Junction Temperature

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V _{CC} (V)	T _A = 25°C			T _A ≤ 85°C		-55 ≤ T _A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V _{IH}	Minimum High-Level Input Voltage		2.0 3.0 4.5 5.5	1.5 2.1 3.15 3.85			1.5 2.1 3.15 3.85		1.5 2.1 3.15 3.85		V
V _{IL}	Maximum Low-Level Input Voltage		2.0 3.0 4.5 5.5			0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65	V
V _{OH}	Minimum High-Level Output Voltage V _{IN} = V _{IH} or V _{IL}	V _{IN} = V _{IH} or V _{IL} I _{OH} = -50 μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		V _{IN} = V _{IH} or V _{IL} I _{OH} = -4 mA I _{OH} = -8 mA	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		V
V _{OL}	Maximum Low-Level Output Voltage V _{IN} = V _{IH} or V _{IL}	V _{IN} = V _{IH} or V _{IL} I _{OL} = 50 μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		V _{IN} = V _{IH} or V _{IL} I _{OL} = 4 mA I _{OL} = 8 mA	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	V
I _{OZ}	Maximum 3-State Leakage Current	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND	5.5			±0.2 5		±2.5		±2.5	μA
I _{IN}	Maximum Input Leakage Current	V _{IN} = 5.5 V or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND	5.5			1.0		20		40	μA

AC ELECTRICAL CHARACTERISTICS C_{load} = 50 pF, Input t_r = t_f = 3.0 ns

Symbol	Parameter	Test Conditions	T _A = 25°C			T _A ≤ 85°C		-55 ≤ T _A ≤ 125°C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A to Y (Figures 3. and 5.)	V _{CC} = 3.3 ± 0.3 V C _L = 15 pF C _L = 50 pF		4.5 6.4	8.0 11.5		9.5 13.0		12.0 16.0	ns
		V _{CC} = 5.0 ± 0.5 V C _L = 15 pF C _L = 50 pF		3.5 4.5	5.5 7.5		6.5 8.5		8.5 10.5	
t _{PZL} , t _{PZH}	Maximum Output Enable Time, Input OE to Y (Figures 4. and 5.)	V _{CC} = 3.3 ± 0.3 V C _L = 15 pF R _L = 1000 Ω C _L = 50 pF		4.5 6.4	8.0 11.5		9.5 13.0		11.5 15.0	ns
		V _{CC} = 5.0 ± 0.5 V C _L = 15 pF R _L = 1000 Ω C _L = 50 pF		3.5 4.5	5.1 7.1		6.0 8.0		8.5 10.5	
t _{PLZ} , t _{PHZ}	Maximum Output Disable Time, Input OE to Y (Figures 4. and 5.)	V _{CC} = 3.3 ± 0.3 V C _L = 15 pF R _L = 1000 Ω C _L = 50 pF		6.5 8.0	9.7 13.2		11.5 15.0		14.5 18.0	ns
		V _{CC} = 5.0 ± 0.5 V C _L = 15 pF R _L = 1000 Ω C _L = 50 pF		4.8 7.0	6.8 8.8		8.0 10.0		10.0 12.0	
C _{IN}	Maximum Input Capacitance			4.0	10		10		10	pF
C _{OUT}	Maximum 3-State Output Capacitance (Output in High Impedance State)			6.0						pF

C _{PD}	Power Dissipation Capacitance (Note 2)	Typical @ 25°C, V _{CC} = 5.0 V	pF
		8.0	

2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

SWITCHING WAVEFORMS

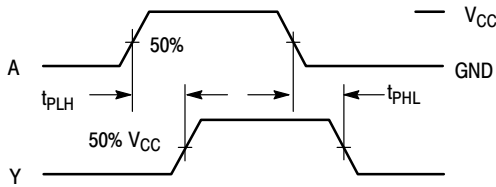


Figure 4. Switching Waveforms

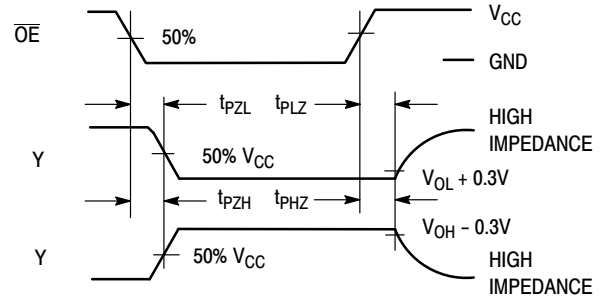
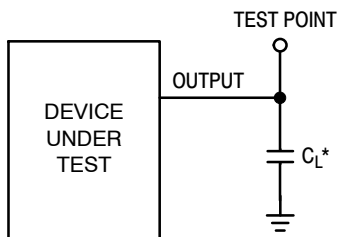
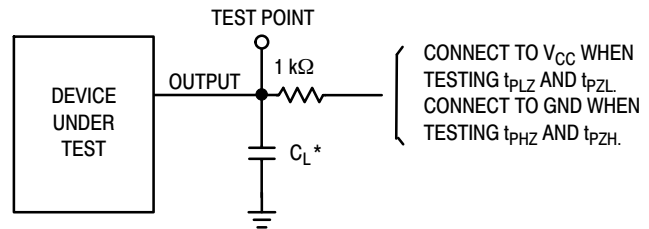


Figure 5.



*Includes all probe and jig capacitance

Figure 6. Test Circuit



*Includes all probe and jig capacitance

Figure 7. Test Circuit

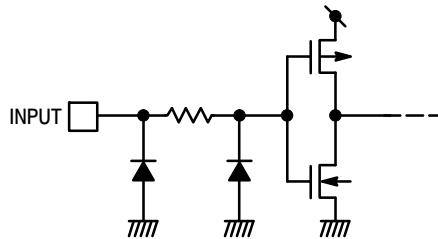


Figure 8. Input Equivalent Circuit

ORDERING INFORMATION

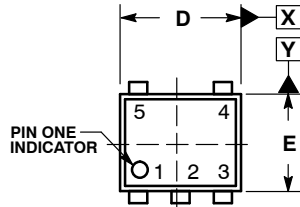
Device	Package	Shipping†
NL17SH126P5T5G	SOT-953 (Pb-Free)	8000 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

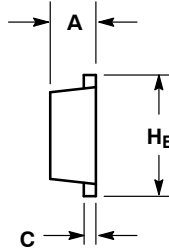
NL17SH126

PACKAGE DIMENSIONS

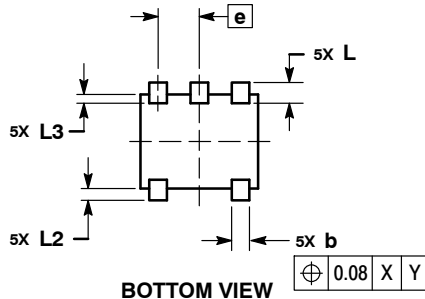
SOT-953
CASE 527AE
ISSUE E



TOP VIEW



SIDE VIEW



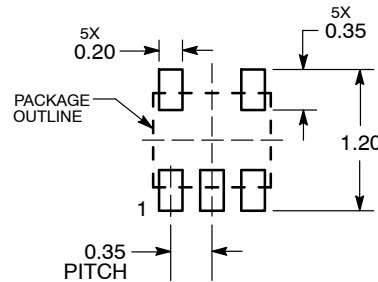
BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.34	0.37	0.40
b	0.10	0.15	0.20
C	0.07	0.12	0.17
D	0.95	1.00	1.05
E	0.75	0.80	0.85
e	0.35 BSC		
H _E	0.95	1.00	1.05
L	0.175 REF		
L2	0.05	0.10	0.15
L3	---	---	0.15

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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