

3-1/2 Digit Analog-to-Digital Converters

Features

- Internal Reference with Low Temperature Drift
 - TC7126: 80ppm/°C Typical
 - TC7126A: 35ppm/°C Typical
- Zero Reading with Zero Input
- Low Noise: 15 μ V_{P-P}
- High Resolution: 0.05%
- Low Input Leakage Current: 1pA Typ., 10pA Max.
- Precision Null Detectors with True Polarity at Zero
- High-Impedance Differential Input
- Convenient 9V Battery Operation with Low Power Dissipation: 500 μ W Typ., 900 μ W Max.

Applications

- Thermometry
- Bridge Readouts: Strain Gauges, Load Cells, Null Detectors
- Digital Meters and Panel Meters:
 - Voltage/Current/Ohms/Power, pH
- Digital Scales, Process Monitors

Device Selection Table

| Package Code | Package | Temperature Range |
|--------------|---------------------------|-------------------|
| CPL | 40-Pin PDIP | 0°C to +70°C |
| IPL | 40-Pin PDIP (TC7126 Only) | -25°C to +85°C |
| CKW | 44-Pin PQFP | 0°C to +70°C |
| CLW | 44-Pin PLCC | 0°C to +70°C |

General Description

The TC7126A is a 3-1/2 digit CMOS analog-to-digital converter (ADC) containing all the active components necessary to construct a 0.05% resolution measurement system. Seven-segment decoders, digit and polarity drivers, voltage reference, and clock circuit are integrated on-chip. The TC7126A directly drives a liquid crystal display (LCD), and includes a backplane driver.

A low cost, high resolution indicating meter requires only a display, four resistors, and four capacitors. The TC7126A's extremely low power drain and 9V battery operation make it ideal for portable applications.

The TC7126A reduces linearity error to less than 1 count. Rollover error (the difference in readings for equal magnitude, but opposite polarity input signals) is below ± 1 count. High-impedance differential inputs offer 1pA leakage current and a 10¹² Ω input impedance. The 15 μ V_{P-P} noise performance ensures a "rock solid" reading, and the auto-zero cycle ensures a zero display reading with a 0V input.

The TC7126A features a precision, low drift internal voltage reference and is functionally identical to the TC7126. A low drift external reference is not normally required with the TC7126A.

TC7126/A

Package Type

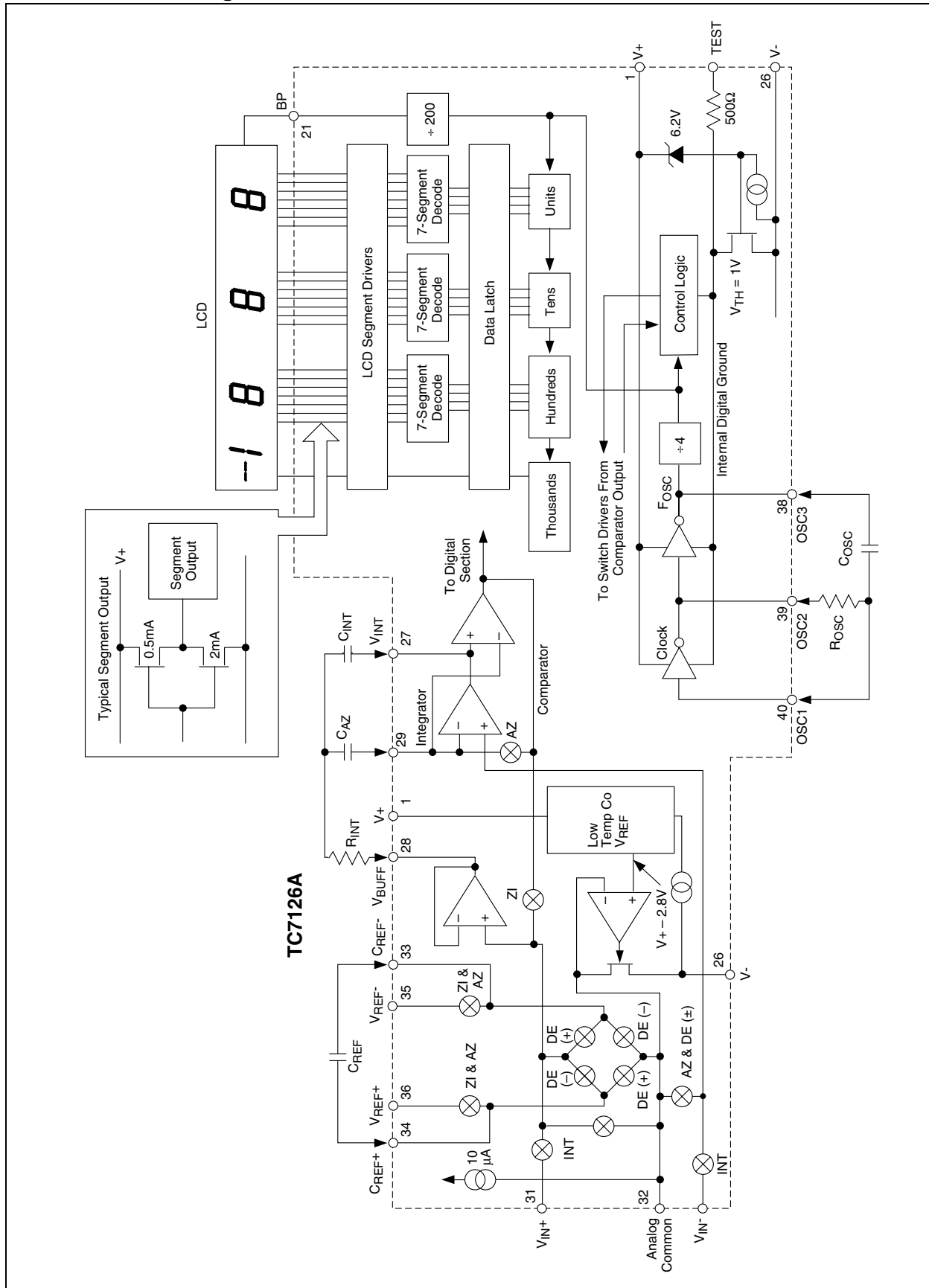


Typical Application



TC7126/A

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

| | |
|---|-----------------|
| Supply Voltage (V+ to V-) | 15V |
| Analog Input Voltage (either Input) (Note 1) ... V+ to V- | |
| Reference Input Voltage (either Input) | V+ to V- |
| Clock Input | Test to V+ |
| Package Power Dissipation (T _A ≤ 70°C) (Note 2): | |
| 44-Pin PQFP | 1.00W |
| 40-Pin PLCC | 1.23W |
| 44-Pin PDIP | 1.23W |
| Operating Temperature Range: | |
| C (Commercial) Devices | 0°C to +70°C |
| I (Industrial) Devices | -25°C to +85°C |
| Storage Temperature Range | -65°C to +150°C |

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TC7126/A ELECTRICAL SPECIFICATIONS

| Electrical Characteristics: V _S = +9V, f _{CLK} = 16kHz, and T _A = +25°C, unless otherwise noted. | | | | | | |
|---|---------------------------------------|--------|----------|--------|-------------------|--|
| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
| Input | | | | | | |
| Z _{IR} | Zero Input Reading | -000.0 | ±000.0 | +000.0 | Digital Reading | V _{IN} = 0V Full Scale = 200mV |
| Z _{RD} | Zero Reading Drift | — | 0.2 | 1 | μV/°C | V _{IN} = 0V, 0°C ≤ T _A ≤ +70°C |
| | Ratiometric Reading | 999 | 999/1000 | 1000 | Digital Reading | V _{IN} = V _{REF} , V _{REF} = 100mV |
| NL | Linearity Error | -1 | ±0.2 | 1 | Count | Full Scale = 200mV or 2V Max Deviation From Best Fit Straight Line |
| | Rollover Error | -1 | ±0.2 | 1 | Count | V _{IN} = V _{IN+} ≈ 200mV |
| e _N | Noise | — | 15 | — | μV _{P-P} | V _{IN} = 0V, Full Scale = 200mV |
| I _L | Input Leakage Current | — | 1 | 10 | pA | V _{IN} = 0V |
| CMRR | Common Mode Rejection Ratio | — | 50 | — | μV/V | V _{CM} = ±1V, V _{IN} = 0V Full Scale = 200mV |
| | Scale Factor Temperature Coefficient | — | 1 | 5 | ppm/°C | V _{IN} = 199mV, 0°C ≤ T _A ≤ +70°C Ext. Ref. Temp Coeff. = 0ppm/°C |
| Analog Common | | | | | | |
| V _{CTC} | Analog Common Temperature Coefficient | — | — | — | — | 250kΩ Between Common and V+ |
| | | — | — | — | — | 0°C ≤ T _A ≤ +70°C ("C" Devices) |
| | | — | 80 | — | ppm/°C | TC7126 |
| | | — | 35 | 75 | ppm/°C | TC7126A |
| | | — | 35 | 100 | ppm/°C | -25°C ≤ T _A ≤ +85°C ("I" Device) (TC7126A) |
| V _C | Analog Common Voltage | 2.7 | 3.05 | 3.35 | V | 250kΩ Between Common and V+ |

- Note**
- 1: Input voltages may exceed the supply voltages, provided the input current is limited to ±100μA.
 - 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
 - 3: Refer to "Differential Input" discussion.
 - 4: Backplane drive is in phase with segment drive for "OFF" segment, 180° out of phase for "ON" segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.
 - 5: See "Typical Application".
 - 6: During Auto-Zero phase, current is 10-20μA higher. A 48kHz oscillator increases current by 8μA (Typical). Common current is not included.

TC7126/A

TC7126/A ELECTRICAL SPECIFICATIONS (CONTINUED)

| Electrical Characteristics: $V_S = +9V$, $f_{CLK} = 16kHz$, and $T_A = +25^\circ C$, unless otherwise noted. | | | | | | |
|---|-----------------------------|-----|-----|-----|-----------|---|
| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
| LCD Drive | | | | | | |
| V_{SD} | LCD Segment Drive Voltage | 4 | 5 | 6 | V_{P-P} | V_+ to $V_- = 9V$ |
| V_{BD} | LCD Backplane Drive Voltage | 4 | 5 | 6 | V_{P-P} | V_+ to $V_- = 9V$ |
| Power Supply | | | | | | |
| I_S | Power Supply Current | — | 55 | 100 | μA | $V_{IN} = 0V$, V_+ to $V_- = 9V$ (Note 6) |

- Note**
- 1: Input voltages may exceed the supply voltages, provided the input current is limited to $\pm 100\mu A$.
 - 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
 - 3: Refer to "Differential Input" discussion.
 - 4: Backplane drive is in phase with segment drive for "OFF" segment, 180° out of phase for "ON" segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.
 - 5: See "Typical Application".
 - 6: During Auto-Zero phase, current is 10-20 μA higher. A 48kHz oscillator increases current by 8 μA (Typical). Common current is not included.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

| Pin Number (40-Pin PDIP) Normal | (Reversed) | Symbol | Description |
|---------------------------------------|------------|-------------------|---|
| 1 | (40) | V+ | Positive supply voltage. |
| 2 | (39) | D ₁ | Activates the D section of the units display. |
| 3 | (38) | C ₁ | Activates the C section of the units display. |
| 4 | (37) | B ₁ | Activates the B section of the units display. |
| 5 | (36) | A ₁ | Activates the A section of the units display. |
| 6 | (35) | F ₁ | Activates the F section of the units display. |
| 7 | (34) | G ₁ | Activates the G section of the units display. |
| 8 | (33) | E ₁ | Activates the E section of the units display. |
| 9 | (32) | D ₂ | Activates the D section of the tens display. |
| 10 | (31) | C ₂ | Activates the C section of the tens display. |
| 11 | (30) | B ₂ | Activates the B section of the tens display. |
| 12 | (29) | A ₂ | Activates the A section of the tens display. |
| 13 | (28) | F ₂ | Activates the F section of the tens display. |
| 14 | (27) | E ₂ | Activates the E section of the tens display. |
| 15 | (26) | D ₃ | Activates the D section of the hundreds display. |
| 16 | (25) | B ₃ | Activates the B section of the hundreds display. |
| 17 | (24) | F ₃ | Activates the F section of the hundreds display. |
| 18 | (23) | E ₃ | Activates the E section of the hundreds display. |
| 19 | (22) | AB ₄ | Activates both halves of the 1 in the thousands display. |
| 20 | (21) | POL | Activates the negative polarity display. |
| 21 | (20) | BP | LCD Backplane drive output (TC7106A). Digital Ground (TC7107A). |
| 22 | (19) | G ₃ | Activates the G section of the hundreds display. |
| 23 | (18) | A ₃ | Activates the A section of the hundreds display. |
| 24 | (17) | C ₃ | Activates the C section of the hundreds display. |
| 25 | (16) | G ₂ | Activates the G section of the tens display. |
| 26 | (15) | V- | Negative power supply voltage. |
| 27 | (14) | V _{INT} | The integrating capacitor should be selected to give the maximum voltage swing that ensures component tolerance buildup will not allow the integrator output to saturate. When analog common is used as a reference and the conversion rate is 3 readings per second, a 0.047μF capacitor may be used. The capacitor must have a low dielectric constant to prevent rollover errors. See Section 6.3, Integrating Capacitor for additional details. |
| 28 | (13) | V _{BUFF} | Integration resistor connection. Use a 180kΩ resistor for a 200mV full-scale range and a 1.8MΩ resistor for a 2V full scale range. |
| 29 | (12) | C _{AZ} | The size of the auto-zero capacitor influences system noise. Use a 0.33μF capacitor for 200mV full scale, and a 0.033μF capacitor for 2V full scale. See Section 6.1, Auto-Zero Capacitor for additional details. |
| 30 | (11) | V _{IN-} | The analog LOW input is connected to this pin. |
| 31 | (10) | V _{IN+} | The analog HIGH input signal is connected to this pin. |
| 32 | (9) | ANALOG COMMON | This pin is primarily used to set the Analog Common mode voltage for battery operation, or in systems where the input signal is referenced to the power supply. It also acts as a reference voltage source. See Section 7.3, Analog Common for additional details. |
| 33 | (8) | C _{REF-} | See Pin 34. |

TC7126/A

TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

| Pin Number (40-Pin PDIP) Normal | (Reversed) | Symbol | Description |
|---------------------------------------|------------|-------------------|--|
| 34 | (7) | C _{REF+} | A 0.1 μ F capacitor is used in most applications. If a large Common mode voltage exists (for example, the V _{IN-} pin is not at analog common) and a 200mV scale is used, a 1 μ F capacitor is recommended and will hold the rollover error to 0.5 count. |
| 35 | (6) | V _{REF-} | See Pin 36. |
| 36 | (5) | V _{REF+} | The analog input required to generate a full scale output (1999 counts). Place 100mV between Pins 35 and 36 for 199.9mV full scale. Place 1V between Pins 35 and 36 for 2V full scale. See Section 6.6, Reference Voltage for additional information. |
| 37 | (4) | TEST | Lamp test. When pulled HIGH (to V+), all segments will be turned on and the display should read -1888. It may also be used as a negative supply for externally generated decimal points. See Section 7.4, TEST for additional information. |
| 38 | (3) | OSC3 | See Pin 40. |
| 39 | (2) | OSC2 | See Pin 40. |
| 40 | (1) | OSC1 | Pins 40, 39 and 38 make up the oscillator section. For a 48kHz clock (3 readings, 39 per second), connect Pin 40 to the junction of a 180k Ω resistor and a 50pF capacitor. The 180k Ω resistor is tied to Pin 39 and the 50pF capacitor is tied to Pin 38. |

4.0 ANALOG SECTION

In addition to the basic integrate and de-integrate dual slope cycles discussed above, the TC7126A design incorporates an auto-zero cycle. This cycle removes buffer amplifier, integrator and comparator offset voltage error terms from the conversion. A true digital zero reading results without external adjusting potentiometers. A complete conversion consists of three phases:

1. Auto-Zero phase
2. Signal Integrate phase
3. Reference Integrate phase

4.1 Auto-Zero Phase

During the auto-zero phase, the differential input signal is disconnected from the circuit by opening internal analog gates. The internal nodes are shorted to analog common (ground) to establish a zero input condition. Additional analog gates close a feedback loop around the integrator and comparator. This loop permits comparator offset voltage error compensation. The voltage level established on C_{AZ} compensates for device offset voltages. The auto-zero phase residual is typically $10\mu V$ to $15\mu V$. The auto-zero cycle length is 1000 to 3000 clock periods.

4.2 Signal Integrate Phase

The auto-zero loop is entered and the internal differential inputs connect to V_{IN+} and V_{IN-} . The differential input signal is integrated for a fixed time period. The TC7126/A signal integration period is 1000 clock periods or counts. The externally set clock frequency is divided by four before clocking the internal counters. The integration time period is:

EQUATION 4-1:

$$T_{SI} = \frac{4}{F_{OSC}} \times 1000$$

Where: F_{OSC} = external clock frequency.

The differential input voltage must be within the device Common mode range when the converter and measured system share the same power supply common (ground). If the converter and measured system do not share the same power supply common, V_{IN-} should be tied to analog common.

Polarity is determined at the end of signal integrate phase. The sign bit is a true polarity indication, in that signals less than 1LSB are correctly determined. This allows precision null detection limited only by device noise and auto-zero residual offsets.

4.3 Reference Integrate Phase

The third phase is reference integrate or de-integrate. V_{IN-} is internally connected to analog common and V_{IN+} is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal and is between 0 and 2000 counts. The digital reading displayed is:

EQUATION 4-2:

$$1000 \frac{V_{IN}}{V_{REF}}$$

5.0 DIGITAL SECTION

The TC7126A contains all the segment drivers necessary to directly drive a 3-1/2 digit LCD, including an LCD backplane driver. The backplane frequency is the external clock frequency divided by 800. For 3 conversions per second, the backplane frequency is 60Hz with a 5V nominal amplitude. When a segment driver is in phase with the backplane signal, the segment is OFF. An out of phase segment drive signal causes the segment to be ON (visible). This AC drive configuration results in negligible DC voltage across each LCD segment, ensuring long LCD life. The polarity segment driver is ON for negative analog inputs. If V_{IN+} and V_{IN-} are reversed, this indicator reverses.

On the TC7126A, when the TEST pin is pulled to $V+$, all segments are turned ON and the display reads -1888. During this mode, LCD segments have a constant DC voltage impressed.

Note: Do not leave the display in this mode for more than several minutes. LCDs may be destroyed if operated with DC levels for extended periods.

The display font and segment drive assignment are shown in Figure 5-1.

FIGURE 5-1: DISPLAY FONT AND SEGMENT ASSIGNMENT



5.1 System Timing

The oscillator frequency is divided by four prior to clocking the internal decade counters. The four-phase measurement cycle takes a total of 4000 counts (16,000 clock pulses). The 4000-count cycle is independent of input signal magnitude.

Each phase of the measurement cycle has the following length:

1. Auto-Zero Phase: 1000 to 3000 counts (4000 to 12,000 clock pulses).

For signals less than full scale, the auto-zero phase is assigned the unused reference integrate time period.

2. Signal Integrate: 1000 counts (4000 clock pulses).

This time period is fixed. The integration period is:

EQUATION 5-1:

$$T_{SI} = 4000 \frac{1}{F_{OSC}}$$

Where: F_{OSC} is the externally set clock frequency.

3. Reference Integrate: 0 to 2000 counts (0 to 8000 clock pulses).

The TC7126A is a drop-in replacement for the TC7126 and ICL7126, which offer a greatly improved internal reference temperature coefficient. No external component value changes are required to upgrade existing designs.

6.0 COMPONENT VALUE SELECTION

6.1 Auto-Zero Capacitor (C_{AZ})

The C_{AZ} capacitor size has some influence on system noise. A $0.47\mu\text{F}$ capacitor is recommended for 200mV full scale applications where 1LSB is $100\mu\text{V}$. A $0.033\mu\text{F}$ capacitor is adequate for 2.0V full scale applications. A mylar type dielectric capacitor is adequate.

6.2 Reference Voltage Capacitor (C_{REF})

The reference voltage, used to ramp the integrator output voltage back to zero during the reference integrate phase, is stored on C_{REF} . A $0.1\mu\text{F}$ capacitor is acceptable when V_{REF-} is tied to analog common. If a large Common mode voltage exists (V_{REF-} – analog common) and the application requires a 200mV full scale, increase C_{REF} to $1\mu\text{F}$. Rollover error will be held to less than 0.5 count. A Mylar type dielectric capacitor is adequate.

6.3 Integrating Capacitor (C_{INT})

C_{INT} should be selected to maximize integrator output voltage swing without causing output saturation. Due to the TC7126A's superior analog common temperature coefficient specification, analog common will normally supply the differential voltage reference. For this case, a $\pm 2\text{V}$ full scale integrator output swing is satisfactory. For 3 readings per second ($F_{OSC} = 48\text{kHz}$), a $0.047\mu\text{F}$ value is suggested. For 1 reading per second, $0.15\mu\text{F}$ is recommended. If a different oscillator frequency is used, C_{INT} must be changed in inverse proportion to maintain the nominal $\pm 2\text{V}$ integrator swing.

An exact expression for C_{INT} is:

EQUATION 6-1:

$$C_{INT} = \frac{(4000) \left(\frac{1}{F_{OSC}} \right) \left(\frac{V_{FS}}{R_{INT}} \right)}{V_{INT}}$$

Where:

- F_{OSC} = Clock frequency at Pin 38
- V_{FS} = Full scale input voltage
- R_{INT} = Integrating resistor
- V_{INT} = Desired full scale integrator output swing

At 3 readings per second, a 750Ω resistor should be placed in series with C_{INT} . This increases accuracy by compensating for comparator delay. C_{INT} must have low dielectric absorption to minimize rollover error. A polypropylene capacitor is recommended.

6.4 Integrating Resistor (R_{INT})

The input buffer amplifier and integrator are designed with Class A output stages. The output stage idling current is $6\mu\text{A}$. The integrator and buffer can supply $1\mu\text{A}$ drive current with negligible linearity errors. R_{INT} is chosen to remain in the output stage linear drive region, but not so large that PC board leakage currents induce errors. For a 200mV full scale, R_{INT} is $180\text{k}\Omega$. A 2V full scale requires $1.8\text{M}\Omega$.

| Component Value | Nominal Full Scale Voltage | |
|-----------------|----------------------------|---------------------|
| | 200mV | 2V |
| C_{AZ} | $0.33\mu\text{F}$ | $0.033\mu\text{F}$ |
| R_{INT} | $180\text{k}\Omega$ | $1.8\text{M}\Omega$ |
| C_{INT} | $0.047\mu\text{F}$ | $0.047\mu\text{F}$ |

Note: $F_{OSC} = 48\text{kHz}$ (3 readings per sec).

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6.5 Oscillator Components

C_{OSC} should be 50pF; R_{OSC} is selected from the equation:

EQUATION 6-2:

$$F_{OSC} = \frac{0.45}{RC}$$

For a 48kHz clock (3 conversions per second), $R = 180k\Omega$.

Note that F_{OSC} is 44 to generate the TC7126A's internal clock. The backplane drive signal is derived by dividing F_{OSC} by 800.

To achieve maximum rejection of 60Hz noise pickup, the signal integrate period should be a multiple of 60Hz. Oscillator frequencies of 24kHz, 12kHz, 80kHz, 60kHz, 40kHz, etc. should be selected. For 50Hz rejection, oscillator frequencies of 20kHz, 100kHz, 66-2/3kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings per second) will reject both 50Hz and 60Hz.

6.6 Reference Voltage Selection

A full scale reading (2000 counts) requires the input signal be twice the reference voltage.

| Required Full Scale Voltage* | V_{REF} |
|------------------------------|-----------|
| 20mV | 100mV |
| 2V | 1V |

Note: $V_{FS} = 2V_{REF}$

In some applications, a scale factor other than unity may exist between a transducer output voltage and the required digital reading. Assume, for example, a pressure transducer output for 2000lb/in² is 400mV. Rather than dividing the input voltage by two, the reference voltage should be set to 200mV. This permits the transducer input to be used directly.

The differential reference can also be used where a digital zero reading is required when V_{IN} is not equal to zero. This is common in temperature measuring instrumentation. A compensating offset voltage can be applied between analog common and V_{IN-} . The transducer output is connected between V_{IN+} and analog common.

7.0 DEVICE PIN FUNCTIONAL DESCRIPTION

(Pin Numbers Refer to the 40-Pin PDIP.)

7.1 Differential Signal Inputs V_{IN+} (Pin 31), V_{IN-} (Pin 30)

The TC7126A is designed with true differential inputs and accepts input signals within the input stage Common mode voltage range (V_{CM}). Typical range is $V_+ - 1V$ to $V_- + 1V$. Common mode voltages are removed from the system when the TC7126A operates from a battery or floating power source (isolated from measured system), and V_{IN-} is connected to analog common (V_{COM}) (see Figure 7-2).

In systems where Common mode voltages exist, the TC7126A's 86 dB Common mode rejection ratio minimizes error. Common mode voltages do, however, affect the integrator output level. A worst case condition exists if a large positive V_{CM} exists in conjunction with a full scale negative differential signal. The negative signal drives the integrator output positive along with V_{CM} (see Figure 7-1). For such applications, the integrator output swing can be reduced below the recommended 2V full scale swing. The integrator output will swing within 0.3V of V_+ or V_- without increased linearity error.

FIGURE 7-1: COMMON MODE VOLTAGE REDUCES AVAILABLE INTEGRATOR SWING ($V_{COM} \neq V_{IN}$)



TC7126/A

7.5 TC7126A Internal Voltage Reference

The TC7126A's analog common voltage temperature stability has been significantly improved (Figure 7-3). The "A" version of the industry standard TC7126 device allows users to upgrade old systems and design new systems, without external voltage references. External R and C values do not need to be changed. Figure 7-4 shows analog common supplying the necessary voltage reference for the TC7126A.

FIGURE 7-3: ANALOG COMMON TEMP. COEFFICIENT

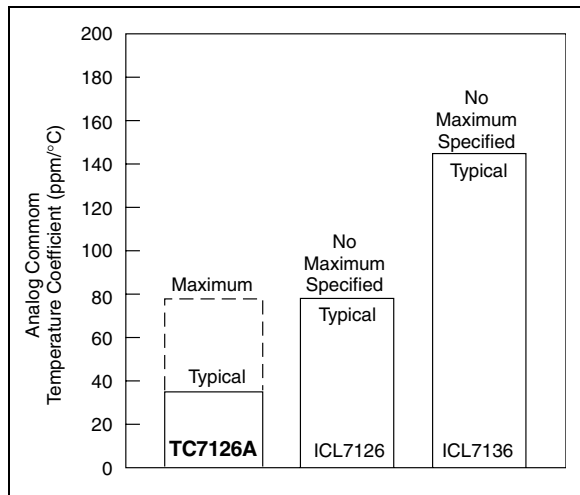
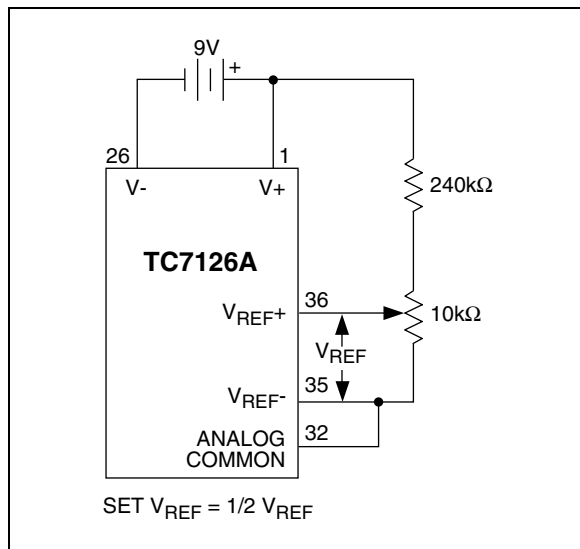


FIGURE 7-4: TC7126A INTERNAL VOLTAGE REFERENCE CONNECTION



8.0 TYPICAL APPLICATIONS

8.1 Liquid Crystal Display Sources

Several manufacturers supply standard LCDs to interface with the TC7126A, 3-1/2 digit analog-to-digital converter.

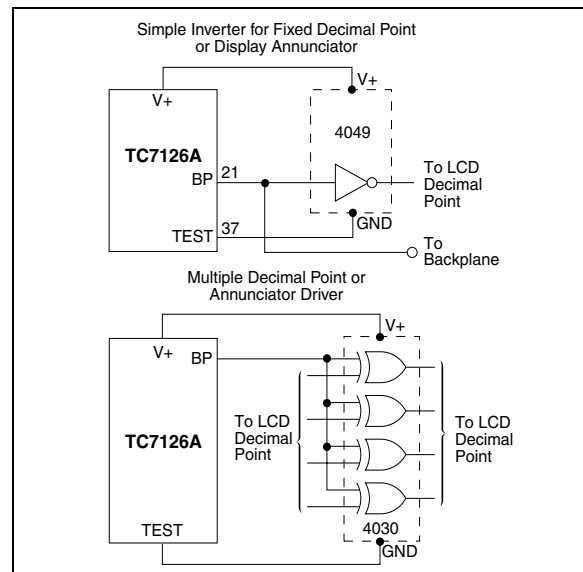
| Manufacturer | Address/Phone | Representative Part Numbers* |
|------------------------|--|-------------------------------|
| Crystaloid Electronics | 5282 Hudson Dr. Hudson, OH 44236 216-655-2429 | C5335, H5535, T5135, SX440 |
| AND | 720 Palomar Ave. Sunnyvale, CA 94086 408-523-8200 | FE 0801 FE 0203 |
| VGI, Inc. | 1800 Vernon St., Ste. 2 Roseville, CA 95678 916-783-7878 | LD-B709BZ LD-H7992AZ |
| Hamlin, Inc. | 612 E. Lake St. Lake Mills, WI 53551 414-648-2361 | 3902, 3933, 3903 |

Note: Contact LCD manufacturer for full product listing/specifications.

8.2 Decimal Point and Annunciator Drive

The TEST pin is connected to the internally generated digital logic supply ground through a 500Ω resistor. The TEST pin may be used as the negative supply for external CMOS gate segment drivers. LCD annunciators for decimal points, low battery indication, or function indication may be added, without adding an additional supply. No more than 1mA should be supplied by the TEST pin; its potential is approximately 5V below V+ (see Figure 8-1).

FIGURE 8-1: DECIMAL POINT AND ANNUNCIATOR DRIVES



8.3 Flat Package

The TC7126 is available in an epoxy 64-pin formed lead package. A test socket for the TC7126ACBQ device is available:

Part Number: IC 51-42
 Manufacturer: Yamaichi
 Distribution: Nepenthe Distribution
 2471 East Bayshore, Ste. 520
 Palo Alto, CA 94043
 (650) 856-9332

8.4 Ratiometric Resistance Measurements

The TC7126A's true differential input and differential reference make ratiometric reading possible. In a ratiometric operation, an unknown resistance is measured with respect to a known standard resistance. No accurately defined reference voltage is needed.

The unknown resistance is put in series with a known standard and a current passed through the pair. The voltage developed across the unknown is applied to the input and the voltage across the known resistor is applied to the reference input. If the unknown equals the standard, the display will read 1000. The displayed reading can be determined from the following expression:

EQUATION 8-1:

$$\text{Displayed (Reading)} = \frac{R_{\text{UNKNOWN}}}{R_{\text{STANDARD}}} \times 1000$$

The display will over range for $R_{\text{UNKNOWN}} \geq 2 \times R_{\text{STANDARD}}$ (see Figure 8-2).

FIGURE 8-2: LOW PARTS COUNT RATIOMETRIC RESISTANCE MEASUREMENT



FIGURE 8-3: 3-1/2 DIGIT TRUE RMS AC DMM



TC7126/A

FIGURE 8-4: INTEGRATED CIRCUIT TEMPERATURE SENSOR



FIGURE 8-5: TEMPERATURE SENSOR

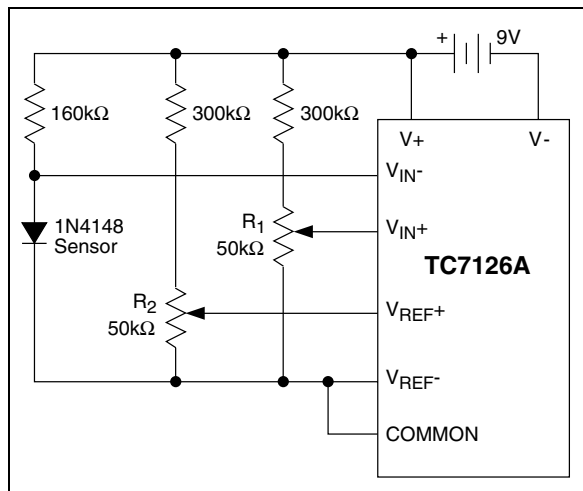
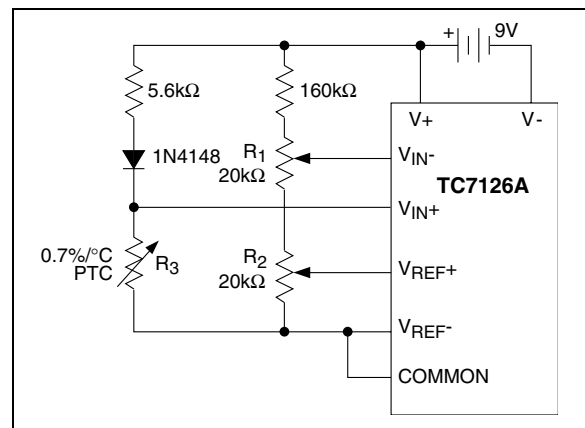


FIGURE 8-6: POSITIVE TEMPERATURE COEFFICIENT RESISTOR TEMPERATURE SENSOR



9.0 PACKAGING INFORMATION

9.1 Package Marking Information

Package marking data not available at this time.

9.2 Taping Form

Component Taping Orientation for 44-Pin PLCC Devices

Standard Reel Component Orientation
for TR Suffix Device

| Package | Carrier Width (W) | Pitch (P) | Part Per Full Reel | Reel Size |
|-------------|-------------------|-----------|--------------------|-----------|
| 44-Pin PLCC | 32 mm | 24 mm | 500 | 13 in |

Note: Drawing does not represent total number of pins.

Component Taping Orientation for 44-Pin PQFP Devices

Standard Reel Component Orientation
for TR Suffix Device

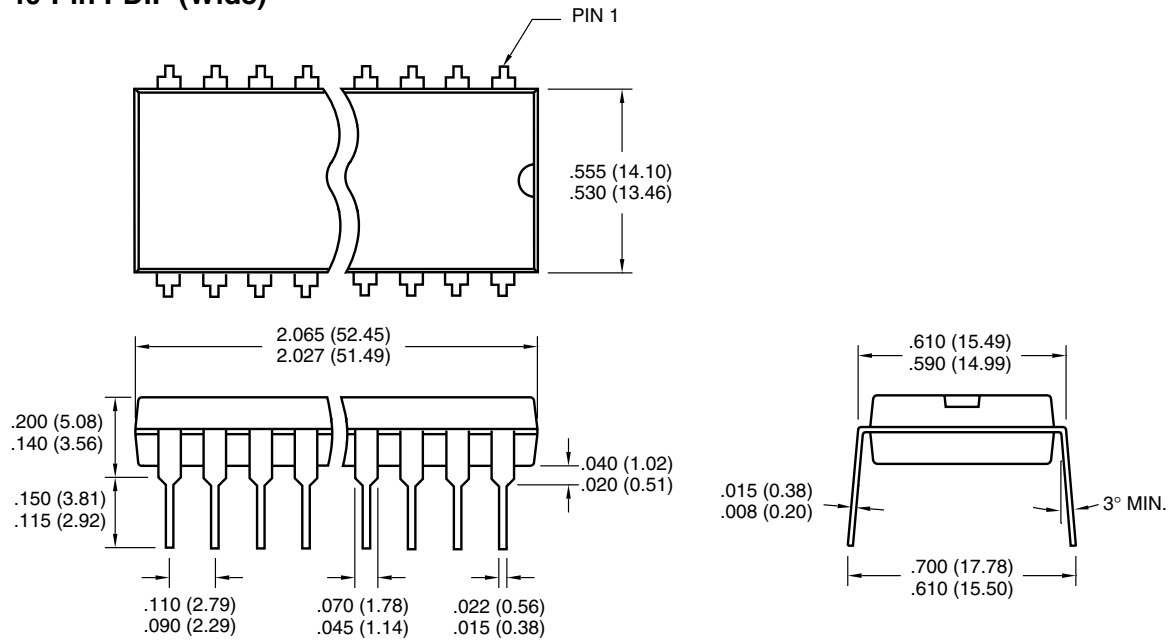
| Package | Carrier Width (W) | Pitch (P) | Part Per Full Reel | Reel Size |
|-------------|-------------------|-----------|--------------------|-----------|
| 44-Pin PQFP | 24 mm | 16 mm | 500 | 13 in |

Note: Drawing does not represent total number of pins.

TC7126/A

9.3 Package Dimensions

40-Pin PDIP (Wide)



Dimensions: inches (mm)

44-Pin PLCC



Dimensions: inches (mm)

9.3 Package Dimensions (Continued)



TC7126/A

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| | |
|--|----------------------|
| PART CODE | TC7126X X XXX |
| A or blank* _____ | |
| R (reversed pins) or blank (CPL pkg only) _____ | |
| * "A" parts have an improved reference TC | |
| Package Code (see Device Selection Table) _____ | |

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Web Address: <http://www.microchip.com>

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New York

150 Motor Parkway, Suite 202
Hauppauge, NY 11788
Tel: 631-273-5305 Fax: 631-273-5335

San Jose

Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950 Fax: 408-436-7955

Toronto

6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699 Fax: 905-673-6509

ASIA/PACIFIC

Australia

Microchip Technology Australia Pty Ltd
Suite 22, 41 Rawson Street
Epping 2121, NSW
Australia
Tel: 61-2-9868-6733 Fax: 61-2-9868-6755

China - Beijing

Microchip Technology Consulting (Shanghai)
Co., Ltd., Beijing Liaison Office
Unit 915
Bei Hai Wan Tai Bldg.
No. 6 Chaoyangmen Beidajie
Beijing, 100027, No. China
Tel: 86-10-85282100 Fax: 86-10-85282104

China - Chengdu

Microchip Technology Consulting (Shanghai)
Co., Ltd., Chengdu Liaison Office
Rm. 2401, 24th Floor,
Ming Xing Financial Tower
No. 88 TIDU Street
Chengdu 610016, China
Tel: 86-28-6766200 Fax: 86-28-6766599

China - Fuzhou

Microchip Technology Consulting (Shanghai)
Co., Ltd., Fuzhou Liaison Office
Unit 28F, World Trade Plaza
No. 71 Wusi Road
Fuzhou 350001, China
Tel: 86-591-7503506 Fax: 86-591-7503521

China - Shanghai

Microchip Technology Consulting (Shanghai)
Co., Ltd.
Room 701, Bldg. B
Far East International Plaza
No. 317 Xian Xia Road
Shanghai, 200051
Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

China - Shenzhen

Microchip Technology Consulting (Shanghai)
Co., Ltd., Shenzhen Liaison Office
Rm. 1315, 13/F, Shenzhen Kerry Centre,
Renminnan Lu
Shenzhen 518001, China
Tel: 86-755-2350361 Fax: 86-755-2366086

Hong Kong

Microchip Technology Hongkong Ltd.
Unit 901-6, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200 Fax: 852-2401-3431

India

Microchip Technology Inc.
India Liaison Office
Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaugnessey Road
Bangalore, 560 025, India
Tel: 91-80-2290061 Fax: 91-80-2290062

Japan

Microchip Technology Japan K.K.
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471-6166 Fax: 81-45-471-6122

Korea

Microchip Technology Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea 135-882
Tel: 82-2-554-7200 Fax: 82-2-558-5934

Singapore

Microchip Technology Singapore Pte Ltd.
200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-6334-8870 Fax: 65-6334-8850

Taiwan

Microchip Technology Taiwan
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

Denmark

Microchip Technology Nordic ApS
Regus Business Centre
Lautrup høj 1-3
Ballerup DK-2750 Denmark
Tel: 45 4420 9895 Fax: 45 4420 9910

France

Microchip Technology SARL
Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - 1er Etage
91300 Massy, France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany

Microchip Technology GmbH
Gustav-Heinemann Ring 125
D-81739 Munich, Germany
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

Italy

Microchip Technology SRL
Centro Direzionale Colleoni
Palazzo Taurus 1 V. Le Colleoni 1
20041 Agrate Brianza
Milan, Italy
Tel: 39-039-65791-1 Fax: 39-039-6899883

United Kingdom

Arizona Microchip Technology Ltd.
505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
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