

KAI-47051

8856 (H) x 5280 (V) Interline CCD Image Sensor

Description

The KAI-47051 Image Sensor is a 47-megapixel CCD designed for the most demanding inspection and surveillance applications. Based on an advanced 5.5-micron Interline Transfer CCD Platform, the sensor features broad dynamic range and excellent imaging performance and uniformity. Full resolution readout of up to 7 frames per second is enabled through a multi-tap output architecture, and a vertical overflow drain structure suppresses image blooming and enables electronic shuttering for precise exposure control.

The sensor is electrically similar to other devices in the 5.5-micron Interline Transfer CCD Platform, allowing cameras designed for that platform to be leveraged in support of this high-resolution device.

Table 1. GENERAL SPECIFICATIONS

| Parameter | Typical Value |
|--|---|
| Architecture | Interline CCD, Progressive Scan |
| Total Number of Pixels | 8880 (H) × 5392 (V) |
| Number of Effective Pixels | 8880 (H) × 5304 (V) |
| Number of Active Pixels | 8856 (H) × 5280 (V) |
| Pixel Size | 5.5 μm (H) × 5.5 μm (V) |
| Active Image Size | 48.7 mm (H) × 29.0 mm (V) 56.7 mm (diagonal) |
| Aspect Ratio | 5:3 |
| Number of Outputs | 8 or 16 |
| Charge Capacity | 20,000 electrons |
| Output Sensitivity | 38 μV/e ⁻ |
| Quantum Efficiency Pan (-AXA, -QXA) R, G, B (-FXA, -QXA) | 43% 28%, 35%, 38% |
| Read Noise (f = 40 MHz) | 10 e ⁻ rms |
| Dark Current Photodiode / VCCD | 7 / 140 e ⁻ /s |
| Dark Current Doubling Temp Photodiode / VCCD | 7°C / 9°C |
| Dynamic Range | 66 dB |
| Charge Transfer Efficiency | 0.999999 |
| Blooming Suppression | > 300 X |
| Smear | -100 dB |
| Image Lag | < 10 electrons |
| Maximum Pixel Clock Speed | 40 MHz |
| Maximum Frame Rate 8 Outputs / 16 Outputs | 3.5 fps / 7.0 fps |
| Package Options | 201 Pin PGA |
| Cover Glass | AR Coated, 2-Sides |

NOTE: All Parameters are specified at T = 40°C unless otherwise noted.



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Figure 1. KAI-47051 Image Sensor

Features

- Bayer Color Pattern, Sparse Color Filter Pattern, and Monochrome Configurations
- Progressive Scan Readout
- Flexible Readout Architecture
- High Frame Rate
- High Sensitivity
- Low Noise Architecture
- Excellent Smear Performance

Applications

- Industrial Imaging and Inspection
- Aerial Surveillance
- Security

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ORDERING INFORMATION

Table 2. ORDERING INFORMATION

| Part Number | Description | Marking Code |
|---------------------|---|--------------------------------|
| KAI-47051-AXA-JD-B1 | Monochrome, Special Microlens, PGA Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Grade 1 | KAI-47051-AXA Serial Number |
| KAI-47051-AXA-JD-B2 | Monochrome, Special Microlens, PGA Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Grade 2 | |
| KAI-47051-AXA-JD-AE | Monochrome, Special Microlens, PGA Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Engineering Grade | |
| KAI-47051-FXA-JD-B1 | Gen2 Color (Bayer RGB), Special Microlens, PGA Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Grade 1 | KAI-47051-FXA Serial Number |
| KAI-47051-FXA-JD-B2 | Gen2 Color (Bayer RGB), Special Microlens, PGA Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Grade 2 | |
| KAI-47051-FXA-JD-AE | Gen2 Color (Bayer RGB), Special Microlens, PGA Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Engineering Grade | |
| KAI-47051-QXA-JD-B1 | Gen2 Color (Sparse CFA), Special Microlens, PGA Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Grade 1 | KAI-47051-QXA Serial Number |
| KAI-47051-QXA-JD-B2 | Gen2 Color (Sparse CFA), Special Microlens, PGA Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Grade 2 | |
| KAI-47051-QXA-JD-AE | Gen2 Color (Sparse CFA), Special Microlens, PGA Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Engineering Grade | |

See the ON Semiconductor *Device Nomenclature* document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

DEVICE DESCRIPTION

Architecture



Figure 2. Block Diagram



Figure 3. HCCD and Output Detail

Dark Pixels

There are 44 dark rows at the top and 44 dark rows at the bottom of the image sensor. The dark rows are not entirely dark and so should not be used for a dark reference level.

Dummy Pixels

Within each horizontal shift register there are 6 leading additional shift phases. These pixels are designated as dummy pixels and should not be used to determine a dark reference level.

Active Buffer Pixels

On the perimeter of the sensor there are 12 unshielded rows and columns that are classified as active buffer pixels. These pixels are light sensitive but are not tested for defects and non-uniformities.

Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the individual silicon photodiodes. These photoelectrons are collected locally by the formation of potential wells at each photo-site. Below photodiode saturation, the number of photoelectrons collected at each pixel is linearly dependent upon light level and exposure time and non-linearly dependent on

wavelength. When the photodiodes charge capacity is reached, excess electrons are discharged into the substrate to prevent blooming.

ESD Protection

Adherence to the power-up and power-down sequence is critical. Failure to follow the proper power-up and power-down sequences may cause damage to the sensor. See Power-Up and Power-Down Sequence section.

Bayer Color Filter Pattern



Figure 4. Bayer Color Filter Pattern

Sparse Color Filter Pattern



Figure 5. Sparse Color Filter Pattern

Physical Description

Pin Description and Device Orientation



Figure 6. Package Pin Designations – Top View



Figure 7. Package Pin Designations – Bottom View

KAI-47051

Table 3. PACKAGE PIN DESCRIPTION

| Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name |
|-----|-------|-----|-------|-----|----------|-----|-------|-----|-------|
| 1 | N/C | 41 | VOUTh | 81 | VOUTh | 121 | VOUTh | 161 | VOUTh |
| 2 | SUB | 42 | VDDd | 82 | VDDh | 122 | VDDp | 162 | VDDI |
| 3 | ESD | 43 | RDd | 83 | RDh | 123 | HLODo | 163 | HLODk |
| 4 | GND | 44 | GND | 84 | GND | 124 | H1o | 164 | H1k |
| 5 | V3B | 45 | OGd | 85 | OGh | 125 | H2Lo | 165 | H2Lk |
| 6 | V4B | 46 | Rd | 86 | Rh | 126 | H2o | 166 | H2k |
| 7 | V1B | 47 | H2Ld | 87 | H2Lh | 127 | OGO | 167 | OGk |
| 8 | FDDB | 48 | H2d | 88 | H2h | 128 | Ro | 168 | Rk |
| 9 | V2B | 49 | HLODd | 89 | HLODh | 129 | RDo | 169 | RDk |
| 10 | FDGB | 50 | H1d | 90 | H1h | 130 | GND | 170 | GND |
| 11 | VOUta | 51 | VOUte | 91 | V1B | 131 | VOUto | 171 | VOUtk |
| 12 | VDDa | 52 | VDDe | 92 | V2B | 132 | VDDo | 172 | VDDk |
| 13 | RDa | 53 | RDe | 93 | SUB | 133 | HLODn | 173 | HLODj |
| 14 | GND | 54 | GND | 94 | FDGB | 134 | H1n | 174 | H1j |
| 15 | OGa | 55 | OGe | 95 | V3B | 135 | H2Ln | 175 | H2Lj |
| 16 | Ra | 56 | Re | 96 | FDDB | 136 | H2n | 176 | H2j |
| 17 | H2La | 57 | H2Le | 97 | GND | 137 | OGn | 177 | OGj |
| 18 | H2a | 58 | H2e | 98 | V4B | 138 | Rn | 178 | Rj |
| 19 | HLODa | 59 | HLODe | 99 | TANODE | 139 | RDn | 179 | RDj |
| 20 | H1a | 60 | H1e | 100 | ESD | 140 | GND | 180 | GND |
| 21 | VOUtb | 61 | VOUte | 101 | TCATHODE | 141 | VOUtn | 181 | VOUte |
| 22 | VDDb | 62 | VDDf | 102 | n/c | 142 | VDDn | 182 | VDDj |
| 23 | RDb | 63 | RDf | 103 | n/c | 143 | HLODm | 183 | HLODi |
| 24 | GND | 64 | GND | 104 | ESD | 144 | H1m | 184 | H1i |
| 25 | OGb | 65 | OGf | 105 | GND | 145 | H2Lm | 185 | H2Li |
| 26 | Rb | 66 | Rf | 106 | V4T | 146 | H2m | 186 | H2i |
| 27 | H2Lb | 67 | H2Lf | 107 | V3T | 147 | OGm | 187 | OGi |
| 28 | H2b | 68 | H2f | 108 | FDDT | 148 | Rm | 188 | Ri |
| 29 | HLODb | 69 | HLODf | 109 | SUB | 149 | RDm | 189 | RDj |
| 30 | H1b | 70 | H1f | 110 | FDGT | 150 | GND | 190 | GND |
| 31 | VOUtc | 71 | VOUtg | 111 | V1T | 151 | VOUtm | 191 | VOUti |
| 32 | VDDc | 72 | VDDg | 112 | V2T | 152 | VDDm | 192 | VDDi |
| 33 | RDc | 73 | RDg | 113 | HLODp | 153 | HLODi | 193 | V2T |
| 34 | GND | 74 | GND | 114 | H1p | 154 | H1l | 194 | FDGT |
| 35 | OGc | 75 | OGg | 115 | H2Lp | 155 | H2Li | 195 | V1T |
| 36 | Rc | 76 | Rg | 116 | H2p | 156 | H2l | 196 | FDDT |
| 37 | H2Lc | 77 | H2Lg | 117 | OGp | 157 | OGl | 197 | V3T |
| 38 | H2c | 78 | H2g | 118 | Rp | 158 | Rl | 198 | V4T |
| 39 | HLODc | 79 | HLODg | 119 | RDp | 159 | RDi | 199 | ESD |
| 40 | H1c | 80 | H1g | 120 | GND | 160 | GND | 200 | GND |
| | | | | | | | | 201 | SUB |

Table 4. PIN NAME DESCRIPTIONS

| Pin Name(s) | Description |
|---------------|--|
| V1B, V1T | Vertical CCD Clock, Phase 1, Bottom (B) or Top (T) |
| V2B, V2T | Vertical CCD Clock, Phase 2, Bottom (B) or Top (T) |
| V3B, V3T | Vertical CCD Clock, Phase 3, Bottom (B) or Top (T) |
| V4B, V4T | Vertical CCD Clock, Phase 4, Bottom (B) or Top (T) |
| FDDB, FDDT | Fast Line Dump Drain, Bottom (B) or Top (T) |
| FDGB, FDGT | Fast Line Dump Gate, Bottom (B) or Top (T) |
| SUB | Substrate |
| GND | Ground |
| ESD | ESD Protection Disable |
| TANODE | Temperature Diode Anode |
| TCATHODE | Temperature Diode Cathode |
| N/C | No connect |
| VOU α | Video Output a to p |
| R α | Reset Gate a to p |
| RD α | Reset Drain a to p |
| OG α | Output Gate a to p |
| VDD α | Output Amplifier Supply a to p |
| H1 α | Horizontal CCD Clock, Phase 1, a to p |
| H2 α | Horizontal CCD Clock, Phase 2, a to p |
| H2L α | Horizontal CCD Clock, Phase 2, Last Phase, a to p |
| HLOD α | Horizontal CCD Overflow Drain, a to p |

IMAGING PERFORMANCE

Table 5. TYPICAL OPERATION CONDITIONS

Unless otherwise noted, the Imaging Performance Specifications are measured using the following conditions.

| Description | Condition | Notes |
|--------------|---|---|
| Light Source | Continuous red, green and blue LED illumination | For monochrome sensor, only green LED used. |
| Operation | Nominal operating voltages and timing | |

Table 6. PERFORMANCE PARAMETERS (Performance parameters are by design)

| Description | Symbol | Nom. | Units | Notes |
|--|----------------------|-------------------------------------|--------------------|-------|
| Maximum Photo-response Nonlinearity | NL | 2 | % | 2 |
| Horizontal CCD Charge Capacity | HNe | 55 | ke ⁻ | |
| Vertical CCD Charge Capacity | VNe | 40 | ke ⁻ | |
| Photodiode Charge Capacity | PNe | 20 | ke ⁻ | 3 |
| Image Lag | Lag | < 10 | e ⁻ | |
| Anti-blooming Factor | Xab | > 300X | | |
| Vertical Smear | Smr | -100 | dB | |
| Read Noise | n _{e-T} | 10 | e ⁻ rms | 4 |
| Dynamic Range | DR | 66 | dB | 4, 5 |
| Output Amplifier DC Offset | V _{odc} | 9.4 | V | |
| Output Amplifier Bandwidth | f _{-3db} | 250 | MHz | 6 |
| Output Amplifier Impedance | R _{OUT} | 127 | Ω | |
| Output Amplifier Sensitivity | ΔV/ΔN | 38 | μV/e ⁻ | |
| Peak Quantum Efficiency (KAI-47051-ABA and KAI-47051-QBA Configurations) | QE _{max} | 43 | % | |
| Peak Quantum Efficiency (KAI-47051-FBA and KAI-47051-QBA Configurations) | Blue Green Red | QE _{max} 37 35 29 | % | |

Table 7. PERFORMANCE SPECIFICATIONS

| Description | Symbol | Min. | Nom. | Max. | Units | Temperature Tested At (°C) | Notes |
|---|-----------------|----------|----------|------|-------|----------------------------|-------|
| Dark Field Global Non-Uniformity | DSNU | - | - | 5 | mVpp | 27, 40 | |
| Bright Field Global Non-Uniformity | | - | - | 5 | %rms | 27, 40 | 1 |
| Bright Field Global Peak to Peak Non-Uniformity | PRNU | - | - | 30 | %pp | 27, 40 | 1 |
| Horizontal CCD Charge Transfer Efficiency | HCTE | 0.999995 | 0.999999 | - | | | |
| Vertical CCD Charge Transfer Efficiency | VCTE | 0.999995 | 0.999999 | - | | | |
| Photodiode Dark Current | l _{pd} | - | 7 | 70 | e/p/s | 40 | |
| Vertical CCD Dark Current | l _{vd} | - | 100 | 300 | e/p/s | 40 | |

1. Per color
2. Value is over the range of 10% to 90% of photodiode saturation.
3. The operating value of the substrate voltage, VAB, will be marked on the shipping container for each device. The value of VAB is set such that the photodiode charge capacity is 680 mV.
4. At 40 MHz
5. Uses 20LOG (PNe/ n_{e-T})
6. Assumes 5 pF load.

TYPICAL PERFORMANCE CURVES

Quantum Efficiency

Monochrome with Microlens

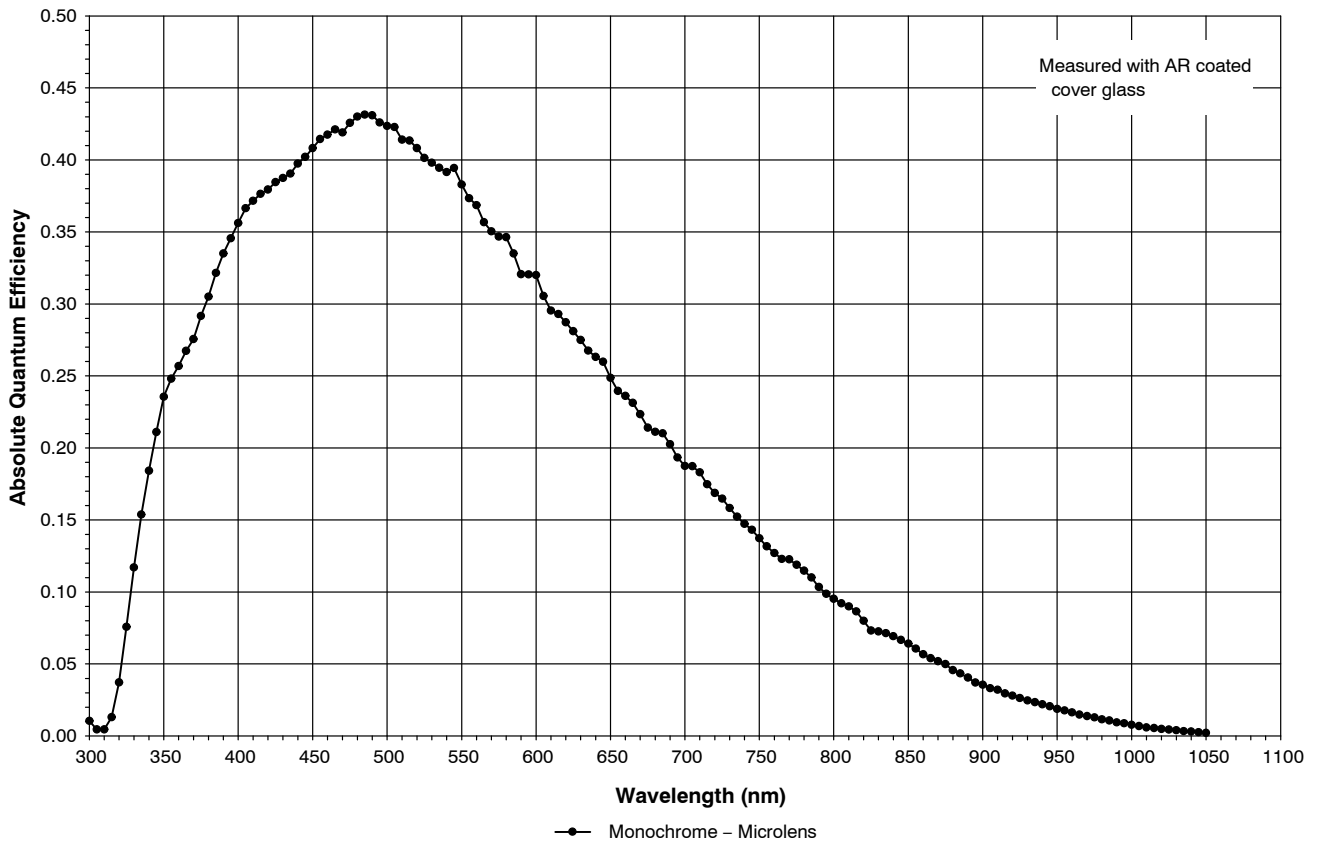


Figure 8. Monochrome with Microlens Quantum Efficiency

Color (Bayer RGB) with Microlens



Figure 9. Color (Bayer) with Microlens Quantum Efficiency

Color (Sparse CFA) with Microlens



Figure 10. Color (Sparse CFA) with Microlens Quantum Efficiency

Angular Quantum Efficiency

For the curves marked “Horizontal”, the incident light angle is varied in a plane parallel to the HCCD. For the curves marked “Vertical”, the incident light angle is varied in a plane parallel to the VCCD.

Monochrome with Microlens



Figure 11. Monochrome with Microlens Angular Quantum Efficiency

Dark Current vs. Temperature



Figure 12. Dark Current vs. Temperature

Power-Estimated



Figure 13. Power

Frame Rates

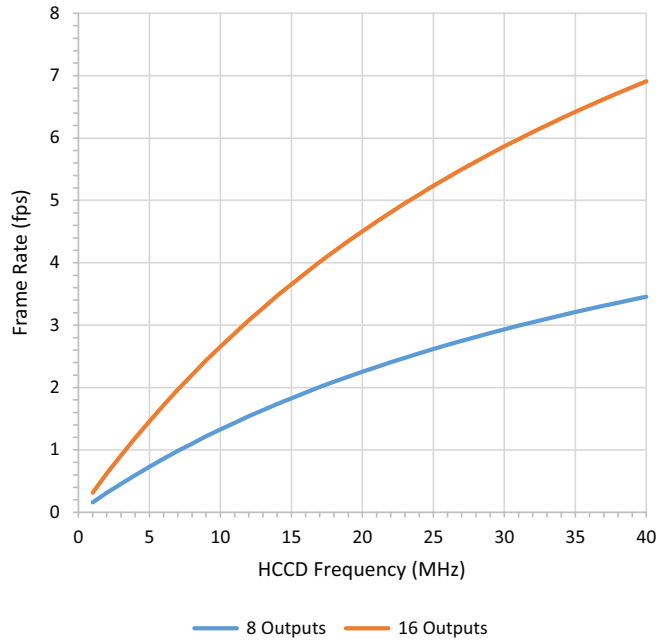


Figure 14. Frame Rates

DEFECT DEFINITIONS

Table 8. OPERATING CONDITIONS

| Description | Condition | Notes |
|--------------|--|--|
| Light Source | Continuous Red, Green and/or Blue LED Illumination | For monochrome sensor, only the green LED is used. |
| Operation | Nominal Operating Voltages and Timing | |

Table 9. OPERATING PARAMETERS

| Description | 8 Outputs | 16 Outputs |
|----------------------|--------------|--------------|
| HCCD Clock Frequency | 20 MHz | 20 MHz |
| Pixels Per Line | 1146 | 1146 |
| Lines Per Frame | 5392 | 2696 |
| Line Time | 82.3 μ s | 82.3 μ s |
| Frame Time | 443.9 ms | 222.0 ms |

Table 10. TIMING MODES

| Timing Modes | Conditions |
|--------------|--|
| Mode A | 8 Output, no electronic shutter used. Photodiode integration time is equal to Frame Time. |
| Mode B | 16 Output, no electronic shutter used. Photodiode integration time is equal to Frame Time. |

Table 11. DEFECT DEFINITIONS

| Description | Definition | Grade 1 | Grade 2 (Mono) | Grade 2 (Color) |
|--------------------|---|-----------------------|-----------------------|-----------------------|
| Column Defect | A group of more than 10 contiguous pixels along a single column that deviate from the neighboring columns by: <ul style="list-style-type: none"> more than 29 mV in the dark field using Timing Mode A at 40°C more than 29 mV in the dark field using Timing Mode A at 27°C more than -12% or +16% in the bright field using Timing Mode B at 27°C or 40°C | 0 | 7 | 27 |
| Cluster Defect | A group of 2 to N contiguous defective pixels, but no more than W adjacent defects horizontally, that deviate from the neighboring pixels by: <ul style="list-style-type: none"> more than 169 mV in the dark field using Timing Mode A at 40°C more than 67 mV in the dark field using Timing Mode A at 27°C more than -12% or +16% in the bright field using Timing Mode B at 40°C or 27°C | 20 W = 4 N = 19 | 50 W = 5 N = 38 | 50 W = 5 N = 38 |
| Major Point Defect | A single defective pixel that deviates from the neighboring pixels by: <ul style="list-style-type: none"> more than 169 mV in the dark field using Timing Mode A at 40°C more than 67 mV in the dark field using Timing Mode A at 27°C more than -12% or +16% in the bright field using Timing Mode B at 27°C or 40°C | 440 | 880 | 880 |
| Minor Point Defect | A single defective pixel that deviates from the neighboring pixels by: <ul style="list-style-type: none"> more than 84 mV in the dark field using Timing Mode A at 40°C | 4400 | 8800 | 8800 |

- Bright field is define as where the average signal level of the sensor is 532 mV, with the substrate voltage set to the recommend VAB setting such that the capacity of the photodiodes is 760 mV (20,000 electrons)
- For the color device (KAI-47051-FBA or KAI-47051-QBA), a bright field defective pixel is with respect to pixels of the same color.
- Column and cluster defects are separated by no less than two (2) good pixels in any direction (excluding single pixel defects).

Defect Map

The defect map supplied with each sensor is based upon testing at an ambient (27°C) temperature. Minor point

defects are not included in the defect map. All defective pixels are reference to pixel 1, 1 in the defect maps.



Figure 15. Pixel 1, 1 Location

OPERATION

Table 12. ABSOLUTE MAXIMUM RATINGS

| Description | Symbol | Minimum | Maximum | Units | Notes |
|-----------------------|------------------|---------|---------|-------|-------|
| Operating Temperature | T _{OP} | -50 | 70 | °C | 1 |
| Humidity | RH | 5 | 90 | % | 2 |
| Output Bias Current | I _{OUT} | - | 240 | mA | 3 |
| Off-Chip Load | C _L | - | 10 | pF | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Noise performance will degrade at higher temperatures.
- T = 25°C. Excessive humidity will degrade MTTF.
- Total for all outputs. Maximum current is -15 mA for each output. Avoid shorting output pins to ground or any low impedance source during operation. Amplifier bandwidth increases at higher current and lower load capacitance at the expense of reduced gain (sensitivity).

Table 13. ABSOLUTE MAXIMUM VOLTAGE RATINGS BETWEEN PINS AND GROUND

| Description | Minimum | Maximum | Units | Notes |
|--|-----------|------------|-------|-------|
| VDD α , VOUT α | -0.4 | 17.5 | V | 1 |
| RD α , FDD α , HLOD α | -0.4 | 15.5 | V | 1 |
| V1B, V1T | ESD - 0.4 | ESD + 24.0 | V | |
| V2B, V2T, V3B, V3T, V4B, V4T | ESD - 0.4 | ESD + 14.0 | V | |
| FDGB, FDGT | ESD - 0.4 | ESD + 15.0 | V | |
| H1 α , H2 α , H2L α | ESD - 0.4 | ESD + 14.0 | V | 1 |
| ESD | -10.0 | 0.0 | V | |
| SUB | -0.4 | 40.0 | V | |

- α refers to a to p.
- Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*

Power-Up and Power-Down Sequence

Adherence to the power-up and power-down sequence is critical. Failure to follow the proper power-up and power-down sequences may cause damage to the sensor.



Notes:

1. Activate all other biases when ESD is stable and SUB is above 3 V.
2. Do not pulse the electronic shutter until ESD is stable.
3. VDD cannot be +15 V when SUB is 0 V.
4. The image sensor can be protected from an accidental improper ESD voltage by current limiting the SUB current to less than 10 mA. SUB and VDD must always be greater than GND. ESD must always be less than GND. Placing diodes between SUB, VDD, ESD and ground will protect the sensor from accidental overshoots of SUB, VDD and ESD during power on and power off. See the figure below.

Figure 16. Power-Up and Power-Down Sequence

The VCCD clock waveform must not have a negative overshoot more than 0.4 V below the ESD voltage.



Figure 17. VCCD Clock Waveform

Example of external diode protection for SUB, VDD and ESD. α denotes a to p.



Figure 18. Example of External Diode Protection

DC Bias Operating Conditions

Table 14. DC BIAS OPERATING CONDITIONS

| Description | Pins | Symbol | Min. | Nom. | Max. | Units | Max. DC Current | Notes |
|-----------------------------------|------------------------|------------------|------|-----------------|-----------------|-------|-----------------|---------|
| Reset Drain | RD α | RD | 11.8 | 12.0 | 12.2 | V | 10 μ A | 1 |
| Fast Line Dump Drain | FDD α , FDDT | FDD | 11.8 | 12.0 | 12.2 | V | 10 μ A | 1 |
| Horizontal Lateral Overflow Drain | HLOD α | HLOD | 11.8 | 12.0 | 12.2 | V | 10 μ A | 1 |
| Output Gate | OG α | OG | -2.2 | -2.0 | -1.8 | V | 10 μ A | 1 |
| Output Amplifier Supply | VDD α | V _{DD} | 14.5 | 15.0 | 15.5 | V | 11.0 mA | 1, 2 |
| Ground | GND | GND | 0.0 | 0.0 | 0.0 | V | -1.0 mA | |
| Substrate | SUB | V _{SUB} | 5.0 | V _{AB} | V _{DD} | V | 50 μ A | 3, 8 |
| ESD Protection Disable | ESD | ESD | -9.5 | -9.0 | -8.8 | V | 50 μ A | 6, 7 |
| Output Bias Current | VOUT α | I _{OUT} | -3.0 | -5.0 | -10.0 | mA | - | 1, 4, 5 |

1. α denotes a to p.
2. The maximum DC current is for one output. $I_{DD} = I_{OUT} + I_{SS}$. See Figure 19.
3. The operating value of the substrate voltage, V_{AB} , will be marked on the shipping container for each device. The value of V_{AB} is set such that the photodiode charge capacity is the nominal P_{Ne} (see Specifications).
4. An output load sink must be applied to each VOUT pin to activate each output amplifier.
5. Nominal value required for 40 MHz operation per output. May be reduced for slower data rates and lower noise.
6. Adherence to the power-up and power-down sequence is critical. See Power Up and Power Down Sequence section.
7. ESD maximum value must be less than or equal to $V1_L + 0.4$ V, $V2_L + 0.4$ V, $V3_L + 0.4$ V, and $V2_L + 0.4$ V.
8. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*.

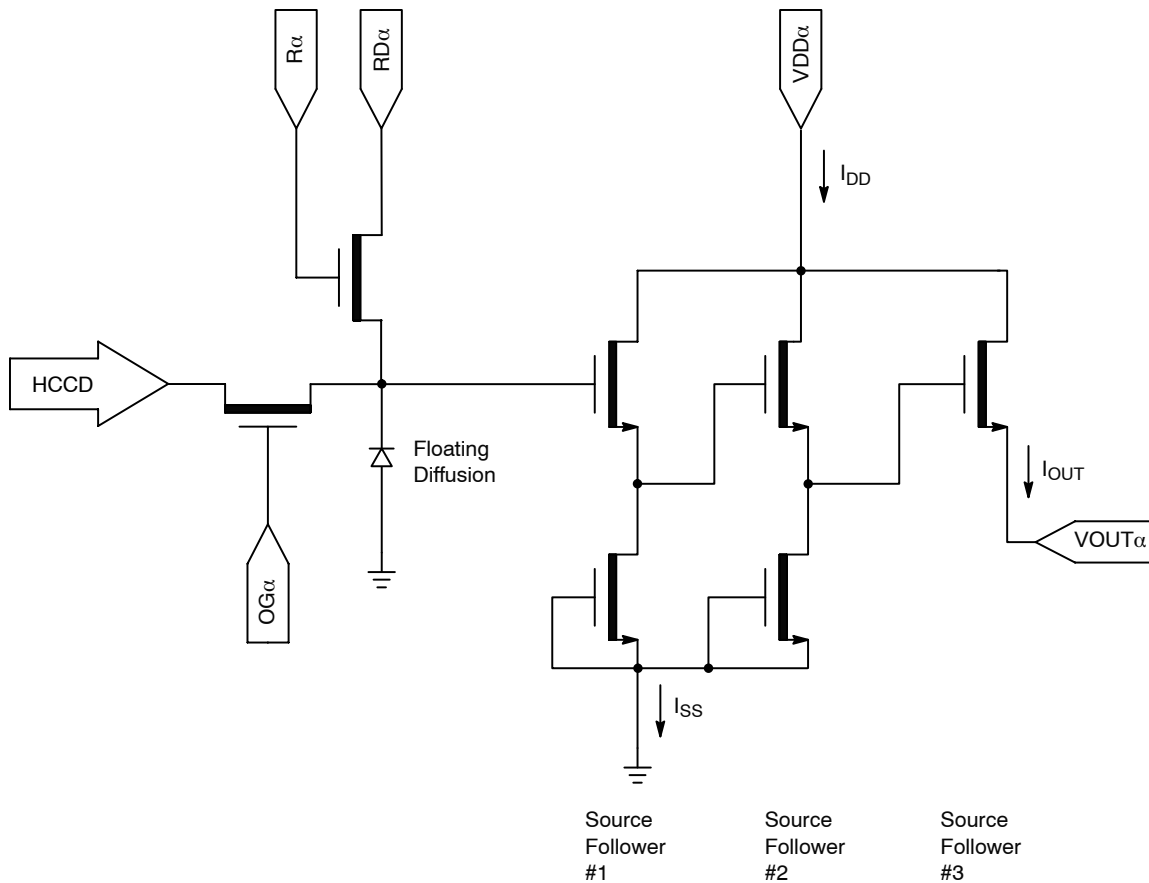


Figure 19. Output Amplifier

AC Operating Conditions

Table 15. CLOCK LEVELS

| Description | Pins (Note 1) | Symbol | Level | Min. | Nom. | Max. | Units | Capacitance (Note 2) |
|--|------------------|-----------------|-----------|------------------|------|-----------------|-------|-------------------------|
| Vertical CCD Clock, Phase 1 | V1B, V1T | V1_L | Low | -8.2 | -8.0 | -7.8 | V | 290 nF (Note 6) |
| | | V1_M | Mid | -0.2 | 0.0 | 0.2 | | |
| | | V1_H | High | 10.8 | 11.0 | 11.2 | | |
| Vertical CCD Clock, Phase 2 | V2B, V2T | V2_L | Low | -8.2 | -8.0 | -7.8 | V | 290 nF (Note 6) |
| | | V2_H | High | -0.2 | 0.0 | 0.2 | | |
| Vertical CCD Clock, Phase 3 | V3B, V3T | V3_L | Low | -8.2 | -8.0 | -7.8 | V | 290 nF (Note 6) |
| | | V3_H | High | -0.2 | 0.0 | 0.2 | | |
| Vertical CCD Clock, Phase 4 | V4B, V4T | V4_L | Low | -8.2 | -8.0 | -7.8 | V | 290 nF (Note 6) |
| | | V4_H | High | -0.2 | 0.0 | 0.2 | | |
| Horizontal CCD Clock, Phase 1 | H1 α | H1_L | Low | -5.2 (Note 7) | -4.0 | -3.8 | V | 1.3 nF (Note 6) |
| | | H1_A | Amplitude | 3.8 | 4.0 | 5.2 (Note 7) | | |
| Horizontal CCD Clock, Phase 2 | H2 α | H2_L | Low | -5.2 (Note 7) | -4.0 | -3.8 | V | 1.3 nF (Note 6) |
| | | H2_A | Amplitude | 3.8 | 4.0 | 5.2 (Note 7) | | |
| Horizontal CCD Clock, Last Phase (Note 3) | H2L α | H2L_L | Low | -5.2 | -5.0 | -4.8 | V | 30 pF (Note 6) |
| | | H2L_A | Amplitude | 4.8 | 5.0 | 5.2 | | |
| Reset Gate | R α | R_L (Note 4) | Low | -3.5 | -2.0 | -1.8 | V | 20 pF (Note 6) |
| | | R_H | High | 2.5 | 3.0 | 4.0 | | |
| Electronic Shutter (Note 5) | SUB | VES | High | 29.0 | 30.0 | 40.0 | V | 20 nF (Note 6) |
| Fast Line Dump Gate | FDGB, FDGT | FDG_L | Low | -8.2 | -8.0 | -7.8 | V | 70 pF (Note 6) |
| | | FDG_H | High | 4.5 | 5.0 | 5.5 | | |

- α denotes a to p.
- Capacitance is total for all like named pins. As an example, if all 16 H1 pins are tied together the total capacitance will be 1.3 nF.
- Use separate clock driver for improved speed performance.
- Reset low should be set to -3 V for signal levels greater than 40,000 electrons.
- Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*.
- Capacitance values are estimated.
- If the minimum horizontal clock low level is used (-5.0 V), then the maximum horizontal clock amplitude should be used (5 V amplitude) to create a -5.0 V to 0.0 V clock.

The figure below shows the DC bias (V_{SUB}) and AC clock (V_{ES}) applied to the SUB pin. Both the DC bias and AC clock are referenced to ground.

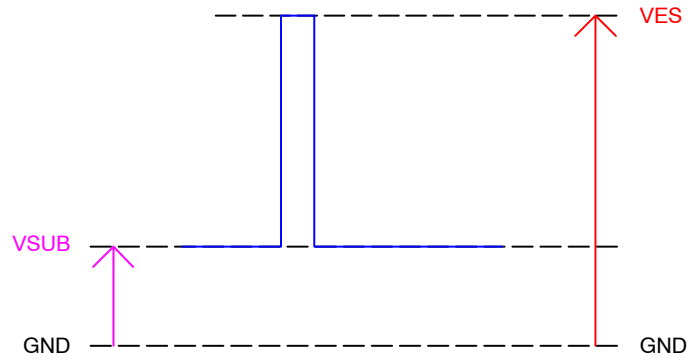


Figure 20. DC Bias and AC Clock Applied to the SUB Pin

Temperature Sensor

Please contact an ON Semiconductor Field Application Engineer for information regarding the operation of the temperature sensing diode.

To operate the Temperature Sensor:

- Source a negative current of $10\ \mu\text{A}$ (I_d) at the TCATHODE pin against the TANODE pin.

- Measure voltage (V_d) at TCATHODE.
- Compare V_d to a linear curve, or a look-up table to calculate the temperature.



Figure 21. Temperature Sensor Connections

TIMING

Table 16. REQUIREMENTS AND CHARACTERISTICS

| Description | Symbol | Min. | Nom. | Max. | Units | Notes |
|------------------------|------------------|-------|------|------|---------------|------------|
| Photodiode Transfer | t_{PD} | 4 | - | - | μs | |
| VCCD Leading Pedestal | t_{3P} | 16 | - | - | μs | |
| VCCD Trailing Pedestal | t_{3D} | 16 | - | - | μs | |
| VCCD Transfer Delay | t_D | 4 | - | - | μs | |
| VCCD Transfer | t_V | 16 | - | - | μs | |
| VCCD Clock Cross-Over | V_{VCR} | 75 | - | 100 | % | 8 |
| VCCD Rise, Fall Times | t_{VR}, t_{VF} | 5 | - | 10 | % | 8, 9 |
| FDG Delay | t_{FDG} | 2 | - | - | μs | |
| HCCD Delay | t_{HS} | 1 | - | - | μs | |
| HCCD Transfer | t_e | 25 | - | - | ns | |
| Shutter Transfer | t_{SUB} | 1 | - | - | μs | |
| Shutter Delay | t_{HD} | 1 | - | - | μs | |
| Reset Pulse | t_R | 2.5 | - | - | ns | |
| Reset – Video Delay | t_{RV} | - | 2.2 | - | ns | |
| H2L – Video Delay | t_{HV} | - | 3.1 | - | ns | |
| Line Time | t_{LINE} | 53.7 | - | - | μs | |
| Frame Time | t_{FRAME} | 144.7 | - | - | ms | 16 outputs |
| | | 289.4 | - | - | | 8 outputs |

8. Refer to Figure 31: VCCD Clock Rise Time, Fall Time and Edge Alignment

9. Relative to the VCCD Transfer pulse width, t_V .

Timing Flow Charts

In the timing flow charts the number of HCCD clock cycles per row, NH, and the number of VCCD clock cycles per frame, NV, are shown in the following table.

Table 17. VALUES FOR NH AND NV WHEN OPERATING THE SENSOR IN VARIOUS MODES OF RESOLUTION

| | Full Resolution | |
|------------|-----------------|------|
| | NV | NH |
| 16 Outputs | 2696 | 1116 |
| 8 Outputs | 5392 | 1116 |

1. The time to read out one line $t_{LINE} = \text{Line Timing} + NH / (\text{Pixel Frequency})$.
2. The time to read out one frame $t_{FRAME} = NV \cdot t_{LINE} + \text{Frame Timing}$.
3. Line Timing: See Table 19: Line Timing.
4. Frame Timing: See Table 18: Frame Timing.

No Electronic Shutter

In this case the photodiode exposure time is equal to the time to read out an image.



Figure 22. Timing Flow when Electronic Shutter is Not Used

Using the Electronic Shutter

The exposure time begins on the falling edge of the electronic shutter pulse on the SUB pin. The exposure time ends on the falling edge of the photodiode transfer (T_{pd}) of

the V1T and V1B pins. The electronic shutter timing is shown in Figure 28.

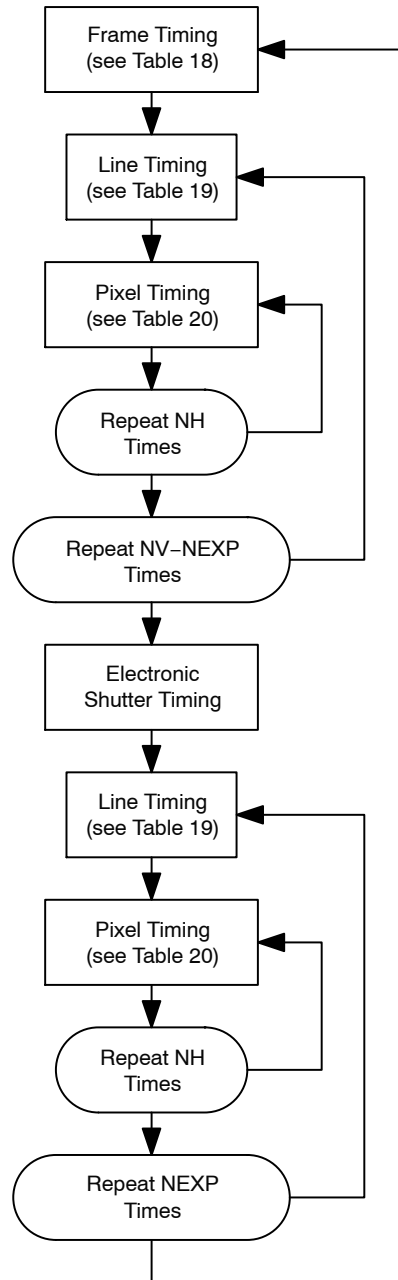


Figure 23. Timing Flow Chart using the Electronic Shutter for Exposure Control

Timing Tables

Frame Timing

This timing table is for transferring charge from the photodiodes to the VCCD. See Figure 24 and Figure 25 for frame timing diagrams.

Table 18. FRAME TIMING

| Device Pin | Full Resolution | |
|------------|-----------------|------------------|
| | 16 Outputs | 8 Outputs |
| V1T | F1T | F1B |
| V2T | F2T | F4B |
| V3T | F3T | F3B |
| V4T | F4T | F2B |
| V1B | F1B | |
| V2B | F2B | |
| V3B | F3B | |
| V4B | F4B | |
| FDGB, FDGT | FDG_L | |
| H1a to h | P1 | P1 |
| H2a to h | P2 | P2 |
| H2La to h | P2 | P2 |
| Ra to h | R | R |
| H1i to p | P1 | P1 or see Note 1 |
| H2i to p | P2 | P2 or see Note 1 |
| H2Li to p | P2 | P2 or see Note 1 |
| Ri to p | R | R or see Note 1 |

1. These clocks may all be held at their high level voltages or +5.0 V

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Line Timing

This timing is for transferring one line of charge from the VCCD to the HCCD. See Figure 26 and Figure 27 for line timing diagrams.

Table 19. LINE TIMING

| Device Pin | Full Resolution | |
|------------|-----------------|------------------|
| | 16 Outputs | 8 Outputs |
| V1T | L1T | L1B |
| V2T | L2T | L4B |
| V3T | L3T | L3B |
| V4T | L4T | L2B |
| V1B | L1B | |
| V2B | L2B | |
| V3B | L3B | |
| V4B | L4B | |
| FDGB, FDGT | FDG_L | |
| H1a to h | P1L | P1L |
| H2a to h | P2L | P2L |
| H2La to h | P2L | P2L |
| Ra to h | R | R |
| H1i to p | P1L | P1 or see Note 1 |
| H2i to p | P2L | P2 or see Note 1 |
| H2Li to p | P2L | P2 or see Note 1 |
| Ri to p | R | R or see Note 1 |

1. These clocks may all be held at their high level voltages or +5.0 V

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Pixel Timing

This timing is for transferring one pixel from the HCCD to the output amplifier.

Table 20. PIXEL TIMING

| Device Pin | Full Resolution | |
|------------|-----------------|------------------|
| | 16 Outputs | 8 Outputs |
| V1T | V1_L | V1_L |
| V2T | V2_L | V2_L |
| V3T | V3_H | V3_H |
| V4T | V4_H | V4_H |
| V1B | V1_L | |
| V2B | V2_H | |
| V3B | V3_H | |
| V4B | V4_L | |
| FDGB, FDGT | FDG_L | |
| H1a to h | P1 | P1 |
| H2a to h | P2 | P2 |
| H2La to h | P2 | P2 |
| Ra to h | R | R |
| H1i to p | P1 | P1 or see Note 1 |
| H2i to p | P2 | P2 or see Note 1 |
| H2Li to p | P2 | P2 or see Note 1 |
| Ri to p | R | R or see Note 1 |

1. These clocks may all be held at their high level voltages or +5.0 V

Timing Diagrams

The charge in the photodiodes is transferred to the VCCD on the rising edge of the +13 V pulse and is completed by the falling edge of the V1_H pulse on F1T and F1B. During the

time period when F1T and F1B are at V1_H (Tpd) anti-blooming protection is disabled. The photodiode integration time ends on the falling edge of the Tpd pulse.

Frame Timing – 16 Output Mode



See the Pin Assignment table for pin assignments.

Figure 24. Frame Timing Diagram 16 Output Mode

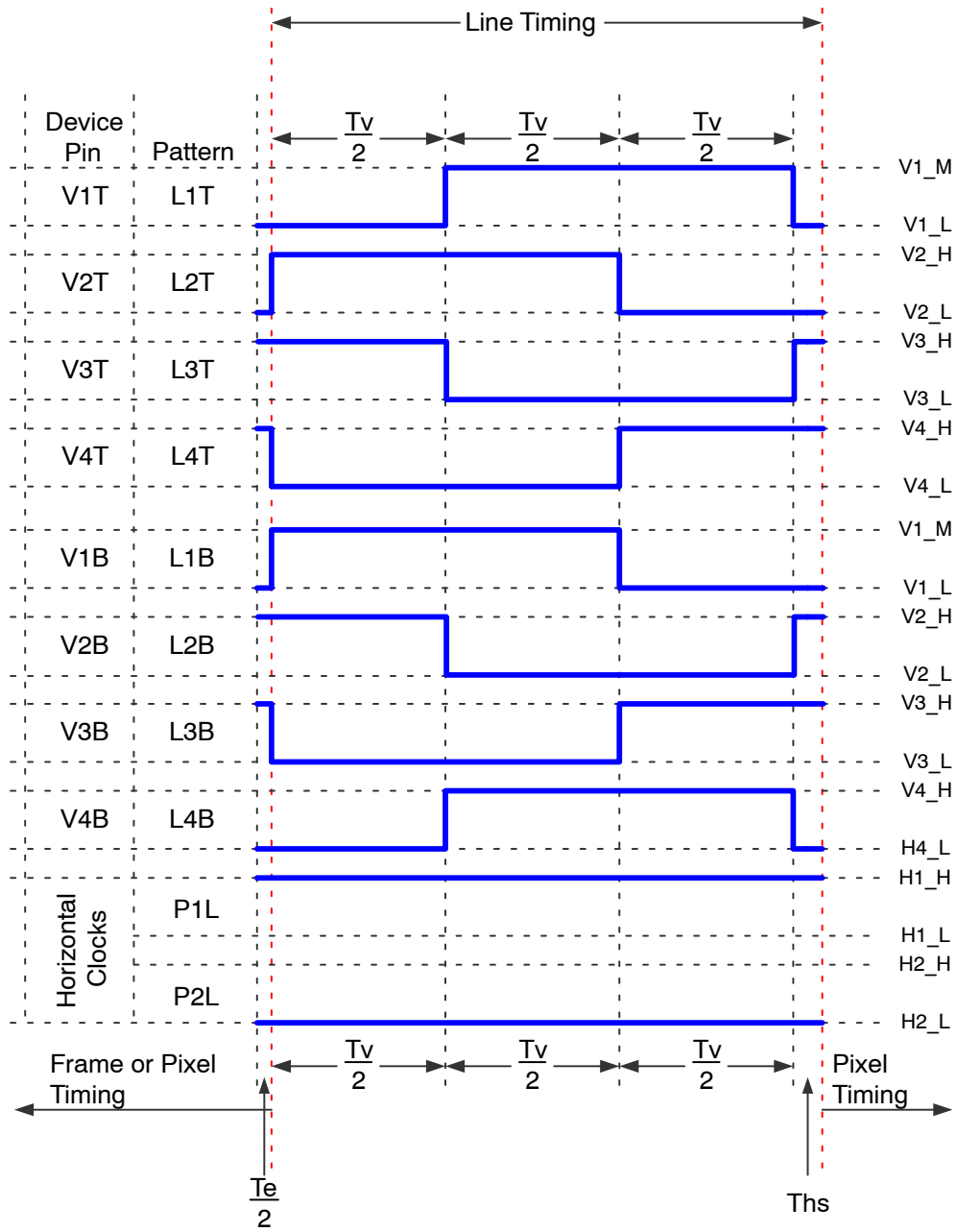
Frame Timing- 8 Output Mode



See the Pin Assignment table for pin assignments.

Figure 25. Frame Timing Diagram 8 Output Mode

Line Timing – Full Resolution – 16 Output Mode



See the Pin Assignment table for pin assignments.

Figure 26. Line Timing Diagram – Full Resolution – 16 Output Mode

Line Timing – Full Resolution – 8 Output Mode



See the Pin Assignment table for pin assignments.

Figure 27. Line Timing Diagram – Full Resolution – 8 Output Mode

Electronic Shutter Timing Diagrams

The electronic shutter pulse can be inserted at the end of any line of the HCCD timing. The HCCD should be empty when the electronic shutter is pulsed. A recommended position for the electronic shutter is just after the last pixel is read out of a line. The VCCD clocks should not resume until at least T_{hd} after the electronic shutter pulse has finished. The HCCD clocks can be run during the electronic

shutter pulse as long as the HCCD does not contain valid image data.

For short exposures less than one line time, the electronic shutter pulse can appear inside the frame timing. Any electronic shutter pulse transition should be T_{hd} away from any VCCD clock transition.

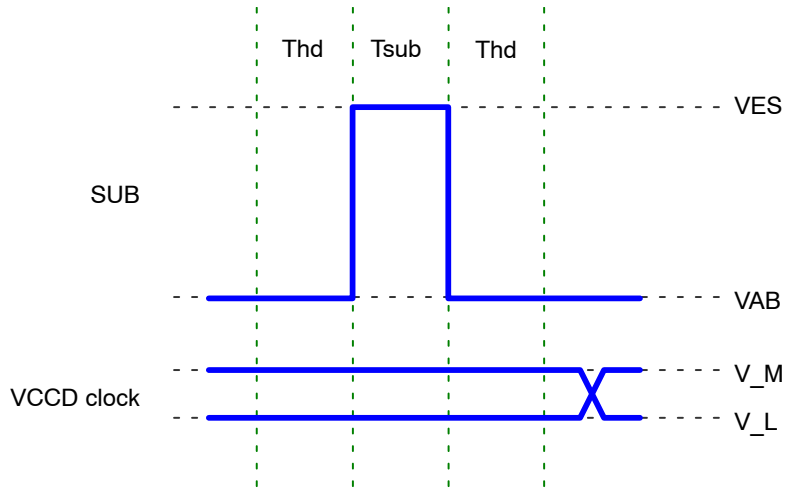


Figure 28. Electronic Shutter Timing

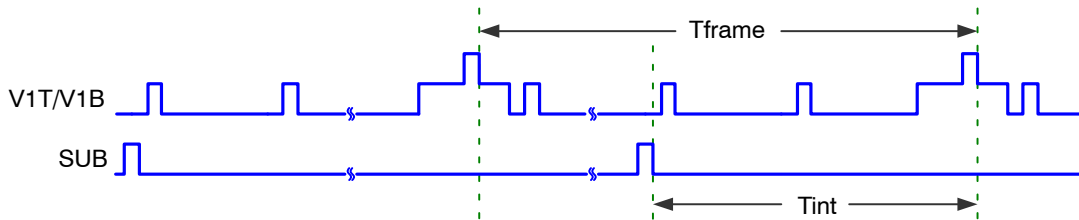


Figure 29. Frame/Electronic Shutter Timing

Pixel Timing – Full Resolution – All Output Modes



Figure 30. Pixel Timing Diagram – Full Resolution

VCCD Clock Edge Alignment



Figure 31. VCCD Clock Rise Time, Fall Time and Edge Alignment

Fast Line Dump Timing

The FDG pins may be optionally clocked to efficiently remove unwanted pins in the image resulting for increased frame rates at the expense of resolution. Below is an example of a 2 line dump sequence followed by a normal readout line.

Note that the FDG timing transitions should complete prior to the beginning of vertical timing transitions as illustrated below.

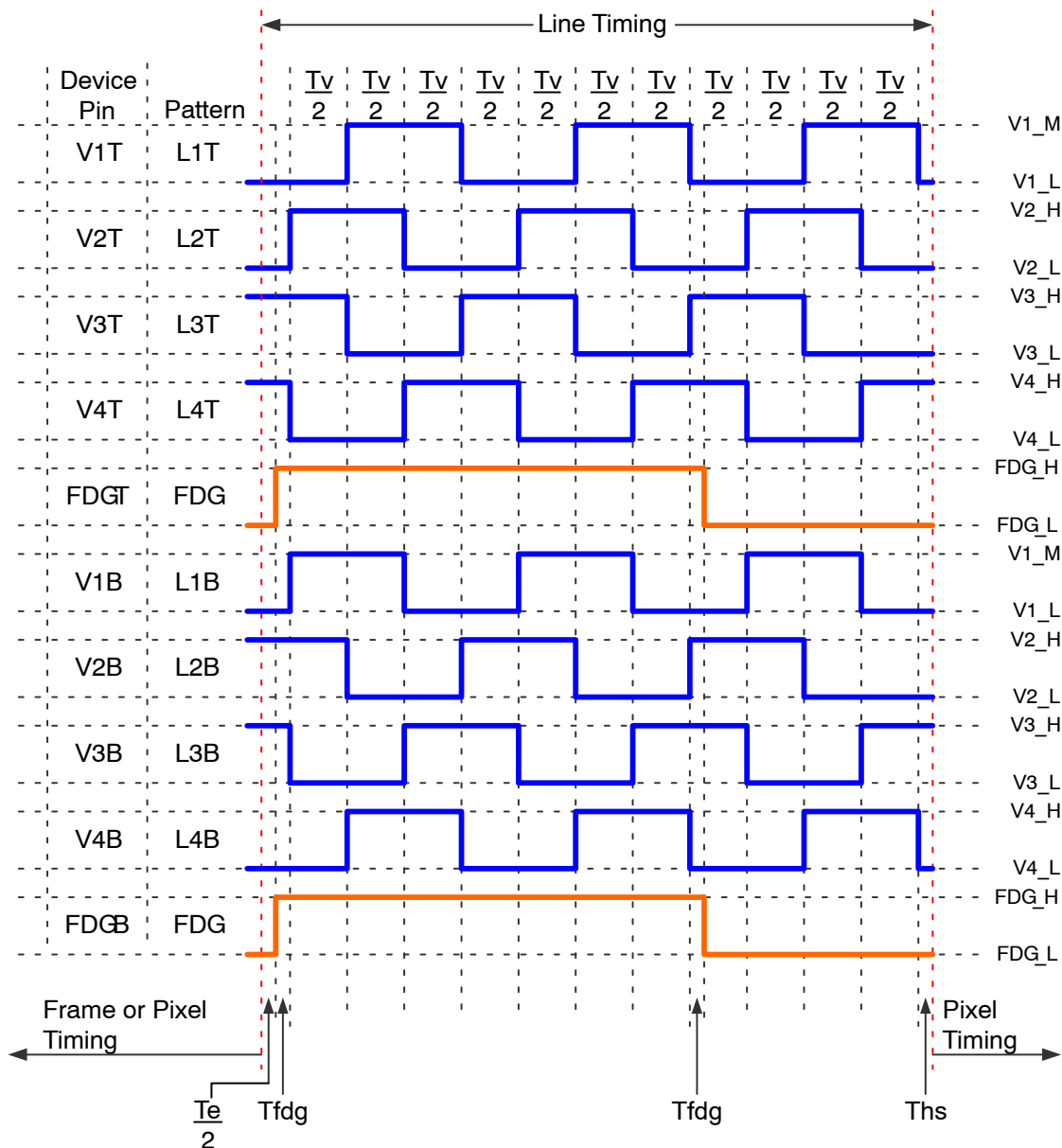


Figure 32. Fast Line Dump Timing Diagram

STORAGE AND HANDLING

Table 21. STORAGE CONDITIONS

| Description | Symbol | Minimum | Maximum | Units | Notes |
|---------------------|-----------------|---------|---------|-------|-------|
| Storage Temperature | T _{ST} | -55 | 80 | °C | 1 |
| Humidity | RH | 5 | 90 | % | 2 |

1. Long-term storage toward the maximum temperature will accelerate color filter degradation.
2. T = 25°C. Excessive humidity will degrade MTTF.

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D) from www.onsemi.com.

For information on environmental exposure, please download the *Using Interline CCD Image Sensors in High Intensity Lighting Conditions* Application Note (AND9183/D) from www.onsemi.com.

For information on soldering recommendations, please download the *Soldering and Mounting Techniques Reference Manual* (SOLDERRM/D) from www.onsemi.com.

For quality and reliability information, please download the *Quality & Reliability Handbook* (HBD851/D) from www.onsemi.com.

For information on device numbering and ordering codes, please download the *Device Nomenclature* technical note (TND310/D) from www.onsemi.com.

For information on Standard terms and Conditions of Sale, please download [Terms and Conditions](http://www.onsemi.com) from www.onsemi.com.

MECHANICAL INFORMATION

Completed Assembly

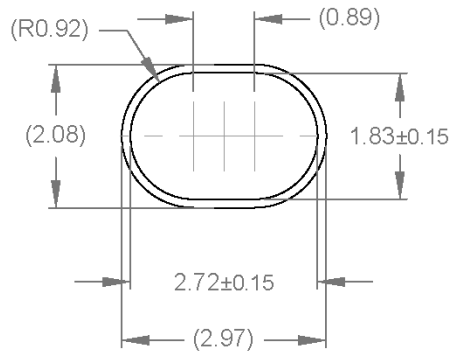


Notes:

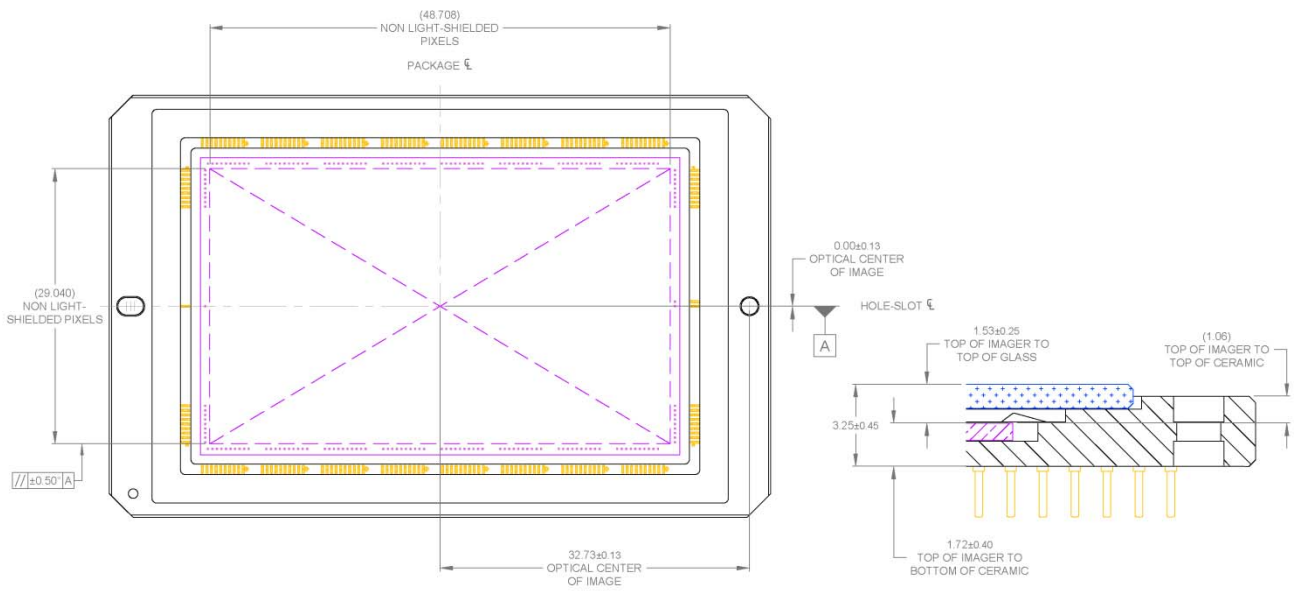
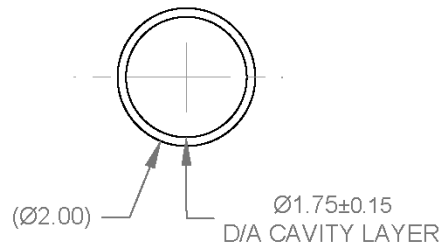
1. See Ordering Information for marking code.
2. Pin to pin distances are measured at pin base.
3. Pins are not centered about the vertical axis.
4. Units: mm

Figure 33. Completed Assembly (1 of 2)

DETAIL OF SLOTTED HOLE



DETAIL OF HOLE



Notes:

1. Units: mm

Figure 34. Completed Assembly (2 of 2)

Cover Glass



Notes:


1. Substrate = Schott D263T eco
2. Dust, Scratch, Inclusion Specification:
 - a.) 20 microns maximum size in Zone A
3. MAR coated both sides
4. Spectral Transmission
 - a.) 350 - 365 nm: $T \geq 88\%$
 - b.) 365 - 405 nm: $T \geq 94\%$
 - c.) 405 - 450 nm: $T \geq 98\%$
 - d.) 450 - 650 nm: $T \geq 99\%$
 - e.) 650 - 690 nm: $T \geq 98\%$
 - f.) 690 - 770 nm: $T \geq 94\%$
 - g.) 770 - 870 nm: $T \geq 88\%$
5. Units: mm

Figure 35. Cover Glass

Cover Glass Transmission



Figure 36. Cover Glass Transmission

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