Power MOSFET, N-Channel, SUPERFET[®] III, Easy Drive, 650 V, 12 A, 260 m Ω

Description

SUPERFET III MOSFET is ON Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate. Consequently, SUPERFET III MOSFET Easy drive series helps manage EMI issues and allows for easier design implementation.

Features

- 700 V @ $T_J = 150$ °C
- Typ. $R_{DS(on)} = 222 \text{ m}\Omega$
- Ultra Low Gate Charge (Typ. Q_g = 24 nC)
- Low Effective Output Capacitance (Typ. Coss(eff.) = 248 pF)
- 100% Avalanche Tested
- These Devices are Pb-Free and are RoHS Compliant

Applications

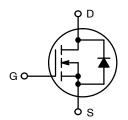
- Computing / Display Power Supplies
- Telecom / Server Power Supplies
- Industrial Power Supplies
- Lighting / Charger / Adapter



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V _{DSS}	R _{DS(ON)} MAX	I _D MAX
650 V	260 mΩ @ 10 V	12 A



POWER MOSFET



D-PAK CASE 369AS

MARKING DIAGRAM



\$Y = ON Semiconductor Logo &Z = Assembly Plant Code &3 = Data Code (Year & Week)

&K = Lot

FCD260N65S3 = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise specified)

Symbol	Paramet	er	FCD260N65S3	Unit	
V_{DSS}	Drain to Source Voltage	650	V		
V_{GSS}	Gate to Source Voltage	DC	±30	V	
		AC (f > 1 Hz)	±30	V	
I _D	Drain Current	Continuous (T _C = 25°C)	12	Α	
		Continuous (T _C = 100°C)	7.6		
I _{DM}	Drain Current	Pulsed (Note 1)	30	Α	
E _{AS}	Single Pulsed Avalanche Energy (Note 2)		57	mJ	
I _{AS}	Avalanche Current (Note 1)		2.3	Α	
E _{AR}	Repetitive Avalanche Energy (Note 1)		0.9	mJ	
dv/dt	MOSFET dv/dt		100	V/ns	
	Peak Diode Recovery dv/dt (Note 3)		20	1	
P_{D}	Power Dissipation	(T _C = 25°C)	90	W	
		Derate Above 25°C	0.72	W/°C	
T _J , T _{STG}	Operating and Storage Temperature Rang	e	-55 to +150	°C	
TL	Maximum Lead Temperature for Soldering	, 1/8" from Case for 5 s	300	°C	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- 1. Repetitive rating: pulse-width limited by maximum junction temperature.
 2. $I_{AS}=2.3$ A, $R_G=25$ Ω , starting $T_J=25^{\circ}C$.
 3. $I_{SD}\leq 6$ A, di/dt ≤ 200 A/ μ s, $V_{DD}\leq 400$ V, starting $T_J=25^{\circ}C$.

THERMAL CHARACTERISTICS

Symbol	Parameter	FCD260N65S3	Unit
$R_{ hetaJC}$	Thermal Resistance, Junction to Case, Max.	1.39	°C/W
$R_{ heta JA}$	Thermal Resistance, Junction to Ambient, Max. (Note 4)	40	

^{4.} Device on 1 in² pad 2 oz copper pad on 1.5 x 1.5 in. board of FR-4 material.

PACKAGE MARKING AND ORDERING INFORMATION

Part Nun	nber	Top Marking	Package	Reel Size	Tape Width	Shipping [†]
FCD260N	65S3	FCD260N65S3	D-PAK	330 mm	16 mm	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
OFF CHARACT	ERISTICS	•	•			
BV _{DSS}	Drain to Source Breakdown Voltage	$V_{GS} = 0 \text{ V, } I_D = 1 \text{ mA, } T_J = 25^{\circ}\text{C}$	650	_	-	V
		$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}, T_J = 150^{\circ}\text{C}$	700	-	-	V
$\Delta BV_{DSS}/\Delta T_{J}$	Breakdown Voltage Temperature Coefficient	I _D = 1 mA, Referenced to 25°C	-	0.66	-	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 650 V, V _{GS} = 0 V	_	-	1	μΑ
		V _{DS} = 520 V, T _C = 125°C	_	0.77	-	
I _{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 30 \text{ V}, V_{DS} = 0 \text{ V}$	_	-	±100	nA
ON CHARACTE	ERISTICS	•	•			
V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 1.2 \text{ mA}$	2.5	-	4.5	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 6 A	_	222	260	mΩ
9FS	Forward Transconductance	V _{DS} = 20 V, I _D = 6 A	_	7.4	-	S
DYNAMIC CHA	RACTERISTICS	•		•		•
C _{iss}	Input Capacitance	V _{DS} = 400 V, V _{GS} = 0 V, f = 1 MHz	_	1010	-	pF
C _{oss}	Output Capacitance		_	25	-	pF
C _{oss(eff.)}	Effective Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V	_	248	-	pF
C _{oss(er.)}	Energy Related Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V	-	33	-	pF
Q _{g(tot)}	Total Gate Charge at 10 V	V _{DS} = 400 V, I _D = 6 A, V _{GS} = 10 V		24	-	nC
Q_{gs}	Gate to Source Gate Charge	(Note 5)	_	6.1	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		_	9.7	-	nC
ESR	Equivalent Series Resistance	f = 1 MHz	_	8.7	-	Ω
SWITCHING CH	HARACTERISTICS	•				
t _{d(on)}	Turn-On Delay Time	$V_{DD} = 400 \text{ V}, I_D = 6 \text{ A},$	_	18	_	ns
t _r	Turn-On Rise Time	$V_{GS} = 10 \text{ V}, R_g = 4.7 \Omega$ (Note 5)	_	18	-	ns
t _{d(off)}	Turn-Off Delay Time	7	_	49	-	ns
t _f	Turn-Off Fall Time		_	12	-	ns
SOURCE-DRAI	N DIODE CHARACTERISTICS	•	•			
I _S	Maximum Continuous Source to Drain Diode	e Forward Current	_	-	12	Α
I _{SM}	Maximum Pulsed Source to Drain Diode For	ward Current	-	-	30	Α
V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 6 A	-	-	1.2	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 6 A,	_	251	-	ns
Q _{rr}	Reverse Recovery Charge	$dI_{F}/dt = 100 A/\mu s$	_	3.4	_	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

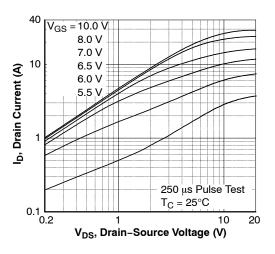


Figure 1. On-Region Characteristics

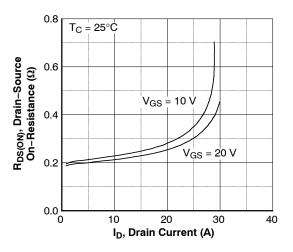


Figure 3. On-Resistance Variation vs.
Drain Current and Gate Voltage

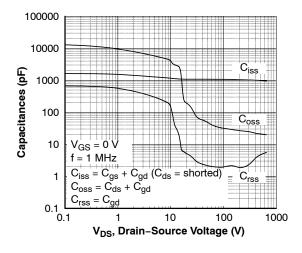


Figure 5. Capacitance Characteristics

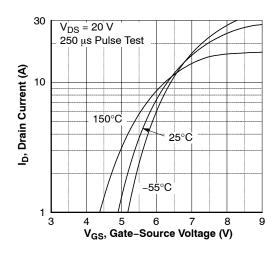


Figure 2. Transfer Characteristics

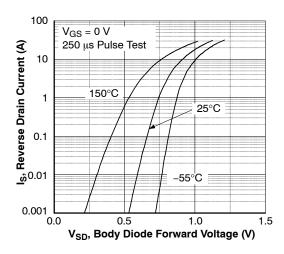


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

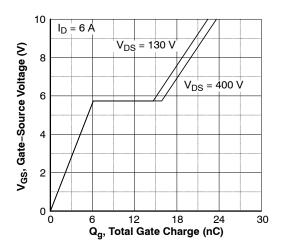


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

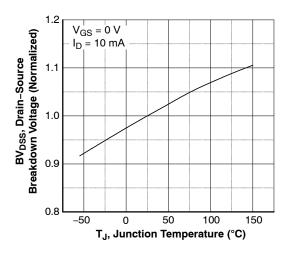


Figure 7. Breakdown Voltage Variation vs. Temperature

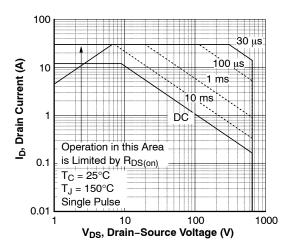


Figure 9. Maximum Safe Operating Area

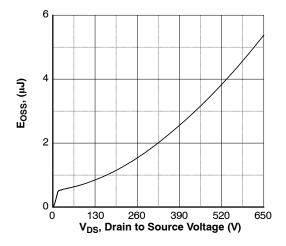


Figure 11. $E_{\mbox{OSS}}$ vs. Drain to Source Voltage

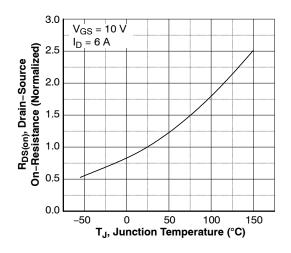


Figure 8. On–Resistance Variation vs. Temperature

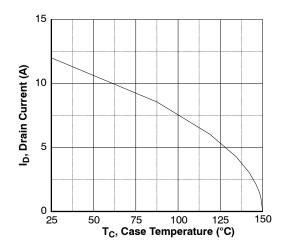


Figure 10. Maximum Drain Current vs. Case Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

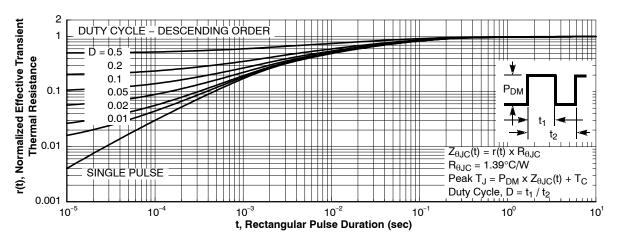


Figure 12. Transient Thermal Response Curve

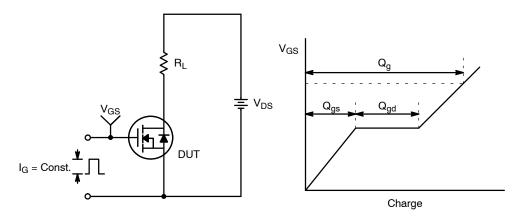


Figure 13. Gate Charge Test Circuit & Waveform

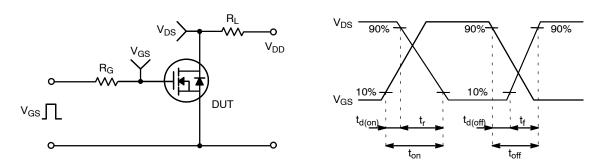


Figure 14. Resistive Switching Test Circuit & Waveforms

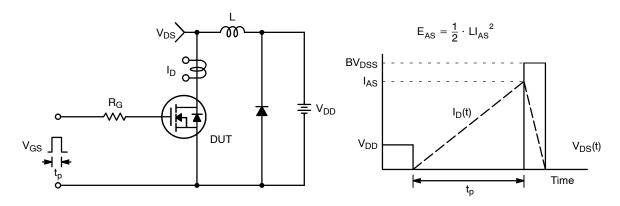


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

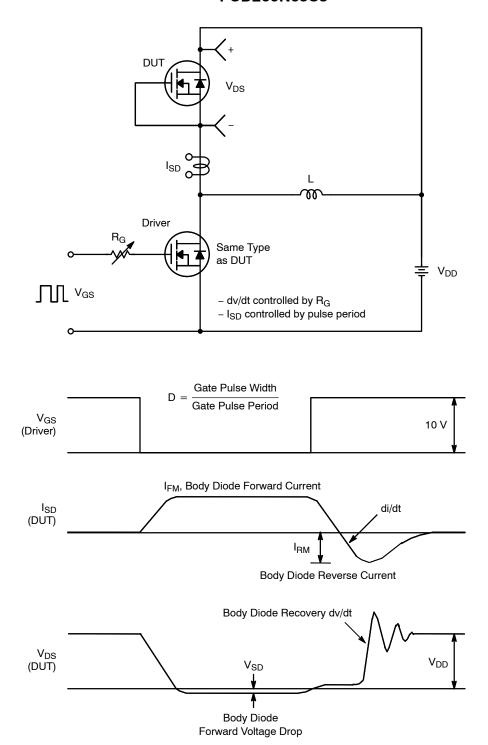


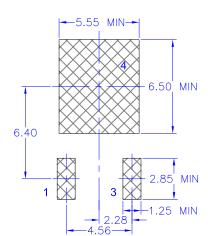
Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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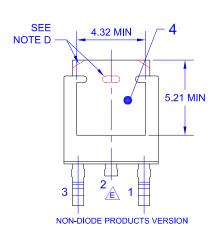
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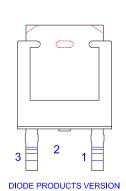
6.73 6.35 Α 5.46 1.02 MAX 0.25 MAX C PLASTIC BODY STUB DIODE PRODUCTS VERSION (0.59)0.89 0.64 ⊕ 0.25 M AM C 2.29 4.57

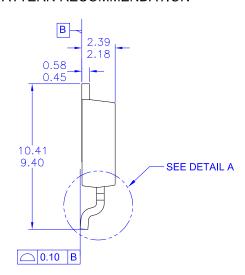


LAND PATTERN RECOMMENDATION



NON-DIODE PRODUCTS VERSION

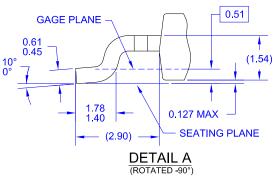




NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.

 B) ALL DIMENSIONS ARE IN MILLIMETERS.
 C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
- E TRIMMED CENTER LEAD IS PRESENT ONLY FOR DIODE PRODUCTS
- F) DIMENSIONS ARE EXCLUSSIVE OF BURSS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- G) LAND PATTERN RECOMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.



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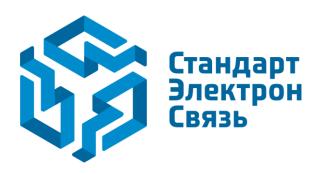
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