OPA1S2385EVM

This user's guide describes the characteristics, operation, and use of the evaluation module (EVM) for the OPA1S2385. The EVM is designed to evaluate the performance of the device in both single- and dual-supply configurations. This document also includes the schematic, printed circuit board (PCB) layout, and a bill of materials (BOM). Throughout this document the terms *evaluation board*, *evaluation module*, and *EVM* are synonymous with the OPA1S2385EVM.

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1 Introduction

1.1 OPA1S2385

The OPA1S2385 combines high bandwidth, FET-input operational amplifiers with a fast SPST CMOS switch. It is well suited for applications that require the tracking and capturing of fast signals, such as wideband photodiode amplification. It is available in a DFN-10 package.

1.2 OPA1S2385EVM

The OPA1S2385EVM is intended to provide basic functional evaluation of the OPA1S2385. It provides the following features:

- Configured for split-supply or single-supply operation.
- Easy access to pertinent nodes with test points, SMA connectors, and banana plugs.
- Default noninverting gain of 1 configuration for basic sample-and-hold mode evaluation.
- Component footprints allow for multiple gain, feedback, and filtering configurations.
- Designed for connection to standard 50-Ω test equipment.

A picture of the OPA1S2385EVM is shown in Figure 1.

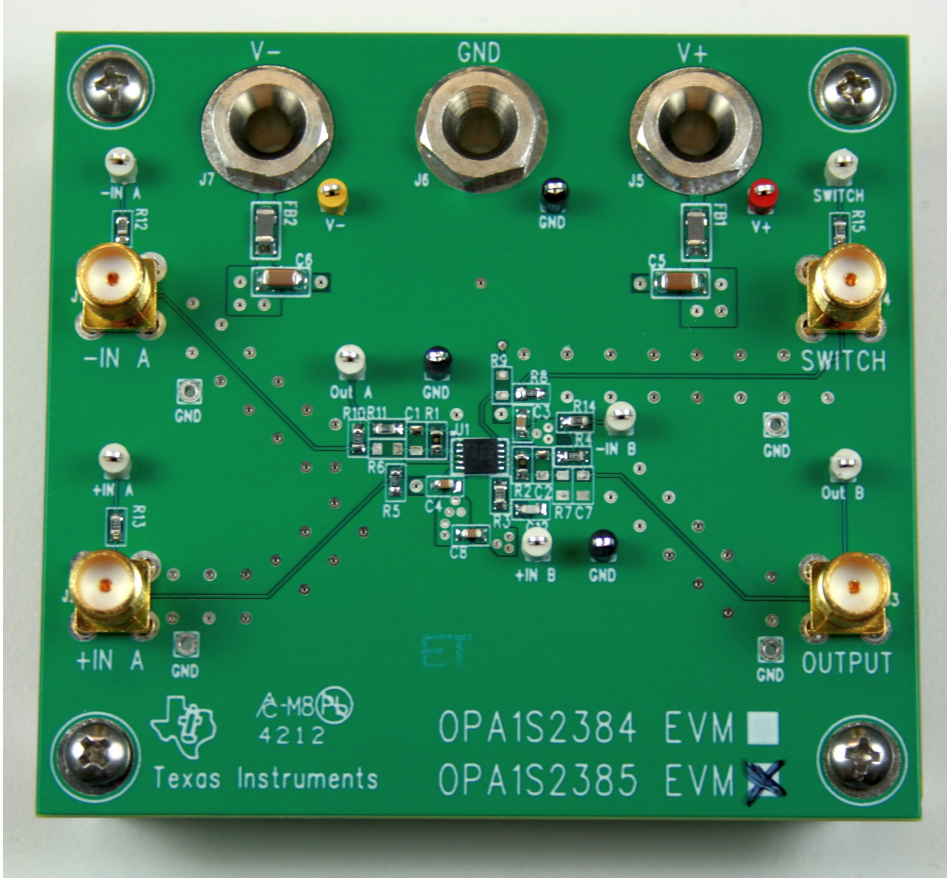

Figure 1. OPA1S2385EVM

2 OPA1S2385EVM Hardware

This section discusses the OPA1S2385EVM hardware schematics and PCB layout.

2.1 Schematic

The schematic of the OPA1S2385EVM is shown in Figure 2.

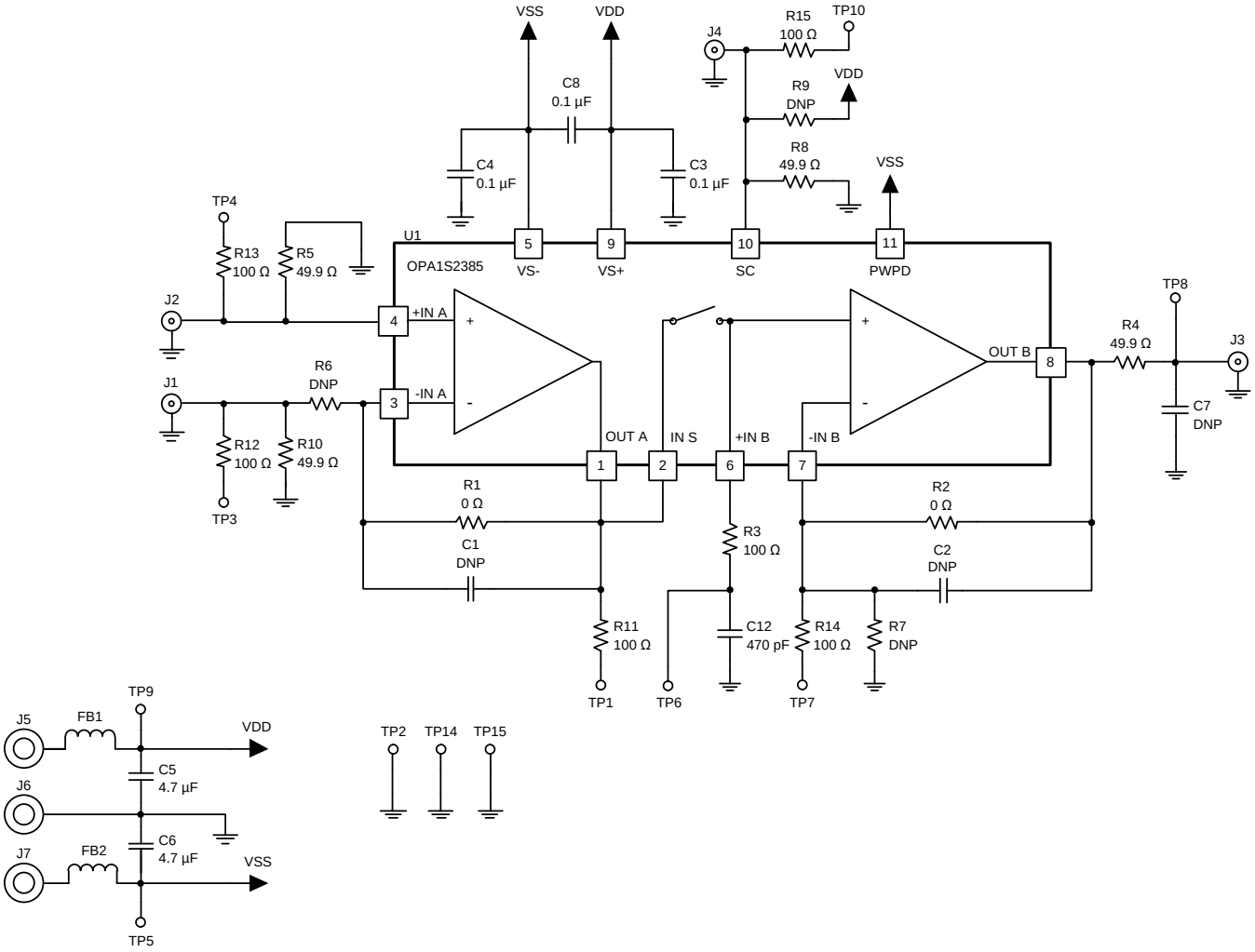

Figure 2. OPA1S2385EVM Schematic

2.1.1 Amplifier A

In the default configuration, amplifier A is set to a noninverting gain of 1. The noninverting input signal is applied through SMA connector J2. If the amplifier is placed in an inverting configuration, the input signal is applied through SMA connector J1. The output of amplifier A can be measured at test point TP1. Both input traces include 50-Ω termination resistors to properly interface with standard test equipment.

The gain and feedback configuration of amplifier A can be changed by modifying components R1, C1, R5, R6, and R10.

2.1.2 Amplifier B

In the default configuration, amplifier B is set to a noninverting gain of 1. The output of amplifier A is passed to the noninverting input of amplifier B through an internal switch. Alternatively, an external signal can be applied to either input of amplifier B using test points TP6 and TP7. The output of amplifier B can be measured at SMA connector J3 or test point TP8. The output trace includes a 50-Ω termination resistor to properly interface with standard test equipment.

The gain, feedback, and filtering configuration of amplifier B can be changed by modifying components R2, C2, R4, R7, and C7.

2.1.3 Switch Control

The control signal to the switch is applied through SMA connector J4. The input trace to the switch control pin includes a 50-Ω termination resistor to properly interface with standard test equipment. The logic table that describes the behavior of the switch is shown in Table 1.

Table 1. Switch Control

SC VOLTAGE	SWITCH BEHAVIOR
High (V+)	Open
Low (V–)	Closed

2.1.4 Power

Power is applied through the banana connectors J5, J6, and J7. The minimum and maximum supply voltage ranges are given below in Table 2.The default configuration utilizes a split supply of ±2.5V. If single-supply operation is desired, short J6 to J7 and connect them to GND, then apply the positive supply voltage to J5.

Table 2. Supply Voltage Range

CONFIGURATION	V_{SUPPLY} (MAX)	V_{SUPPLY} (MIN)
Split supply	±2.75 V	±1.35 V
Single supply	+5.5 V	+2.7 V

2.2 OPA1S2385EVM PCB Layout

Figure 3, Figure 4, Figure 5, and Figure 6 depict the four layers of the OPA1S2385EVM PCB layout.

NOTE: Board layouts are not to scale. These figures are intended to show how the board is laid out; they are not intended to be used for manufacturing OPA1S2385EVM PCBs.

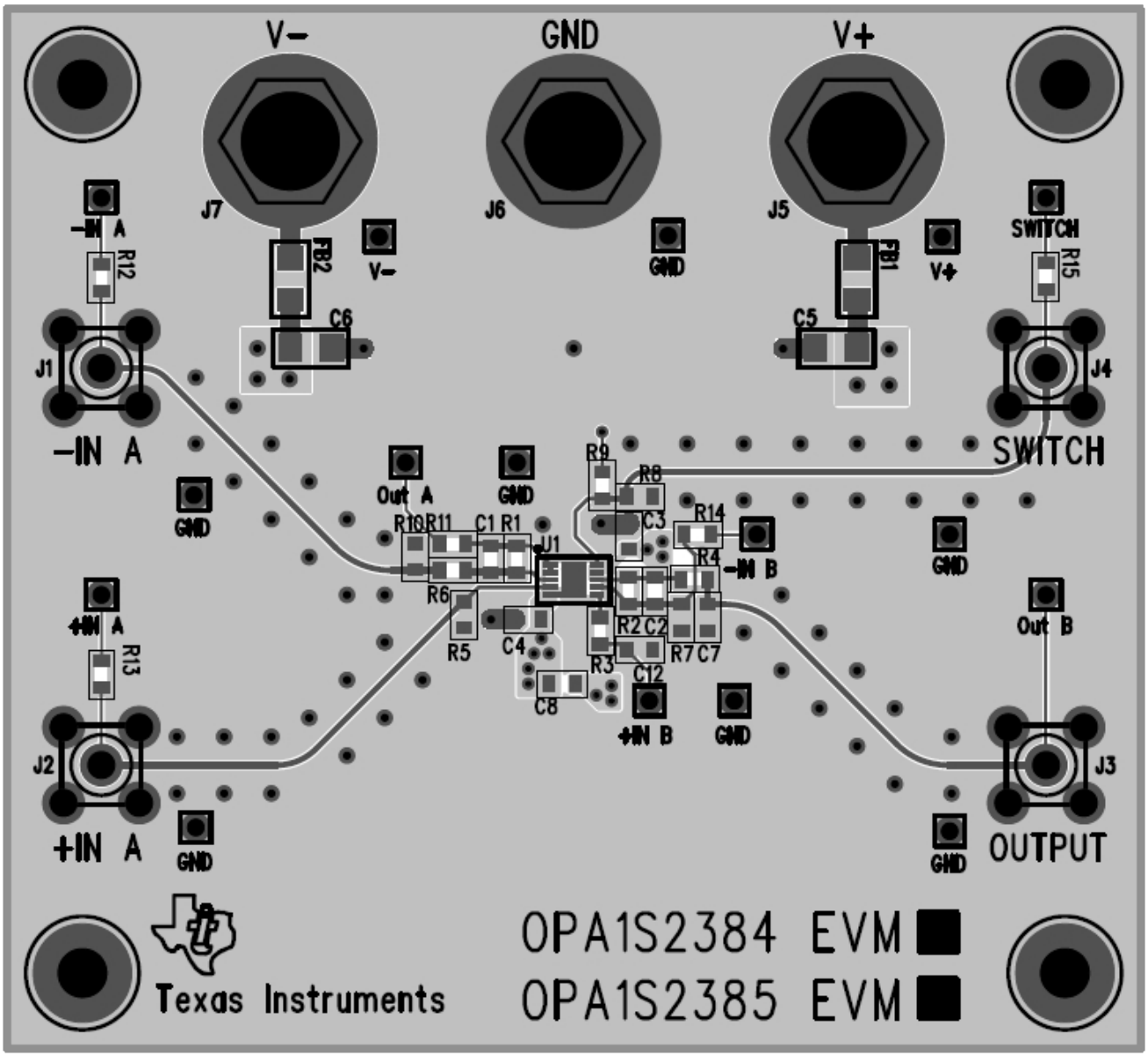

Figure 3. Top Layer (Signal and Ground)

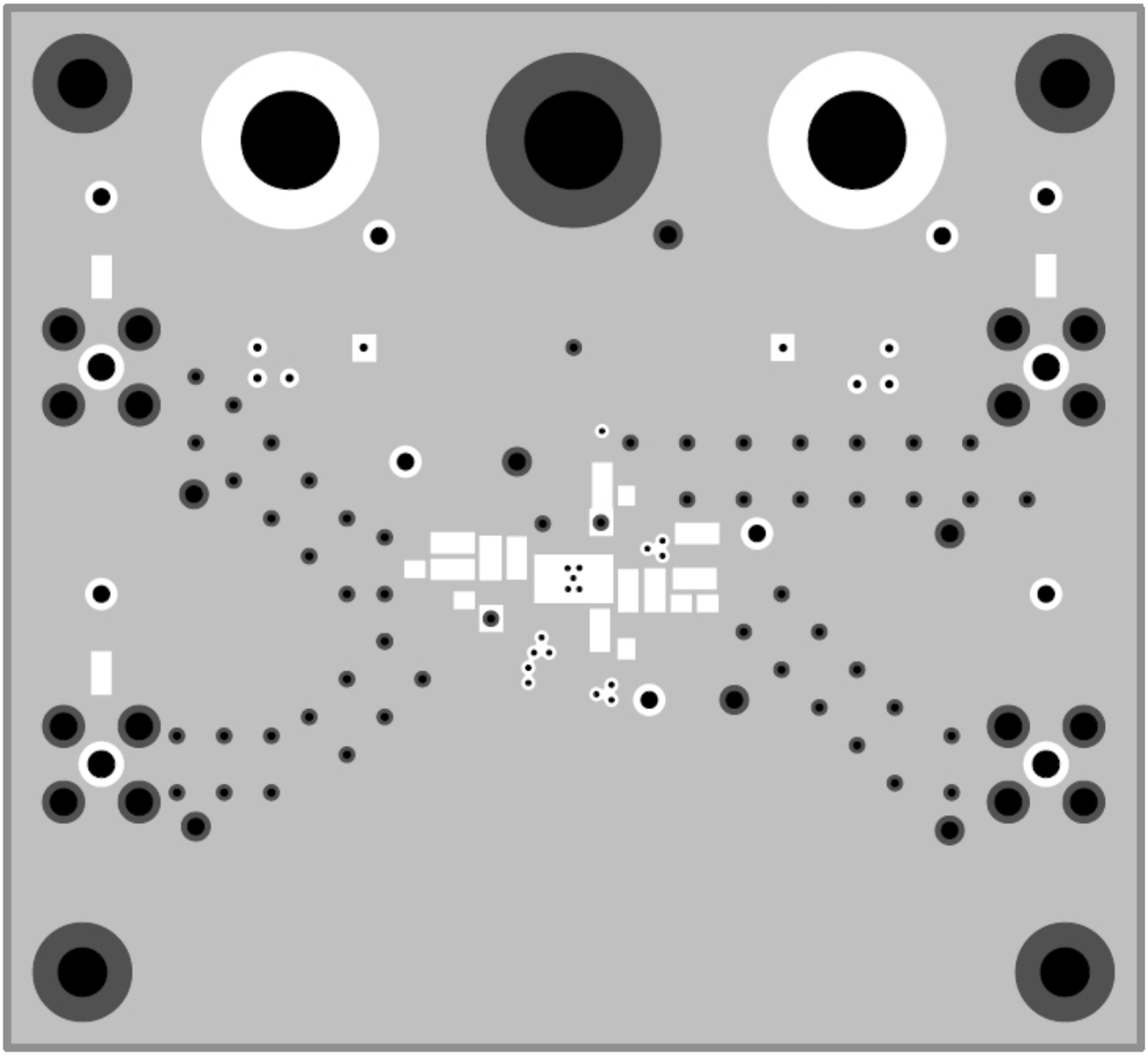

Figure 4. Layer 2 (Ground)

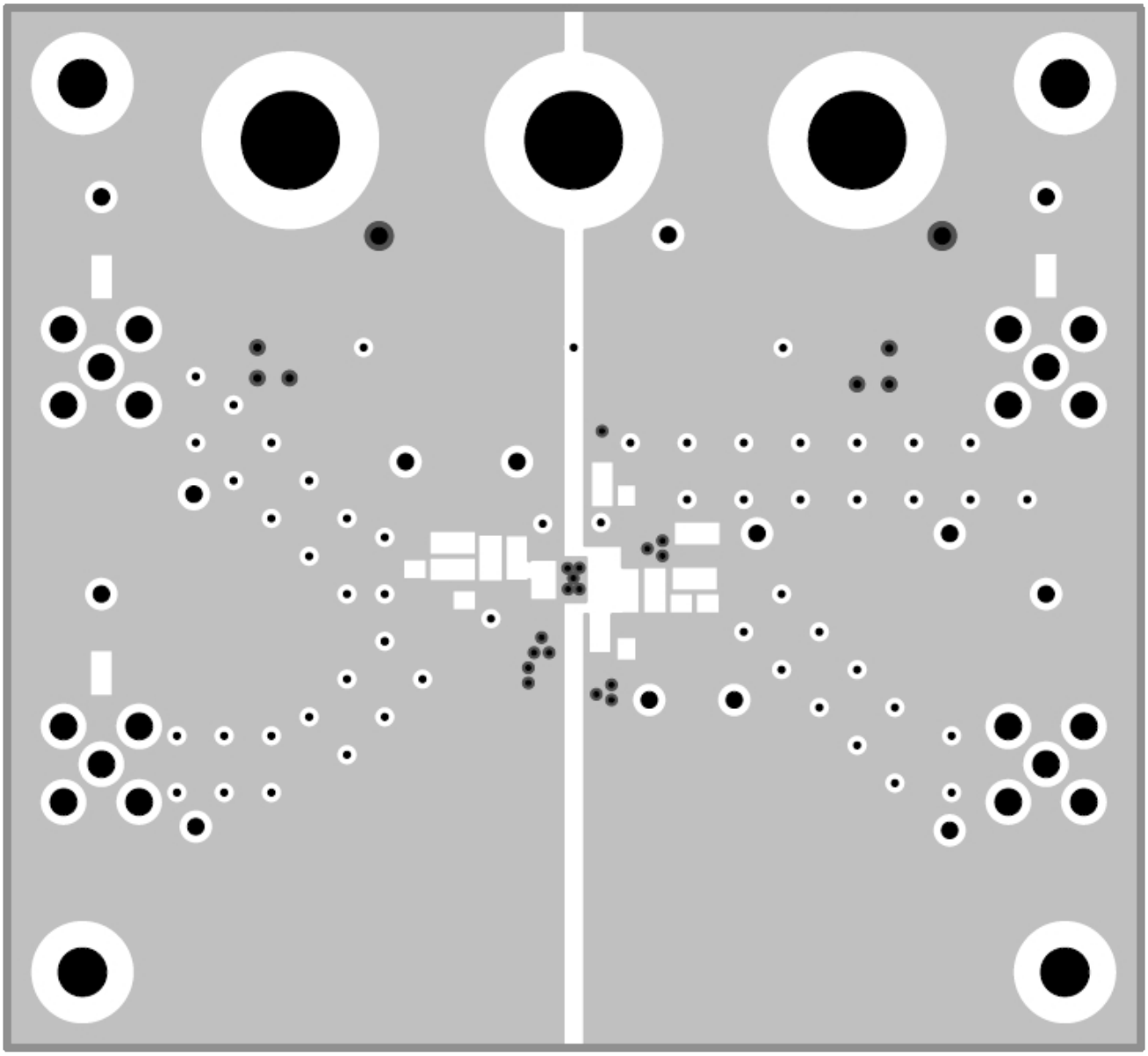

Figure 5. Layer 3 (Power)

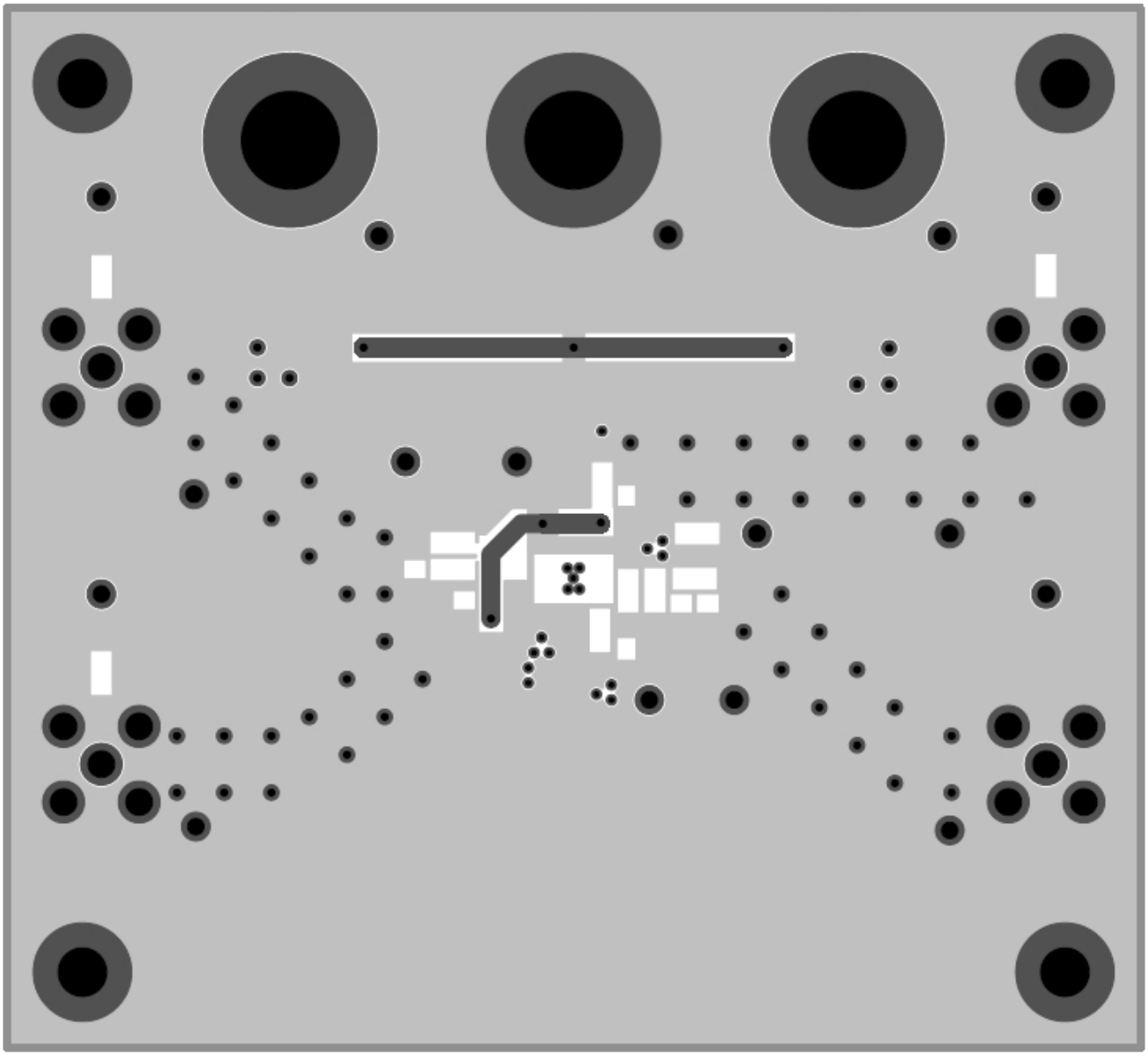

Figure 6. Bottom Layer (Ground)

3 Bill of Materials

Table 3 gives the bill of materials (BOM) used for the OPA1S2385EVM. It also lists examples of optional components.

Table 3. OPA1S2385EVM Bill of Materials

Count	RefDes	Value	Description	Part Number	Manufacturer
1	U1	N/A	OPA1S2385, DFN-10	OPA1S2385	Texas Instruments
3	C3, C4, C8	0.1µF	Capacitor, .010µF, 16V, X7R, 0603	C1608X7R1C104K	TDK Corporation
2	C5, C6	4.7µF	Capacitor, 4.7µF, 16V, X7R, 1206	C3216X7R1C475K/1.60	TDK Corporation
1	C12	470pF	Capacitor, 470pF, 50V, NP0, 0603	GRM1885C1H471JA01D	Murata Electronics
2	FB1, FB2	N/A	Ferrite Bead, 3A, 80 ohms, 1206	HI1206N800R-10	Laird-Signal Integrity Products
2	R1, R2	0ohm	Resistor, 0Ohm, 0603	ERJ-3GEY0R00V	Panasonic Electronic Components
6	R3, R11-R15	100ohm	Resistor, 100Ohm, 0603	ERJ-3EKF1000V	Panasonic Electronic Components
4	R4, R5, R8, R10	49.9ohm	Resistor, 49.9Ohm, 0603	ERJ-3EKF49R9V	Panasonic Electronic Components
7	TP1, TP3, TP4, TP6, TP7, TP8, TP10	N/A	Test Point, PC Mini, 0.040", White	5002	Keystone Electronics
1	TP5	N/A	Test Point, PC Mini, 0.040", Yellow	5004	Keystone Electronics
1	TP9	N/A	Test Point, PC Mini, 0.040", Red	5000	Keystone Electronics
3	TP2, TP14, TP15	N/A	Test Point, PC Mini, 0.040", Black	5001	Keystone Electronics
4	J1-J4	N/A	Connector Socket, SMA, Die-cast, PCB Mount	5-1814832-1	TE Connectivity
3	J5-J7	N/A	Connector Jack, Banana, Panel Mount	108-0740-001	Emerson Network Power Connectivity
4	Screws	N/A	Screw, Phillips, 4-40x3/8	PMS 440 0038 PH	B&F Fastener Supply
4	Standoffs	N/A	Standoff, Hex, 4-40THR, Aluminum, 0.500"	2203	Keystone Electronics
Not Installed	C1, C2, C7	N/A	Capacitor, 0603		
Not Installed	R6, R7, R9	N/A	Resistor, 0603		
Not Installed	TP11-TP13, TP16	N/A	Test Point, PC Mini, 0.040"		

4 Related Documentation from Texas Instruments

The following documents provide information regarding Texas Instruments' integrated circuits and support tools for the OPA1S2385EVM. This user's guide is available from the TI web site under literature number ***SBOU127***. Any letter appended to the literature number corresponds to the document revision that is current at the time of the writing of this document. Newer revisions may be available from the TI web site, or call the Texas Instruments' Literature Response Center at (800) 477-8924 or the Product Information Center at (972) 644-5580. When ordering, identify the document by both title and literature number.

Related Documentation

Document	Literature Number
OPA1S2385 product data sheet	SBOS645

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of (V–) – 0.1 V to (V+) + 0.1 V common-mode and the output voltage range of (V–) + 0.02 V to (V+) – 0.02 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +85°C. The EVM is designed to operate properly with certain components above +85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

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