

SX Family FPGAs



Leading Edge Performance

- 320 MHz Internal Performance
- 3.7 ns Clock-to-Out (Pin-to-Pin)
- 0.1 ns Input Setup
- 0.25 ns Clock Skew

Specifications

- 12,000 to 48,000 System Gates
- Up to 249 User-Programmable I/O Pins
- Up to 1,080 Flip-Flops
- 0.35 μ CMOS

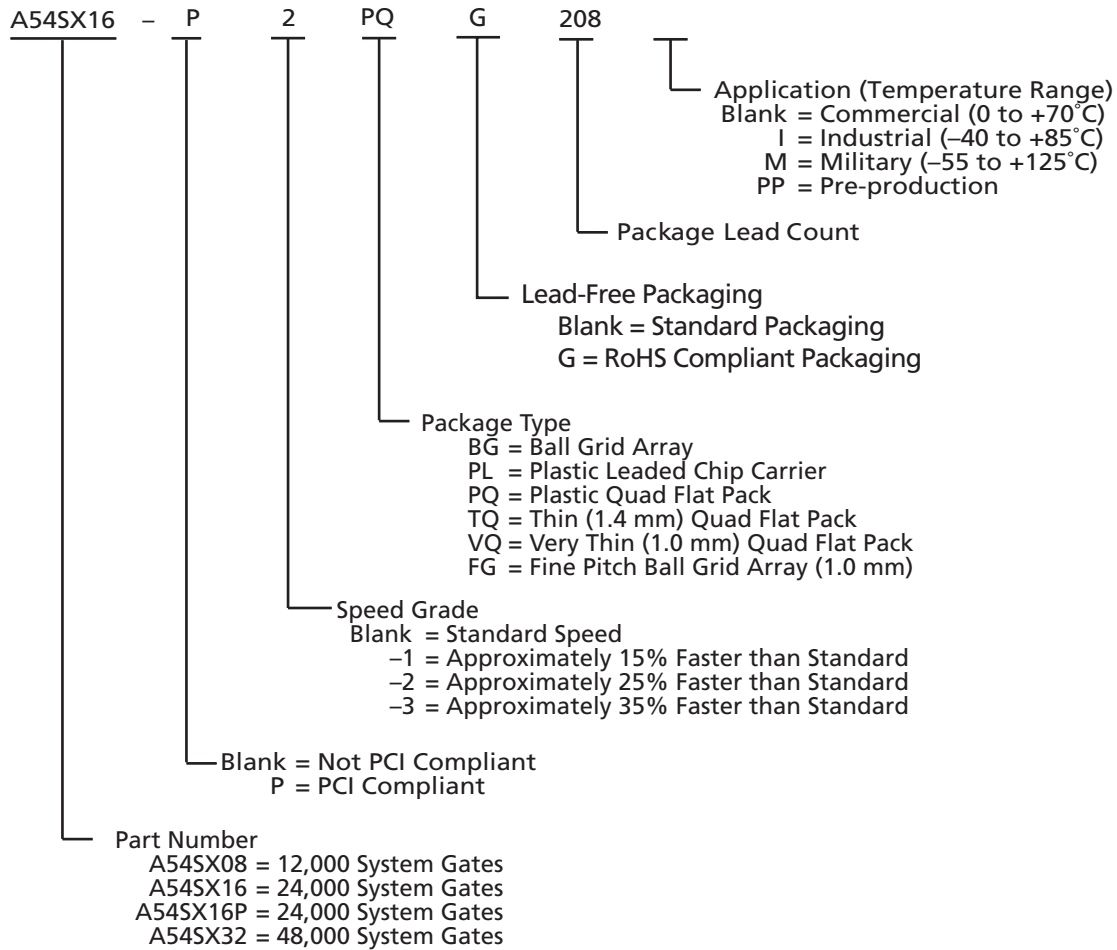
Features

- 66 MHz PCI
- CPLD and FPGA Integration
- Single-Chip Solution
- 100% Resource Utilization with 100% Pin Locking
- 3.3 V and 5.0 V Operation with 5.0 V Input Tolerance
- Very Low Power Consumption
- Deterministic, User-Controllable Timing
- Unique In-System Diagnostic and Debug Capability with Silicon Explorer II
- Boundary Scan Testing in Compliance with IEEE Standard 1149.1 (JTAG)
- Secure Programming Technology Prevents Reverse Engineering and Design Theft

SX Product Profile

| Device | A54SX08 | A54SX16 | A54SX16P | A54SX32 |
|--|-----------------|-----------------|-----------------|-----------------|
| Capacity | | | | |
| Typical Gates | 8,000 | 16,000 | 16,000 | 32,000 |
| System Gates | 12,000 | 24,000 | 24,000 | 48,000 |
| Logic Modules | 768 | 1,452 | 1,452 | 2,880 |
| Combinatorial Cells | 512 | 924 | 924 | 1,800 |
| Register Cells (Dedicated Flip-Flops) | 256 | 528 | 528 | 1,080 |
| Maximum User I/Os | 130 | 175 | 175 | 249 |
| Clocks | 3 | 3 | 3 | 3 |
| JTAG | Yes | Yes | Yes | Yes |
| PCI | – | – | Yes | – |
| Clock-to-Out | 3.7 ns | 3.9 ns | 4.4 ns | 4.6 ns |
| Input Setup (external) | 0.8 ns | 0.5 ns | 0.5 ns | 0.1 ns |
| Speed Grades | Std, –1, –2, –3 | Std, –1, –2, –3 | Std, –1, –2, –3 | Std, –1, –2, –3 |
| Temperature Grades | C, I, M | C, I, M | C, I, M | C, I, M |
| Packages (by pin count) | | | | |
| PLCC | 84 | – | – | – |
| PQFP | 208 | 208 | 208 | 208 |
| VQFP | 100 | 100 | 100 | – |
| TQFP | 144, 176 | 176 | 144, 176 | 144, 176 |
| PBGA | – | – | – | 313, 329 |
| FBGA | 144 | – | – | – |

Ordering Information



Plastic Device Resources

| Device | User I/Os (including clock buffers) | | | | | | | |
|----------|-------------------------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| | PLCC 84-Pin | VQFP 100-Pin | PQFP 208-Pin | TQFP 144-Pin | TQFP 176-Pin | PBGA 313-Pin | PBGA 329-Pin | FBGA 144-Pin |
| A54SX08 | 69 | 81 | 130 | 113 | 128 | - | - | 111 |
| A54SX16 | - | 81 | 175 | - | 147 | - | - | - |
| A54SX16P | - | 81 | 175 | 113 | 147 | - | - | - |
| A54SX32 | - | - | 174 | 113 | 147 | 249 | 249 | - |

Note: Package Definitions (Consult your local Actel sales representative for product availability):

- PLCC = Plastic Leaded Chip Carrier
- PQFP = Plastic Quad Flat Pack
- TQFP = Thin Quad Flat Pack
- VQFP = Very Thin Quad Flat Pack
- PBGA = Plastic Ball Grid Array
- FBGA = Fine Pitch (1.0 mm) Ball Grid Array

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SX Family FPGAs

General Description

The Actel SX family of FPGAs features a sea-of-modules architecture that delivers device performance and integration levels not currently achieved by any other FPGA architecture. SX devices greatly simplify design time, enable dramatic reductions in design costs and power consumption, and further decrease time to market for performance-intensive applications.

The Actel SX architecture features two types of logic modules, the combinatorial cell (C-cell) and the register cell (R-cell), each optimized for fast and efficient mapping of synthesized logic functions. The routing and interconnect resources are in the metal layers above the logic modules, providing optimal use of silicon. This enables the entire floor of the device to be spanned with an uninterrupted grid of fine-grained, synthesis-friendly logic modules (or “sea-of-modules”), which reduces the distance signals have to travel between logic modules. To minimize signal propagation delay, SX devices employ both local and general routing resources. The high-speed local routing resources (DirectConnect and FastConnect) enable very fast local signal propagation that is optimal for fast counters, state machines, and datapath logic. The general system of segmented routing tracks allows any logic module in the array to be connected to any other logic or I/O module. Within this system, propagation delay is minimized by limiting the number of antifuse interconnect elements to five (90 percent of connections typically use only three antifuses). The unique local and general routing structure featured in SX devices gives fast and predictable performance, allows 100 percent pin-locking with full logic utilization, enables concurrent PCB development, reduces design time, and allows designers to achieve performance goals with minimum effort.

Further complementing SX’s flexible routing structure is a hardwired, constantly loaded clock network that has been tuned to provide fast clock propagation with minimal clock skew. Additionally, the high performance of the internal logic has eliminated the need to embed latches or flip-flops in the I/O cells to achieve fast clock-to-out or fast input setup times. SX devices have easy to use I/O cells that do not require HDL instantiation, facilitating design reuse and reducing design and verification time.

SX Family Architecture

The SX family architecture was designed to satisfy next-generation performance and integration requirements for production-volume designs in a broad range of applications.

Programmable Interconnect Element

The SX family provides efficient use of silicon by locating the routing interconnect resources between the Metal 2 (M2) and Metal 3 (M3) layers (Figure 1-1 on page 1-2). This completely eliminates the channels of routing and interconnect resources between logic modules (as implemented on SRAM FPGAs and previous generations of antifuse FPGAs), and enables the entire floor of the device to be spanned with an uninterrupted grid of logic modules.

Interconnection between these logic modules is achieved using The Actel patented metal-to-metal programmable antifuse interconnect elements, which are embedded between the M2 and M3 layers. The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection.

The extremely small size of these interconnect elements gives the SX family abundant routing resources and provides excellent protection against design pirating. Reverse engineering is virtually impossible because it is extremely difficult to distinguish between programmed and unprogrammed antifuses, and there is no configuration bitstream to intercept.

Additionally, the interconnect elements (i.e., the antifuses and metal tracks) have lower capacitance and lower resistance than any other device of similar capacity, leading to the fastest signal propagation in the industry.

Logic Module Design

The SX family architecture is described as a “sea-of-modules” architecture because the entire floor of the device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing. The Actel SX family provides two types of logic modules, the register cell (R-cell) and the combinatorial cell (C-cell).

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and clock enable (using the S0 and S1 lines) control signals (Figure 1-2). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional

flexibility while allowing mapping of synthesized functions into the SX FPGA. The clock source for the R-cell can be chosen from either the hardwired clock or the routed clock.

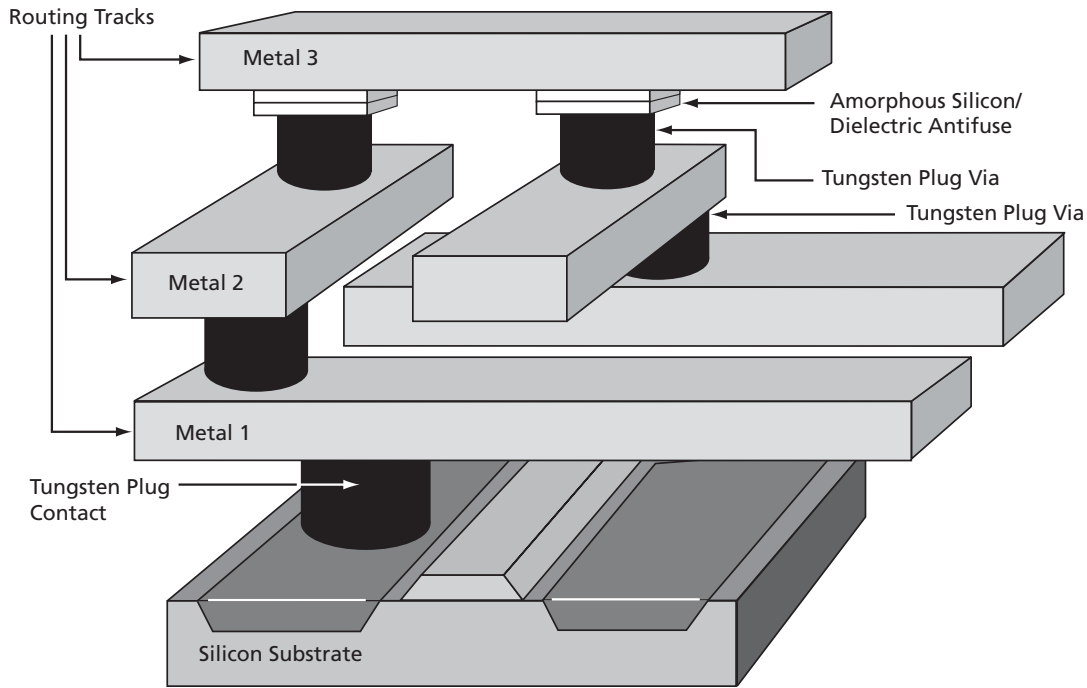


Figure 1-1 • SX Family Interconnect Elements

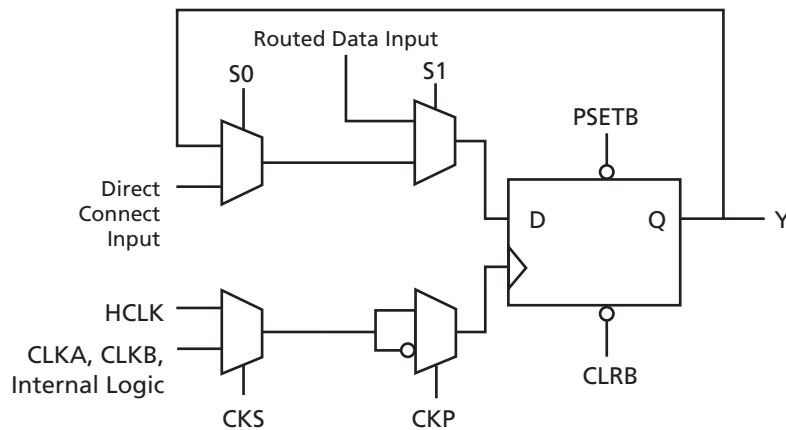


Figure 1-2 • R-Cell

The C-cell implements a range of combinatorial functions up to 5-inputs (Figure 1-3 on page 1-3). Inclusion of the DB input and its associated inverter function dramatically increases the number of combinatorial functions that can be implemented in a single module from 800 options in previous architectures to more than 4,000 in the SX architecture. An example of the improved flexibility

enabled by the inversion capability is the ability to integrate a 3-input exclusive-OR function into a single C-cell. This facilitates construction of 9-bit parity-tree functions with 2 ns propagation delays. At the same time, the C-cell structure is extremely synthesis friendly, simplifying the overall design and reducing synthesis time.

Chip Architecture

The SX family chip architecture provides a unique approach to module organization and chip routing that delivers the best register/logic mix for a wide variety of new and emerging applications.

Module Organization

Actel has arranged all C-cell and R-cell logic modules into horizontal banks called *clusters*. There are two types of *clusters*: Type 1 contains two C-cells and one R-cell, while Type 2 contains one C-cell and two R-cells.

To increase design efficiency and device performance, Actel has further organized these modules into *SuperClusters* (Figure 1-4). SuperCluster 1 is a two-wide grouping of Type 1 clusters. SuperCluster 2 is a two-wide group containing one Type 1 cluster and one Type 2 cluster. SX devices feature more SuperCluster 1 modules than SuperCluster 2 modules because designers typically require significantly more combinatorial logic than flip-flops.

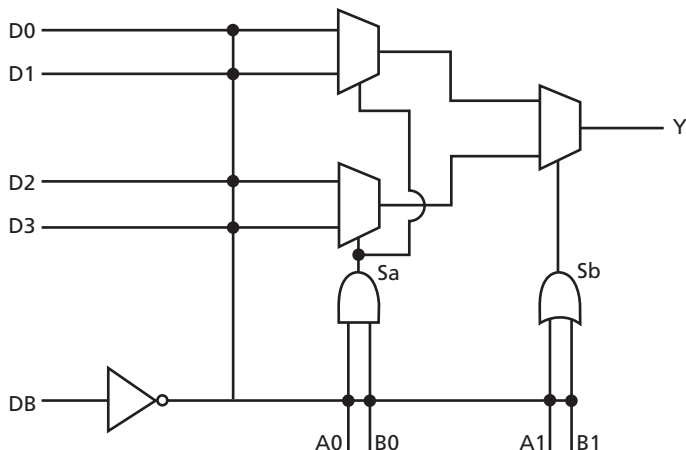


Figure 1-3 • C-Cell

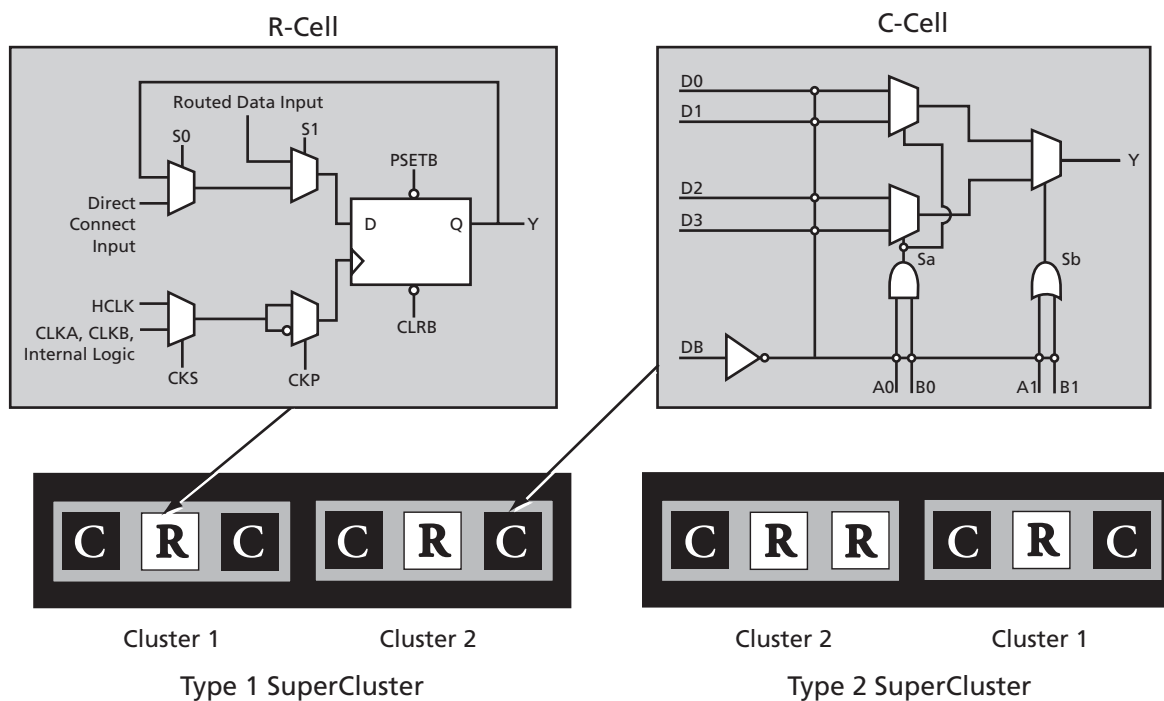


Figure 1-4 • Cluster Organization

Routing Resources

Clusters and SuperClusters can be connected through the use of two innovative local routing resources called *FastConnect* and *DirectConnect*, which enable extremely fast and predictable interconnection of modules within clusters and SuperClusters (Figure 1-5 and Figure 1-6). This routing architecture also dramatically reduces the number of antifuses required to complete a circuit, ensuring the highest possible performance.

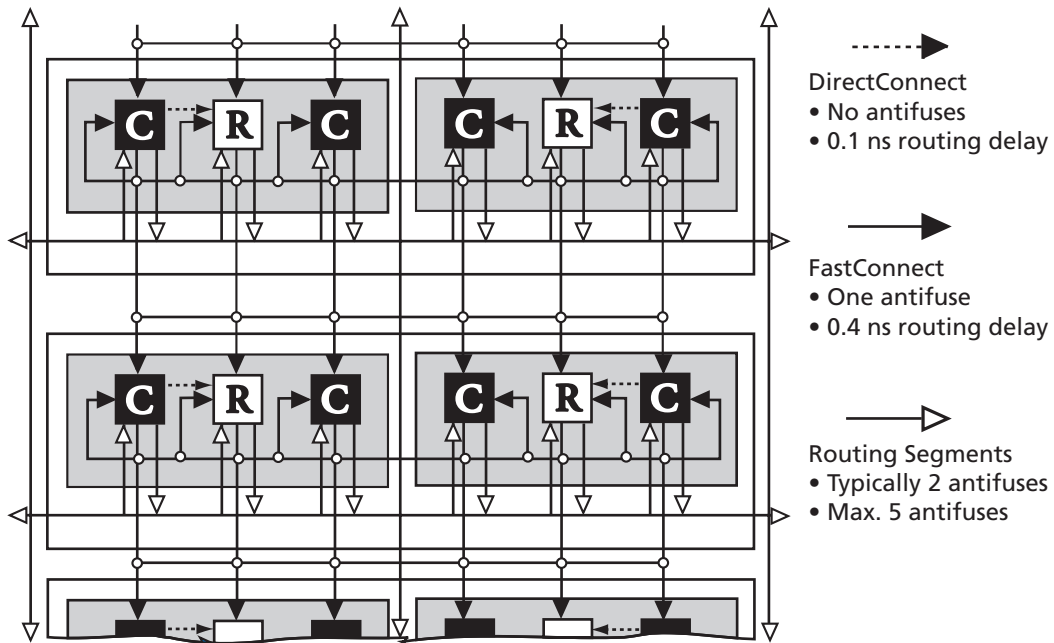


Figure 1-5 • DirectConnect and FastConnect for Type 1 SuperClusters

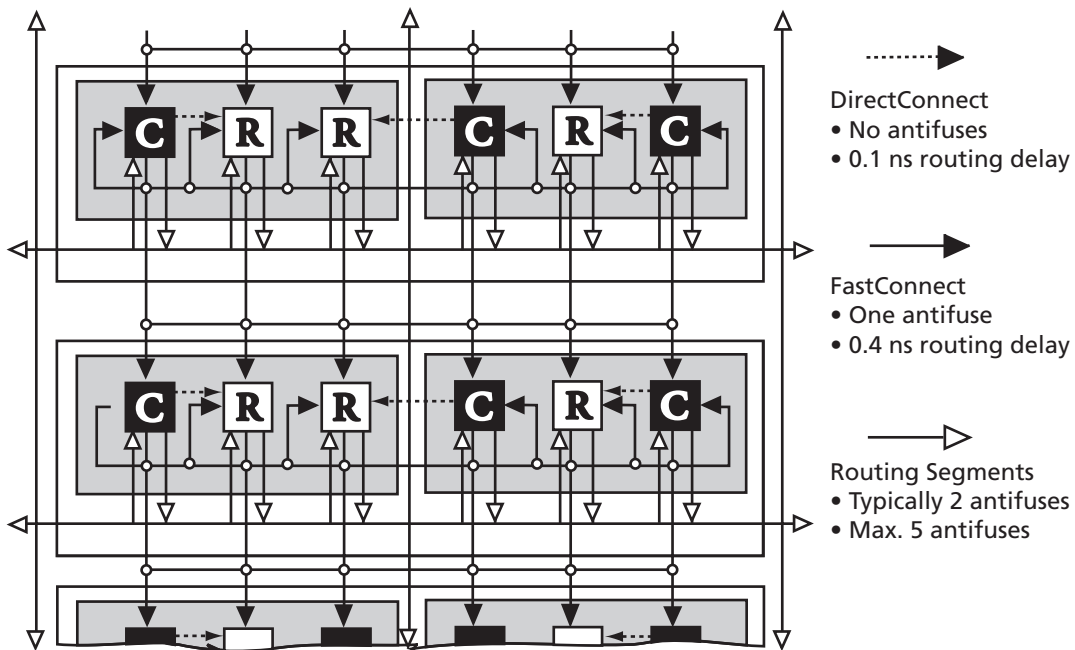


Figure 1-6 • DirectConnect and FastConnect for Type 2 SuperClusters

DirectConnect is a horizontal routing resource that provides connections from a C-cell to its neighboring R-cell in a given SuperCluster. DirectConnect uses a hardwired signal path requiring no programmable interconnection to achieve its fast signal propagation time of less than 0.1 ns.

FastConnect enables horizontal routing between any two logic modules within a given SuperCluster and vertical routing with the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering maximum pin-to-pin propagation of 0.4 ns.

In addition to DirectConnect and FastConnect, the architecture makes use of two globally oriented routing resources known as segmented routing and high-drive routing. The Actel segmented routing structure provides a variety of track lengths for extremely fast routing between SuperClusters. The exact combination of track lengths and antifuses within each path is chosen by the 100 percent automatic place-and-route software to minimize signal propagation delays.

The Actel high-drive routing structure provides three clock networks. The first clock, called HCLK, is hardwired from the HCLK buffer to the clock select multiplexer (MUX) in each R-cell. This provides a fast propagation path for the clock signal, enabling the 3.7 ns clock-to-out (pin-to-pin) performance of the SX devices. The hardwired clock is tuned to provide clock skew as low as 0.25 ns. The remaining two clocks (CLKA, CLKB) are global clocks that can be sourced from external pins or from internal logic signals within the SX device.

Other Architectural Features

Technology

The Actel SX family is implemented on a high-voltage twin-well CMOS process using 0.35 μ design rules. The metal-to-metal antifuse is made up of a combination of amorphous silicon and dielectric material with barrier metals and has a programmed ("on" state) resistance of 25 Ω with a capacitance of 1.0 fF for low signal impedance.

Performance

The combination of architectural features described above enables SX devices to operate with internal clock frequencies exceeding 300 MHz, enabling very fast execution of even complex logic functions. Thus, the SX family is an optimal platform upon which to integrate the functionality previously contained in multiple CPLDs. In addition, designs that previously would have required a gate array to meet performance goals can now be integrated into an SX device with dramatic improvements in cost and time to market. Using timing-driven place-and-route tools, designers can achieve highly deterministic device performance. With SX devices, designers do not need to use complicated performance-enhancing design techniques such as the use of redundant logic to reduce fanout on critical nets or the instantiation of macros in HDL code to achieve high performance.

I/O Modules

Each I/O on an SX device can be configured as an input, an output, a tristate output, or a bidirectional pin.

Even without the inclusion of dedicated I/O registers, these I/Os, in combination with array registers, can achieve clock-to-out (pad-to-pad) timing as fast as 3.7 ns. I/O cells that have embedded latches and flip-flops require instantiation in HDL code; this is a design complication not encountered in SX FPGAs. Fast pin-to-pin timing ensures that the device will have little trouble interfacing with any other device in the system, which in turn enables parallel design of system components and reduces overall design time.

Power Requirements

The SX family supports 3.3 V operation and is designed to tolerate 5.0 V inputs. (Table 1-1). Power consumption is extremely low due to the very short distances signals are required to travel to complete a circuit. Power requirements are further reduced because of the small number of low-resistance antifuses in the path. The antifuse architecture does not require active circuitry to hold a charge (as do SRAM or EPROM), making it the lowest power architecture on the market.

Table 1-1 • Supply Voltages

| Device | V _{CCA} | V _{CCI} | V _{CCR} | Maximum Input Tolerance | Maximum Output Drive |
|-------------------------------|------------------|------------------|------------------|-------------------------|----------------------|
| A54SX08 A54SX16 A54SX32 | 3.3 V | 3.3 V | 5.0 V | 5.0 V | 3.3 V |
| A54SX16-P* | 3.3 V | 3.3 V | 3.3 V | 3.3 V | 3.3 V |
| | 3.3 V | 3.3 V | 5.0 V | 5.0 V | 3.3 V |
| | 3.3 V | 5.0 V | 5.0 V | 5.0 V | 5.0 V |

Note: *A54SX16-P has three different entries because it is capable of both a 3.3 V and a 5.0 V drive.

Boundary Scan Testing (BST)

All SX devices are IEEE 1149.1 compliant. SX devices offer superior diagnostic and testing capabilities by providing Boundary Scan Testing (BST) and probing capabilities. These functions are controlled through the special test pins in conjunction with the program fuse. The functionality of each pin is described in [Table 1-2](#). In the dedicated test mode, TCK, TDI, and TDO are dedicated pins and cannot be used as regular I/Os. In flexible mode, TMS should be set HIGH through a pull-up resistor of 10 kΩ. TMS can be pulled LOW to initiate the test sequence.

The program fuse determines whether the device is in dedicated or flexible mode. The default (fuse not blown) is flexible mode.

Table 1-2 • Boundary Scan Pin Functionality

| Program Fuse Blown (Dedicated Test Mode) | Program Fuse Not Blown (Flexible Mode) |
|--|---|
| TCK, TDI, TDO are dedicated BST pins. | TCK, TDI, TDO are flexible and may be used as I/Os. |
| No need for pull-up resistor for TMS | Use a pull-up resistor of 10 kΩ on TMS. |

Dedicated Test Mode

In Dedicated mode, all JTAG pins are reserved for BST; designers cannot use them as regular I/Os. An internal pull-up resistor is automatically enabled on both TMS and TDI pins, and the TMS pin will function as defined in the IEEE 1149.1 (JTAG) specification.

To select Dedicated mode, users need to reserve the JTAG pins in Actel's Designer software by checking the "Reserve JTAG" box in "Device Selection Wizard" ([Figure 1-7](#)). JTAG pins comply with LVTTTL/TTL I/O specification regardless of whether they are used as a user I/O or a JTAG I/O. Refer to the [Table 1-5 on page 1-8](#) for detailed specifications.



Figure 1-7 • Device Selection Wizard

Development Tool Support

The SX family of FPGAs is fully supported by both the Actel Libero® Integrated Design Environment (IDE) and Designer FPGA Development software. Actel Libero IDE is a design management environment, seamlessly integrating design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment. Libero IDE includes Synplify® for Actel from Synplicity®, ViewDraw® for Actel from Mentor Graphics®, ModelSim® HDL Simulator from Mentor Graphics, WaveFormer Lite™ from SynaptiCAD™, and Designer software from Actel. Refer to the [Libero IDE flow diagram](#) (located on the Actel website) for more information.

Actel Designer software is a place-and-route tool and provides a comprehensive suite of backend support tools for FPGA development. The Designer software includes timing-driven place-and-route, and a world-class integrated static timing analyzer and constraints editor. With the Designer software, a user can select and lock package pins while only minimally impacting the results of place-and-route. Additionally, the back-annotation flow is compatible with all the major simulators, and the simulation results can be cross-probed with Silicon Explorer II, Actel integrated verification and logic analysis tool. Another tool included in the Designer software is the SmartGen core generator, which easily creates popular and commonly used logic functions for implementation into your schematic or HDL design. Actel Designer software is compatible with the most popular FPGA design entry and verification tools from companies such as Mentor Graphics, Synplicity, Synopsys®, and Cadence® Design Systems. The Designer software is available for both the Windows® and UNIX® operating systems.

Probe Circuit Control Pins

The Silicon Explorer II tool uses the boundary scan ports (TDI, TCK, TMS, and TDO) to select the desired nets for verification. The selected internal nets are assigned to the PRA/PRB pins for observation. [Figure 1-8 on page 1-7](#) illustrates the interconnection between Silicon Explorer II and the FPGA to perform in-circuit verification.

Design Considerations

The TDI, TCK, TDO, PRA, and PRB pins should not be used as input or bidirectional ports. Because these pins are active during probing, critical signals input through these pins are not available while probing. In addition, the Security Fuse should not be programmed because doing so disables the Probe Circuitry.

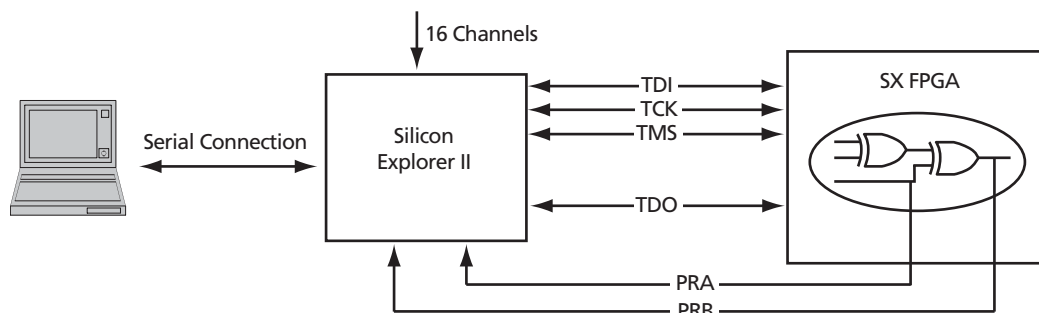


Figure 1-8 • Probe Setup

Programming

Device programming is supported through Silicon Sculptor series of programmers. In particular, Silicon Sculptor II are compact, robust, single-site and multi-site device programmer for the PC.

With standalone software, Silicon Sculptor II allows concurrent programming of multiple units from the same PC, ensuring the fastest programming times possible. Each fuse is subsequently verified by Silicon Sculptor II to insure correct programming. In addition, integrity tests ensure that no extra fuses are programmed. Silicon Sculptor II also provides extensive hardware self-testing capability.

The procedure for programming an SX device using Silicon Sculptor II are as follows:

1. Load the .AFM file
2. Select the device to be programmed
3. Begin programming

When the design is ready to go to production, Actel offers device volume-programming services either through distribution partners or via in-house programming from the factory.

For more details on programming SX devices, refer to the [Programming Antifuse Devices](#) application note and the [Silicon Sculptor II User's Guide](#).

3.3 V / 5 V Operating Conditions

 Table 1-3 • Absolute Maximum Ratings¹

| Symbol | Parameter | Limits | Units |
|-------------|---|---------------|-------|
| V_{CCR}^2 | DC Supply Voltage ³ | -0.3 to + 6.0 | V |
| V_{CCA}^2 | DC Supply Voltage | -0.3 to + 4.0 | V |
| V_{CCI}^2 | DC Supply Voltage (A54SX08, A54SX16, A54SX32) | -0.3 to + 4.0 | V |
| V_{CCI}^2 | DC Supply Voltage (A54SX16P) | -0.3 to + 6.0 | V |
| V_I | Input Voltage | -0.5 to + 5.5 | V |
| V_O | Output Voltage | -0.5 to + 3.6 | V |
| I_{IO} | I/O Source Sink Current ³ | -30 to + 5.0 | mA |
| T_{STG} | Storage Temperature | -65 to +150 | °C |

Notes:

1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.
2. V_{CCR} in the A54SX16P must be greater than or equal to V_{CCI} during power-up and power-down sequences and during normal operation.
3. Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than $V_{CC} + 0.5$ V or less than $GND - 0.5$ V, the internal protection diodes will forward-bias and can draw excessive current.

Table 1-4 • Recommended Operating Conditions

| Parameter | Commercial | Industrial | Military | Units |
|------------------------------|------------|-------------|-------------|------------------|
| Temperature Range* | 0 to + 70 | -40 to + 85 | -55 to +125 | °C |
| 3.3 V Power Supply Tolerance | ±10 | ±10 | ±10 | %V _{CC} |
| 5.0 V Power Supply Tolerance | ±5 | ±10 | ±10 | %V _{CC} |

Note: *Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.

Table 1-5 • Electrical Specifications

| Symbol | Parameter | Commercial | | Industrial | | Units |
|---------------------------------|---|--|--------------------------------------|---------------------------------|--------------------------------------|-------|
| | | Min. | Max. | Min. | Max. | |
| V _{OH} | (I _{OH} = -20 μA) (CMOS) (I _{OH} = -8 mA) (TTL) (I _{OH} = -6 mA) (TTL) | (V _{CCI} - 0.1) 2.4 | V _{CCI} V _{CCI} | (V _{CCI} - 0.1) 2.4 | V _{CCI} V _{CCI} | V |
| V _{OL} | (I _{OL} = 20 μA) (CMOS) (I _{OL} = 12 mA) (TTL) (I _{OL} = 8 mA) (TTL) | | 0.10 0.50 | | 0.50 | V |
| V _{IL} | | | 0.8 | | 0.8 | V |
| V _{IH} | | 2.0 | | 2.0 | | V |
| t _R , t _F | Input Transition Time t _R , t _F | | 50 | | 50 | ns |
| C _{IO} | C _{IO} I/O Capacitance | | 10 | | 10 | pF |
| I _{CC} | Standby Current, I _{CC} | | 4.0 | | 4.0 | mA |
| I _{CC(D)} | I _{CC(D)} I _{Dynamic} V _{CC} Supply Current | See "Evaluating Power in SX Devices" on page 1-16. | | | | |

PCI Compliance for the SX Family

The SX family supports 3.3 V and 5.0 V PCI and is compliant with the PCI Local Bus Specification Rev. 2.1.

Table 1-6 • A54SX16P DC Specifications (5.0 V PCI Operation)

| Symbol | Parameter | Condition | Min. | Max. | Units |
|--------------------|--|-------------------------------|------|-----------------------|-------|
| V _{CCA} | Supply Voltage for Array | | 3.0 | 3.6 | V |
| V _{CCR} | Supply Voltage required for Internal Biasing | | 4.75 | 5.25 | V |
| V _{CCI} | Supply Voltage for I/Os | | 4.75 | 5.25 | V |
| V _{IH} | Input High Voltage ¹ | | 2.0 | V _{CC} + 0.5 | V |
| V _{IL} | Input Low Voltage ¹ | | -0.5 | 0.8 | V |
| I _{IH} | Input High Leakage Current | V _{IN} = 2.7 | | 70 | μA |
| I _{IL} | Input Low Leakage Current | V _{IN} = 0.5 | | -70 | μA |
| V _{OH} | Output High Voltage | I _{OUT} = -2 mA | 2.4 | | V |
| V _{OL} | Output Low Voltage ² | I _{OUT} = 3 mA, 6 mA | | 0.55 | V |
| C _{IN} | Input Pin Capacitance ³ | | | 10 | pF |
| C _{CLK} | CLK Pin Capacitance | | 5 | 12 | pF |
| C _{IDSEL} | IDSEL Pin Capacitance ⁴ | | | 8 | pF |

Notes:

1. Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.
2. Signals without pull-up resistors must have 3 mA low output current. Signals requiring pull-up must have 6 mA; the latter include, FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, SERR#, PERR#, LOCK#, and, when used, AD[63::32], C/BE[7::4]#, PAR64, REQ64#, and ACK64#.
3. Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).
4. Lower capacitance on this input-only pin allows for non-resistive coupling to AD[xx].

A54SX16P AC Specifications for (PCI Operation)

Table 1-7 • A54SX16P AC Specifications for (PCI Operation)

| Symbol | Parameter | Condition | Min. | Max. | Units |
|--------------|------------------------|----------------------------------|-------------------------------|---------------------|-------|
| $I_{OH(AC)}$ | Switching Current High | $0 < V_{OUT} \leq 1.4^1$ | -44 | | mA |
| | | $1.4 \leq V_{OUT} < 2.4^1, 2$ | $-44 + (V_{OUT} - 1.4)/0.024$ | | mA |
| | | $3.1 < V_{OUT} < V_{CC}^{1, 3}$ | | EQ 1-1 on page 1-11 | |
| | (Test Point) | $V_{OUT} = 3.1^3$ | | -142 | mA |
| $I_{OL(AC)}$ | Switching Current High | $V_{OUT} \geq 2.2^1$ | 95 | | mA |
| | | $2.2 > V_{OUT} > 0.55^1$ | $V_{OUT}/0.023$ | | |
| | | $0.71 > V_{OUT} > 0^{1, 3}$ | | EQ 1-2 on page 1-11 | mA |
| | (Test Point) | $V_{OUT} = 0.71^3$ | | 206 | mA |
| I_{CL} | Low Clamp Current | $-5 < V_{IN} \leq -1$ | $-25 + (V_{IN} + 1)/0.015$ | | mA |
| $slew_R$ | Output Rise Slew Rate | 0.4 V to 2.4 V load ⁴ | 1 | 5 | V/ns |
| $slew_F$ | Output Fall Slew Rate | 2.4 V to 0.4 V load ⁴ | 1 | 5 | V/ns |

Notes:

1. Refer to the V/I curves in Figure 1-9 on page 1-11. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half-size output drivers may be used on these signals. This specification does not apply to CLK and RST#, which are system outputs. "Switching Current High" specifications are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD#, which are open drain outputs.
2. Note that this segment of the minimum current curve is drawn from the AC drive point directly to the DC drive point rather than toward the voltage rail (as is done in the pull-down curve). This difference is intended to allow for an optional N-channel pull-up.
3. Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (A and B) are provided with the respective diagrams in Figure 1-9 on page 1-11. The equation defined maxima should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.
4. This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per revision 2.0 of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is now required (the maximum is no longer simply a guideline). Since adherence to the maximum slew rate was not required prior to revision 2.1 of the specification, there may be components in the market for some time that have faster edge rates; therefore, motherboard designers must bear in mind that rise and fall times faster than this specification could occur, and should ensure that signal integrity modeling accounts for this. Rise slew rate does not apply to open drain outputs.

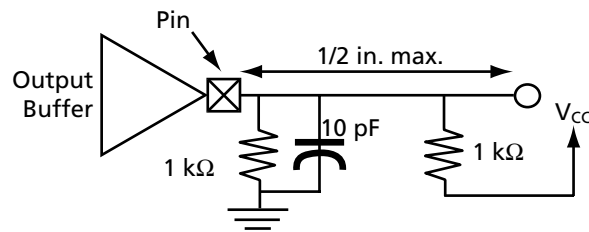


Figure 1-9 shows the 5.0 V PCI V/I curve and the minimum and maximum PCI drive characteristics of the A54SX16P device.

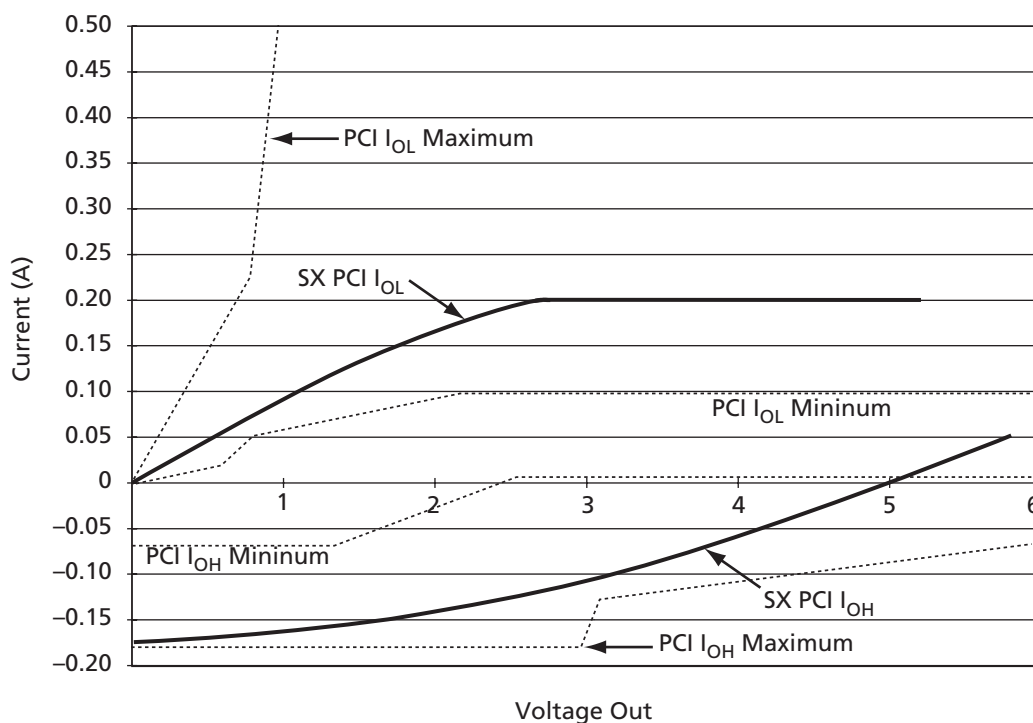


Figure 1-9 • 5.0 V PCI Curve for A54SX16P Device

$$I_{OH} = 11.9 \times (V_{OUT} - 5.25) \times (V_{OUT} + 2.45)$$

for $V_{CC} > V_{OUT} > 3.1$ V

EQ 1-1

$$I_{OL} = 78.5 \times V_{OUT} \times (4.4 - V_{OUT})$$

for 0 V $< V_{OUT} < 0.71$ V

EQ 1-2

A54SX16P DC Specifications (3.3 V PCI Operation)

Table 1-8 • A54SX16P DC Specifications (3.3 V PCI Operation)

| Symbol | Parameter | Condition | Min. | Max. | Units |
|-------------|--|------------------------|-------------|----------------|---------|
| V_{CCA} | Supply Voltage for Array | | 3.0 | 3.6 | V |
| V_{CCR} | Supply Voltage required for Internal Biasing | | 3.0 | 3.6 | V |
| V_{CCI} | Supply Voltage for I/Os | | 3.0 | 3.6 | V |
| V_{IH} | Input High Voltage | | $0.5V_{CC}$ | $V_{CC} + 0.5$ | V |
| V_{IL} | Input Low Voltage | | -0.5 | $0.3V_{CC}$ | V |
| I_{IPU} | Input Pull-up Voltage ¹ | | $0.7V_{CC}$ | | V |
| I_{IL} | Input Leakage Current ² | $0 < V_{IN} < V_{CC}$ | | ± 10 | μA |
| V_{OH} | Output High Voltage | $I_{OUT} = -500 \mu A$ | $0.9V_{CC}$ | | V |
| V_{OL} | Output Low Voltage | $I_{OUT} = 1500 \mu A$ | | $0.1V_{CC}$ | V |
| C_{IN} | Input Pin Capacitance ³ | | | 10 | pF |
| C_{CLK} | CLK Pin Capacitance | | 5 | 12 | pF |
| C_{IDSEL} | IDSEL Pin Capacitance ⁴ | | | 8 | pF |

Notes:

1. This specification should be guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Applications sensitive to static power utilization should assure that the input buffer is conducting minimum current at this input voltage.
2. Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.
3. Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).
4. Lower capacitance on this input-only pin allows for non-resistive coupling to AD[xx].

A54SX16P AC Specifications (3.3 V PCI Operation)

Table 1-9 • A54SX16P AC Specifications (3.3 V PCI Operation)

| Symbol | Parameter | Condition | Min. | Max. | Units |
|--------------|------------------------------------|---|-------------------------------------|---------------------|-------|
| $I_{OH(AC)}$ | Switching Current High | $0 < V_{OUT} \leq 0.3V_{CC}^1$ | | | mA |
| | | $0.3V_{CC} \leq V_{OUT} < 0.9V_{CC}^1$ | $-12V_{CC}$ | | mA |
| | | $0.7V_{CC} < V_{OUT} < V_{CC}^{1,2}$ | $-17.1 + (V_{CC} - V_{OUT})$ | EQ 1-3 on page 1-14 | |
| | (Test Point) | $V_{OUT} = 0.7V_{CC}^2$ | | $-32V_{CC}$ | mA |
| $I_{OL(AC)}$ | Switching Current High | $V_{CC} > V_{OUT} \geq 0.6V_{CC}^1$ | | | mA |
| | | $0.6V_{CC} > V_{OUT} > 0.1V_{CC}^1$ | $16V_{CC}$ | | mA |
| | | $0.18V_{CC} > V_{OUT} > 0^{1,2}$ | $26.7V_{OUT}$ | EQ 1-4 on page 1-14 | mA |
| | (Test Point) | $V_{OUT} = 0.18V_{CC}^2$ | | $38V_{CC}$ | |
| I_{CL} | Low Clamp Current | $-3 < V_{IN} \leq -1$ | $-25 + (V_{IN} + 1)/0.015$ | | mA |
| I_{CH} | High Clamp Current | $-3 < V_{IN} \leq -1$ | $25 + (V_{IN} - V_{OUT} - 1)/0.015$ | | mA |
| $slew_R$ | Output Rise Slew Rate ³ | 0.2V _{CC} to 0.6V _{CC} load | 1 | 4 | V/ns |
| $slew_F$ | Output Fall Slew Rate ³ | 0.6V _{CC} to 0.2V _{CC} load | 1 | 4 | V/ns |

Notes:

1. Refer to the VII curves in Figure 1-10 on page 1-14. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST# which are system outputs. "Switching Current High" specification are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD# which are open drain outputs.
2. Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (C and D) are provided with the respective diagrams in Figure 1-10 on page 1-14. The equation defined maxima should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.
3. This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per the latest revision of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is required (the maximum is no longer simply a guideline). Rise slew rate does not apply to open drain outputs.

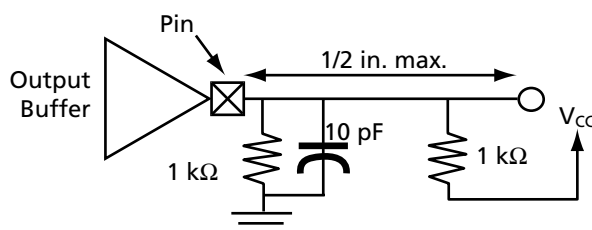


Figure 1-10 shows the 3.3 V PCI V/I curve and the minimum and maximum PCI drive characteristics of the A54SX16P device.

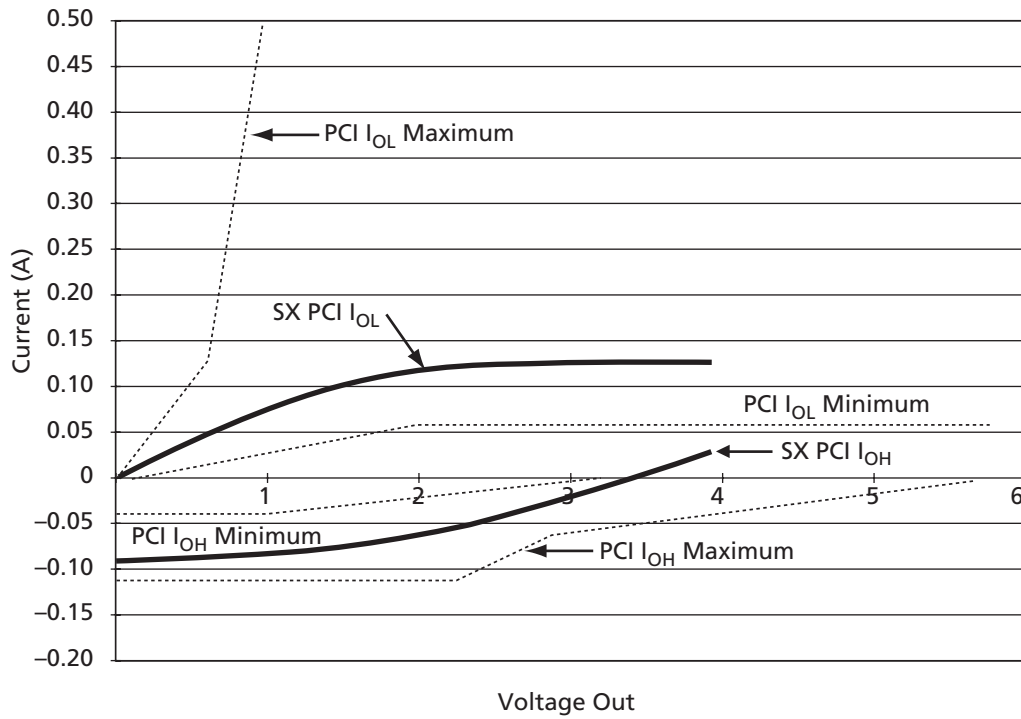


Figure 1-10 • 3.3 V PCI Curve for A54SX16P Device

$$I_{OH} = (98.0/V_{CC}) \times (V_{OUT} - V_{CC}) \times (V_{OUT} + 0.4V_{CC})$$

for $V_{CC} > V_{OUT} > 0.7 V_{CC}$

EQ 1-3

$$I_{OL} = (256/V_{CC}) \times V_{OUT} \times (V_{CC} - V_{OUT})$$

for $0 V < V_{OUT} < 0.18 V_{CC}$

EQ 1-4

Power-Up Sequencing

Table 1-10 • Power-Up Sequencing

| V _{CCA} | V _{CCR} | V _{CCI} | Power-Up Sequence | Comments |
|----------------------------------|------------------|------------------|-----------------------------|------------------------------|
| A54SX08, A54SX16, A54SX32 | | | | |
| 3.3 V | 5.0 V | 3.3 V | 5.0 V First 3.3 V Second | No possible damage to device |
| | | | 3.3 V First 5.0 V Second | Possible damage to device |
| A54SX16P | | | | |
| 3.3 V | 3.3 V | 3.3 V | 3.3 V Only | No possible damage to device |
| 3.3 V | 5.0 V | 3.3 V | 5.0 V First 3.3 V Second | No possible damage to device |
| | | | 3.3 V First 5.0 V Second | Possible damage to device |
| 3.3 V | 5.0 V | 5.0 V | 5.0 V First 3.3 V Second | No possible damage to device |
| | | | 3.3 V First 5.0 V Second | No possible damage to device |

Note: No inputs should be driven (high or low) before completion of power-up.

Power-Down Sequencing

Table 1-11 • Power-Down Sequencing

| V _{CCA} | V _{CCR} | V _{CCI} | Power-Down Sequence | Comments |
|----------------------------------|------------------|------------------|-----------------------------|------------------------------|
| A54SX08, A54SX16, A54SX32 | | | | |
| 3.3 V | 5.0 V | 3.3 V | 5.0 V First 3.3 V Second | Possible damage to device |
| | | | 3.3 V First 5.0 V Second | No possible damage to device |
| A54SX16P | | | | |
| 3.3 V | 3.3 V | 3.3 V | 3.3 V Only | No possible damage to device |
| 3.3 V | 5.0 V | 3.3 V | 5.0 V First 3.3 V Second | Possible damage to device |
| | | | 3.3 V First 5.0 V Second | No possible damage to device |
| 3.3 V | 5.0 V | 5.0 V | 5.0 V First 3.3 V Second | No possible damage to device |
| | | | 3.3 V First 5.0 V Second | No possible damage to device |

Note: No inputs should be driven (high or low) after the beginning of the power-down sequence.

Evaluating Power in SX Devices

A critical element of system reliability is the ability of electronic devices to safely dissipate the heat generated during operation. The thermal characteristics of a circuit depend on the device and package used, the operating temperature, the operating current, and the system's ability to dissipate heat.

You should complete a power evaluation early in the design process to help identify potential heat-related problems in the system and to prevent the system from exceeding the device's maximum allowed junction temperature.

The actual power dissipated by most applications is significantly lower than the power the package can dissipate. However, a thermal analysis should be performed for all projects. To perform a power evaluation, follow these steps:

1. Estimate the power consumption of the application.
2. Calculate the maximum power allowed for the device and package.
3. Compare the estimated power and maximum power values.

Estimating Power Consumption

The total power dissipation for the SX family is the sum of the DC power dissipation and the AC power dissipation. Use EQ 1-5 to calculate the estimated power consumption of your application.

$$P_{\text{Total}} = P_{\text{DC}} + P_{\text{AC}} \tag{EQ 1-5}$$

DC Power Dissipation

The power due to standby current is typically a small component of the overall power. The Standby power is shown in Table 1-12 for commercial, worst-case conditions (70°C).

Table 1-12 • Standby Power

| I _{CC} | V _{CC} | Power |
|-----------------|-----------------|---------|
| 4 mA | 3.6 V | 14.4 mW |

The DC power dissipation is defined in EQ 1-6.

$$P_{\text{DC}} = (I_{\text{standby}}) \times V_{\text{CCA}} + (I_{\text{standby}}) \times V_{\text{CCR}} + (I_{\text{standby}}) \times V_{\text{CCI}} + xV_{\text{OL}} \times I_{\text{OL}} + y(V_{\text{CCI}} - V_{\text{OH}}) \times V_{\text{OH}} \tag{EQ 1-6}$$

AC Power Dissipation

The power dissipation of the SX Family is usually dominated by the dynamic power dissipation. Dynamic power dissipation is a function of frequency, equivalent capacitance, and power supply voltage. The AC power dissipation is defined in EQ 1-7 and EQ 1-8.

$$P_{\text{AC}} = P_{\text{Module}} + P_{\text{RCLKA Net}} + P_{\text{RCLKB Net}} + P_{\text{HCLK Net}} + P_{\text{Output Buffer}} + P_{\text{Input Buffer}} \tag{EQ 1-7}$$

$$P_{\text{AC}} = V_{\text{CCA}}^2 \times [(m \times C_{\text{EQM}} \times f_m)_{\text{Module}} + (n \times C_{\text{EQI}} \times f_n)_{\text{Input Buffer}} + (p \times (C_{\text{EQO}} + C_L) \times f_p)_{\text{Output Buffer}} + (0.5 \times (q_1 \times C_{\text{EQCR}} \times f_{q1}) + (r_1 \times f_{q1}))_{\text{RCLKA}} + (0.5 \times (q_2 \times C_{\text{EQCR}} \times f_{q2}) + (r_2 \times f_{q2}))_{\text{RCLKB}} + (0.5 \times (s_1 \times C_{\text{EQHV}} \times f_{s1}) + (C_{\text{EQHF}} \times f_{s1}))_{\text{HCLK}}] \tag{EQ 1-8}$$

Definition of Terms Used in Formula

- m = Number of logic modules switching at f_m
- n = Number of input buffers switching at f_n
- p = Number of output buffers switching at f_p
- q₁ = Number of clock loads on the first routed array clock
- q₂ = Number of clock loads on the second routed array clock
- x = Number of I/Os at logic low
- y = Number of I/Os at logic high
- r₁ = Fixed capacitance due to first routed array clock
- r₂ = Fixed capacitance due to second routed array clock
- s₁ = Number of clock loads on the dedicated array clock
- C_{EQM} = Equivalent capacitance of logic modules in pF
- C_{EQI} = Equivalent capacitance of input buffers in pF
- C_{EQO} = Equivalent capacitance of output buffers in pF
- C_{EQCR} = Equivalent capacitance of routed array clock in pF
- C_{EQHV} = Variable capacitance of dedicated array clock
- C_{EQHF} = Fixed capacitance of dedicated array clock
- C_L = Output lead capacitance in pF
- f_m = Average logic module switching rate in MHz
- f_n = Average input buffer switching rate in MHz
- f_p = Average output buffer switching rate in MHz
- f_{q1} = Average first routed array clock rate in MHz
- f_{q2} = Average second routed array clock rate in MHz
- f_{s1} = Average dedicated array clock rate in MHz

Table 1-13 shows capacitance values for various devices.

Table 1-13 • Capacitance Values for Devices

| | A545X08 | A545X16 | A545X16P | A545X32 |
|------------------------|---------|---------|----------|---------|
| C _{EQM} (pF) | 4.0 | 4.0 | 4.0 | 4.0 |
| C _{EQI} (pF) | 3.4 | 3.4 | 3.4 | 3.4 |
| C _{EQO} (pF) | 4.7 | 4.7 | 4.7 | 4.7 |
| C _{EQCR} (pF) | 1.6 | 1.6 | 1.6 | 1.6 |
| C _{EQHV} | 0.615 | 0.615 | 0.615 | 0.615 |
| C _{EQHF} | 60 | 96 | 96 | 140 |
| r ₁ (pF) | 87 | 138 | 138 | 171 |
| r ₂ (pF) | 87 | 138 | 138 | 171 |

Table 1-14 • Power Consumption Guidelines

| Description | Power Consumption Guideline |
|---|-----------------------------|
| Logic Modules (m) | 20% of modules |
| Inputs Switching (n) | # inputs/4 |
| Outputs Switching (p) | # outputs/4 |
| First Routed Array Clock Loads (q ₁) | 20% of register cells |
| Second Routed Array Clock Loads (q ₂) | 20% of register cells |
| Load Capacitance (C _L) | 35 pF |
| Average Logic Module Switching Rate (f _m) | f/10 |
| Average Input Switching Rate (f _n) | f/5 |
| Average Output Switching Rate (f _p) | f/10 |
| Average First Routed Array Clock Rate (f _{q1}) | f/2 |
| Average Second Routed Array Clock Rate (f _{q2}) | f/2 |
| Average Dedicated Array Clock Rate (f _{s1}) | f |
| Dedicated Clock Array Clock Loads (s ₁) | 20% of regular modules |

Follow the steps below to estimate power consumption. The values provided for the sample calculation below are for the shift register design above. This method for estimating power consumption is conservative and the actual power consumption of your design may be less than the estimated power consumption.

The total power dissipation for the SX family is the sum of the AC power dissipation and the DC power dissipation.

$$P_{\text{Total}} = P_{\text{AC}} \text{ (dynamic power)} + P_{\text{DC}} \text{ (static power)}$$

EQ 1-9

Guidelines for Calculating Power Consumption

The power consumption guidelines are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation. These guidelines are shown in Table 1-14.

Sample Power Calculation

One of the designs used to characterize the SX family was a 528 bit serial-in, serial-out shift register. The design utilized 100 percent of the dedicated flip-flops of an A545X16P device. A pattern of 0101... was clocked into the device at frequencies ranging from 1 MHz to 200 MHz. Shifting in a series of 0101... caused 50 percent of the flip-flops to toggle from low to high at every clock cycle.

AC Power Dissipation

$$P_{\text{AC}} = P_{\text{Module}} + P_{\text{RCLKA Net}} + P_{\text{RCLKB Net}} + P_{\text{HCLK Net}} + P_{\text{Output Buffer}} + P_{\text{Input Buffer}}$$

EQ 1-10

$$P_{\text{AC}} = V_{\text{CCA}}^2 \times [(m \times C_{\text{EQM}} \times f_m)_{\text{Module}} + (n \times C_{\text{EQI}} \times f_n)_{\text{Input Buffer}} + (p \times (C_{\text{EQO}} + C_L) \times f_p)_{\text{Output Buffer}} + (0.5 (q_1 \times C_{\text{EQCR}} \times f_{q1}) + (r_1 \times f_{q1}))_{\text{RCLKA}} + (0.5 (q_2 \times C_{\text{EQCR}} \times f_{q2}) + (r_2 \times f_{q2}))_{\text{RCLKB}} + (0.5 (s_1 \times C_{\text{EQHV}} \times f_{s1}) + (C_{\text{EQHF}} \times f_{s1}))_{\text{HCLK}}]$$

EQ 1-11

Step 1: Define Terms Used in Formula

| | | |
|---|------------|-----------|
| | V_{CCA} | 3.3 |
| Module | | |
| Number of logic modules switching at f_m (Used 50%) | m | 264 |
| Average logic modules switching rate f_m (MHz) (Guidelines: $f/10$) | f_m | 20 |
| Module capacitance C_{EQM} (pF) | C_{EQM} | 4.0 |
| Input Buffer | | |
| Number of input buffers switching at f_n | n | 1 |
| Average input switching rate f_n (MHz) (Guidelines: $f/5$) | f_n | 40 |
| Input buffer capacitance C_{EQI} (pF) | C_{EQI} | 3.4 |
| Output Buffer | | |
| Number of output buffers switching at f_p | p | 1 |
| Average output buffers switching rate f_p (MHz) (Guidelines: $f/10$) | f_p | 20 |
| Output buffers buffer capacitance C_{EQO} (pF) | C_{EQO} | 4.7 |
| Output Load capacitance C_L (pF) | C_L | 35 |
| RCLKA | | |
| Number of Clock loads q_1 | q_1 | 528 |
| Capacitance of routed array clock (pF) | C_{EQCR} | 1.6 |
| Average clock rate (MHz) | f_{q1} | 200 |
| Fixed capacitance (pF) | r_1 | 138 |
| RCLKB | | |
| Number of Clock loads q_2 | q_2 | 0 |
| Capacitance of routed array clock (pF) | C_{EQCR} | 1.6 |
| Average clock rate (MHz) | f_{q2} | 0 |
| Fixed capacitance (pF) | r_2 | 138 |
| HCLK | | |
| Number of Clock loads | s_1 | 0 |
| Variable capacitance of dedicated array clock (pF) | C_{EQHV} | 0.61 5 |
| Fixed capacitance of dedicated array clock (pF) | C_{EQHF} | 96 |
| Average clock rate (MHz) | f_{s1} | 0 |

Step 2: Calculate Dynamic Power Consumption

| | |
|--|----------|
| $V_{CCA} \times V_{CCA}$ | 10.89 |
| $m \times f_m \times C_{EQM}$ | 0.02112 |
| $n \times f_n \times C_{EQI}$ | 0.000136 |
| $p \times f_p \times (C_{EQO} + C_L)$ | 0.000794 |
| $0.5 (q_1 \times C_{EQCR} \times f_{q1}) + (r_1 \times f_{q1})$ | 0.11208 |
| $0.5(q_2 \times C_{EQCR} \times f_{q2}) + (r_2 \times f_{q2})$ | 0 |
| $0.5 (s_1 \times C_{EQHV} \times f_{s1}) + (C_{EQHF} \times f_{s1})$ | 0 |
| $P_{AC} = 1.461 \text{ W}$ | |

Step 3: Calculate DC Power Dissipation
DC Power Dissipation

$$P_{DC} = (I_{standby}) \times V_{CCA} + (I_{standby}) \times V_{CCR} + (I_{standby}) \times V_{CCI} + X \times V_{OL} \times I_{OL} + Y(V_{CCI} - V_{OH}) \times V_{OH}$$

EQ 1-12

For a rough estimate of DC Power Dissipation, only use $P_{DC} = (I_{standby}) \times V_{CCA}$. The rest of the formula provides a very small number that can be considered negligible.

$$P_{DC} = (I_{standby}) \times V_{CCA}$$

$$P_{DC} = .55 \text{ mA} \times 3.3 \text{ V}$$

$$P_{DC} = 0.001815 \text{ W}$$

Step 4: Calculate Total Power Consumption

$$P_{Total} = P_{AC} + P_{DC}$$

$$P_{Total} = 1.461 + 0.001815$$

$$P_{Total} = 1.4628 \text{ W}$$

Step 5: Compare Estimated Power Consumption against Characterized Power Consumption

The estimated total power consumption for this design is 1.46 W. The characterized power consumption for this design at 200 MHz is 1.0164 W.

Figure 1-11 shows the characterized power dissipation numbers for the shift register design using frequencies ranging from 1 MHz to 200 MHz.

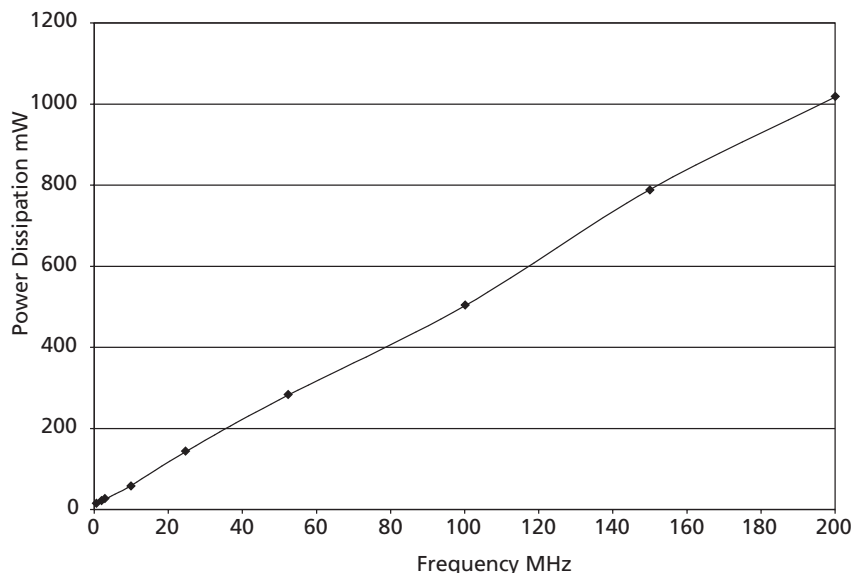


Figure 1-11 • Power Dissipation

Junction Temperature (T_j)

The temperature that you select in Designer Series software is the junction temperature, not ambient temperature. This is an important distinction because the heat generated from dynamic power consumption is usually hotter than the ambient temperature. Use the equation below to calculate junction temperature.

$$\text{Junction Temperature} = \Delta T + T_a$$

EQ 1-13

Where:

T_a = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient

$$\Delta T = \theta_{ja} \times P$$

P = Power calculated from Estimating Power Consumption section

θ_{ja} = Junction to ambient of package. θ_{ja} numbers are located in the "Package Thermal Characteristics" section.

Package Thermal Characteristics

The device junction to case thermal characteristic is θ_{jc} , and the junction to ambient air characteristic is θ_{ja} . The thermal characteristics for θ_{ja} are shown with two different air flow rates.

The maximum junction temperature is 150 °C.

A sample calculation of the absolute maximum power dissipation allowed for a TQFP 176-pin package at commercial temperature and still air is as follows:

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (}^\circ\text{C)} - \text{Max. ambient temp. (}^\circ\text{C)}}{\theta_{ja} \text{ (}^\circ\text{C/W)}} = \frac{150^\circ\text{C} - 70^\circ\text{C}}{28^\circ\text{C/W}} = 2.86 \text{ W}$$

EQ 1-14

Table 1-15 • Package Thermal Characteristics

| Package Type | Pin Count | θ_{jc} | θ_{ja} Still Air | θ_{ja} 300 ft/min. | Units |
|---|-----------|---------------|----------------------------|------------------------------|-------|
| Plastic Leaded Chip Carrier (PLCC) | 84 | 12 | 32 | 22 | °C/W |
| Thin Quad Flat Pack (TQFP) | 144 | 11 | 32 | 24 | °C/W |
| Thin Quad Flat Pack (TQFP) | 176 | 11 | 28 | 21 | °C/W |
| Very Thin Quad Flatpack (VQFP) | 100 | 10 | 38 | 32 | °C/W |
| Plastic Quad Flat Pack (PQFP) without Heat Spreader | 208 | 8 | 30 | 23 | °C/W |
| Plastic Quad Flat Pack (PQFP) with Heat Spreader | 208 | 3.8 | 20 | 17 | °C/W |
| Plastic Ball Grid Array (PBGA) | 272 | 3 | 20 | 14.5 | °C/W |
| Plastic Ball Grid Array (PBGA) | 313 | 3 | 23 | 17 | °C/W |
| Plastic Ball Grid Array (PBGA) | 329 | 3 | 18 | 13.5 | °C/W |
| Fine Pitch Ball Grid Array (FBGA) | 144 | 3.8 | 38.8 | 26.7 | °C/W |

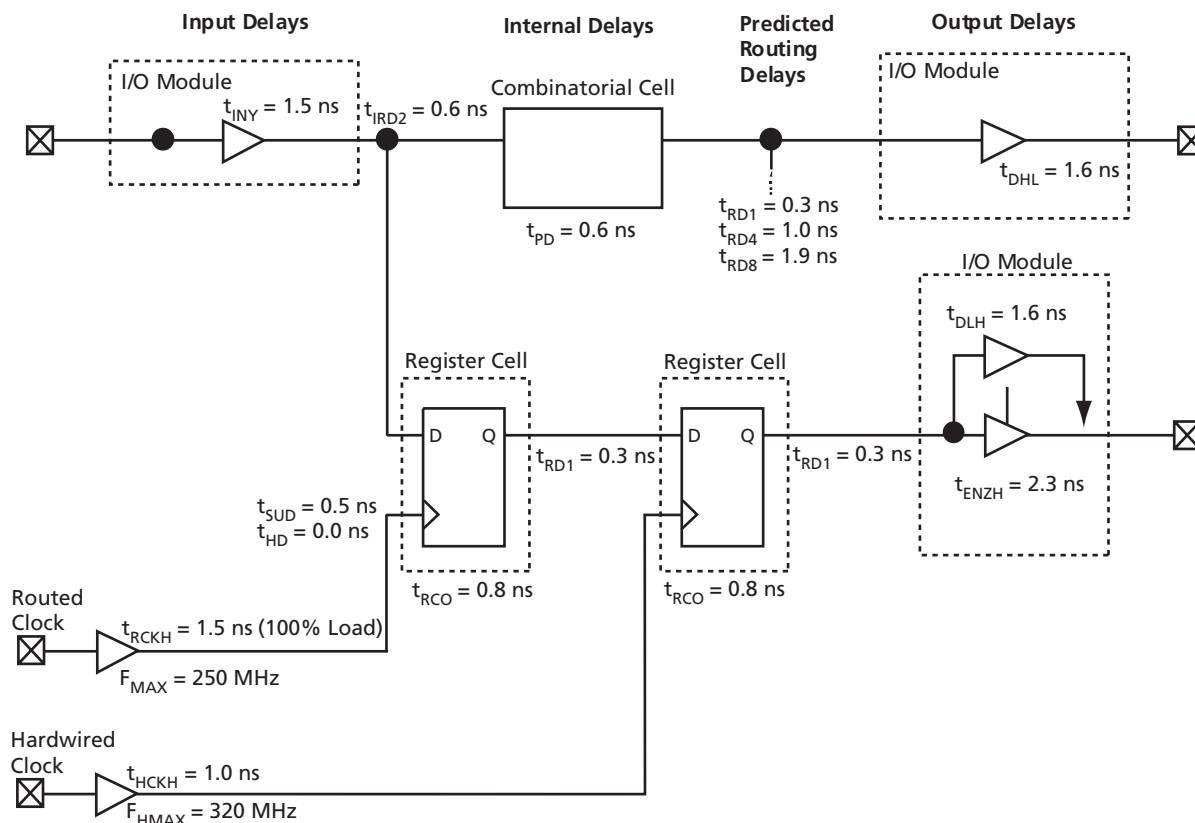
Note: SX08 does not have a heat spreader.

Table 1-16 • Temperature and Voltage Derating Factors*

| V_{CCA} | Junction Temperature | | | | | | |
|-----------|----------------------|------|------|------|------|------|------|
| | -55 | -40 | 0 | 25 | 70 | 85 | 125 |
| 3.0 | 0.75 | 0.78 | 0.87 | 0.89 | 1.00 | 1.04 | 1.16 |
| 3.3 | 0.70 | 0.73 | 0.82 | 0.83 | 0.93 | 0.97 | 1.08 |
| 3.6 | 0.66 | 0.69 | 0.77 | 0.78 | 0.87 | 0.92 | 1.02 |

Note: *Normalized to worst-case commercial, $T_J = 70^\circ\text{C}$, $V_{CCA} = 3.0\text{ V}$

SX Timing Model



Note: Values shown for A54SX08-3, worst-case commercial conditions.

Figure 1-12 • SX Timing Model

Hardwired Clock

$$\begin{aligned} \text{External Setup} &= t_{INY} + t_{IRD1} + t_{SUD} - t_{HCKH} \\ &= 1.5 + 0.3 + 0.5 - 1.0 = 1.3 \text{ ns} \end{aligned}$$

EQ 1-15

Clock-to-Out (Pin-to-Pin)

$$\begin{aligned} &= t_{HCKH} + t_{RCO} + t_{RD1} + t_{DHL} \\ &= 1.0 + 0.8 + 0.3 + 1.6 = 3.7 \text{ ns} \end{aligned}$$

EQ 1-16

Routed Clock

$$\begin{aligned} \text{External Setup} &= t_{INY} + t_{IRD1} + t_{SUD} - t_{RCKH} \\ &= 1.5 + 0.3 + 0.5 - 1.5 = 0.8 \text{ ns} \end{aligned}$$

EQ 1-17

Clock-to-Out (Pin-to-Pin)

$$\begin{aligned} &= t_{RCKH} + t_{RCO} + t_{RD1} + t_{DHL} \\ &= 1.52 + 0.8 + 0.3 + 1.6 = 4.2 \text{ ns} \end{aligned}$$

EQ 1-18

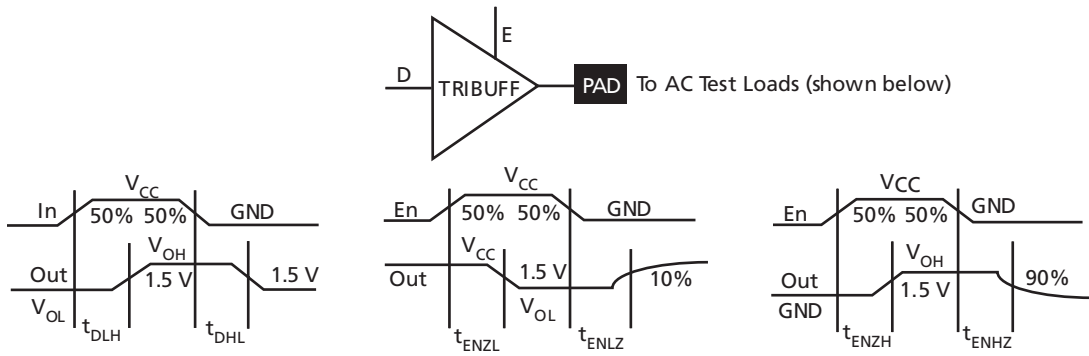


Figure 1-13 • Output Buffer Delays

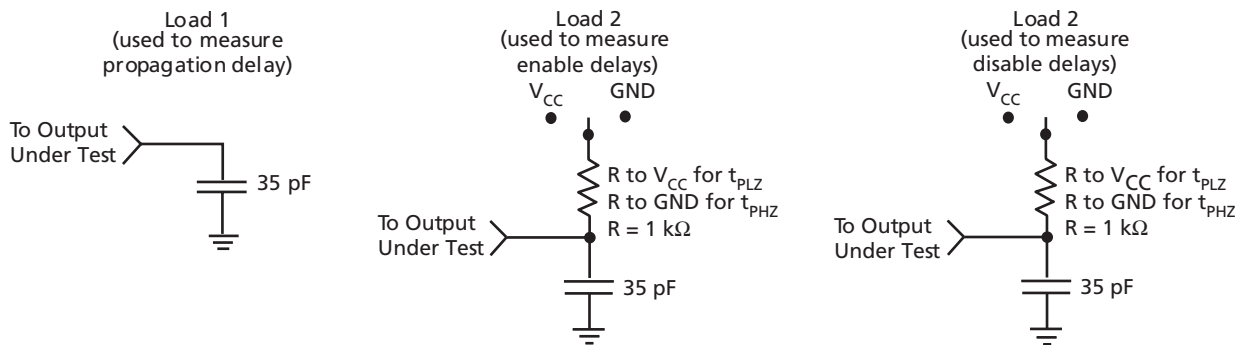


Figure 1-14 • AC Test Loads

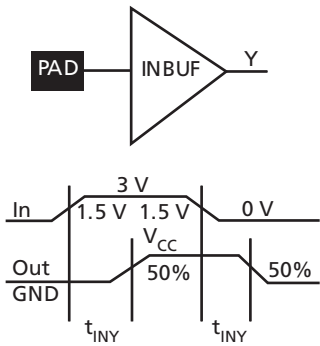


Figure 1-15 • Input Buffer Delays

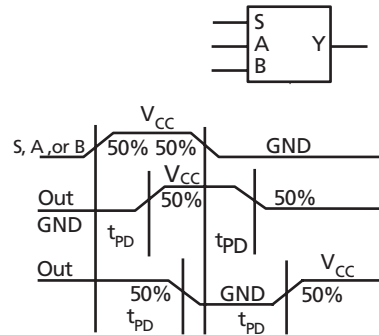


Figure 1-16 • C-Cell Delays

Register Cell Timing Characteristics

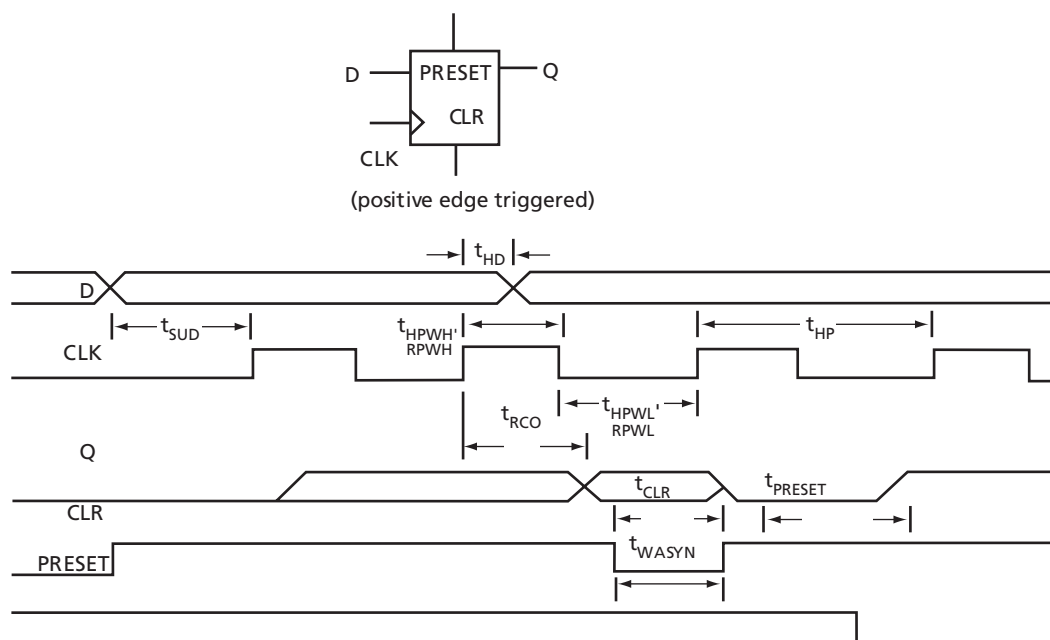


Figure 1-17 • Flip-Flops

Timing Characteristics

Timing characteristics for SX devices fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all SX family members. Internal routing delays are device-dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design is complete. Delay values may then be determined by using the DirectTime Analyzer utility or performing simulation with post-layout delays.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most time-critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to 6% of the nets in a design may be designated as critical, while 90% of the nets in a design are typical.

Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes five antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically up to 6 percent of nets in a fully utilized device require long tracks. Long tracks contribute approximately 4 ns to 8.4 ns delay. This additional delay is represented statistically in higher fanout ($FO = 24$) routing delays in the datasheet specifications section.

Timing Derating

SX devices are manufactured in a CMOS process. Therefore, device performance varies according to temperature, voltage, and process variations. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

A54SX08 Timing Characteristics

Table 1-17 • A54SX08 Timing Characteristics
(Worst-Case Commercial Conditions, $V_{CCR} = 4.75\text{ V}$, $V_{CCA}, V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

| Parameter | Description | '-3' Speed | | '-2' Speed | | '-1' Speed | | 'Std' Speed | | Units |
|--|--------------------------------------|------------|------|------------|------|------------|------|-------------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| C-Cell Propagation Delays¹ | | | | | | | | | | |
| t_{PD} | Internal Array Module | | 0.6 | | 0.7 | | 0.8 | | 0.9 | ns |
| Predicted Routing Delays² | | | | | | | | | | |
| t_{DC} | FO = 1 Routing Delay, Direct Connect | | 0.1 | | 0.1 | | 0.1 | | 0.1 | ns |
| t_{FC} | FO = 1 Routing Delay, Fast Connect | | 0.3 | | 0.4 | | 0.4 | | 0.5 | ns |
| t_{RD1} | FO = 1 Routing Delay | | 0.3 | | 0.4 | | 0.4 | | 0.5 | ns |
| t_{RD2} | FO = 2 Routing Delay | | 0.6 | | 0.7 | | 0.8 | | 0.9 | ns |
| t_{RD3} | FO = 3 Routing Delay | | 0.8 | | 0.9 | | 1.0 | | 1.2 | ns |
| t_{RD4} | FO = 4 Routing Delay | | 1.0 | | 1.2 | | 1.4 | | 1.6 | ns |
| t_{RD8} | FO = 8 Routing Delay | | 1.9 | | 2.2 | | 2.5 | | 2.9 | ns |
| t_{RD12} | FO = 12 Routing Delay | | 2.8 | | 3.2 | | 3.7 | | 4.3 | ns |
| R-Cell Timing | | | | | | | | | | |
| t_{RCO} | Sequential Clock-to-Q | | 0.8 | | 1.1 | | 1.2 | | 1.4 | ns |
| t_{CLR} | Asynchronous Clear-to-Q | | 0.5 | | 0.6 | | 0.7 | | 0.8 | ns |
| t_{PRESET} | Asynchronous Preset-to-Q | | 0.7 | | 0.8 | | 0.9 | | 1.0 | ns |
| t_{SUD} | Flip-Flop Data Input Set-Up | 0.5 | | 0.5 | | 0.7 | | 0.8 | | ns |
| t_{HD} | Flip-Flop Data Input Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| t_{WASYN} | Asynchronous Pulse Width | 1.4 | | 1.6 | | 1.8 | | 2.1 | | ns |
| Input Module Propagation Delays | | | | | | | | | | |
| t_{INYH} | Input Data Pad-to-Y HIGH | | 1.5 | | 1.7 | | 1.9 | | 2.2 | ns |
| t_{INYL} | Input Data Pad-to-Y LOW | | 1.5 | | 1.7 | | 1.9 | | 2.2 | ns |
| Input Module Predicted Routing Delays² | | | | | | | | | | |
| t_{IRD1} | FO = 1 Routing Delay | | 0.3 | | 0.4 | | 0.4 | | 0.5 | ns |
| t_{IRD2} | FO = 2 Routing Delay | | 0.6 | | 0.7 | | 0.8 | | 0.9 | ns |
| t_{IRD3} | FO = 3 Routing Delay | | 0.8 | | 0.9 | | 1.0 | | 1.2 | ns |
| t_{IRD4} | FO = 4 Routing Delay | | 1.0 | | 1.2 | | 1.4 | | 1.6 | ns |
| t_{IRD8} | FO = 8 Routing Delay | | 1.9 | | 2.2 | | 2.5 | | 2.9 | ns |
| t_{IRD12} | FO = 12 Routing Delay | | 2.8 | | 3.2 | | 3.7 | | 4.3 | ns |

Note:

- For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

Table 1-17 • A54SX08 Timing Characteristics (Continued)
 (Worst-Case Commercial Conditions, $V_{CCR} = 4.75\text{ V}$, $V_{CCA}, V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

| Parameter | Description | '-3' Speed | | '-2' Speed | | '-1' Speed | | 'Std' Speed | | Units |
|--|---|------------|------|------------|------|------------|------|-------------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Dedicated (Hardwired) Array Clock Network | | | | | | | | | | |
| t_{HCKH} | Input LOW to HIGH (pad to R-Cell input) | | 1.0 | | 1.1 | | 1.3 | | 1.5 | ns |
| t_{HCKL} | Input HIGH to LOW (pad to R-Cell input) | | 1.0 | | 1.2 | | 1.4 | | 1.6 | ns |
| t_{HPWH} | Minimum Pulse Width HIGH | 1.4 | | 1.6 | | 1.8 | | 2.1 | | ns |
| t_{HPWL} | Minimum Pulse Width LOW | 1.4 | | 1.6 | | 1.8 | | 2.1 | | ns |
| t_{HCKSW} | Maximum Skew | | 0.1 | | 0.2 | | 0.2 | | 0.2 | ns |
| t_{HP} | Minimum Period | 2.7 | | 3.1 | | 3.6 | | 4.2 | | ns |
| f_{HMAX} | Maximum Frequency | | 350 | | 320 | | 280 | | 240 | MHz |
| Routed Array Clock Networks | | | | | | | | | | |
| t_{RCKH} | Input LOW to HIGH (light load) (pad to R-Cell input) | | 1.3 | | 1.5 | | 1.7 | | 2.0 | ns |
| t_{RCKL} | Input HIGH to LOW (light load) (pad to R-Cell Input) | | 1.4 | | 1.6 | | 1.8 | | 2.1 | ns |
| t_{RCKH} | Input LOW to HIGH (50% load) (pad to R-Cell input) | | 1.4 | | 1.7 | | 1.9 | | 2.2 | ns |
| t_{RCKL} | Input HIGH to LOW (50% load) (pad to R-Cell input) | | 1.5 | | 1.7 | | 2.0 | | 2.3 | ns |
| t_{RCKH} | Input LOW to HIGH (100% load) (pad to R-Cell input) | | 1.5 | | 1.7 | | 1.9 | | 2.2 | ns |
| t_{RCKL} | Input HIGH to LOW (100% load) (pad to R-Cell input) | | 1.5 | | 1.8 | | 2.0 | | 2.3 | ns |
| t_{RPWH} | Min. Pulse Width HIGH | 2.1 | | 2.4 | | 2.7 | | 3.2 | | ns |
| t_{RPWL} | Min. Pulse Width LOW | 2.1 | | 2.4 | | 2.7 | | 3.2 | | ns |
| t_{RCKSW} | Maximum Skew (light load) | | 0.1 | | 0.2 | | 0.2 | | 0.2 | ns |
| t_{RCKSW} | Maximum Skew (50% load) | | 0.3 | | 0.3 | | 0.4 | | 0.4 | ns |
| t_{RCKSW} | Maximum Skew (100% load) | | 0.3 | | 0.3 | | 0.4 | | 0.4 | ns |
| TTL Output Module Timing¹ | | | | | | | | | | |
| t_{DLH} | Data-to-Pad LOW to HIGH | | 1.6 | | 1.9 | | 2.1 | | 2.5 | ns |
| t_{DHL} | Data-to-Pad HIGH to LOW | | 1.6 | | 1.9 | | 2.1 | | 2.5 | ns |
| t_{ENZL} | Enable-to-Pad, Z to L | | 2.1 | | 2.4 | | 2.8 | | 3.2 | ns |
| t_{ENZH} | Enable-to-Pad, Z to H | | 2.3 | | 2.7 | | 3.1 | | 3.6 | ns |
| t_{ENLZ} | Enable-to-Pad, L to Z | | 1.4 | | 1.7 | | 1.9 | | 2.2 | ns |

Note:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A54SX16 Timing Characteristics

Table 1-18 • A54SX16 Timing Characteristics
(Worst-Case Commercial Conditions, $V_{CCR} = 4.75\text{ V}$, $V_{CCA}, V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

| Parameter | Description | '-3' Speed | | '-2' Speed | | '-1' Speed | | 'Std' Speed | | Units |
|---|--------------------------------------|------------|------|------------|------|------------|------|-------------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| C-Cell Propagation Delays¹ | | | | | | | | | | |
| t_{PD} | Internal Array Module | | 0.6 | | 0.7 | | 0.8 | | 0.9 | ns |
| Predicted Routing Delays² | | | | | | | | | | |
| t_{DC} | FO = 1 Routing Delay, Direct Connect | | 0.1 | | 0.1 | | 0.1 | | 0.1 | ns |
| t_{FC} | FO = 1 Routing Delay, Fast Connect | | 0.3 | | 0.4 | | 0.4 | | 0.5 | ns |
| t_{RD1} | FO = 1 Routing Delay | | 0.3 | | 0.4 | | 0.4 | | 0.5 | ns |
| t_{RD2} | FO = 2 Routing Delay | | 0.6 | | 0.7 | | 0.8 | | 0.9 | ns |
| t_{RD3} | FO = 3 Routing Delay | | 0.8 | | 0.9 | | 1.0 | | 1.2 | ns |
| t_{RD4} | FO = 4 Routing Delay | | 1.0 | | 1.2 | | 1.4 | | 1.6 | ns |
| t_{RD8} | FO = 8 Routing Delay | | 1.9 | | 2.2 | | 2.5 | | 2.9 | ns |
| t_{RD12} | FO = 12 Routing Delay | | 2.8 | | 3.2 | | 3.7 | | 4.3 | ns |
| R-Cell Timing | | | | | | | | | | |
| t_{RCO} | Sequential Clock-to-Q | | 0.8 | | 1.1 | | 1.2 | | 1.4 | ns |
| t_{CLR} | Asynchronous Clear-to-Q | | 0.5 | | 0.6 | | 0.7 | | 0.8 | ns |
| t_{PRESET} | Asynchronous Preset-to-Q | | 0.7 | | 0.8 | | 0.9 | | 1.0 | ns |
| t_{SUD} | Flip-Flop Data Input Set-Up | 0.5 | | 0.5 | | 0.7 | | 0.8 | | ns |
| t_{HD} | Flip-Flop Data Input Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| t_{WASYN} | Asynchronous Pulse Width | 1.4 | | 1.6 | | 1.8 | | 2.1 | | ns |
| Input Module Propagation Delays | | | | | | | | | | |
| t_{INYH} | Input Data Pad-to-Y HIGH | | 1.5 | | 1.7 | | 1.9 | | 2.2 | ns |
| t_{INYL} | Input Data Pad-to-Y LOW | | 1.5 | | 1.7 | | 1.9 | | 2.2 | ns |
| Predicted Input Routing Delays² | | | | | | | | | | |
| t_{IRD1} | FO = 1 Routing Delay | | 0.3 | | 0.4 | | 0.4 | | 0.5 | ns |
| t_{IRD2} | FO = 2 Routing Delay | | 0.6 | | 0.7 | | 0.8 | | 0.9 | ns |
| t_{IRD3} | FO = 3 Routing Delay | | 0.8 | | 0.9 | | 1.0 | | 1.2 | ns |
| t_{IRD4} | FO = 4 Routing Delay | | 1.0 | | 1.2 | | 1.4 | | 1.6 | ns |
| t_{IRD8} | FO = 8 Routing Delay | | 1.9 | | 2.2 | | 2.5 | | 2.9 | ns |
| t_{IRD12} | FO = 12 Routing Delay | | 2.8 | | 3.2 | | 3.7 | | 4.3 | ns |

Notes:

- For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
- Delays based on 35 pF loading, except t_{ENZL} and t_{ENZH} . For t_{ENZL} and t_{ENZH} , the loading is 5 pF.

Table 1-18 • A54SX16 Timing Characteristics (Continued)
 (Worst-Case Commercial Conditions, $V_{CCR} = 4.75\text{ V}$, $V_{CCA}, V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

| Parameter | Description | '-3' Speed | | '-2' Speed | | '-1' Speed | | 'Std' Speed | | Units |
|--|---|------------|------|------------|------|------------|------|-------------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Dedicated (Hardwired) Array Clock Network | | | | | | | | | | |
| t_{HCKH} | Input LOW to HIGH (pad to R-Cell input) | | 1.2 | | 1.4 | | 1.5 | | 1.8 | ns |
| t_{HCKL} | Input HIGH to LOW (pad to R-Cell input) | | 1.2 | | 1.4 | | 1.6 | | 1.9 | ns |
| t_{HPWH} | Minimum Pulse Width HIGH | 1.4 | | 1.6 | | 1.8 | | 2.1 | | ns |
| t_{HPWL} | Minimum Pulse Width LOW | 1.4 | | 1.6 | | 1.8 | | 2.1 | | ns |
| t_{HCKSW} | Maximum Skew | | 0.2 | | 0.2 | | 0.3 | | 0.3 | ns |
| t_{HP} | Minimum Period | 2.7 | | 3.1 | | 3.6 | | 4.2 | | ns |
| f_{HMAX} | Maximum Frequency | | 350 | | 320 | | 280 | | 240 | MHz |
| Routed Array Clock Networks | | | | | | | | | | |
| t_{RCKH} | Input LOW to HIGH (light load) (pad to R-Cell input) | | 1.6 | | 1.8 | | 2.1 | | 2.5 | ns |
| t_{RCKL} | Input HIGH to LOW (light load) (pad to R-Cell input) | | 1.8 | | 2.0 | | 2.3 | | 2.7 | ns |
| t_{RCKH} | Input LOW to HIGH (50% load) (pad to R-Cell input) | | 1.8 | | 2.1 | | 2.5 | | 2.8 | ns |
| t_{RCKL} | Input HIGH to LOW (50% load) (pad to R-Cell input) | | 2.0 | | 2.2 | | 2.5 | | 3.0 | ns |
| t_{RCKH} | Input LOW to HIGH (100% load) (pad to R-Cell input) | | 1.8 | | 2.1 | | 2.4 | | 2.8 | ns |
| t_{RCKL} | Input HIGH to LOW (100% load) (pad to R-Cell input) | | 2.0 | | 2.2 | | 2.5 | | 3.0 | ns |
| t_{RPWH} | Min. Pulse Width HIGH | 2.1 | | 2.4 | | 2.7 | | 3.2 | | ns |
| t_{RPWL} | Min. Pulse Width LOW | 2.1 | | 2.4 | | 2.7 | | 3.2 | | ns |
| t_{RCKSW} | Maximum Skew (light load) | | 0.5 | | 0.5 | | 0.5 | | 0.7 | ns |
| t_{RCKSW} | Maximum Skew (50% load) | | 0.5 | | 0.6 | | 0.7 | | 0.8 | ns |
| t_{RCKSW} | Maximum Skew (100% load) | | 0.5 | | 0.6 | | 0.7 | | 0.8 | ns |
| TTL Output Module Timing³ | | | | | | | | | | |
| t_{DLH} | Data-to-Pad LOW to HIGH | | 1.6 | | 1.9 | | 2.1 | | 2.5 | ns |
| t_{DHL} | Data-to-Pad HIGH to LOW | | 1.6 | | 1.9 | | 2.1 | | 2.5 | ns |
| t_{ENZL} | Enable-to-Pad, Z to L | | 2.1 | | 2.4 | | 2.8 | | 3.2 | ns |
| t_{ENZH} | Enable-to-Pad, Z to H | | 2.3 | | 2.7 | | 3.1 | | 3.6 | ns |
| t_{ENLZ} | Enable-to-Pad, L to Z | | 1.4 | | 1.7 | | 1.9 | | 2.2 | ns |
| t_{ENHZ} | Enable-to-Pad, H to Z | | 1.3 | | 1.5 | | 1.7 | | 2.0 | ns |

Notes:

- For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
- Delays based on 35 pF loading, except t_{ENZL} and t_{ENZH} . For t_{ENZL} and t_{ENZH} , the loading is 5 pF.

A54SX16P Timing Characteristics

Table 1-19 • A54SX16P Timing Characteristics
(Worst-Case Commercial Conditions, $V_{CCR} = 4.75\text{ V}$, $V_{CCA}, V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

| Parameter | Description | '-3' Speed | | '-2' Speed | | '-1' Speed | | 'Std' Speed | | Units |
|---|--------------------------------------|------------|------|------------|------|------------|------|-------------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| C-Cell Propagation Delays¹ | | | | | | | | | | |
| t_{PD} | Internal Array Module | | 0.6 | | 0.7 | | 0.8 | | 0.9 | ns |
| Predicted Routing Delays² | | | | | | | | | | |
| t_{DC} | FO = 1 Routing Delay, Direct Connect | | 0.1 | | 0.1 | | 0.1 | | 0.1 | ns |
| t_{FC} | FO = 1 Routing Delay, Fast Connect | | 0.3 | | 0.4 | | 0.4 | | 0.5 | ns |
| t_{RD1} | FO = 1 Routing Delay | | 0.3 | | 0.4 | | 0.4 | | 0.5 | ns |
| t_{RD2} | FO = 2 Routing Delay | | 0.6 | | 0.7 | | 0.8 | | 0.9 | ns |
| t_{RD3} | FO = 3 Routing Delay | | 0.8 | | 0.9 | | 1.0 | | 1.2 | ns |
| t_{RD4} | FO = 4 Routing Delay | | 1.0 | | 1.2 | | 1.4 | | 1.6 | ns |
| t_{RD8} | FO = 8 Routing Delay | | 1.9 | | 2.2 | | 2.5 | | 2.9 | ns |
| t_{RD12} | FO = 12 Routing Delay | | 2.8 | | 3.2 | | 3.7 | | 4.3 | ns |
| R-Cell Timing | | | | | | | | | | |
| t_{RCO} | Sequential Clock-to-Q | | 0.9 | | 1.1 | | 1.3 | | 1.4 | ns |
| t_{CLR} | Asynchronous Clear-to-Q | | 0.5 | | 0.6 | | 0.7 | | 0.8 | ns |
| t_{PRESET} | Asynchronous Preset-to-Q | | 0.7 | | 0.8 | | 0.9 | | 1.0 | ns |
| t_{SUD} | Flip-Flop Data Input Set-Up | 0.5 | | 0.5 | | 0.7 | | 0.8 | | ns |
| t_{HD} | Flip-Flop Data Input Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| t_{WASYN} | Asynchronous Pulse Width | 1.4 | | 1.6 | | 1.8 | | 2.1 | | ns |
| Input Module Propagation Delays | | | | | | | | | | |
| t_{INYH} | Input Data Pad-to-Y HIGH | | 1.5 | | 1.7 | | 1.9 | | 2.2 | ns |
| t_{INYL} | Input Data Pad-to-Y LOW | | 1.5 | | 1.7 | | 1.9 | | 2.2 | ns |
| Predicted Input Routing Delays² | | | | | | | | | | |
| t_{IRD1} | FO = 1 Routing Delay | | 0.3 | | 0.4 | | 0.4 | | 0.5 | ns |
| t_{IRD2} | FO = 2 Routing Delay | | 0.6 | | 0.7 | | 0.8 | | 0.9 | ns |
| t_{IRD3} | FO = 3 Routing Delay | | 0.8 | | 0.9 | | 1.0 | | 1.2 | ns |
| t_{IRD4} | FO = 4 Routing Delay | | 1.0 | | 1.2 | | 1.4 | | 1.6 | ns |
| t_{IRD8} | FO = 8 Routing Delay | | 1.9 | | 2.2 | | 2.5 | | 2.9 | ns |
| t_{IRD12} | FO = 12 Routing Delay | | 2.8 | | 3.2 | | 3.7 | | 4.3 | ns |

Note:

- For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
- Delays based on 10 pF loading.

Table 1-19 • A54SX16P Timing Characteristics (Continued)
 (Worst-Case Commercial Conditions, $V_{CCR} = 4.75\text{ V}$, $V_{CCA}, V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

| Parameter | Description | '-3' Speed | | '-2' Speed | | '-1' Speed | | 'Std' Speed | | Units |
|--|---|------------|------|------------|------|------------|------|-------------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Dedicated (Hardwired) Array Clock Network | | | | | | | | | | |
| t_{HCKH} | Input LOW to HIGH (pad to R-Cell input) | | 1.2 | | 1.4 | | 1.5 | | 1.8 | ns |
| t_{HCKL} | Input HIGH to LOW (pad to R-Cell input) | | 1.2 | | 1.4 | | 1.6 | | 1.9 | ns |
| t_{HPWH} | Minimum Pulse Width HIGH | 1.4 | | 1.6 | | 1.8 | | 2.1 | | ns |
| t_{HPWL} | Minimum Pulse Width LOW | 1.4 | | 1.6 | | 1.8 | | 2.1 | | ns |
| t_{HCKSW} | Maximum Skew | | 0.2 | | 0.2 | | 0.3 | | 0.3 | ns |
| t_{HP} | Minimum Period | 2.7 | | 3.1 | | 3.6 | | 4.2 | | ns |
| f_{HMAX} | Maximum Frequency | | 350 | | 320 | | 280 | | 240 | MHz |
| Routed Array Clock Networks | | | | | | | | | | |
| t_{RCKH} | Input LOW to HIGH (light load) (pad to R-Cell input) | | 1.6 | | 1.8 | | 2.1 | | 2.5 | ns |
| t_{RCKL} | Input HIGH to LOW (Light Load) (pad to R-Cell input) | | 1.8 | | 2.0 | | 2.3 | | 2.7 | ns |
| t_{RCKH} | Input LOW to HIGH (50% load) (pad to R-Cell input) | | 1.8 | | 2.1 | | 2.5 | | 2.8 | ns |
| t_{RCKL} | Input HIGH to LOW (50% load) (pad to R-Cell input) | | 2.0 | | 2.2 | | 2.5 | | 3.0 | ns |
| t_{RCKH} | Input LOW to HIGH (100% load) (pad to R-Cell input) | | 1.8 | | 2.1 | | 2.4 | | 2.8 | ns |
| t_{RCKL} | Input HIGH to LOW (100% load) (pad to R-Cell input) | | 2.0 | | 2.2 | | 2.5 | | 3.0 | ns |
| t_{RPWH} | Min. Pulse Width HIGH | 2.1 | | 2.4 | | 2.7 | | 3.2 | | ns |
| t_{RPWL} | Min. Pulse Width LOW | 2.1 | | 2.4 | | 2.7 | | 3.2 | | ns |
| t_{RCKSW} | Maximum Skew (light load) | | 0.5 | | 0.5 | | 0.5 | | 0.7 | ns |
| t_{RCKSW} | Maximum Skew (50% load) | | 0.5 | | 0.6 | | 0.7 | | 0.8 | ns |
| t_{RCKSW} | Maximum Skew (100% load) | | 0.5 | | 0.6 | | 0.7 | | 0.8 | ns |
| TTL Output Module Timing | | | | | | | | | | |
| t_{DLH} | Data-to-Pad LOW to HIGH | | 2.4 | | 2.8 | | 3.1 | | 3.7 | ns |
| t_{DHL} | Data-to-Pad HIGH to LOW | | 2.3 | | 2.9 | | 3.2 | | 3.8 | ns |
| t_{ENZL} | Enable-to-Pad, Z to L | | 3.0 | | 3.4 | | 3.9 | | 4.6 | ns |
| t_{ENZH} | Enable-to-Pad, Z to H | | 3.3 | | 3.8 | | 4.3 | | 5.0 | ns |
| t_{ENLZ} | Enable-to-Pad, L to Z | | 2.3 | | 2.7 | | 3.0 | | 3.5 | ns |
| t_{ENHZ} | Enable-to-Pad, H to Z | | 2.8 | | 3.2 | | 3.7 | | 4.3 | ns |

Note:

- For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
- Delays based on 10 pF loading.

Table 1-19 • A54SX16P Timing Characteristics (Continued)
 (Worst-Case Commercial Conditions, $V_{CCR} = 4.75\text{ V}$, $V_{CCA}, V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

| Parameter | Description | '-3' Speed | | '-2' Speed | | '-1' Speed | | 'Std' Speed | | Units |
|---|-------------------------|------------|------|------------|------|------------|------|-------------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| TTL/PCI Output Module Timing | | | | | | | | | | |
| t_{DLH} | Data-to-Pad LOW to HIGH | | 1.5 | | 1.7 | | 2.0 | | 2.3 | ns |
| t_{DHL} | Data-to-Pad HIGH to LOW | | 1.9 | | 2.2 | | 2.4 | | 2.9 | ns |
| t_{ENZL} | Enable-to-Pad, Z to L | | 2.3 | | 2.6 | | 3.0 | | 3.5 | ns |
| t_{ENZH} | Enable-to-Pad, Z to H | | 1.5 | | 1.7 | | 1.9 | | 2.3 | ns |
| t_{ENLZ} | Enable-to-Pad, L to Z | | 2.7 | | 3.1 | | 3.5 | | 4.1 | ns |
| t_{ENHZ} | Enable-to-Pad, H to Z | | 2.9 | | 3.3 | | 3.7 | | 4.4 | ns |
| PCI Output Module Timing³ | | | | | | | | | | |
| t_{DLH} | Data-to-Pad LOW to HIGH | | 1.8 | | 2.0 | | 2.3 | | 2.7 | ns |
| t_{DHL} | Data-to-Pad HIGH to LOW | | 1.7 | | 2.0 | | 2.2 | | 2.6 | ns |
| t_{ENZL} | Enable-to-Pad, Z to L | | 0.8 | | 1.0 | | 1.1 | | 1.3 | ns |
| t_{ENZH} | Enable-to-Pad, Z to H | | 1.2 | | 1.2 | | 1.5 | | 1.8 | ns |
| t_{ENLZ} | Enable-to-Pad, L to Z | | 1.0 | | 1.1 | | 1.3 | | 1.5 | ns |
| t_{ENHZ} | Enable-to-Pad, H to Z | | 1.1 | | 1.3 | | 1.5 | | 1.7 | ns |
| TTL Output Module Timing | | | | | | | | | | |
| t_{DLH} | Data-to-Pad LOW to HIGH | | 2.1 | | 2.5 | | 2.8 | | 3.3 | ns |
| t_{DHL} | Data-to-Pad HIGH to LOW | | 2.0 | | 2.3 | | 2.6 | | 3.1 | ns |
| t_{ENZL} | Enable-to-Pad, Z to L | | 2.5 | | 2.9 | | 3.2 | | 3.8 | ns |
| t_{ENZH} | Enable-to-Pad, Z to H | | 3.0 | | 3.5 | | 3.9 | | 4.6 | ns |
| t_{ENLZ} | Enable-to-Pad, L to Z | | 2.3 | | 2.7 | | 3.1 | | 3.6 | ns |
| t_{ENHZ} | Enable-to-Pad, H to Z | | 2.9 | | 3.3 | | 3.7 | | 4.4 | ns |

Note:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
3. Delays based on 10 pF loading.

A54SX32 Timing Characteristics

Table 1-20 • A54SX32 Timing Characteristics
(Worst-Case Commercial Conditions, $V_{CCR} = 4.75\text{ V}$, $V_{CCA}, V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

| Parameter | Description | '-3' Speed | | '-2' Speed | | '-1' Speed | | 'Std' Speed | | Units |
|---|--------------------------------------|------------|------|------------|------|------------|------|-------------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| C-Cell Propagation Delays¹ | | | | | | | | | | |
| t_{PD} | Internal Array Module | | 0.6 | | 0.7 | | 0.8 | | 0.9 | ns |
| Predicted Routing Delays² | | | | | | | | | | |
| t_{DC} | FO = 1 Routing Delay, Direct Connect | | 0.1 | | 0.1 | | 0.1 | | 0.1 | ns |
| t_{FC} | FO = 1 Routing Delay, Fast Connect | | 0.3 | | 0.4 | | 0.4 | | 0.5 | ns |
| t_{RD1} | FO = 1 Routing Delay | | 0.3 | | 0.4 | | 0.4 | | 0.5 | ns |
| t_{RD2} | FO = 2 Routing Delay | | 0.7 | | 0.8 | | 0.9 | | 1.0 | ns |
| t_{RD3} | FO = 3 Routing Delay | | 1.0 | | 1.2 | | 1.4 | | 1.6 | ns |
| t_{RD4} | FO = 4 Routing Delay | | 1.4 | | 1.6 | | 1.8 | | 2.1 | ns |
| t_{RD8} | FO = 8 Routing Delay | | 2.7 | | 3.1 | | 3.5 | | 4.1 | ns |
| t_{RD12} | FO = 12 Routing Delay | | 4.0 | | 4.7 | | 5.3 | | 6.2 | ns |
| R-Cell Timing | | | | | | | | | | |
| t_{RCO} | Sequential Clock-to-Q | | 0.8 | | 1.1 | | 1.3 | | 1.4 | ns |
| t_{CLR} | Asynchronous Clear-to-Q | | 0.5 | | 0.6 | | 0.7 | | 0.8 | ns |
| t_{PRESET} | Asynchronous Preset-to-Q | | 0.7 | | 0.8 | | 0.9 | | 1.0 | ns |
| t_{SUD} | Flip-Flop Data Input Set-Up | 0.5 | | 0.6 | | 0.7 | | 0.8 | | ns |
| t_{HD} | Flip-Flop Data Input Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| t_{WASYN} | Asynchronous Pulse Width | 1.4 | | 1.6 | | 1.8 | | 2.1 | | ns |
| Input Module Propagation Delays | | | | | | | | | | |
| t_{INYH} | Input Data Pad-to-Y HIGH | | 1.5 | | 1.7 | | 1.9 | | 2.2 | ns |
| t_{INYL} | Input Data Pad-to-Y LOW | | 1.5 | | 1.7 | | 1.9 | | 2.2 | ns |
| Predicted Input Routing Delays² | | | | | | | | | | |
| t_{IRD1} | FO = 1 Routing Delay | | 0.3 | | 0.4 | | 0.4 | | 0.5 | ns |
| t_{IRD2} | FO = 2 Routing Delay | | 0.7 | | 0.8 | | 0.9 | | 1.0 | ns |
| t_{IRD3} | FO = 3 Routing Delay | | 1.0 | | 1.2 | | 1.4 | | 1.6 | ns |
| t_{IRD4} | FO = 4 Routing Delay | | 1.4 | | 1.6 | | 1.8 | | 2.1 | ns |
| t_{IRD8} | FO = 8 Routing Delay | | 2.7 | | 3.1 | | 3.5 | | 4.1 | ns |
| t_{IRD12} | FO = 12 Routing Delay | | 4.0 | | 4.7 | | 5.3 | | 6.2 | ns |

Note:

- For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
- Delays based on 35 pF loading, except t_{ENZL} and t_{ENZH} . For t_{ENZL} and t_{ENZH} the loading is 5 pF.

Table 1-20 • A54SX32 Timing Characteristics (Continued)
 (Worst-Case Commercial Conditions, $V_{CCR} = 4.75\text{ V}$, $V_{CCA}, V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

| Parameter | Description | '-3' Speed | | '-2' Speed | | '-1' Speed | | 'Std' Speed | | Units |
|--|---|------------|------|------------|------|------------|------|-------------|------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Dedicated (Hardwired) Array Clock Network | | | | | | | | | | |
| t_{HCKH} | Input LOW to HIGH (pad to R-Cell input) | | 1.9 | | 2.1 | | 2.4 | | 2.8 | ns |
| t_{HCKL} | Input HIGH to LOW (pad to R-Cell input) | | 1.9 | | 2.1 | | 2.4 | | 2.8 | ns |
| t_{HPWH} | Minimum Pulse Width HIGH | 1.4 | | 1.6 | | 1.8 | | 2.1 | | ns |
| t_{HPWL} | Minimum Pulse Width LOW | 1.4 | | 1.6 | | 1.8 | | 2.1 | | ns |
| t_{HCKSW} | Maximum Skew | | 0.3 | | 0.4 | | 0.4 | | 0.5 | ns |
| t_{HP} | Minimum Period | 2.7 | | 3.1 | | 3.6 | | 4.2 | | ns |
| f_{HMAX} | Maximum Frequency | | 350 | | 320 | | 280 | | 240 | MHz |
| Routed Array Clock Networks | | | | | | | | | | |
| t_{RCKH} | Input LOW to HIGH (light load) (pad to R-Cell input) | | 2.4 | | 2.7 | | 3.0 | | 3.5 | ns |
| t_{RCKL} | Input HIGH to LOW (light load) (pad to R-Cell input) | | 2.4 | | 2.7 | | 3.1 | | 3.6 | ns |
| t_{RCKH} | Input LOW to HIGH (50% load) (pad to R-Cell input) | | 2.7 | | 3.0 | | 3.5 | | 4.1 | ns |
| t_{RCKL} | Input HIGH to LOW (50% load) (pad to R-Cell input) | | 2.7 | | 3.1 | | 3.6 | | 4.2 | ns |
| t_{RCKH} | Input LOW to HIGH (100% load) (pad to R-Cell input) | | 2.7 | | 3.1 | | 3.5 | | 4.1 | ns |
| t_{RCKL} | Input HIGH to LOW (100% load) (pad to R-Cell input) | | 2.8 | | 3.2 | | 3.6 | | 4.3 | ns |
| t_{RPWH} | Min. Pulse Width HIGH | 2.1 | | 2.4 | | 2.7 | | 3.2 | | ns |
| t_{RPWL} | Min. Pulse Width LOW | 2.1 | | 2.4 | | 2.7 | | 3.2 | | ns |
| t_{RCKSW} | Maximum Skew (light load) | | 0.85 | | 0.98 | | 1.1 | | 1.3 | ns |
| t_{RCKSW} | Maximum Skew (50% load) | | 1.23 | | 1.4 | | 1.6 | | 1.9 | ns |
| t_{RCKSW} | Maximum Skew (100% load) | | 1.30 | | 1.5 | | 1.7 | | 2.0 | ns |
| TTL Output Module Timing³ | | | | | | | | | | |
| t_{DLH} | Data-to-Pad LOW to HIGH | | 1.6 | | 1.9 | | 2.1 | | 2.5 | ns |
| t_{DHL} | Data-to-Pad HIGH to LOW | | 1.6 | | 1.9 | | 2.1 | | 2.5 | ns |
| t_{ENZL} | Enable-to-Pad, Z to L | | 2.1 | | 2.4 | | 2.8 | | 3.2 | ns |
| t_{ENZH} | Enable-to-Pad, Z to H | | 2.3 | | 2.7 | | 3.1 | | 3.6 | ns |
| t_{ENLZ} | Enable-to-Pad, L to Z | | 1.4 | | 1.7 | | 1.9 | | 2.2 | ns |
| t_{ENHZ} | Enable-to-Pad, H to Z | | 1.3 | | 1.5 | | 1.7 | | 2.0 | ns |

Note:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
3. Delays based on 35 pF loading, except t_{ENZL} and t_{ENZH} . For t_{ENZL} and t_{ENZH} the loading is 5 pF.

Pin Description

CLKA/B Clock A and B

These pins are 3.3 V / 5.0 V PCI/TTL clock inputs for clock distribution networks. The clock input is buffered prior to clocking the R-cells. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating. (For A54SX72A, these clocks can be configured as bidirectional.)

GND Ground

LOW supply voltage.

HCLK Dedicated (hardwired) Array Clock

This pin is the 3.3 V / 5.0 V PCI/TTL clock input for sequential modules. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating.

I/O Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Based on certain configurations, input and output levels are compatible with standard TTL, LVTTTL, 3.3 V PCI or 5.0 V PCI specifications. Unused I/O pins are automatically tristated by the Designer Series software.

NC No Connection

This pin is not connected to circuitry within the device.

PRA, I/O Probe A

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

PRB, I/O Probe B

The Probe B pin is used to output data from any node within the device. This diagnostic pin can be used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

TCK Test Clock

Test clock input for diagnostic probe and device programming. In flexible mode, TCK becomes active when the TMS pin is set LOW (refer to [Table 1-2 on page 1-6](#)). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDI Test Data Input

Serial input for boundary scan testing and diagnostic probe. In flexible mode, TDI is active when the TMS pin is set LOW (refer to [Table 1-2 on page 1-6](#)). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDO Test Data Output

Serial output for boundary scan testing. In flexible mode, TDO is active when the TMS pin is set LOW (refer to [Table 1-2 on page 1-6](#)). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TMS Test Mode Select

The TMS pin controls the use of the IEEE 1149.1 Boundary Scan pins (TCK, TDI, TDO). In flexible mode when the TMS pin is set LOW, the TCK, TDI, and TDO pins are boundary scan pins (refer to [Table 1-2 on page 1-6](#)). Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the "logic reset" state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The "logic reset" state is reached 5 TCK cycles after the TMS pin is set HIGH. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications.

V_{CCI} Supply Voltage

Supply voltage for I/Os. See [Table 1-1 on page 1-5](#).

V_{CCA} Supply Voltage

Supply voltage for Array. See [Table 1-1 on page 1-5](#).

V_{CCR} Supply Voltage

Supply voltage for input tolerance (required for internal biasing). See [Table 1-1 on page 1-5](#).

Package Pin Assignments

84-Pin PLCC

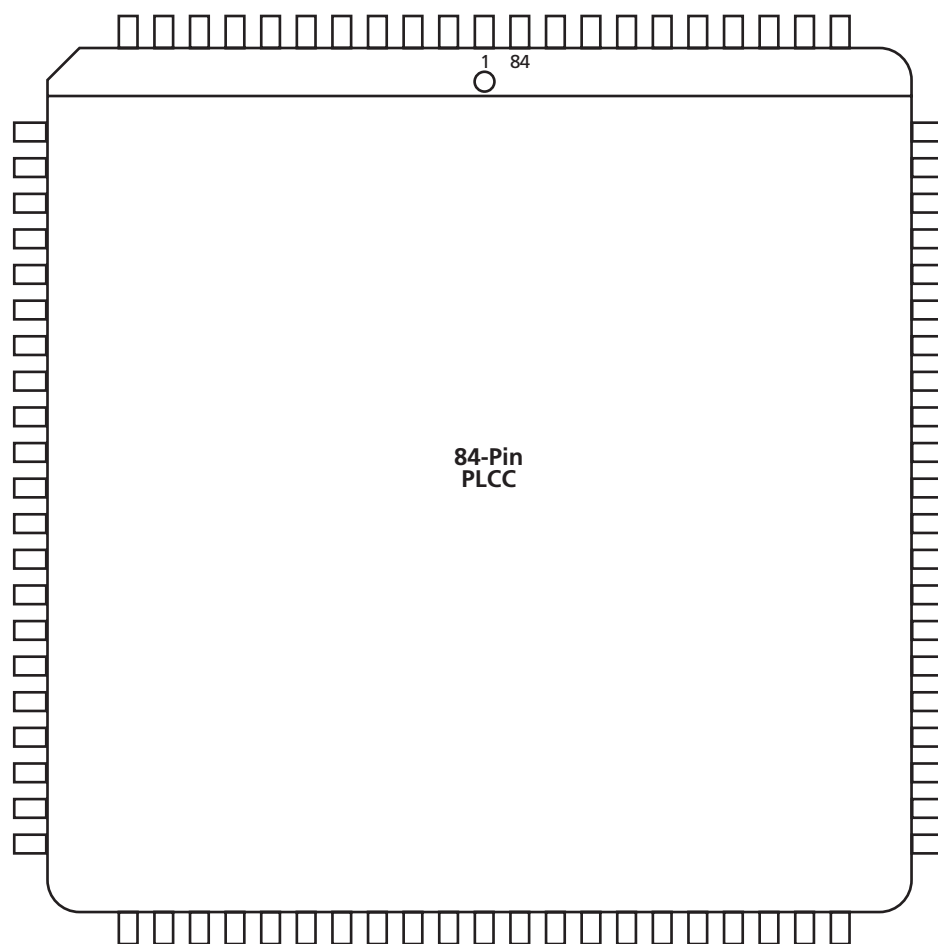


Figure 2-1 • 84-Pin PLCC (Top View)

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

| 84-Pin PLCC | |
|-------------|------------------|
| Pin Number | A54SX08 Function |
| 1 | V _{CCR} |
| 2 | GND |
| 3 | V _{CCA} |
| 4 | PRA, I/O |
| 5 | I/O |
| 6 | I/O |
| 7 | V _{CCI} |
| 8 | I/O |
| 9 | I/O |
| 10 | I/O |
| 11 | TCK, I/O |
| 12 | TDI, I/O |
| 13 | I/O |
| 14 | I/O |
| 15 | I/O |
| 16 | TMS |
| 17 | I/O |
| 18 | I/O |
| 19 | I/O |
| 20 | I/O |
| 21 | I/O |
| 22 | I/O |
| 23 | I/O |
| 24 | I/O |
| 25 | I/O |
| 26 | I/O |
| 27 | GND |
| 28 | V _{CCI} |
| 29 | I/O |
| 30 | I/O |
| 31 | I/O |
| 32 | I/O |
| 33 | I/O |
| 34 | I/O |
| 35 | I/O |

| 84-Pin PLCC | |
|-------------|------------------|
| Pin Number | A54SX08 Function |
| 36 | I/O |
| 37 | I/O |
| 38 | I/O |
| 39 | I/O |
| 40 | PRB, I/O |
| 41 | V _{CCA} |
| 42 | GND |
| 43 | V _{CCR} |
| 44 | I/O |
| 45 | HCLK |
| 46 | I/O |
| 47 | I/O |
| 48 | I/O |
| 49 | I/O |
| 50 | I/O |
| 51 | I/O |
| 52 | TDO, I/O |
| 53 | I/O |
| 54 | I/O |
| 55 | I/O |
| 56 | I/O |
| 57 | I/O |
| 58 | I/O |
| 59 | V _{CCA} |
| 60 | V _{CCI} |
| 61 | GND |
| 62 | I/O |
| 63 | I/O |
| 64 | I/O |
| 65 | I/O |
| 66 | I/O |
| 67 | I/O |
| 68 | V _{CCA} |
| 69 | GND |
| 70 | I/O |

| 84-Pin PLCC | |
|-------------|------------------|
| Pin Number | A54SX08 Function |
| 71 | I/O |
| 72 | I/O |
| 73 | I/O |
| 74 | I/O |
| 75 | I/O |
| 76 | I/O |
| 77 | I/O |
| 78 | I/O |
| 79 | I/O |
| 80 | I/O |
| 81 | I/O |
| 82 | I/O |
| 83 | CLKA |
| 84 | CLKB |

208-Pin PQFP

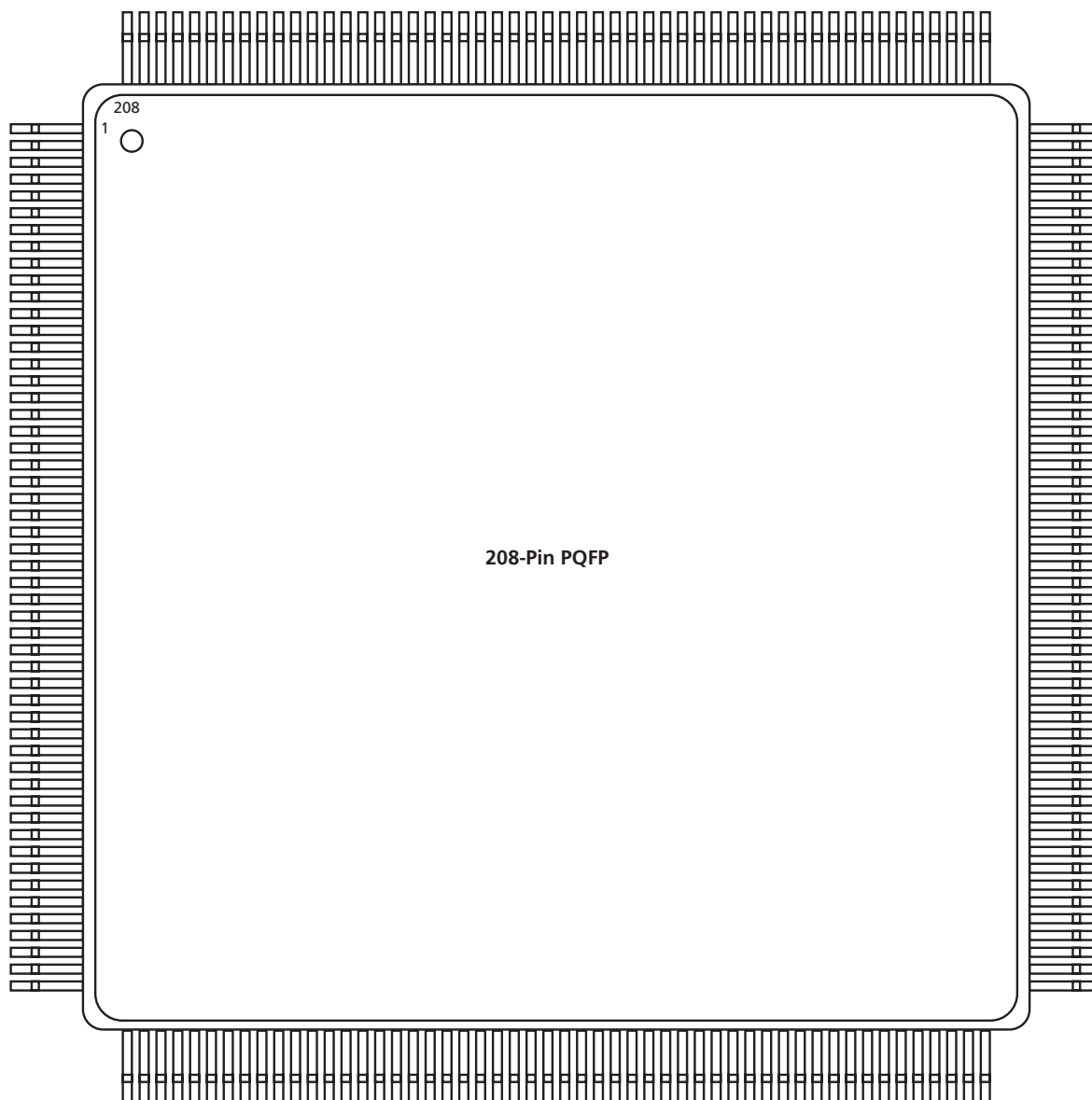


Figure 2-2 • 208-Pin PQFP (Top View)

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

| 208-Pin PQFP | | | |
|--------------|------------------|----------------------------|------------------|
| Pin Number | A54SX08 Function | A54SX16, A54SX16P Function | A54SX32 Function |
| 1 | GND | GND | GND |
| 2 | TDI, I/O | TDI, I/O | TDI, I/O |
| 3 | I/O | I/O | I/O |
| 4 | NC | I/O | I/O |
| 5 | I/O | I/O | I/O |
| 6 | NC | I/O | I/O |
| 7 | I/O | I/O | I/O |
| 8 | I/O | I/O | I/O |
| 9 | I/O | I/O | I/O |
| 10 | I/O | I/O | I/O |
| 11 | TMS | TMS | TMS |
| 12 | V _{CCI} | V _{CCI} | V _{CCI} |
| 13 | I/O | I/O | I/O |
| 14 | NC | I/O | I/O |
| 15 | I/O | I/O | I/O |
| 16 | I/O | I/O | I/O |
| 17 | NC | I/O | I/O |
| 18 | I/O | I/O | I/O |
| 19 | I/O | I/O | I/O |
| 20 | NC | I/O | I/O |
| 21 | I/O | I/O | I/O |
| 22 | I/O | I/O | I/O |
| 23 | NC | I/O | I/O |
| 24 | I/O | I/O | I/O |
| 25 | V _{CCR} | V _{CCR} | V _{CCR} |
| 26 | GND | GND | GND |
| 27 | V _{CCA} | V _{CCA} | V _{CCA} |
| 28 | GND | GND | GND |
| 29 | I/O | I/O | I/O |
| 30 | I/O | I/O | I/O |
| 31 | NC | I/O | I/O |
| 32 | I/O | I/O | I/O |
| 33 | I/O | I/O | I/O |
| 34 | I/O | I/O | I/O |
| 35 | NC | I/O | I/O |
| 36 | I/O | I/O | I/O |

| 208-Pin PQFP | | | |
|--------------|------------------|----------------------------|------------------|
| Pin Number | A54SX08 Function | A54SX16, A54SX16P Function | A54SX32 Function |
| 37 | I/O | I/O | I/O |
| 38 | I/O | I/O | I/O |
| 39 | NC | I/O | I/O |
| 40 | V _{CCI} | V _{CCI} | V _{CCI} |
| 41 | V _{CCA} | V _{CCA} | V _{CCA} |
| 42 | I/O | I/O | I/O |
| 43 | I/O | I/O | I/O |
| 44 | I/O | I/O | I/O |
| 45 | I/O | I/O | I/O |
| 46 | I/O | I/O | I/O |
| 47 | I/O | I/O | I/O |
| 48 | NC | I/O | I/O |
| 49 | I/O | I/O | I/O |
| 50 | NC | I/O | I/O |
| 51 | I/O | I/O | I/O |
| 52 | GND | GND | GND |
| 53 | I/O | I/O | I/O |
| 54 | I/O | I/O | I/O |
| 55 | I/O | I/O | I/O |
| 56 | I/O | I/O | I/O |
| 57 | I/O | I/O | I/O |
| 58 | I/O | I/O | I/O |
| 59 | I/O | I/O | I/O |
| 60 | V _{CCI} | V _{CCI} | V _{CCI} |
| 61 | NC | I/O | I/O |
| 62 | I/O | I/O | I/O |
| 63 | I/O | I/O | I/O |
| 64 | NC | I/O | I/O |
| 65* | I/O | I/O | NC* |
| 66 | I/O | I/O | I/O |
| 67 | NC | I/O | I/O |
| 68 | I/O | I/O | I/O |
| 69 | I/O | I/O | I/O |
| 70 | NC | I/O | I/O |
| 71 | I/O | I/O | I/O |
| 72 | I/O | I/O | I/O |

Note: * Note that Pin 65 in the A54SX32—PQ208 is a no connect (NC).

| 208-Pin PQFP | | | |
|--------------|------------------|----------------------------|------------------|
| Pin Number | A545X08 Function | A545X16, A545X16P Function | A545X32 Function |
| 73 | NC | I/O | I/O |
| 74 | I/O | I/O | I/O |
| 75 | NC | I/O | I/O |
| 76 | PRB, I/O | PRB, I/O | PRB, I/O |
| 77 | GND | GND | GND |
| 78 | V _{CCA} | V _{CCA} | V _{CCA} |
| 79 | GND | GND | GND |
| 80 | V _{CCR} | V _{CCR} | V _{CCR} |
| 81 | I/O | I/O | I/O |
| 82 | HCLK | HCLK | HCLK |
| 83 | I/O | I/O | I/O |
| 84 | I/O | I/O | I/O |
| 85 | NC | I/O | I/O |
| 86 | I/O | I/O | I/O |
| 87 | I/O | I/O | I/O |
| 88 | NC | I/O | I/O |
| 89 | I/O | I/O | I/O |
| 90 | I/O | I/O | I/O |
| 91 | NC | I/O | I/O |
| 92 | I/O | I/O | I/O |
| 93 | I/O | I/O | I/O |
| 94 | NC | I/O | I/O |
| 95 | I/O | I/O | I/O |
| 96 | I/O | I/O | I/O |
| 97 | NC | I/O | I/O |
| 98 | V _{CCI} | V _{CCI} | V _{CCI} |
| 99 | I/O | I/O | I/O |
| 100 | I/O | I/O | I/O |
| 101 | I/O | I/O | I/O |
| 102 | I/O | I/O | I/O |
| 103 | TDO, I/O | TDO, I/O | TDO, I/O |
| 104 | I/O | I/O | I/O |
| 105 | GND | GND | GND |
| 106 | NC | I/O | I/O |
| 107 | I/O | I/O | I/O |
| 108 | NC | I/O | I/O |

| 208-Pin PQFP | | | |
|--------------|------------------|----------------------------|------------------|
| Pin Number | A545X08 Function | A545X16, A545X16P Function | A545X32 Function |
| 109 | I/O | I/O | I/O |
| 110 | I/O | I/O | I/O |
| 111 | I/O | I/O | I/O |
| 112 | I/O | I/O | I/O |
| 113 | I/O | I/O | I/O |
| 114 | V _{CCA} | V _{CCA} | V _{CCA} |
| 115 | V _{CCI} | V _{CCI} | V _{CCI} |
| 116 | NC | I/O | I/O |
| 117 | I/O | I/O | I/O |
| 118 | I/O | I/O | I/O |
| 119 | NC | I/O | I/O |
| 120 | I/O | I/O | I/O |
| 121 | I/O | I/O | I/O |
| 122 | NC | I/O | I/O |
| 123 | I/O | I/O | I/O |
| 124 | I/O | I/O | I/O |
| 125 | NC | I/O | I/O |
| 126 | I/O | I/O | I/O |
| 127 | I/O | I/O | I/O |
| 128 | I/O | I/O | I/O |
| 129 | GND | GND | GND |
| 130 | V _{CCA} | V _{CCA} | V _{CCA} |
| 131 | GND | GND | GND |
| 132 | V _{CCR} | V _{CCR} | V _{CCR} |
| 133 | I/O | I/O | I/O |
| 134 | I/O | I/O | I/O |
| 135 | NC | I/O | I/O |
| 136 | I/O | I/O | I/O |
| 137 | I/O | I/O | I/O |
| 138 | NC | I/O | I/O |
| 139 | I/O | I/O | I/O |
| 140 | I/O | I/O | I/O |
| 141 | NC | I/O | I/O |
| 142 | I/O | I/O | I/O |
| 143 | NC | I/O | I/O |
| 144 | I/O | I/O | I/O |

Note: * Note that Pin 65 in the A545X32—PQ208 is a no connect (NC).

| 208-Pin PQFP | | | |
|--------------|------------------|----------------------------|------------------|
| Pin Number | A54SX08 Function | A54SX16, A54SX16P Function | A54SX32 Function |
| 145 | V _{CCA} | V _{CCA} | V _{CCA} |
| 146 | GND | GND | GND |
| 147 | I/O | I/O | I/O |
| 148 | V _{CCI} | V _{CCI} | V _{CCI} |
| 149 | I/O | I/O | I/O |
| 150 | I/O | I/O | I/O |
| 151 | I/O | I/O | I/O |
| 152 | I/O | I/O | I/O |
| 153 | I/O | I/O | I/O |
| 154 | I/O | I/O | I/O |
| 155 | NC | I/O | I/O |
| 156 | NC | I/O | I/O |
| 157 | GND | GND | GND |
| 158 | I/O | I/O | I/O |
| 159 | I/O | I/O | I/O |
| 160 | I/O | I/O | I/O |
| 161 | I/O | I/O | I/O |
| 162 | I/O | I/O | I/O |
| 163 | I/O | I/O | I/O |
| 164 | V _{CCI} | V _{CCI} | V _{CCI} |
| 165 | I/O | I/O | I/O |
| 166 | I/O | I/O | I/O |
| 167 | NC | I/O | I/O |
| 168 | I/O | I/O | I/O |
| 169 | I/O | I/O | I/O |
| 170 | NC | I/O | I/O |
| 171 | I/O | I/O | I/O |
| 172 | I/O | I/O | I/O |
| 173 | NC | I/O | I/O |
| 174 | I/O | I/O | I/O |
| 175 | I/O | I/O | I/O |
| 176 | NC | I/O | I/O |
| 177 | I/O | I/O | I/O |
| 178 | I/O | I/O | I/O |
| 179 | I/O | I/O | I/O |
| 180 | CLKA | CLKA | CLKA |

| 208-Pin PQFP | | | |
|--------------|------------------|----------------------------|------------------|
| Pin Number | A54SX08 Function | A54SX16, A54SX16P Function | A54SX32 Function |
| 181 | CLKB | CLKB | CLKB |
| 182 | V _{CCR} | V _{CCR} | V _{CCR} |
| 183 | GND | GND | GND |
| 184 | V _{CCA} | V _{CCA} | V _{CCA} |
| 185 | GND | GND | GND |
| 186 | PRA, I/O | PRA, I/O | PRA, I/O |
| 187 | I/O | I/O | I/O |
| 188 | I/O | I/O | I/O |
| 189 | NC | I/O | I/O |
| 190 | I/O | I/O | I/O |
| 191 | I/O | I/O | I/O |
| 192 | NC | I/O | I/O |
| 193 | I/O | I/O | I/O |
| 194 | I/O | I/O | I/O |
| 195 | NC | I/O | I/O |
| 196 | I/O | I/O | I/O |
| 197 | I/O | I/O | I/O |
| 198 | NC | I/O | I/O |
| 199 | I/O | I/O | I/O |
| 200 | I/O | I/O | I/O |
| 201 | V _{CCI} | V _{CCI} | V _{CCI} |
| 202 | NC | I/O | I/O |
| 203 | NC | I/O | I/O |
| 204 | I/O | I/O | I/O |
| 205 | NC | I/O | I/O |
| 206 | I/O | I/O | I/O |
| 207 | I/O | I/O | I/O |
| 208 | TCK, I/O | TCK, I/O | TCK, I/O |

Note: * Note that Pin 65 in the A54SX32—PQ208 is a no connect (NC).

144-Pin TQFP

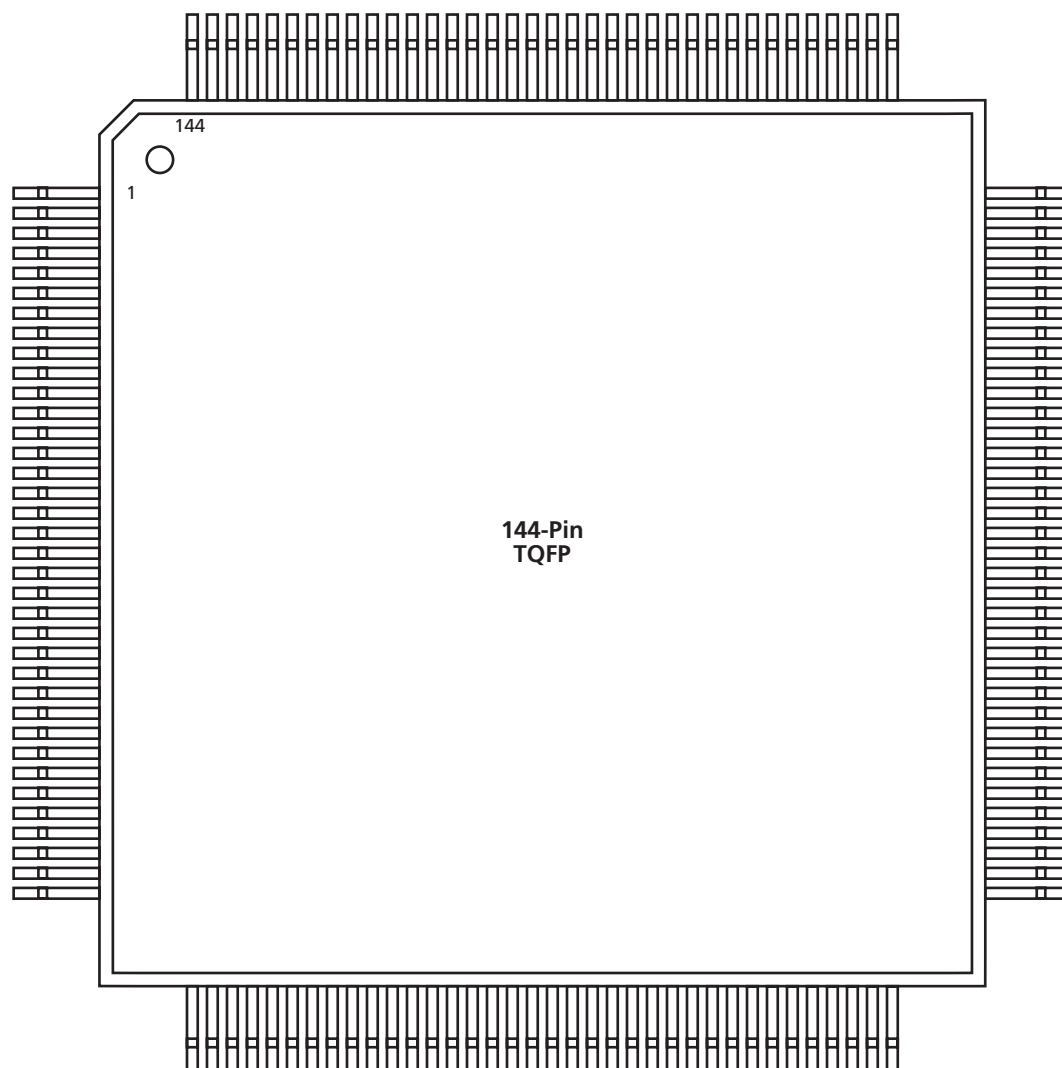


Figure 2-3 • 144-Pin TQFP (Top View)

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

| 144-Pin TQFP | | | |
|--------------|------------------|-------------------|------------------|
| Pin Number | A54SX08 Function | A54SX16P Function | A54SX32 Function |
| 1 | GND | GND | GND |
| 2 | TDI, I/O | TDI, I/O | TDI, I/O |
| 3 | I/O | I/O | I/O |
| 4 | I/O | I/O | I/O |
| 5 | I/O | I/O | I/O |
| 6 | I/O | I/O | I/O |
| 7 | I/O | I/O | I/O |
| 8 | I/O | I/O | I/O |
| 9 | TMS | TMS | TMS |
| 10 | V _{CCI} | V _{CCI} | V _{CCI} |
| 11 | GND | GND | GND |
| 12 | I/O | I/O | I/O |
| 13 | I/O | I/O | I/O |
| 14 | I/O | I/O | I/O |
| 15 | I/O | I/O | I/O |
| 16 | I/O | I/O | I/O |
| 17 | I/O | I/O | I/O |
| 18 | I/O | I/O | I/O |
| 19 | V _{CCR} | V _{CCR} | V _{CCR} |
| 20 | V _{CCA} | V _{CCA} | V _{CCA} |
| 21 | I/O | I/O | I/O |
| 22 | I/O | I/O | I/O |
| 23 | I/O | I/O | I/O |
| 24 | I/O | I/O | I/O |
| 25 | I/O | I/O | I/O |
| 26 | I/O | I/O | I/O |
| 27 | I/O | I/O | I/O |
| 28 | GND | GND | GND |
| 29 | V _{CCI} | V _{CCI} | V _{CCI} |
| 30 | V _{CCA} | V _{CCA} | V _{CCA} |
| 31 | I/O | I/O | I/O |
| 32 | I/O | I/O | I/O |
| 33 | I/O | I/O | I/O |
| 34 | I/O | I/O | I/O |
| 35 | I/O | I/O | I/O |
| 36 | GND | GND | GND |

| 144-Pin TQFP | | | |
|--------------|------------------|-------------------|------------------|
| Pin Number | A54SX08 Function | A54SX16P Function | A54SX32 Function |
| 37 | I/O | I/O | I/O |
| 38 | I/O | I/O | I/O |
| 39 | I/O | I/O | I/O |
| 40 | I/O | I/O | I/O |
| 41 | I/O | I/O | I/O |
| 42 | I/O | I/O | I/O |
| 43 | I/O | I/O | I/O |
| 44 | V _{CCI} | V _{CCI} | V _{CCI} |
| 45 | I/O | I/O | I/O |
| 46 | I/O | I/O | I/O |
| 47 | I/O | I/O | I/O |
| 48 | I/O | I/O | I/O |
| 49 | I/O | I/O | I/O |
| 50 | I/O | I/O | I/O |
| 51 | I/O | I/O | I/O |
| 52 | I/O | I/O | I/O |
| 53 | I/O | I/O | I/O |
| 54 | PRB, I/O | PRB, I/O | PRB, I/O |
| 55 | I/O | I/O | I/O |
| 56 | V _{CCA} | V _{CCA} | V _{CCA} |
| 57 | GND | GND | GND |
| 58 | V _{CCR} | V _{CCR} | V _{CCR} |
| 59 | I/O | I/O | I/O |
| 60 | HCLK | HCLK | HCLK |
| 61 | I/O | I/O | I/O |
| 62 | I/O | I/O | I/O |
| 63 | I/O | I/O | I/O |
| 64 | I/O | I/O | I/O |
| 65 | I/O | I/O | I/O |
| 66 | I/O | I/O | I/O |
| 67 | I/O | I/O | I/O |
| 68 | V _{CCI} | V _{CCI} | V _{CCI} |
| 69 | I/O | I/O | I/O |
| 70 | I/O | I/O | I/O |
| 71 | TDO, I/O | TDO, I/O | TDO, I/O |
| 72 | I/O | I/O | I/O |

| 144-Pin TQFP | | | |
|--------------|------------------|-------------------|------------------|
| Pin Number | A54SX08 Function | A54SX16P Function | A54SX32 Function |
| 73 | GND | GND | GND |
| 74 | I/O | I/O | I/O |
| 75 | I/O | I/O | I/O |
| 76 | I/O | I/O | I/O |
| 77 | I/O | I/O | I/O |
| 78 | I/O | I/O | I/O |
| 79 | V _{CCA} | V _{CCA} | V _{CCA} |
| 80 | V _{CCI} | V _{CCI} | V _{CCI} |
| 81 | GND | GND | GND |
| 82 | I/O | I/O | I/O |
| 83 | I/O | I/O | I/O |
| 84 | I/O | I/O | I/O |
| 85 | I/O | I/O | I/O |
| 86 | I/O | I/O | I/O |
| 87 | I/O | I/O | I/O |
| 88 | I/O | I/O | I/O |
| 89 | V _{CCA} | V _{CCA} | V _{CCA} |
| 90 | V _{CCR} | V _{CCR} | V _{CCR} |
| 91 | I/O | I/O | I/O |
| 92 | I/O | I/O | I/O |
| 93 | I/O | I/O | I/O |
| 94 | I/O | I/O | I/O |
| 95 | I/O | I/O | I/O |
| 96 | I/O | I/O | I/O |
| 97 | I/O | I/O | I/O |
| 98 | V _{CCA} | V _{CCA} | V _{CCA} |
| 99 | GND | GND | GND |
| 100 | I/O | I/O | I/O |
| 101 | GND | GND | GND |
| 102 | V _{CCI} | V _{CCI} | V _{CCI} |
| 103 | I/O | I/O | I/O |
| 104 | I/O | I/O | I/O |
| 105 | I/O | I/O | I/O |
| 106 | I/O | I/O | I/O |
| 107 | I/O | I/O | I/O |
| 108 | I/O | I/O | I/O |

| 144-Pin TQFP | | | |
|--------------|------------------|-------------------|------------------|
| Pin Number | A54SX08 Function | A54SX16P Function | A54SX32 Function |
| 109 | GND | GND | GND |
| 110 | I/O | I/O | I/O |
| 111 | I/O | I/O | I/O |
| 112 | I/O | I/O | I/O |
| 113 | I/O | I/O | I/O |
| 114 | I/O | I/O | I/O |
| 115 | V _{CCI} | V _{CCI} | V _{CCI} |
| 116 | I/O | I/O | I/O |
| 117 | I/O | I/O | I/O |
| 118 | I/O | I/O | I/O |
| 119 | I/O | I/O | I/O |
| 120 | I/O | I/O | I/O |
| 121 | I/O | I/O | I/O |
| 122 | I/O | I/O | I/O |
| 123 | I/O | I/O | I/O |
| 124 | I/O | I/O | I/O |
| 125 | CLKA | CLKA | CLKA |
| 126 | CLKB | CLKB | CLKB |
| 127 | V _{CCR} | V _{CCR} | V _{CCR} |
| 128 | GND | GND | GND |
| 129 | V _{CCA} | V _{CCA} | V _{CCA} |
| 130 | I/O | I/O | I/O |
| 131 | PRA, I/O | PRA, I/O | PRA, I/O |
| 132 | I/O | I/O | I/O |
| 133 | I/O | I/O | I/O |
| 134 | I/O | I/O | I/O |
| 135 | I/O | I/O | I/O |
| 136 | I/O | I/O | I/O |
| 137 | I/O | I/O | I/O |
| 138 | I/O | I/O | I/O |
| 139 | I/O | I/O | I/O |
| 140 | V _{CCI} | V _{CCI} | V _{CCI} |
| 141 | I/O | I/O | I/O |
| 142 | I/O | I/O | I/O |
| 143 | I/O | I/O | I/O |
| 144 | TCK, I/O | TCK, I/O | TCK, I/O |

176-Pin TQFP

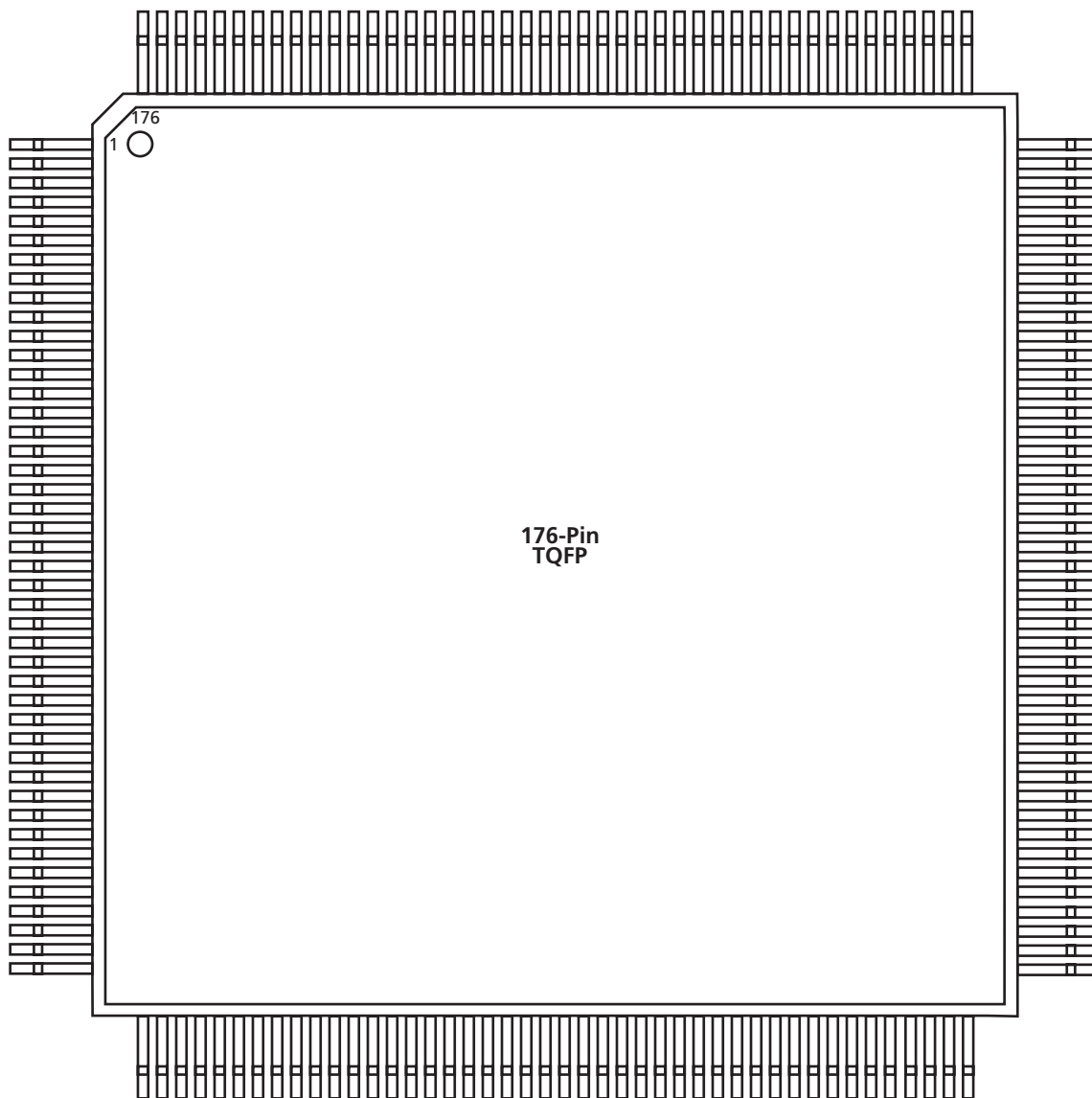


Figure 2-4 • 176-Pin TQFP (Top View)

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

| 176-Pin TQFP | | | |
|--------------|------------------|----------------------------|------------------|
| Pin Number | A54SX08 Function | A54SX16, A54SX16P Function | A54SX32 Function |
| 1 | GND | GND | GND |
| 2 | TDI, I/O | TDI, I/O | TDI, I/O |
| 3 | NC | I/O | I/O |
| 4 | I/O | I/O | I/O |
| 5 | I/O | I/O | I/O |
| 6 | I/O | I/O | I/O |
| 7 | I/O | I/O | I/O |
| 8 | I/O | I/O | I/O |
| 9 | I/O | I/O | I/O |
| 10 | TMS | TMS | TMS |
| 11 | V _{CCI} | V _{CCI} | V _{CCI} |
| 12 | NC | I/O | I/O |
| 13 | I/O | I/O | I/O |
| 14 | I/O | I/O | I/O |
| 15 | I/O | I/O | I/O |
| 16 | I/O | I/O | I/O |
| 17 | I/O | I/O | I/O |
| 18 | I/O | I/O | I/O |
| 19 | I/O | I/O | I/O |
| 20 | I/O | I/O | I/O |
| 21 | GND | GND | GND |
| 22 | V _{CCA} | V _{CCA} | V _{CCA} |
| 23 | GND | GND | GND |
| 24 | I/O | I/O | I/O |
| 25 | I/O | I/O | I/O |
| 26 | I/O | I/O | I/O |
| 27 | I/O | I/O | I/O |
| 28 | I/O | I/O | I/O |
| 29 | I/O | I/O | I/O |
| 30 | I/O | I/O | I/O |
| 31 | I/O | I/O | I/O |
| 32 | V _{CCI} | V _{CCI} | V _{CCI} |
| 33 | V _{CCA} | V _{CCA} | V _{CCA} |
| 34 | I/O | I/O | I/O |

| 176-Pin TQFP | | | |
|--------------|------------------|----------------------------|------------------|
| Pin Number | A54SX08 Function | A54SX16, A54SX16P Function | A54SX32 Function |
| 35 | I/O | I/O | I/O |
| 36 | I/O | I/O | I/O |
| 37 | I/O | I/O | I/O |
| 38 | I/O | I/O | I/O |
| 39 | I/O | I/O | I/O |
| 40 | NC | I/O | I/O |
| 41 | I/O | I/O | I/O |
| 42 | NC | I/O | I/O |
| 43 | I/O | I/O | I/O |
| 44 | GND | GND | GND |
| 45 | I/O | I/O | I/O |
| 46 | I/O | I/O | I/O |
| 47 | I/O | I/O | I/O |
| 48 | I/O | I/O | I/O |
| 49 | I/O | I/O | I/O |
| 50 | I/O | I/O | I/O |
| 51 | I/O | I/O | I/O |
| 52 | V _{CCI} | V _{CCI} | V _{CCI} |
| 53 | I/O | I/O | I/O |
| 54 | NC | I/O | I/O |
| 55 | I/O | I/O | I/O |
| 56 | I/O | I/O | I/O |
| 57 | NC | I/O | I/O |
| 58 | I/O | I/O | I/O |
| 59 | I/O | I/O | I/O |
| 60 | I/O | I/O | I/O |
| 61 | I/O | I/O | I/O |
| 62 | I/O | I/O | I/O |
| 63 | I/O | I/O | I/O |
| 64 | PRB, I/O | PRB, I/O | PRB, I/O |
| 65 | GND | GND | GND |
| 66 | V _{CCA} | V _{CCA} | V _{CCA} |
| 67 | V _{CCR} | V _{CCR} | V _{CCR} |
| 68 | I/O | I/O | I/O |

| 176-Pin TQFP | | | |
|--------------|------------------|----------------------------|------------------|
| Pin Number | A54SX08 Function | A54SX16, A54SX16P Function | A54SX32 Function |
| 69 | HCLK | HCLK | HCLK |
| 70 | I/O | I/O | I/O |
| 71 | I/O | I/O | I/O |
| 72 | I/O | I/O | I/O |
| 73 | I/O | I/O | I/O |
| 74 | I/O | I/O | I/O |
| 75 | I/O | I/O | I/O |
| 76 | I/O | I/O | I/O |
| 77 | I/O | I/O | I/O |
| 78 | I/O | I/O | I/O |
| 79 | NC | I/O | I/O |
| 80 | I/O | I/O | I/O |
| 81 | NC | I/O | I/O |
| 82 | V _{CCI} | V _{CCI} | V _{CCI} |
| 83 | I/O | I/O | I/O |
| 84 | I/O | I/O | I/O |
| 85 | I/O | I/O | I/O |
| 86 | I/O | I/O | I/O |
| 87 | TDO, I/O | TDO, I/O | TDO, I/O |
| 88 | I/O | I/O | I/O |
| 89 | GND | GND | GND |
| 90 | NC | I/O | I/O |
| 91 | NC | I/O | I/O |
| 92 | I/O | I/O | I/O |
| 93 | I/O | I/O | I/O |
| 94 | I/O | I/O | I/O |
| 95 | I/O | I/O | I/O |
| 96 | I/O | I/O | I/O |
| 97 | I/O | I/O | I/O |
| 98 | V _{CCA} | V _{CCA} | V _{CCA} |
| 99 | V _{CCI} | V _{CCI} | V _{CCI} |
| 100 | I/O | I/O | I/O |
| 101 | I/O | I/O | I/O |
| 102 | I/O | I/O | I/O |

| 176-Pin TQFP | | | |
|--------------|------------------|----------------------------|------------------|
| Pin Number | A54SX08 Function | A54SX16, A54SX16P Function | A54SX32 Function |
| 103 | I/O | I/O | I/O |
| 104 | I/O | I/O | I/O |
| 105 | I/O | I/O | I/O |
| 106 | I/O | I/O | I/O |
| 107 | I/O | I/O | I/O |
| 108 | GND | GND | GND |
| 109 | V _{CCA} | V _{CCA} | V _{CCA} |
| 110 | GND | GND | GND |
| 111 | I/O | I/O | I/O |
| 112 | I/O | I/O | I/O |
| 113 | I/O | I/O | I/O |
| 114 | I/O | I/O | I/O |
| 115 | I/O | I/O | I/O |
| 116 | I/O | I/O | I/O |
| 117 | I/O | I/O | I/O |
| 118 | NC | I/O | I/O |
| 119 | I/O | I/O | I/O |
| 120 | NC | I/O | I/O |
| 121 | NC | I/O | I/O |
| 122 | V _{CCA} | V _{CCA} | V _{CCA} |
| 123 | GND | GND | GND |
| 124 | V _{CCI} | V _{CCI} | V _{CCI} |
| 125 | I/O | I/O | I/O |
| 126 | I/O | I/O | I/O |
| 127 | I/O | I/O | I/O |
| 128 | I/O | I/O | I/O |
| 129 | I/O | I/O | I/O |
| 130 | I/O | I/O | I/O |
| 131 | NC | I/O | I/O |
| 132 | NC | I/O | I/O |
| 133 | GND | GND | GND |
| 134 | I/O | I/O | I/O |
| 135 | I/O | I/O | I/O |
| 136 | I/O | I/O | I/O |

| 176-Pin TQFP | | | |
|--------------|------------------|----------------------------|------------------|
| Pin Number | A545X08 Function | A545X16, A545X16P Function | A545X32 Function |
| 137 | I/O | I/O | I/O |
| 138 | I/O | I/O | I/O |
| 139 | I/O | I/O | I/O |
| 140 | V _{CCI} | V _{CCI} | V _{CCI} |
| 141 | I/O | I/O | I/O |
| 142 | I/O | I/O | I/O |
| 143 | I/O | I/O | I/O |
| 144 | I/O | I/O | I/O |
| 145 | I/O | I/O | I/O |
| 146 | I/O | I/O | I/O |
| 147 | I/O | I/O | I/O |
| 148 | I/O | I/O | I/O |
| 149 | I/O | I/O | I/O |
| 150 | I/O | I/O | I/O |
| 151 | I/O | I/O | I/O |
| 152 | CLKA | CLKA | CLKA |
| 153 | CLKB | CLKB | CLKB |
| 154 | V _{CCR} | V _{CCR} | V _{CCR} |
| 155 | GND | GND | GND |
| 156 | V _{CCA} | V _{CCA} | V _{CCA} |

| 176-Pin TQFP | | | |
|--------------|------------------|----------------------------|------------------|
| Pin Number | A545X08 Function | A545X16, A545X16P Function | A545X32 Function |
| 157 | PRA, I/O | PRA, I/O | PRA, I/O |
| 158 | I/O | I/O | I/O |
| 159 | I/O | I/O | I/O |
| 160 | I/O | I/O | I/O |
| 161 | I/O | I/O | I/O |
| 162 | I/O | I/O | I/O |
| 163 | I/O | I/O | I/O |
| 164 | I/O | I/O | I/O |
| 165 | I/O | I/O | I/O |
| 166 | I/O | I/O | I/O |
| 167 | I/O | I/O | I/O |
| 168 | NC | I/O | I/O |
| 169 | V _{CCI} | V _{CCI} | V _{CCI} |
| 170 | I/O | I/O | I/O |
| 171 | NC | I/O | I/O |
| 172 | NC | I/O | I/O |
| 173 | NC | I/O | I/O |
| 174 | I/O | I/O | I/O |
| 175 | I/O | I/O | I/O |
| 176 | TCK, I/O | TCK, I/O | TCK, I/O |

100-Pin VQFP

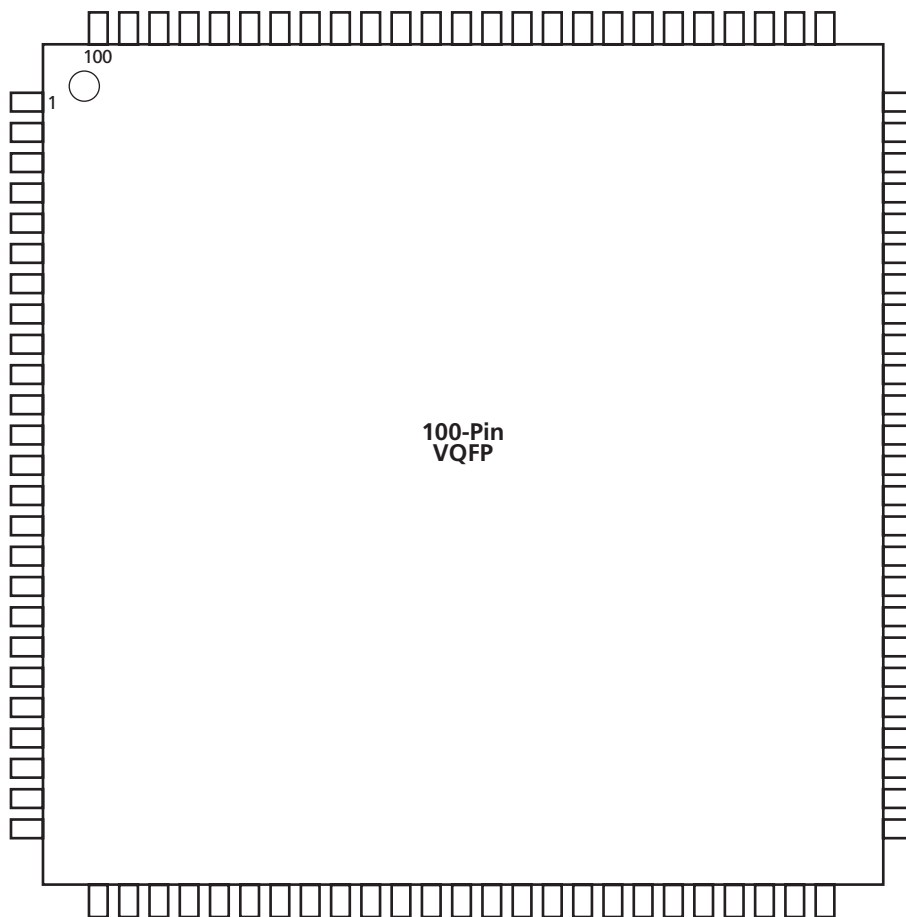


Figure 2-5 • 100-Pin VQFP (Top View)

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

| 100-Pin VQFP | | |
|--------------|------------------|----------------------------|
| Pin Number | A545X08 Function | A545X16, A545X16P Function |
| 1 | GND | GND |
| 2 | TDI, I/O | TDI, I/O |
| 3 | I/O | I/O |
| 4 | I/O | I/O |
| 5 | I/O | I/O |
| 6 | I/O | I/O |
| 7 | TMS | TMS |
| 8 | V _{CCI} | V _{CCI} |
| 9 | GND | GND |
| 10 | I/O | I/O |
| 11 | I/O | I/O |
| 12 | I/O | I/O |
| 13 | I/O | I/O |
| 14 | I/O | I/O |
| 15 | I/O | I/O |
| 16 | I/O | I/O |
| 17 | I/O | I/O |
| 18 | I/O | I/O |
| 19 | I/O | I/O |
| 20 | V _{CCI} | V _{CCI} |
| 21 | I/O | I/O |
| 22 | I/O | I/O |
| 23 | I/O | I/O |
| 24 | I/O | I/O |
| 25 | I/O | I/O |
| 26 | I/O | I/O |
| 27 | I/O | I/O |
| 28 | I/O | I/O |
| 29 | I/O | I/O |
| 30 | I/O | I/O |
| 31 | I/O | I/O |
| 32 | I/O | I/O |
| 33 | I/O | I/O |
| 34 | PRB, I/O | PRB, I/O |

| 100-Pin VQFP | | |
|--------------|------------------|----------------------------|
| Pin Number | A545X08 Function | A545X16, A545X16P Function |
| 35 | V _{CCA} | V _{CCA} |
| 36 | GND | GND |
| 37 | V _{CCR} | V _{CCR} |
| 38 | I/O | I/O |
| 39 | HCLK | HCLK |
| 40 | I/O | I/O |
| 41 | I/O | I/O |
| 42 | I/O | I/O |
| 43 | I/O | I/O |
| 44 | V _{CCI} | V _{CCI} |
| 45 | I/O | I/O |
| 46 | I/O | I/O |
| 47 | I/O | I/O |
| 48 | I/O | I/O |
| 49 | TDO, I/O | TDO, I/O |
| 50 | I/O | I/O |
| 51 | GND | GND |
| 52 | I/O | I/O |
| 53 | I/O | I/O |
| 54 | I/O | I/O |
| 55 | I/O | I/O |
| 56 | I/O | I/O |
| 57 | V _{CCA} | V _{CCA} |
| 58 | V _{CCI} | V _{CCI} |
| 59 | I/O | I/O |
| 60 | I/O | I/O |
| 61 | I/O | I/O |
| 62 | I/O | I/O |
| 63 | I/O | I/O |
| 64 | I/O | I/O |
| 65 | I/O | I/O |
| 66 | I/O | I/O |
| 67 | V _{CCA} | V _{CCA} |
| 68 | GND | GND |

| 100-Pin VQFP | | |
|--------------|------------------|----------------------------|
| Pin Number | A545X08 Function | A545X16, A545X16P Function |
| 69 | GND | GND |
| 70 | I/O | I/O |
| 71 | I/O | I/O |
| 72 | I/O | I/O |
| 73 | I/O | I/O |
| 74 | I/O | I/O |
| 75 | I/O | I/O |
| 76 | I/O | I/O |
| 77 | I/O | I/O |
| 78 | I/O | I/O |
| 79 | I/O | I/O |
| 80 | I/O | I/O |
| 81 | I/O | I/O |
| 82 | V _{CCI} | V _{CCI} |
| 83 | I/O | I/O |
| 84 | I/O | I/O |
| 85 | I/O | I/O |
| 86 | I/O | I/O |
| 87 | CLKA | CLKA |
| 88 | CLKB | CLKB |
| 89 | V _{CCR} | V _{CCR} |
| 90 | V _{CCA} | V _{CCA} |
| 91 | GND | GND |
| 92 | PRA, I/O | PRA, I/O |
| 93 | I/O | I/O |
| 94 | I/O | I/O |
| 95 | I/O | I/O |
| 96 | I/O | I/O |
| 97 | I/O | I/O |
| 98 | I/O | I/O |
| 99 | I/O | I/O |
| 100 | TCK, I/O | TCK, I/O |

313-Pin PBGA

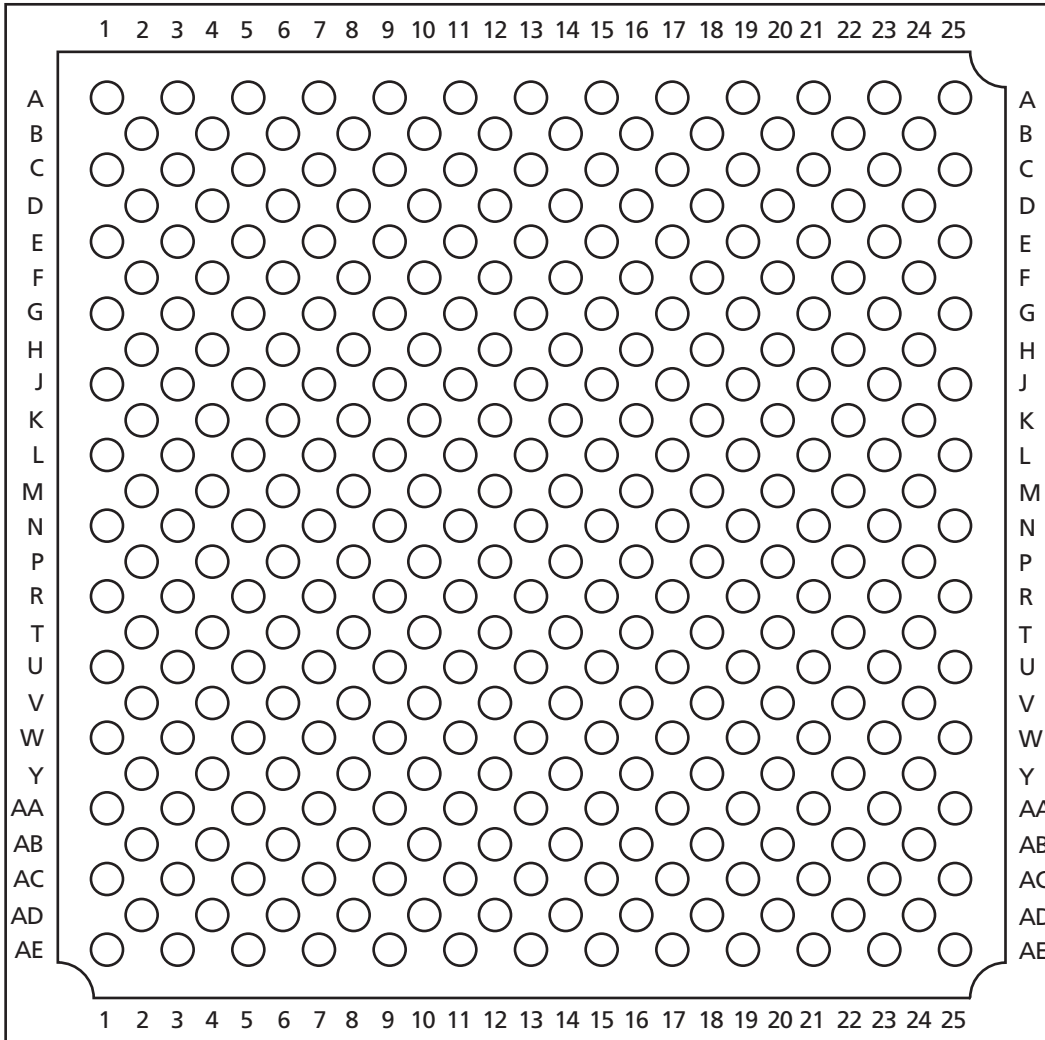


Figure 2-6 • 313-Pin PBGA (Top View)

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

| 313-Pin PBGA | |
|--------------|------------------|
| Pin Number | A54SX32 Function |
| A1 | GND |
| A3 | NC |
| A5 | I/O |
| A7 | I/O |
| A9 | I/O |
| A11 | I/O |
| A13 | V _{CCR} |
| A15 | I/O |
| A17 | I/O |
| A19 | I/O |
| A21 | I/O |
| A23 | NC |
| A25 | GND |
| AA1 | I/O |
| AA3 | I/O |
| AA5 | NC |
| AA7 | I/O |
| AA9 | NC |
| AA11 | I/O |
| AA13 | I/O |
| AA15 | I/O |
| AA17 | I/O |
| AA19 | I/O |
| AA21 | I/O |
| AA23 | NC |
| AA25 | I/O |
| AB2 | NC |
| AB4 | NC |
| AB6 | I/O |
| AB8 | I/O |
| AB10 | I/O |
| AB12 | I/O |
| AB14 | I/O |
| AB16 | I/O |
| AB18 | V _{CCI} |
| AB20 | NC |
| AB22 | I/O |
| AB24 | I/O |
| AC1 | I/O |
| AC3 | I/O |

| 313-Pin PBGA | |
|--------------|------------------|
| Pin Number | A54SX32 Function |
| AC5 | I/O |
| AC7 | I/O |
| AC9 | I/O |
| AC11 | I/O |
| AC13 | V _{CCR} |
| AC15 | I/O |
| AC17 | I/O |
| AC19 | I/O |
| AC21 | I/O |
| AC23 | I/O |
| AC25 | NC |
| AD2 | GND |
| AD4 | I/O |
| AD6 | V _{CCI} |
| AD8 | I/O |
| AD10 | I/O |
| AD12 | PRB, I/O |
| AD14 | I/O |
| AD16 | I/O |
| AD18 | I/O |
| AD20 | I/O |
| AD22 | NC |
| AD24 | I/O |
| AE1 | NC |
| AE3 | I/O |
| AE5 | I/O |
| AE7 | I/O |
| AE9 | I/O |
| AE11 | I/O |
| AE13 | V _{CCA} |
| AE15 | I/O |
| AE17 | I/O |
| AE19 | I/O |
| AE21 | I/O |
| AE23 | TDO, I/O |
| AE25 | GND |
| B2 | TCK, I/O |
| B4 | I/O |
| B6 | I/O |
| B8 | I/O |

| 313-Pin PBGA | |
|--------------|------------------|
| Pin Number | A54SX32 Function |
| B10 | I/O |
| B12 | I/O |
| B14 | I/O |
| B16 | I/O |
| B18 | I/O |
| B20 | I/O |
| B22 | I/O |
| B24 | I/O |
| C1 | TDI, I/O |
| C3 | I/O |
| C5 | NC |
| C7 | I/O |
| C9 | I/O |
| C11 | I/O |
| C13 | V _{CCI} |
| C15 | I/O |
| C17 | I/O |
| C19 | V _{CCI} |
| C21 | I/O |
| C23 | I/O |
| C25 | NC |
| D2 | I/O |
| D4 | NC |
| D6 | I/O |
| D8 | I/O |
| D10 | I/O |
| D12 | I/O |
| D14 | I/O |
| D16 | I/O |
| D18 | I/O |
| D20 | I/O |
| D22 | I/O |
| D24 | NC |
| E1 | I/O |
| E3 | NC |
| E5 | I/O |
| E7 | I/O |
| E9 | I/O |
| E11 | I/O |
| E13 | V _{CCA} |

| 313-Pin PBGA | |
|--------------|------------------|
| Pin Number | A54SX32 Function |
| E15 | I/O |
| E17 | I/O |
| E19 | I/O |
| E21 | I/O |
| E23 | I/O |
| E25 | I/O |
| F2 | I/O |
| F4 | I/O |
| F6 | NC |
| F8 | I/O |
| F10 | NC |
| F12 | I/O |
| F14 | I/O |
| F16 | NC |
| F18 | I/O |
| F20 | I/O |
| F22 | I/O |
| F24 | I/O |
| G1 | I/O |
| G3 | TMS |
| G5 | I/O |
| G7 | I/O |
| G9 | V _{CCI} |
| G11 | I/O |
| G13 | CLKB |
| G15 | I/O |
| G17 | I/O |
| G19 | I/O |
| G21 | I/O |
| G23 | I/O |
| G25 | I/O |
| H2 | I/O |
| H4 | I/O |
| H6 | I/O |
| H8 | I/O |
| H10 | I/O |
| H12 | PRA, I/O |
| H14 | I/O |
| H16 | I/O |
| H18 | NC |

| 313-Pin PBGA | |
|--------------|------------------|
| Pin Number | A54SX32 Function |
| H20 | I/O |
| H22 | V _{CCI} |
| H24 | I/O |
| J1 | I/O |
| J3 | I/O |
| J5 | I/O |
| J7 | NC |
| J9 | I/O |
| J11 | I/O |
| J13 | CLKA |
| J15 | I/O |
| J17 | I/O |
| J19 | I/O |
| J21 | GND |
| J23 | I/O |
| J25 | I/O |
| K2 | I/O |
| K4 | I/O |
| K6 | I/O |
| K8 | V _{CCI} |
| K10 | I/O |
| K12 | I/O |
| K14 | I/O |
| K16 | I/O |
| K18 | I/O |
| K20 | V _{CCA} |
| K22 | I/O |
| K24 | I/O |
| L1 | I/O |
| L3 | I/O |
| L5 | I/O |
| L7 | I/O |
| L9 | I/O |
| L11 | I/O |
| L13 | GND |
| L15 | I/O |
| L17 | I/O |
| L19 | I/O |
| L21 | I/O |
| L23 | I/O |

| 313-Pin PBGA | |
|--------------|------------------|
| Pin Number | A54SX32 Function |
| L25 | I/O |
| M2 | I/O |
| M4 | I/O |
| M6 | I/O |
| M8 | I/O |
| M10 | I/O |
| M12 | GND |
| M14 | GND |
| M16 | V _{CCI} |
| M18 | I/O |
| M20 | I/O |
| M22 | I/O |
| M24 | I/O |
| N1 | I/O |
| N3 | V _{CCA} |
| N5 | V _{CCR} |
| N7 | I/O |
| N9 | V _{CCI} |
| N11 | GND |
| N13 | GND |
| N15 | GND |
| N17 | I/O |
| N19 | I/O |
| N21 | I/O |
| N23 | V _{CCR} |
| N25 | V _{CCA} |
| P2 | I/O |
| P4 | I/O |
| P6 | I/O |
| P8 | I/O |
| P10 | I/O |
| P12 | GND |
| P14 | GND |
| P16 | I/O |
| P18 | I/O |
| P20 | NC |
| P22 | I/O |
| P24 | I/O |
| R1 | I/O |
| R3 | I/O |

| 313-Pin PBGA | |
|--------------|------------------|
| Pin Number | A54SX32 Function |
| R5 | I/O |
| R7 | I/O |
| R9 | I/O |
| R11 | I/O |
| R13 | GND |
| R15 | I/O |
| R17 | I/O |
| R19 | I/O |
| R21 | I/O |
| R23 | I/O |
| R25 | I/O |
| T2 | I/O |
| T4 | I/O |
| T6 | I/O |
| T8 | I/O |
| T10 | I/O |
| T12 | I/O |
| T14 | HCLK |
| T16 | I/O |
| T18 | I/O |
| T20 | I/O |
| T22 | I/O |
| T24 | I/O |
| U1 | I/O |
| U3 | I/O |
| U5 | V _{CCI} |
| U7 | I/O |
| U9 | I/O |
| U11 | I/O |
| U13 | I/O |
| U15 | I/O |
| U17 | I/O |
| U19 | I/O |
| U21 | I/O |
| U23 | I/O |
| U25 | I/O |
| V2 | V _{CCA} |
| V4 | I/O |
| V6 | I/O |
| V8 | I/O |

| 313-Pin PBGA | |
|--------------|------------------|
| Pin Number | A54SX32 Function |
| V10 | I/O |
| V12 | I/O |
| V14 | I/O |
| V16 | NC |
| V18 | I/O |
| V20 | I/O |
| V22 | V _{CCA} |
| V24 | V _{CCI} |
| W1 | I/O |
| W3 | I/O |
| W5 | I/O |
| W7 | NC |
| W9 | I/O |
| W11 | I/O |
| W13 | V _{CCI} |
| W15 | I/O |
| W17 | I/O |
| W19 | I/O |
| W21 | I/O |
| W23 | I/O |
| W25 | I/O |
| Y2 | I/O |
| Y4 | I/O |
| Y6 | I/O |
| Y8 | I/O |
| Y10 | I/O |
| Y12 | I/O |
| Y14 | I/O |
| Y16 | I/O |
| Y18 | I/O |
| Y20 | NC |
| Y22 | I/O |
| Y24 | NC |

329-Pin PBGA

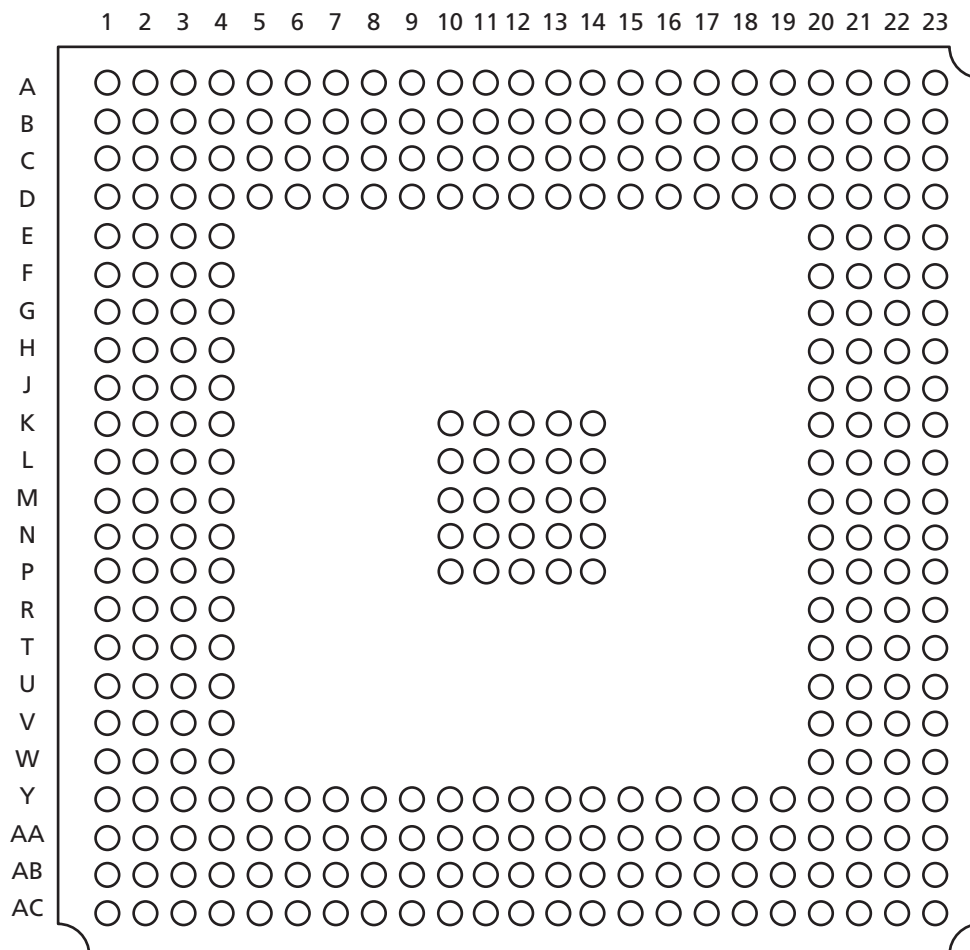


Figure 2-7 • 329-Pin PBGA (Top View)

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

| 329-Pin PBGA | |
|--------------|------------------|
| Pin Number | A54SX32 Function |
| A1 | GND |
| A2 | GND |
| A3 | V _{CCI} |
| A4 | NC |
| A5 | I/O |
| A6 | I/O |
| A7 | V _{CCI} |
| A8 | NC |
| A9 | I/O |
| A10 | I/O |
| A11 | I/O |
| A12 | I/O |
| A13 | CLKB |
| A14 | I/O |
| A15 | I/O |
| A16 | I/O |
| A17 | I/O |
| A18 | I/O |
| A19 | I/O |
| A20 | I/O |
| A21 | NC |
| A22 | V _{CCI} |
| A23 | GND |
| AA1 | V _{CCI} |
| AA2 | I/O |
| AA3 | GND |
| AA4 | I/O |
| AA5 | I/O |
| AA6 | I/O |
| AA7 | I/O |
| AA8 | I/O |
| AA9 | I/O |
| AA10 | I/O |
| AA11 | I/O |
| AA12 | I/O |

| 329-Pin PBGA | |
|--------------|------------------|
| Pin Number | A54SX32 Function |
| AA13 | I/O |
| AA14 | I/O |
| AA15 | I/O |
| AA16 | I/O |
| AA17 | I/O |
| AA18 | I/O |
| AA19 | I/O |
| AA20 | TDO, I/O |
| AA21 | V _{CCI} |
| AA22 | I/O |
| AA23 | V _{CCI} |
| AB1 | I/O |
| AB2 | GND |
| AB3 | I/O |
| AB4 | I/O |
| AB5 | I/O |
| AB6 | I/O |
| AB7 | I/O |
| AB8 | I/O |
| AB9 | I/O |
| AB10 | I/O |
| AB11 | PRB, I/O |
| AB12 | I/O |
| AB13 | HCLK |
| AB14 | I/O |
| AB15 | I/O |
| AB16 | I/O |
| AB17 | I/O |
| AB18 | I/O |
| AB19 | I/O |
| AB20 | I/O |
| AB21 | I/O |
| AB22 | GND |
| AB23 | I/O |
| AC1 | GND |

| 329-Pin PBGA | |
|--------------|------------------|
| Pin Number | A54SX32 Function |
| AC2 | V _{CCI} |
| AC3 | NC |
| AC4 | I/O |
| AC5 | I/O |
| AC6 | I/O |
| AC7 | I/O |
| AC8 | I/O |
| AC9 | V _{CCI} |
| AC10 | I/O |
| AC11 | I/O |
| AC12 | I/O |
| AC13 | I/O |
| AC14 | I/O |
| AC15 | NC |
| AC16 | I/O |
| AC17 | I/O |
| AC18 | I/O |
| AC19 | I/O |
| AC20 | I/O |
| AC21 | NC |
| AC22 | V _{CCI} |
| AC23 | GND |
| B1 | V _{CCI} |
| B2 | GND |
| B3 | I/O |
| B4 | I/O |
| B5 | I/O |
| B6 | I/O |
| B7 | I/O |
| B8 | I/O |
| B9 | I/O |
| B10 | I/O |
| B11 | I/O |
| B12 | PRA, I/O |
| B13 | CLKA |

| 329-Pin PBGA | |
|--------------|------------------|
| Pin Number | A54SX32 Function |
| B14 | I/O |
| B15 | I/O |
| B16 | I/O |
| B17 | I/O |
| B18 | I/O |
| B19 | I/O |
| B20 | I/O |
| B21 | I/O |
| B22 | GND |
| B23 | V _{CCI} |
| C1 | NC |
| C2 | TDI, I/O |
| C3 | GND |
| C4 | I/O |
| C5 | I/O |
| C6 | I/O |
| C7 | I/O |
| C8 | I/O |
| C9 | I/O |
| C10 | I/O |
| C11 | I/O |
| C12 | I/O |
| C13 | I/O |
| C14 | I/O |
| C15 | I/O |
| C16 | I/O |
| C17 | I/O |
| C18 | I/O |
| C19 | I/O |
| C20 | I/O |
| C21 | V _{CCI} |
| C22 | GND |
| C23 | NC |
| D1 | I/O |
| D2 | I/O |

| 329-Pin PBGA | |
|--------------|------------------|
| Pin Number | A545X32 Function |
| D3 | I/O |
| D4 | TCK, I/O |
| D5 | I/O |
| D6 | I/O |
| D7 | I/O |
| D8 | I/O |
| D9 | I/O |
| D10 | I/O |
| D11 | V _{CCA} |
| D12 | V _{CCR} |
| D13 | I/O |
| D14 | I/O |
| D15 | I/O |
| D16 | I/O |
| D17 | I/O |
| D18 | I/O |
| D19 | I/O |
| D20 | I/O |
| D21 | I/O |
| D22 | I/O |
| D23 | I/O |
| E1 | V _{CCI} |
| E2 | I/O |
| E3 | I/O |
| E4 | I/O |
| E20 | I/O |
| E21 | I/O |
| E22 | I/O |
| E23 | I/O |
| F1 | I/O |
| F2 | TMS |
| F3 | I/O |
| F4 | I/O |
| F20 | I/O |
| F21 | I/O |

| 329-Pin PBGA | |
|--------------|------------------|
| Pin Number | A545X32 Function |
| F22 | I/O |
| F23 | I/O |
| G1 | I/O |
| G2 | I/O |
| G3 | I/O |
| G4 | I/O |
| G20 | I/O |
| G21 | I/O |
| G22 | I/O |
| G23 | GND |
| H1 | I/O |
| H2 | I/O |
| H3 | I/O |
| H4 | I/O |
| H20 | V _{CCA} |
| H21 | I/O |
| H22 | I/O |
| H23 | I/O |
| J1 | NC |
| J2 | I/O |
| J3 | I/O |
| J4 | I/O |
| J20 | I/O |
| J21 | I/O |
| J22 | I/O |
| J23 | I/O |
| K1 | I/O |
| K2 | I/O |
| K3 | I/O |
| K4 | I/O |
| K10 | GND |
| K11 | GND |
| K12 | GND |
| K13 | GND |
| K14 | GND |

| 329-Pin PBGA | |
|--------------|------------------|
| Pin Number | A545X32 Function |
| K20 | I/O |
| K21 | I/O |
| K22 | I/O |
| K23 | I/O |
| L1 | I/O |
| L2 | I/O |
| L3 | I/O |
| L4 | V _{CCR} |
| L10 | GND |
| L11 | GND |
| L12 | GND |
| L13 | GND |
| L14 | GND |
| L20 | V _{CCR} |
| L21 | I/O |
| L22 | I/O |
| L23 | NC |
| M1 | I/O |
| M2 | I/O |
| M3 | I/O |
| M4 | V _{CCA} |
| M10 | GND |
| M11 | GND |
| M12 | GND |
| M13 | GND |
| M14 | GND |
| M20 | V _{CCA} |
| M21 | I/O |
| M22 | I/O |
| M23 | V _{CCI} |
| N1 | I/O |
| N2 | I/O |
| N3 | I/O |
| N4 | I/O |
| N10 | GND |

| 329-Pin PBGA | |
|--------------|------------------|
| Pin Number | A545X32 Function |
| N11 | GND |
| N12 | GND |
| N13 | GND |
| N14 | GND |
| N20 | NC |
| N21 | I/O |
| N22 | I/O |
| N23 | I/O |
| P1 | I/O |
| P2 | I/O |
| P3 | I/O |
| P4 | I/O |
| P10 | GND |
| P11 | GND |
| P12 | GND |
| P13 | GND |
| P14 | GND |
| P20 | I/O |
| P21 | I/O |
| P22 | I/O |
| P23 | I/O |
| R1 | I/O |
| R2 | I/O |
| R3 | I/O |
| R4 | I/O |
| R20 | I/O |
| R21 | I/O |
| R22 | I/O |
| R23 | I/O |
| T1 | I/O |
| T2 | I/O |
| T3 | I/O |
| T4 | I/O |
| T20 | I/O |
| T21 | I/O |

| 329-Pin PBGA | |
|--------------|------------------|
| Pin Number | A54SX32 Function |
| T22 | I/O |
| T23 | I/O |
| U1 | I/O |
| U2 | I/O |
| U3 | V _{CCA} |
| U4 | I/O |
| U20 | I/O |
| U21 | V _{CCA} |
| U22 | I/O |
| U23 | I/O |
| V1 | V _{CCI} |
| V2 | I/O |
| V3 | I/O |

| 329-Pin PBGA | |
|--------------|------------------|
| Pin Number | A54SX32 Function |
| V4 | I/O |
| V20 | I/O |
| V21 | I/O |
| V22 | I/O |
| V23 | I/O |
| W1 | I/O |
| W2 | I/O |
| W3 | I/O |
| W4 | I/O |
| W20 | I/O |
| W21 | I/O |
| W22 | I/O |

| 329-Pin PBGA | |
|--------------|------------------|
| Pin Number | A54SX32 Function |
| W23 | NC |
| Y1 | NC |
| Y2 | I/O |
| Y3 | I/O |
| Y4 | GND |
| Y5 | I/O |
| Y6 | I/O |
| Y7 | I/O |
| Y8 | I/O |
| Y9 | I/O |
| Y10 | I/O |
| Y11 | I/O |

| 329-Pin PBGA | |
|--------------|------------------|
| Pin Number | A54SX32 Function |
| Y12 | V _{CCA} |
| Y13 | V _{CCR} |
| Y14 | I/O |
| Y15 | I/O |
| Y16 | I/O |
| Y17 | I/O |
| Y18 | I/O |
| Y19 | I/O |
| Y20 | GND |
| Y21 | I/O |
| Y22 | I/O |
| Y23 | I/O |

144-Pin FBGA

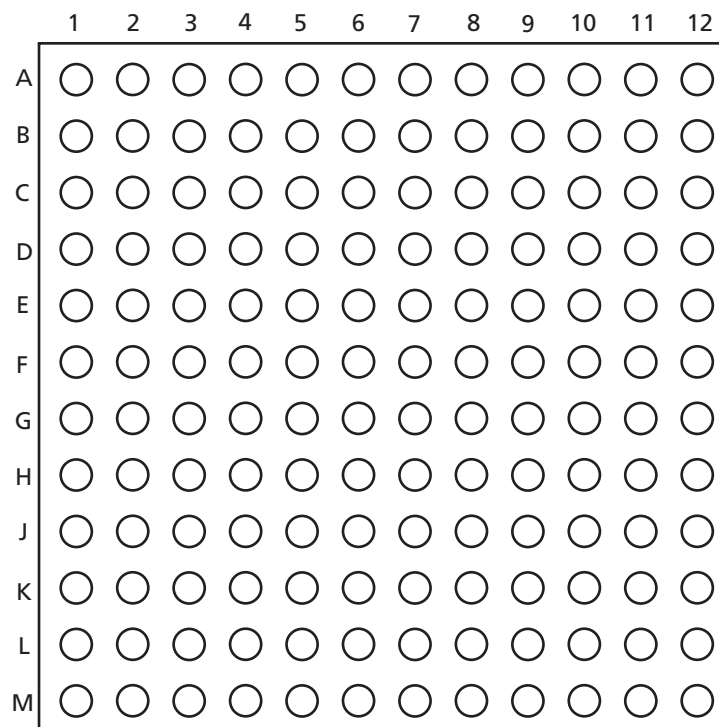


Figure 2-8 • 144-Pin FBGA (Top View)

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at <http://www.actel.com/products/rescenter/package/index.html>.

| 144-Pin FBGA | |
|--------------|------------------|
| Pin Number | A54SX08 Function |
| A1 | I/O |
| A2 | I/O |
| A3 | I/O |
| A4 | I/O |
| A5 | V _{CCA} |
| A6 | GND |
| A7 | CLKA |
| A8 | I/O |
| A9 | I/O |
| A10 | I/O |
| A11 | I/O |
| A12 | I/O |
| B1 | I/O |
| B2 | GND |
| B3 | I/O |
| B4 | I/O |
| B5 | I/O |
| B6 | I/O |
| B7 | CLKB |
| B8 | I/O |
| B9 | I/O |
| B10 | I/O |
| B11 | GND |
| B12 | I/O |
| C1 | I/O |
| C2 | I/O |
| C3 | TCK, I/O |
| C4 | I/O |
| C5 | I/O |
| C6 | PRA, I/O |
| C7 | I/O |
| C8 | I/O |
| C9 | I/O |
| C10 | I/O |
| C11 | I/O |
| C12 | I/O |

| 144-Pin FBGA | |
|--------------|------------------|
| Pin Number | A54SX08 Function |
| D1 | I/O |
| D2 | V _{CCI} |
| D3 | TDI, I/O |
| D4 | I/O |
| D5 | I/O |
| D6 | I/O |
| D7 | I/O |
| D8 | I/O |
| D9 | I/O |
| D10 | I/O |
| D11 | I/O |
| D12 | I/O |
| E1 | I/O |
| E2 | I/O |
| E3 | I/O |
| E4 | I/O |
| E5 | TMS |
| E6 | V _{CCI} |
| E7 | V _{CCI} |
| E8 | V _{CCI} |
| E9 | V _{CCA} |
| E10 | I/O |
| E11 | GND |
| E12 | I/O |
| F1 | I/O |
| F2 | I/O |
| F3 | V _{CCR} |
| F4 | I/O |
| F5 | GND |
| F6 | GND |
| F7 | GND |
| F8 | V _{CCI} |
| F9 | I/O |
| F10 | GND |
| F11 | I/O |
| F12 | I/O |

| 144-Pin FBGA | |
|--------------|------------------|
| Pin Number | A54SX08 Function |
| G1 | I/O |
| G2 | GND |
| G3 | I/O |
| G4 | I/O |
| G5 | GND |
| G6 | GND |
| G7 | GND |
| G8 | V _{CCI} |
| G9 | I/O |
| G10 | I/O |
| G11 | I/O |
| G12 | I/O |
| H1 | I/O |
| H2 | I/O |
| H3 | I/O |
| H4 | I/O |
| H5 | V _{CCA} |
| H6 | V _{CCA} |
| H7 | V _{CCI} |
| H8 | V _{CCI} |
| H9 | V _{CCA} |
| H10 | I/O |
| H11 | I/O |
| H12 | V _{CCR} |
| J1 | I/O |
| J2 | I/O |
| J3 | I/O |
| J4 | I/O |
| J5 | I/O |
| J6 | PRB, I/O |
| J7 | I/O |
| J8 | I/O |
| J9 | I/O |
| J10 | I/O |
| J11 | I/O |
| J12 | V _{CCA} |

| 144-Pin FBGA | |
|--------------|------------------|
| Pin Number | A54SX08 Function |
| K1 | I/O |
| K2 | I/O |
| K3 | I/O |
| K4 | I/O |
| K5 | I/O |
| K6 | I/O |
| K7 | GND |
| K8 | I/O |
| K9 | I/O |
| K10 | GND |
| K11 | I/O |
| K12 | I/O |
| L1 | GND |
| L2 | I/O |
| L3 | I/O |
| L4 | I/O |
| L5 | I/O |
| L6 | I/O |
| L7 | HCLK |
| L8 | I/O |
| L9 | I/O |
| L10 | I/O |
| L11 | I/O |
| L12 | I/O |
| M1 | I/O |
| M2 | I/O |
| M3 | I/O |
| M4 | I/O |
| M5 | I/O |
| M6 | I/O |
| M7 | V _{CCA} |
| M8 | I/O |
| M9 | I/O |
| M10 | I/O |
| M11 | TDO, I/O |
| M12 | I/O |

Datasheet Information

List of Changes

The following table lists critical changes that were made in the current version of the document.

| Previous Version | Changes in Current Version (v3.2) | Page |
|---------------------|--|------|
| v3.1 (June 2003) | The "Ordering Information" was updated to include RoHS information. | 1-ii |
| | The Product Plan was removed since all products have been released. | N/A |
| | Information concerning the TRST pin in the "Probe Circuit Control Pins" section was removed. | 1-6 |
| | The "Dedicated Test Mode" section is new. | 1-6 |
| | The "Programming" section is new. | 1-7 |
| | A note was added to the "Power-Up Sequencing" table. | 1-15 |
| | A note was added to the "Power-Down Sequencing" table. The 3.3 V comments were updated for the following devices: A545X08, A545X16, A545X32. | 1-15 |
| v3.0.1 | U11 and U13 were added to the "313-Pin PBGA" table. | 2-17 |
| | Storage temperature in Table 1-3 was updated. | 1-7 |
| | Table 1-1 was updated. | 1-5 |

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In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," "Production," and "Datasheet Supplement." The definitions of these categories are as follows:

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Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

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