dsPIC33EP256MC506 Plug-In Module (PIM) Information Sheet for Internal Op amp Configuration

The dsPIC33EP256MC506 Internal Op amp Motor Control PIM is designed to demonstrate the capabilities of the dsPIC33EP256MC506 Motor Control device using internal op amps with development boards such as the dsPICDEM™ MCLV-2 Development Board (DM330021-2) and the dsPICDEM MCHV-2 Development board (DM330023-2), which support 100-pin PIM interfaces.

The dsPIC33EP256MC506 is a high-performance, 16-bit Digital Signal Controller (DSC) in a 64-pin TQFP package. This device is equipped with three internal Op amp/Comparators and one dedicated Analog Comparator. The dsPIC33EP256MC506 Internal Op amp Motor Control PIM takes advantage of these analog peripherals configured using on-board passive components (resistors and capacitors) to support motor control applications without requiring external op amps or comparators.

To operate this PIM with the dsPICDEM MCLV-2 and dsPICDEM MCHV-2 Development Boards, please insert the Internal Op amp Configuration Board into the header J4 (for the dsPICDEM MCHV-2 Development Board) or header J14 (for the dsPICDEM MCLV-2 Development Board).

Figure 1 shows the connection location for the dsPICDEM MCHV-2 Development Board.

FIGURE 1: INTERNAL OP AMP CONFIGURATION BOARD

Hardware Compatibility

Table 1 provides information on the hardware versions of the motor control boards that are compatible with this PIM. Refer to the user's guide for the specific motor control board for hardware version identification information.

TABLE 1: HARDWARE COMPATIBILITY

Development Board	Part Number	Compatible Hardware Version(s)
dsPICDEM™ MCHV Development Board	DM330023	Not compatible
dsPICDEM™ MCLV Development Board	DM330021	Not compatible
dsPICDEM™ MCSM Development Board	DM330022	Not compatible
dsPICDEM™ MCHV-2 Development Board	DM330023-2	All revisions
dsPICDEM™ MCLV-2 Development Board	DM330021-2	All revisions

Warning:

Do not connect non-isolated oscilloscope probes to the test points on the dsPIC33EP256MC506 Internal Op amp Motor Control PIM while using the PIM with the dsPICDEM™ MCHV-2 Development Board. Use a high voltage differential probe rated in excess of 600 V_{RMS} (common mode). Failure to heed this warning could result in hardware damage.

Table 2 provides the static mapping between the 100-pin PIM pins and the device pins.

TABLE 2: 64-PIN DEVICE TO 100-PIN PIM MAPPING

Device Pin #	dsPIC33EP256MC506 Device Functional Description	PIM Pin #	PIM Functional Description
1	TDI/RA7	—	Not connected
2	RPI46/PWM1H/T3CK/RB14	94	PWM Out – H1
3	RPI47/PWM1L/T5CK/RB15	93	PWM Out – L1
4	RP118/RG6	84	Switch/UART TX
5	RPI119/RG7	83	Switch
6	RP120/RG8	76	HALLB/QEB/USB TX
7	$\overline{\text{MCLR}}$	13	Device Master Clear
8	RPI121/RG9	72	HALLA/QEA/USB RX
9	VSS	15, 36, 45, 65, 75	N/A
10	VDD	2, 16, 37, 46, 62, 86	N/A
11	AN10/RPI28/RA12	35	DC_BUS voltage (scaled)
12	AN9/RPI27/RA11	25	IA/IPFC current
13	AN0/OA2OUT/RA0	42	V_M2 motor phase voltage
14	AN1/C2IN1+/RA1	22, 41	QEA/IA/V_M1/POT
15	PGED3/VREF-/AN2/C2IN1-/SS1/RPI32/CTED2/RB0	43	V_M3/IBUS/HALLC
16	PGEC3/VREF+/AN3/OA1OUT/RPI33/CTED1/RB1	59	Op amp 1 output
17	PGEC1/AN4/C1IN1+/RPI34/RB2	21	QEB/IB/V_M2
18	PGED1/AN5/C1IN1-/RP35/RB3	—	Used by Op amp circuit
19	AVDD	30	N/A
20	AVSS	31	N/A
21	AN6/OA3OUT/C4IN1+/OCFB/RC0	58	Op amp 3 output
22	AN7/C3IN1-/C4IN1-/RC1	—	Used by Op amp circuit
23	AN8/C3IN1+/U1RTS/BCLK1/FLT3/RC2	20	INDX/POT/V_M3
24	AN11/C1IN2-/U1CTS/FLT4/RC11	24	IB/POT
25	VSS	15, 36, 45, 65, 75	N/A
26	VDD	2, 16, 37, 46, 62, 86	N/A
27	AN12/C2IN2-/U2RTS/BCLK2/RE12	—	Reconstructed motor neutral input
28	AN13/C3IN2-/U2CTS/RE13	32, 33	Potentiometer
29	AN14/RPI94/RE14	23	IBUS / VBUS
30	AN15/RPI95/RE15	34	General purpose I/O
31	SDA2/RPI24/RA8	80	HALLA/QEA
32	FLT32/SCL2/RP36/RB4	18	Overcurrent Fault input
33	CVREF2O/SDO1/RP20/T1CK/RA4	—	Used by Op amp circuit
34	SDI1/RPI25/RA9	77	HALLC/INDX/STP_PWM
35	SCK1/RPI51/RC3	79	AC input zero cross
36	SDA1/RPI52/RC4	69	LIN Fault
37	SCL1/RPI53/RC5	49	UART RX
38	VDD	2, 16, 37, 46, 62, 86	N/A
39	OSC1/CLKI/RC12	63	OSCI
40	OSC2/CLKO/RC15	64	OSCO
41	VSS	15, 36, 45, 65, 75	N/A
42	RD8	—	Debug test point
43	PGED2/ASDA2/RP37/RB5	27	PGED2
44	PGEC2/ASCL2/RP38/RB6	26	PGEC2
45	RPI58/RC10	61	HOME signal (QEI)
46	RP39/INT0/RB7	19	PFC Fault/UART TX
47	RC13	82	General purpose I/O
48	TCK/CVREF1O/ASCL1/RP40/T4CK/RB8	68	BTN/LINCS
49	TMS/ASDA1/RP41/RB9	78	PFC PWM/CAN RX
50	RP54/RC6	47	HALLB/QEB
51	RP55/RC7	70	BTN/RX
52	RP56/RC8	88	CAN TX
53	RD5	60	Debug LED2
54	RD6	1	Debug LED1
55	RP57/RC9	87	CAN RX
56	VCAP	—	Not connected
57	VDD	2, 16, 37, 46, 62, 86	N/A
58	RPI96/RF0	48	HALLC/INDX
59	RP97/RF1	50	UART TX
60	RP42/PWM3H/RB10	3	PWM Out – H3
61	RP43/PWM3L/RB11	100	PWM Out – L3
62	RPI44/PWM2H/RB12	99	PWM Out – H2
63	RPI45/PWM2L/CTPLS/RB13	98	PWM Out – L2
64	TDO/RA10	—	Not connected

FIGURE 2: 100-PIN HEADER SCHEMATIC

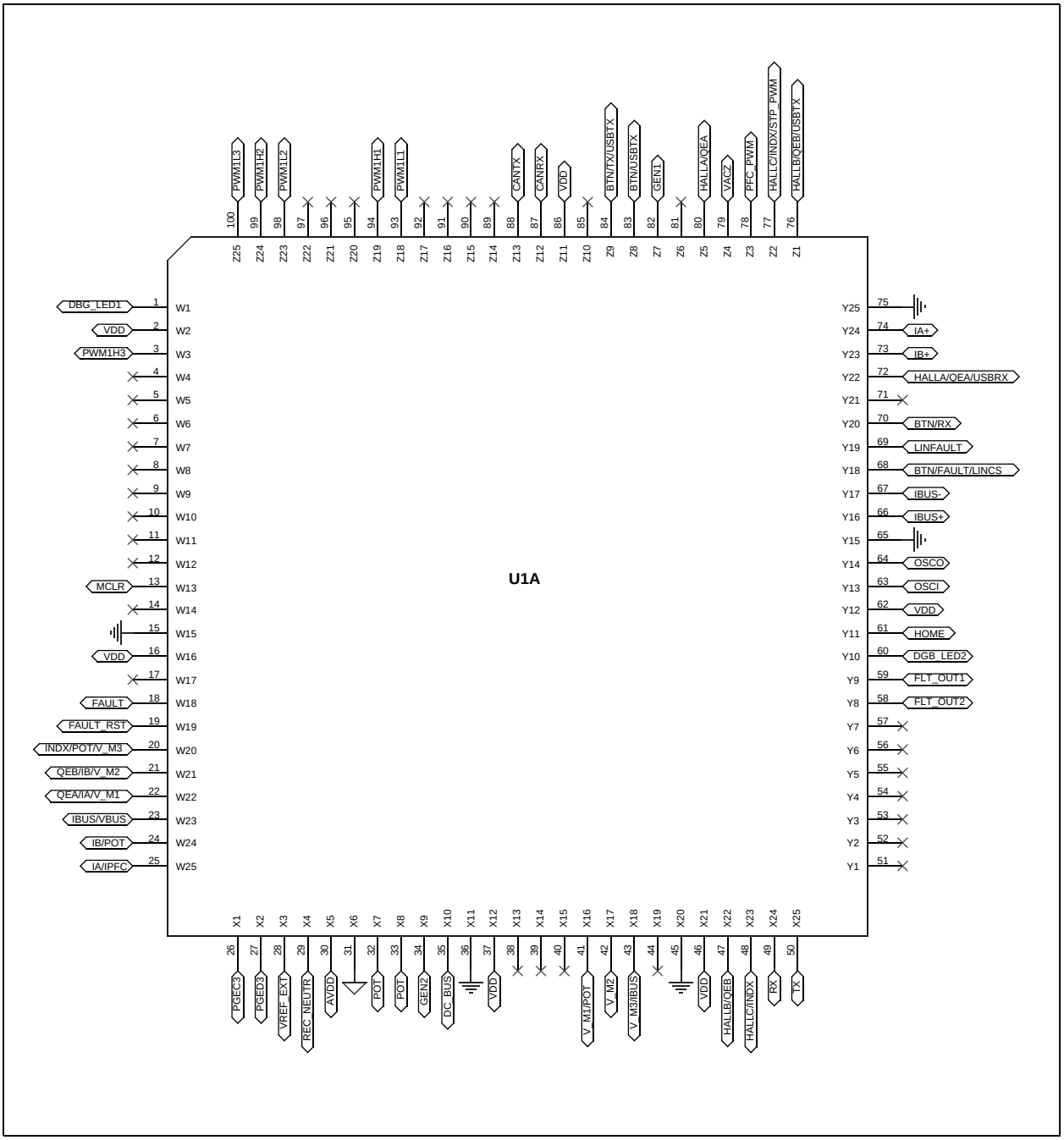
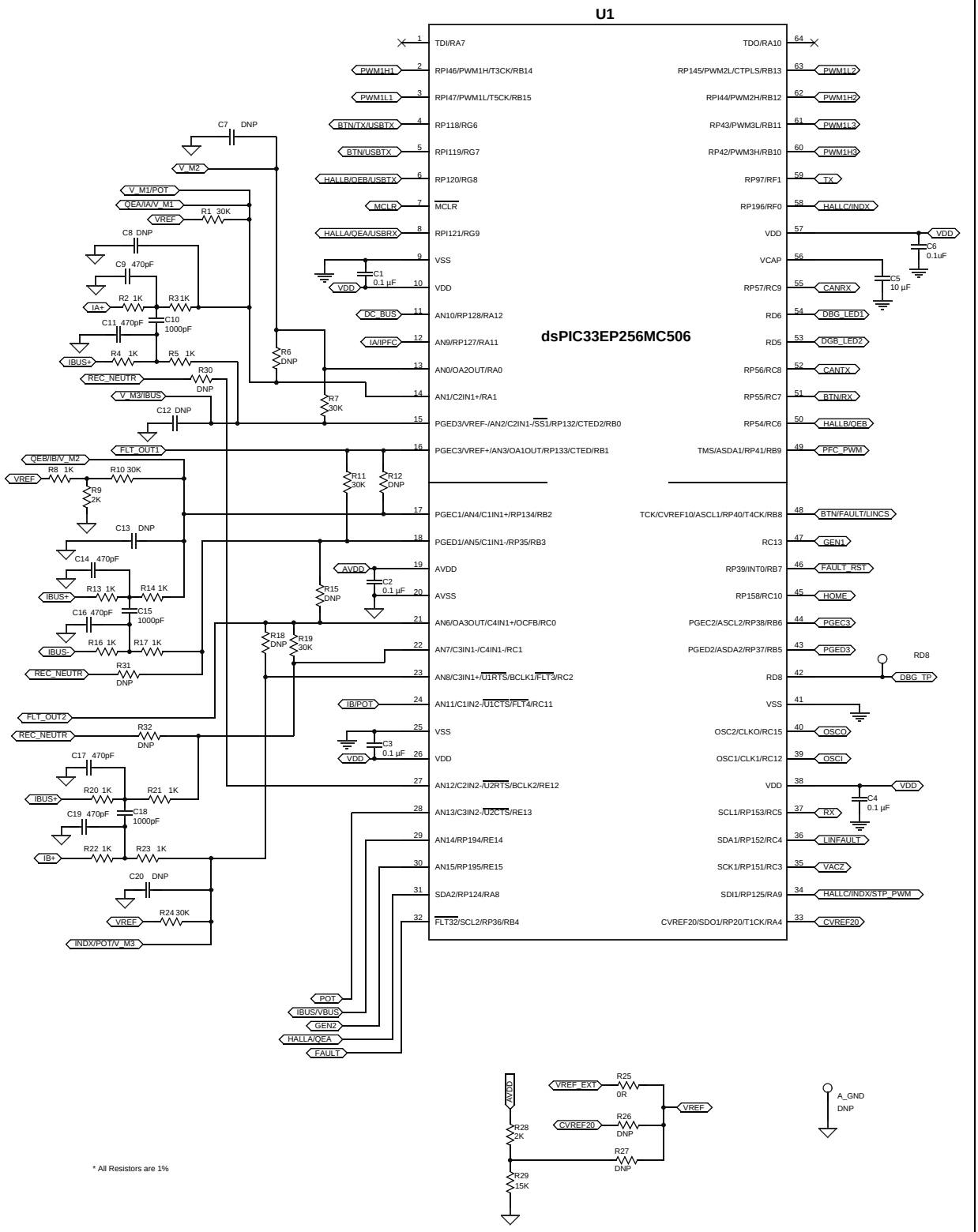


FIGURE 3: 64-PIN DEVICE SCHEMATIC



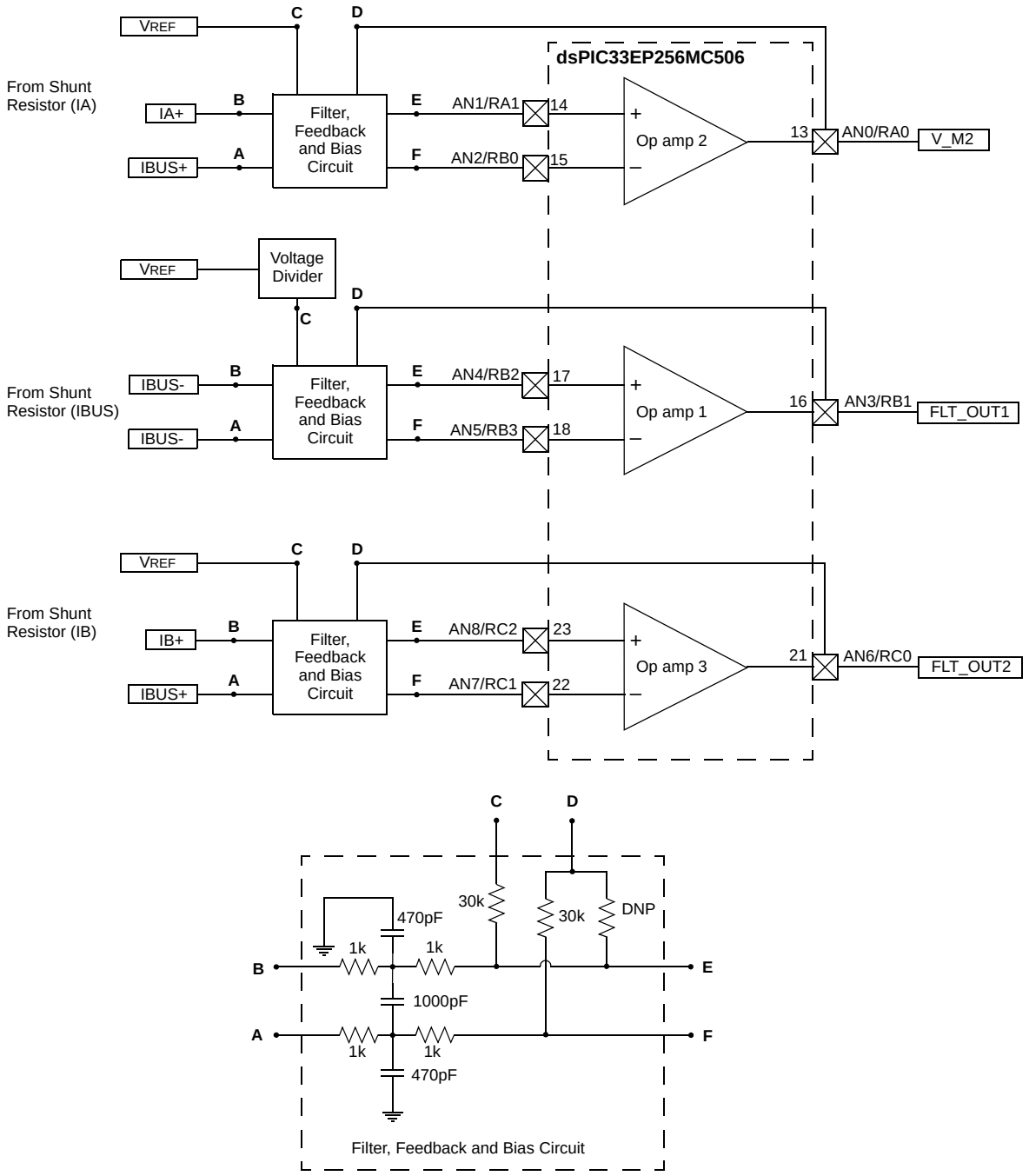
In the schematic shown in Figure 3, resistors R25, R26 and R27 are used to choose the reference voltage (V_{REF}) from motor control board (VREF_EXT) or device internal reference (CVREF20) or a simple voltage divider (R28-R29), respectively. By default, the PIM is configured to source the reference voltage from the motor control board.

Table 3 classifies the passive components according to their functionality and also quotes the design equations applicable in each case.

TABLE 3: ANALOG FUNCTIONALITY LISTING

Op amp #	Analog Function	Passive Components	Design Equations
1	Low Pass Filter	R13, R14, R16, R17, C14, C15, C16	$R13 = R14 = R16 = R17 = R$ $C14 = C16 = C$ $R10 = R11$ $Common\ mode\ f_{-3dB} \cong \frac{1}{2\pi RC}$ $Differential\ mode\ f_{-3dB} \cong \frac{1}{2\pi(2R)\left(\frac{C}{2} + C_{15}\right)}$ $DifferentialAmplifierGain = \frac{R_{11}}{2R}$
	Reference Voltage Bias	R10, R11	
	Voltage Divider	R8, R9	
	Differential Amplifier Input	R13, R14, R16, R17	
	Differential Amplifier Feedback	R11	
2	Low Pass Filter	R2, R3, R4, R5, C9, C10, C11	$R2 = R3 = R4 = R5 = R$ $C9 = C11 = C$ $R1 = R7$ $Common\ mode\ f_{-3dB} \cong \frac{1}{2\pi RC}$ $Differential\ mode\ f_{-3dB} \cong \frac{1}{2\pi(2R)\left(\frac{C}{2} + C_{10}\right)}$ $DifferentialAmplifierGain = \frac{R_7}{2R}$
	Reference Voltage Bias	R1, R7	
	Differential Amplifier Input	R2, R3, R4, R5	
	Differential Amplifier Feedback	R7	
3	Low Pass Filter	R20, R21, R22, R23, C17, C18, C19	$R20 = R21 = R22 = R23 = R$ $C17 = C19 = C$ $R24 = R19$ $Common\ mode\ f_{-3dB} \cong \frac{1}{2\pi RC}$ $Differential\ mode\ f_{-3dB} \cong \frac{1}{2\pi(2R)\left(\frac{C}{2} + C_{18}\right)}$ $DifferentialAmplifierGain = \frac{R_{19}}{2R}$
	Reference Voltage Bias	R24, R19	
	Differential Amplifier Input	R20, R21, R22, R23	
	Differential Amplifier Feedback	R19	

FIGURE 4: OP AMP CIRCUIT BLOCK DIAGRAM



$$\textit{Differential Amplifier Gain} = \frac{30k\Omega}{2 \times 1k\Omega} = 15$$

$$\textit{Differential mode } f_{-3dB} \cong \frac{1}{2\pi(2 \times 1k\Omega)\left(\frac{470pF}{2} + 1000pF\right)} \cong 65kHz$$

$$\textit{Common mode } f_{-3dB} \cong \frac{1}{2\pi(1k\Omega)(470pF)} \cong 340kHz$$

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