19-3172; Rev 0; 2/04

MAXIM

±15kV ESD-Protected USB Transceiver in UCSP

General Description

The MAX3346E bidirectional transceiver converts logic-level signals to USB signals, and USB signals to logic-level signals. The MAX3346E includes the 1.5kΩ USB pullup resistor internally, and supports both full-speed (12Mbps) and low-speed (1.5Mbps) USB operation. The device has built-in ±15kV ESD protection circuitry to guard the USB I/O pins, D+ and D-.

The MAX3346E operates with V_L voltages as low as 1.65V, ensuring compatibility with low-voltage ASICs. The device features a logic-selectable suspend mode that lowers current draw to less than 40µA. The MAX3346E has an enumerate function that allows devices to logically disconnect while plugged in. The MAX3346E is fully compliant with USB specification 1.1, and the full-speed and low-speed operation under USB specification 2.0.

The MAX3346E is available in the miniature 4 x 4 chip-scale package (UCSP™), as well as the small 14-pin TSSOP, and is rated for the -40°C to +85°C extended temperature range.

Applications

Cell Phones

PC Peripherals

Data Cradles

PDAs

MP3 Players

UCSP is trademark of Maxim Integrated Products, Inc.

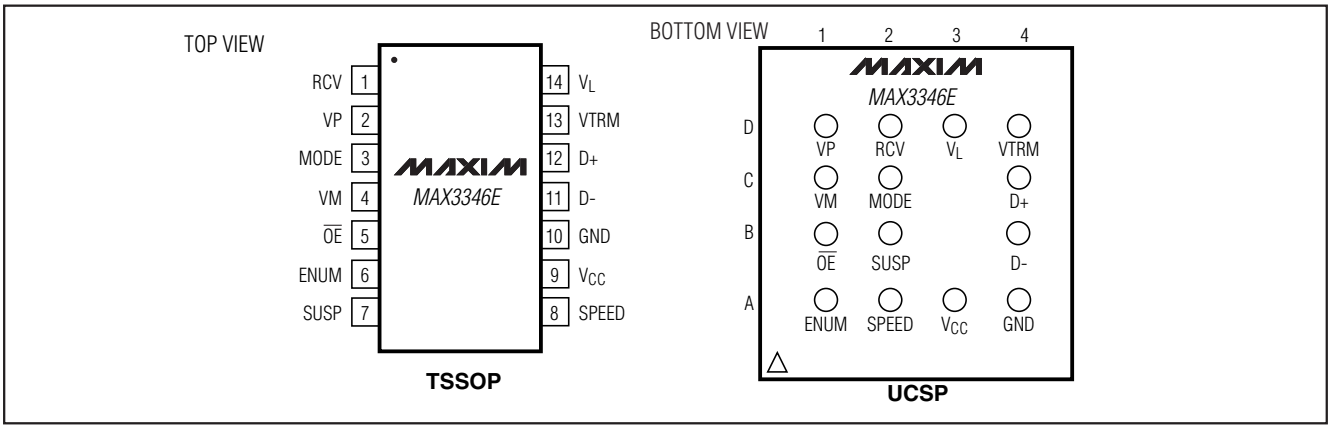
Features

- **±15kV ESD Protection on D+ and D-**
- **Internal Linear Regulator Allows Direct Powering from the USB Cable**
- **Internal 1.5kΩ Pullup Resistor for Low/Full-Speed Operation**
- **Supports Low-Speed and Full-Speed USB Communications**
- **Complies with USB Specification Revision 1.1 and 2.0 (Low Speed and Full Speed)**
- **Three-State Outputs**
- **Enumerate Input—Allows USB Connection through Software**
- **No Power-Supply Sequencing Required**
- **Operates with V_L of 1.65V to 3.6V, Ensuring Compatibility with Low-Voltage ASICs**
- **Available in Miniature Chip-Scale Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3346EEUD	-40°C to +85°C	14 TSSOP
MAX3346EEBE-T	-40°C to +85°C	4 x 4 UCSP

Pin Configurations



ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND, unless otherwise noted.)

Supply Voltage (V_{CC}) .....-0.3V to +6V
Output of Internal Regulator (VTRM).....-0.3V to (V_{CC} + 0.3V)
Input Voltage (D+, D-) .....-0.3V to +6V
System Supply Voltage (V_L) .....-0.3V to +6V
RCV, SUSP, VM, VP, MODE,
$\overline{OE}$, SPEED, ENUM .....-0.3V to (V_L + 0.3V)
Short-Circuit Current (D+, D-)
to V_{CC} or GND (Note 1) .....Continuous
Maximum Continuous Current (all other pins).....±15mA

Continuous Power Dissipation (T_A = +70°C)
4 x 4 UCSP (derate 7.4mW/°C above +70°C).....589mW [B16-2]
14-Pin TSSOP (derate 9.1mW/°C above +70°C)..727mW [U14-1]
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Bump Temperature (soldering) Reflow.....+235°C

Note 1: External 23.7Ω resistors connected to D+ and D-.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +4V to +5.5V, GND = 0, VTRM = +3.0V to +3.6V, V_L = +1.65V to +3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V, V_L = +2.5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY INPUTS (V_{CC}, VTRM, V_L)						
Regulated Supply Voltage	V_{VTRM}	Internal regulator	3.0	3.3	3.6	V
V_L Input Range			1.65		3.60	V
V_{CC} Input Range			4.0		5.5	V
Operating V_{CC} Supply Current	I_{VCC}	Full-speed transmitting/receiving at 12Mbps, C_L = 50pF on D+ and D-			8	mA
Operating V_L Supply Current	I_{VL}	Full-speed transmitting/receiving at 12Mbps			6	mA
Full-Speed Idle and SE0 Supply Current	$I_{VCC(IDLE)}$	Full-speed idle: V_{D+} > 2.7V, V_{D-} < 0.3V		340	450	µA
		SE0: V_{D+} < 0.3V, V_{D-} < 0.3V		390	500	
Static V_L Supply Current	$I_{VL(STATIC)}$	Full-speed idle, SE0, or suspend mode			5	µA
Suspend Supply Current	$I_{VCC(SUSP)}$	SUSP = $\overline{OE}$ = high			40	µA
Disable-Mode Supply Current	$I_{VCC(DIS)}$	V_L = GND or open			20	µA
D+/D- Disable-Mode Load Current	$I_{D\_(DIS)}$	V_L = GND or open, $V_{D\_}$ = 0 or +5.5V			5	µA
Sharing-Mode V_L Supply Current	$I_{VL(SHARING)}$	V_{CC} = GND or open, $\overline{OE}$ = low, SUSP = high			20	µA
D+/D- Sharing-Mode Load Current	$I_{D\_(SHARING)}$	V_{CC} = GND or open, $V_{D\_}$ = 0 or +5.5V			20	µA
LINEAR REGULATOR						
External Capacitor	C_{OUT}	Compensation of linear regulator	1			µF

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +4V to +5.5V, GND = 0, VTRM = +3.0V to +3.6V, V_L = +1.65V to +3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V, V_L = +2.5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ESD PROTECTION (D+, D-)						
Human Body Model				±15		kV
IEC 1000-4-2 Air-Gap Discharge				±10		kV
IEC 1000-4-2 Contact Discharge				±8		kV
LOGIC-SIDE I/O						
Input High Voltage	V_{IH}	VP, VM, SUSP, SPEED, $\overline{OE}$, MODE, ENUM	(2/3) x V_L			V
Input Low Voltage	V_{IL}	VP, VM, SUSP, SPEED, $\overline{OE}$, MODE, ENUM			0.4	V
Output High Voltage	V_{OH}	I_{SOURCE} = +2mA, RCV, VP, VM	V_L - 0.4			V
Output Low Voltage	V_{OL}	I_{SINK} = -2mA, RCV, VP, VM			0.4	V
Input Leakage Current		VP, VM, SUSP, ENUM, $\overline{OE}$, MODE = 0 or V_L			±1	µA
USB-SIDE I/O						
Output-Voltage Low	V_{OLD}	R_L = 1.5kΩ from D+ or D- to 3.6V			0.3	V
Output-Voltage High	V_{OHD}	R_L = 15kΩ from D+ and D- to GND	2.8		3.6	V
Input Impedance	Z_{IN}	$V_{D\_}$ = 0 or +3.6V, ENUM = 0, three-state driver	1			MΩ
Single-Ended Input-Voltage High	V_{IH}		2.0			V
Single-Ended Input-Voltage Low	V_{IL}				0.8	V
D+, D- Receiver Hysteresis				200		mV
Driver Output Impedance	R_{OUT}		4.6		16.0	Ω
Internal Resistor	R_{PULLUP}		1.410	1.5	1.540	kΩ
Input Common-Mode Voltage			0.8		2.5	V
Differential Input Sensitivity			200			mV

TIMING CHARACTERISTICS

(V_{CC} = +4V to +5.5V, GND = 0, VTRM = +3.0V to +3.6V, V_L = +1.65V to +3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V, V_L = +2.5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SPEED INDEPENDENT TIMING CHARACTERISTICS						
$\overline{OE}$ to VP/VM Three-State Delay Disable Time	t_{PVZ}	Figures 1a and 4a			20	ns
$\overline{OE}$ to VP/VM Delay Enable Time	t_{PZV}	Figures 1a and 4a			25	ns
D+/D- to RCV Propagation Delay	t_{PLH}	C_L = 25pF, Figures 4b and 5			18	ns
D+/D- to RCV Propagation Delay	t_{PHL}	C_L = 25pF, Figures 4b and 5			18	ns

TIMING CHARACTERISTICS (continued)

(V_{CC} = +4V to +5.5V, GND = 0, VTRM = +3.0V to 3.6V, V_L = +1.65V to +3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V, V_L = +2.5V, T_A = +25°C.) (Note 2)

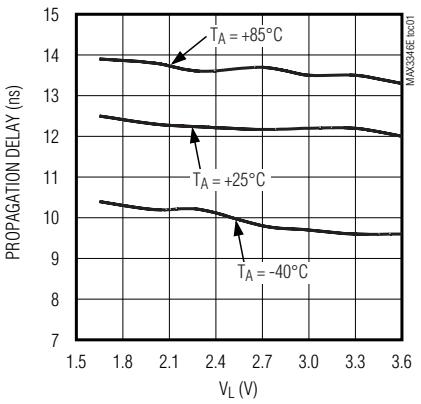
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
D+/D- to VP/VM Propagation Delay	t_{PLH}	C_L = 25pF, Figures 4b and 5			18	ns
	t_{PHL}	C_L = 25pF, Figures 4b and 5			18	
FULL-SPEED TIMING CHARACTERISTICS						
$\overline{OE}$ to Transmit Delay Enable Time	t_{PZD}	(Figures 1b, 4d)			20	ns
$\overline{OE}$ to Driver Three-State Delay Disable Time	t_{PDZ}	(Figures1b, 4d)			20	ns
VP/VM to D+/D- Propagation Delay (MODE = 1)	t_{PLH}	(Figures 3, 4c)			18	ns
	t_{PHL}	(Figures 3, 4c)			18	
VP to D+/D- Propagation Delay (MODE = 0)	t_{PHL0}	C_L = 50pF (Figures 2, 4c)			20	ns
	t_{PLH0}	C_L = 50pF (Figures 2, 4c)			20	
D+, D- Rise Time	t_R	C_L = 50pF, 10% to 90% of $\lvert V_{OH} - V_{OL} \rvert$	4		20	ns
D+, D- Fall Time	t_F	C_L = 50pF, 90% to 10% of $\lvert V_{OH} - V_{OL} \rvert$	4		20	ns
Rise- and Fall-Time Matching (Note 3)	t_R/t_F	C_L = 50pF	90		110	%
Output-Signal Crossover Voltage (Note 3)	V_{CRS}	C_L = 50pF	1.3		2.0	V
LOW-SPEED TIMING CHARACTERISTICS						
VP/VM to D+/D- Propagation Delay (MODE = 1)	t_{PLH}	Figures 3 and 4c, C_L = 50pF to 600pF	30		250	ns
	t_{PHL}	Figures 3 and 4c, C_L = 50pF to 600pF	30		250	
VP to D+/D- Propagation Delay (MODE = 0)	t_{PHL0}	Figures 2 and 4c, C_L = 50pF to 600pF	30		250	ns
	t_{PLH0}	Figures 2 and 4c, C_L = 50pF to 600pF	30		250	
D+/D- Rise Time	t_R	C_L = 50pF to 600pF	75		300	ns
D+/D- Fall Time	t_F	C_L = 50pF to 600pF	75		300	ns
Rise- and Fall-Time Matching	t_R/t_F	C_L = 50pF to 600pF	80		125	%
Output-Signal Crossover Voltage	V_{CRS}	C_L = 50pF to 600pF	1.3		2.0	V

Note 2: Parameters are 100% production tested at +25°C, limits over temperature are guaranteed by design.
Note 3: Guaranteed by design, not production tested.

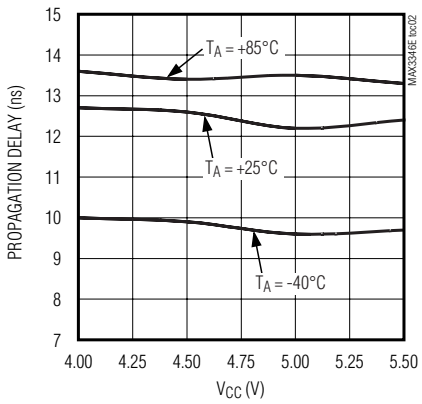
Typical Operating Characteristics

(V_{CC} = +5V, V_L =+3.3V, T_A = +25°C, unless otherwise noted.)

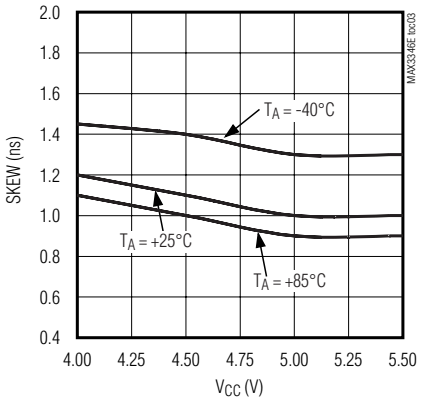
SINGLE-ENDED RECEIVER PROPAGATION DELAY vs. V_L



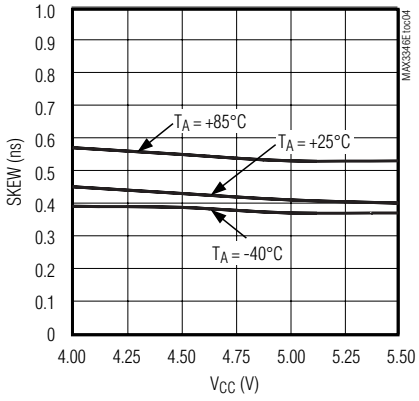
SINGLE-ENDED RECEIVER PROPAGATION DELAY vs. V_{CC}



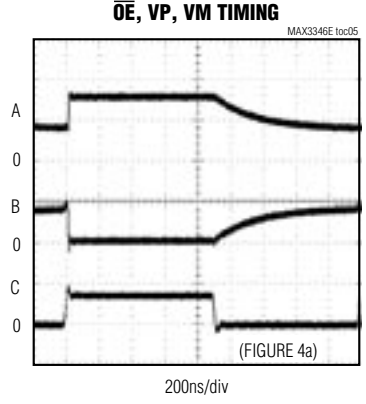
SKEW vs. V_{CC} (MODE 0, FULL SPEED)



SKEW vs. V_{CC} (MODE 0, LOW SPEED)

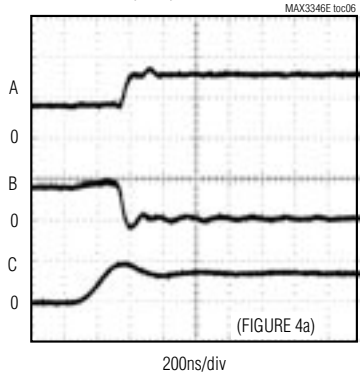


$\overline{OE}$, VP, VM TIMING



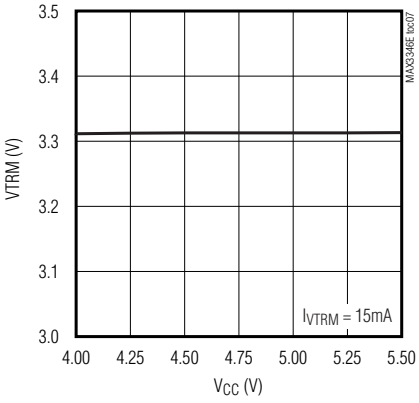
A: VP, 2V/div
B: VM, 2V/div
C: $\overline{OE}$, 5V/div

$\overline{OE}$, VP, VM TIMING



A: VP, 2V/div
B: VM, 2V/div
C: $\overline{OE}$, 5V/div

VTRM vs. V_{CC}

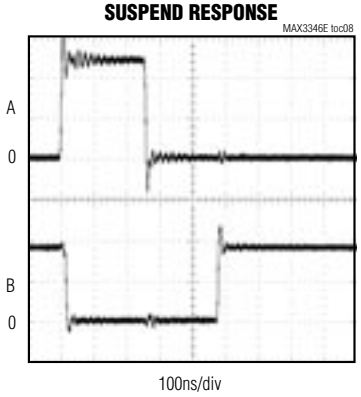


±15kV ESD-Protected USB Transceiver in UCSP

Typical Operating Characteristics (continued)

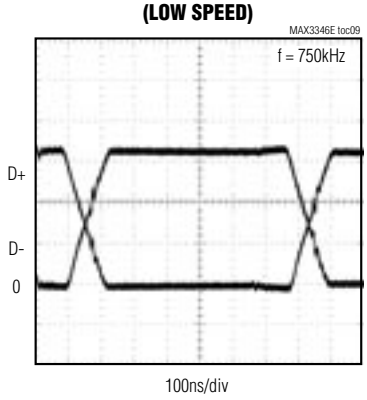
(V_{CC} = +5V, V_L = +3.3V, T_A = +25°C, unless otherwise noted.)

SUSPEND RESPONSE

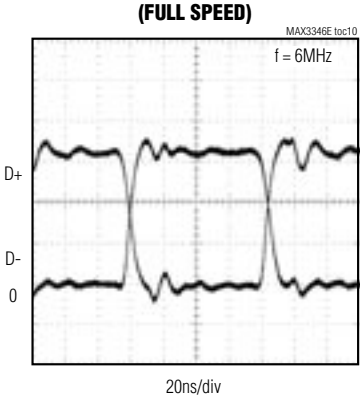


A: SUSP, 2V/div
B: RCV, 2V/div

RISE- AND FALL-TIME MATCHING (LOW SPEED)



RISE- AND FALL-TIME MATCHING (FULL SPEED)



Pin Description

PIN		NAME	INPUT/ OUTPUT	FUNCTION
TSSOP	UCSP			
1	D2	RCV	Output	Receiver Output. Single-ended CMOS output. RCV responds to the differential input on D+ and D- (see Table 3).
2	D1	VP	Input/ Output	System-Side Data Input/Output. Drive $\overline{OE}$ high to make VP a receiver output. Drive $\overline{OE}$ low to make VP a driver input (see Table 3).
3	C2	MODE	Input	Mode Control Input. Selects single-ended (mode zero) or differential (mode one) input for the system side when converting logic-level signals to USB-level signals. If MODE is forced high, mode one is selected. If MODE is forced low, mode zero is selected (see Table 3).
4	C1	VM	Input/ Output	System-Side Data Input/Output. Drive $\overline{OE}$ high to make VM a receiver output. Drive $\overline{OE}$ low to make VM a driver input (see Table 3).
5	B1	$\overline{OE}$	Input	Output Enable. Drive $\overline{OE}$ high to enable the receiver. Drive $\overline{OE}$ low to enable the driver input.
6	A1	ENUM	Input	Enumerate Input. Drive ENUM low to disconnect the internal 1.5kΩ resistor, and enumerate the USB. With ENUM high, the internal 1.5kΩ resistor is connected to either D+ or D-, depending on the state of SPEED.

Pin Description (continued)

PIN		NAME	INPUT/ OUTPUT	FUNCTION
TSSOP	UCSP			
7	B2	SUSP	Input	Suspend Input. Drive SUSP low for normal operation. Force SUSP high for low-power state. In low-power state RCV is low, D+/D- are high impedance if $\overline{OE}$ is floating, and VP/VM are active outputs.
8	A2	SPEED	Input	USB Transmission Speed Select Input. If SPEED is forced high, full speed (12Mbps) is selected and the internal 1.5kΩ pullup resistor is connected to D+. If SPEED is forced low, low speed (1.5Mbps) is selected and the internal 1.5kΩ pullup resistor is connected to D-.
9	A3	V_{CC}	Power	USB-Side Power-Supply Input. Connect V_{CC} to the incoming USB power supply. Bypass V_{CC} to GND with a 1µF ceramic capacitor.
10	A4	GND	Power	Ground
11	B4	D-	Input/ Output	USB Differential Data Input/Output. Connect to the USB's D- signal through a 24.3Ω ±1% resistor.
12	C4	D+	Input/ Output	USB Differential Data Input/Output. Connect to the USB's D+ signal through a 24.3Ω ±1% resistor.
13	D4	VTRM	Power	Regulated Output Voltage. 3.3V output derived from the V_{CC} input. Bypass VTRM to GND with a 1µF (or more) low-ESR capacitor, such as ceramic or plastic film types.
14	D3	V_L	Power	System-Side Power-Supply Input. Connect to the system's logic-level power supply, 1.65V to 3.6V. Bypass to GND with a 0.1µF capacitor.
—	B3, C3	—	—	Not populated. The solder sphere is omitted from these locations (see the *Package Information*).

Detailed Description

The MAX3346E is a bidirectional transceiver that converts single-ended or differential logic-level signals to differential USB signals, and converts differential USB signals to single-ended or differential logic-level signals. The MAX3346E includes an internal 1.5kΩ pullup resistor that can be connected to either D+ or D- for full-speed or low-speed operation (see the *Functional Diagram*). The MAX3346E can be energized without concern about power-supply sequencing. Additionally, the USB I/O, D+ and D-, are ESD protected to ±15kV. The MAX3346E can get its USB-side power, V_{CC}, directly from the USB connection, and can operate with system-side power, V_L, down to 1.65V and still meet the USB physical layer specifications. The MAX3346E supports both full-speed (12Mbps) and low-speed (1.5Mbps), USB specification 1.1 operation.

The MAX3346E has an enumerate feature that works when power is on. Driving ENUM low disconnects the internal 1.5kΩ pullup resistor from both D+ and D-, reenumerating the USB. This is useful if changes in communication protocol are required while power is applied, and while the USB cable is connected.

±15kV ESD-Protected USB Transceiver in UCSP

Applications Information

Power-Supply Configurations

Normal Operating Mode

Connect V_L and V_{CC} to system power supplies (Table 1). Connect V_L to a +1.65V to +3.6V supply. Connect V_{CC} to a +4.0V to +5.5V supply. Alternatively, the MAX3346E can derive power from a single Li+ battery. Connect the battery to V_{CC}. VTRM remains above +3.0V for V_{CC} as low as +3.1V.

Additionally, the MAX3346E can derive power from a 3.3V ±10% voltage regulator. Connect V_{CC} and VTRM to an external +3.3V voltage regulator.

Disable Mode

Connect V_{CC} to a system power supply and leave V_L unconnected or connect to GND. D+ and D- enter a tri-state mode and V_{CC} consumes less than 20µA of supply current. D+ and D- withstand external signals up to +5.5V in disable mode (Table 2).

Sharing Mode

Connect V_L to a system power supply and leave V_{CC} (or V_{CC} and V_{VTRM}) unconnected or connect to GND. D+ and D- enter a tri-state mode, allowing other circuitry to share the USB D+ and D- lines, and V_L consumes less than 20µA of supply current. D+ and D- withstand external signals up to +5.5V in sharing mode (Table 2).

Device Control

$\overline{OE}$

$\overline{OE}$ controls the direction of communication through the device. With $\overline{OE}$ low, the MAX3346E transfers data from the system side to the USB side. With $\overline{OE}$ high, the MAX3346E transfers data from the USB side to the system side.

ENUM

The MAX3346E allows software control of USB enumeration. USB specification 1.1 requires a 1.5kΩ pullup resistor to D+ or D- to set the transmission speed (see the *SPEED* section). Enumerating the USB requires removing the 1.5kΩ resistor from the circuit, and is accomplished with the MAX3346E by driving ENUM low. With ENUM high, the voltage at SPEED determines how the internal resistor is connected (see the *Functional Diagram*).

MODE

MODE is a control input that selects whether differential or single-ended logic signals are recognized by the system side of the MAX3346E (Table 3).

If MODE is forced high, differential input is selected. With differential input selected, outputs D+ and D- follow the differential inputs at VP and VM. If VP and VM are both forced low, an SE0 condition is forced on the USB.

Drive MODE and VM low for single-ended input mode. With single-ended input selected, the differential signal on D+ and D- is controlled by VP. If VM is high when MODE is low, D- and D+ are both low, forcing an SE0 condition.

Table 1. Power-Supply Configurations

V_{CC} (V)	VTRM (V)	V_L (V)	CONFIGURATION	NOTES
+4.0 to +5.5	+3.3 Output	+1.65 to +3.6	Normal mode	—
+3.1 to +4.5	+3.3 Output	+1.65 to +3.6	Battery supply	—
+3.0 to +3.6	+3.0 to +3.6 Input	+1.65 to +3.6	Voltage regulator supply	—
GND or floating	Output	+1.65 to +3.6	Sharing mode	Table 2
+3.0 to +5.5	Output	GND or floating	Disable mode	Table 2

Table 2. Disable-Mode and Sharing-Mode Configurations

INPUTS/OUTPUTS	DISABLE MODE	SHARING MODE
V_{CC}/VTRM	• +5V input/+3.3V output • +3.3V input/+3.3V output • +3.7V input/+3.3V output	Floating or connected to GND
V_L	Floating or connected to GND	+1.65V to +3.6V input
D+ and D-	High impedance	High impedance
SPEED, SUSP, $\overline{OE}$, ENUM	High impedance	High impedance

Timing Diagrams

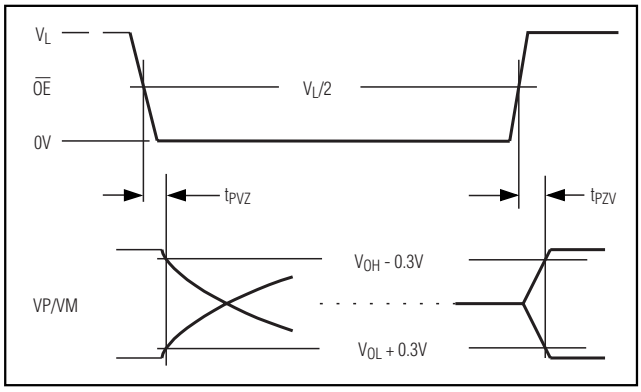


Figure 1a. Enable and Disable Timing, Receiver

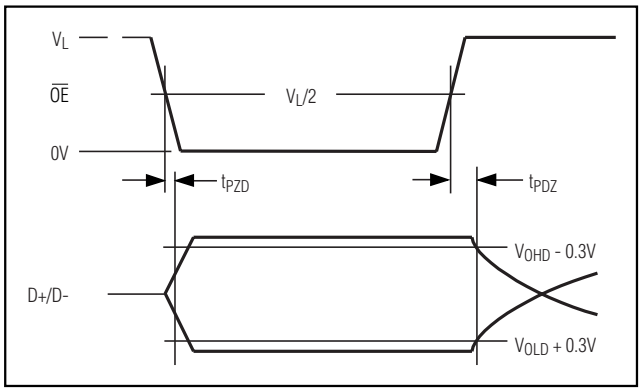


Figure 1b. Enable and Disable Timing, Transmitter

SUSP

SUSP, or suspend, is a control input. When SUSP is forced high the MAX3346E enters a low-power state. In this state, the quiescent supply current into V_{CC} is less than 40µA. In this mode, RCV is forced low, and D+ and D- are high-impedance inputs (Table 3d).

In suspend mode, data can only be transmitted with full-speed slope control.

SPEED

SPEED is a control input that selects between low-speed (1.5Mbps) and full-speed (12Mbps) USB transmission. Internally, it selects whether the 1.5kΩ pullup resistor is connected to D+ (full-speed) or D- (low-speed) (*Functional Diagram*). Force SPEED high to select full speed, or force SPEED low to select low speed.

VTRM

VTRM is the 3.3V output of the internal linear voltage regulator. The regulator is used to power the internal portions of the USB side of the MAX3346E. The VTRM

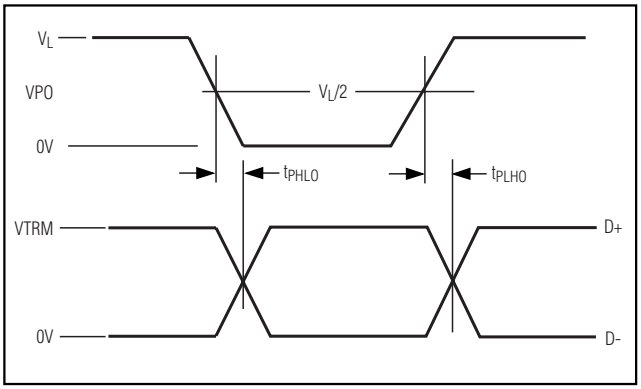


Figure 2. Mode 0 Timing

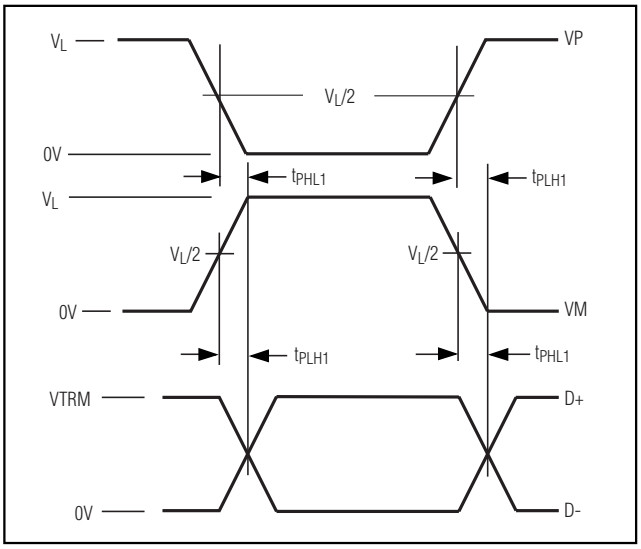


Figure 3. Mode 1 Timing

regulator's supply input is V_{CC}. Connect a 1.0µF (or greater) ceramic or plastic capacitor from VTRM to GND, as close to VTRM as possible. Do not use VTRM to provide power to external circuitry.

D+ and D-

D+ and D- are the transceiver I/O connections, and are ESD protected to ±15kV using the Human Body Model, making the MAX3346E ideal for applications where a robust transmitter is required.

V_{CC}

Bypass V_{CC} to GND with a 1µF capacitor. Place the 1µF capacitor as close as possible to the MAX3346E.

±15kV ESD-Protected USB Transceiver in UCSP

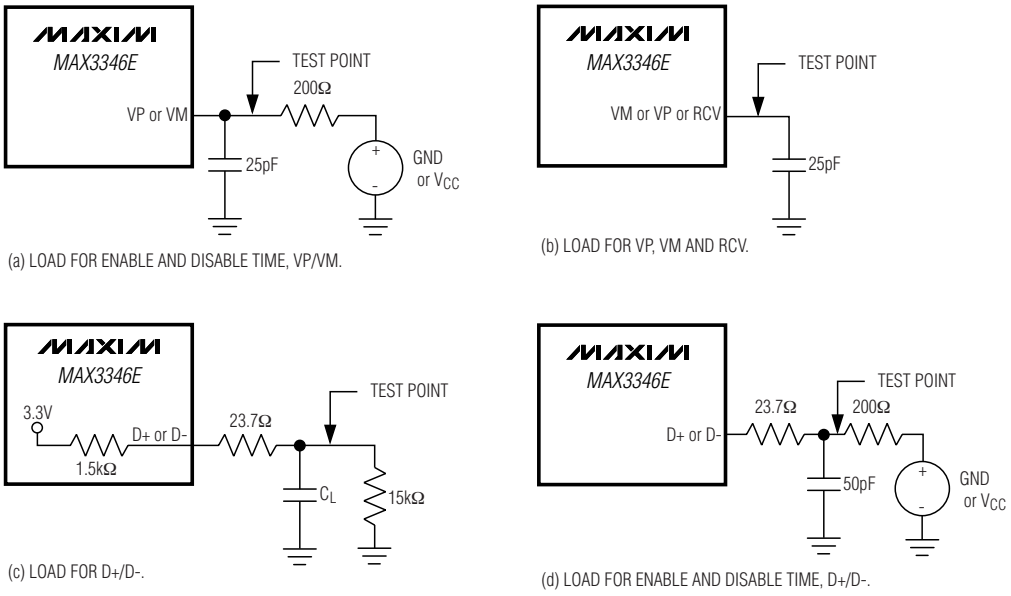


Figure 4. Test Circuits

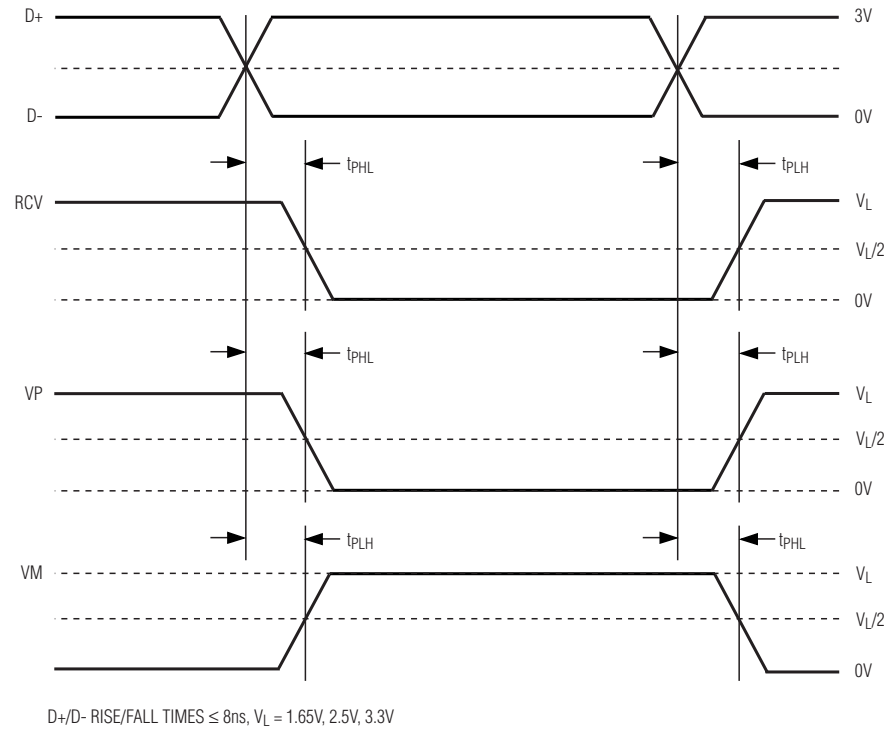


Figure 5. D+/D- to RCV, VP, VM Propagation Delays

Table 3a. Truth Table, Transmit (MODE = 0)

$\overline{OE}$ = 0 (TRANSMIT)					
INPUT		OUTPUT			RESULT
VP	VM	D+	D-	RCV	
0	0	0	1	0	Logic 0
0	1	0	0	RCV*	SE0
1	0	1	0	1	Logic 1
1	1	0	0	X	SE0

**RCV denotes the signal level on output RCV just before SE0 state occurs. This level is stable during the SE0 period.*

Table 3b. Truth Table, Transmit (MODE = 1)

$\overline{OE}$ = 0 (TRANSMIT)					
INPUT		OUTPUT			RESULT
VP	VM	D+	D-	RCV	
0	0	0	0	RCV*	SE0
0	1	0	1	0	Logic 0
1	0	1	0	1	Logic 1
1	1	1	1	X	Undefined

**RCV denotes the signal level on output RCV just before SE0 state occurs. This level is stable during the SE0 period.*

Table 3c. Truth Table, Receive

$\overline{OE}$ = 1 (RECEIVE)					
INPUT		OUTPUT			RESULT
D+	D-	VP	VM	RCV	
0	0	0	0	RCV*	SE0
0	1	0	1	0	Logic 0
1	0	1	0	1	Logic 1
1	1	1	1	X	Undefined

**RCV denotes the signal level on output RCV just before SE0 state occurs. This level is stable during the SE0 period.*

Table 3d. Function Select

SUSP	ENUMERATE	$\overline{OE}$	D+/D-	RCV	VP/VM	FUNCTION
0	0	0	Driving	Active	High-Z	Normal driving
0	0	1	High-Z	Active	Active	Normal receiving, R_{PULLUP} disconnected
0	1	0	Driving	Active	High-Z	Normal driving
0	1	1	High-Z	Active	Active	Normal receiving, R_{PULLUP} connected
1	0	0 or 1	High-Z	0	Active	Suspend mode, R_{PULLUP} disconnected
1	1	0 or 1	High-Z	0	Active	Suspend mode, R_{PULLUP} connected

±15kV ESD-Protected USB Transceiver in UCSP

External Components

External Resistors

Two external resistors are required for USB connection, each of them from 23.7Ω ±1% to 27.4Ω ±1%, 1/2W (or greater). Place one resistor in series between D+ of the MAX3346E and D+ of the USB connector. Place the other resistor in series between D- of the MAX3346E and D- of the USB connector. The *Typical Operating Circuit* shows these connections.

External Capacitors

Four external capacitors are recommended for proper operation. Use a 0.1µF ceramic for decoupling V_L, a 1µF ceramic capacitor for decoupling V_{CC}, and a 1.0µF (or greater) ceramic or plastic filter capacitor on VTRM. Return all capacitors to GND.

Receiving Data from the USB

Data received from the USB are output to VP/VM and RCV in either of two ways, differentially or single ended. To receive data from the USB, force $\overline{OE}$ high, and force SUSP low. Differential data arriving at D+/D- appears as differential logic signals at VP/VM, and as a single-ended logic signal at RCV. If both D+ and D- are low, then VP and VM are low, signaling an SE0 condition on the bus; RCV retains the last state before SE0 (see Table 3).

Transmitting Data to the USB

The MAX3346E outputs data to the USB differentially on D+ and D-. The logic driving the signals may be either differential or single ended. For sending differential logic, force MODE high, force $\overline{OE}$ and SUSP low, and apply data to VP and VM. If sending single-ended logic, force MODE, SUSP, $\overline{OE}$, and VM low, and apply data to VP. With VP low, D+ is low and D- high, resulting in a logic 0 state. With VP high, D+ is high and D- low, resulting in a logic 1 state (see Table 3).

ESD protection

To protect the MAX3346E against ESD, D+ and D- have extra protection against static electricity to protect the device up to ±15kV. The ESD structures withstand high ESD in all states; normal operation, suspend, and powered down. For the 15kV ESD structures to work correctly, a 1µF or greater capacitor must be connected from VTRM to GND.

ESD protection can be tested in various ways; the D+ and D- input/output pins are characterized for protection to the following limits:

1) ±15kV using the Human Body Model.
2) ±8kV using the Contact Discharge method specified in IEC 1000-4-2.
3) ±10kV using the IEC 1000-4-2 Air-Gap method.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 6a shows the Human Body Model, and Figure 6b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

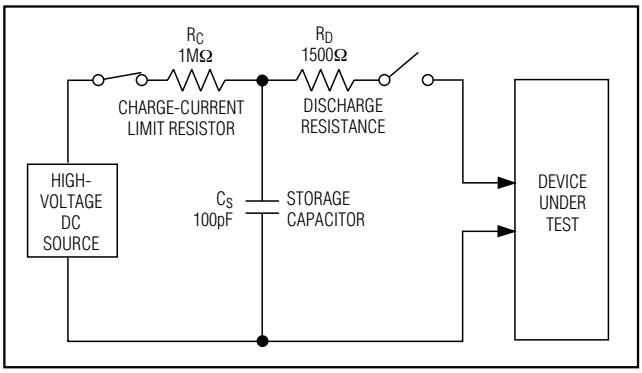


Figure 6a. Human Body ESD Test Models

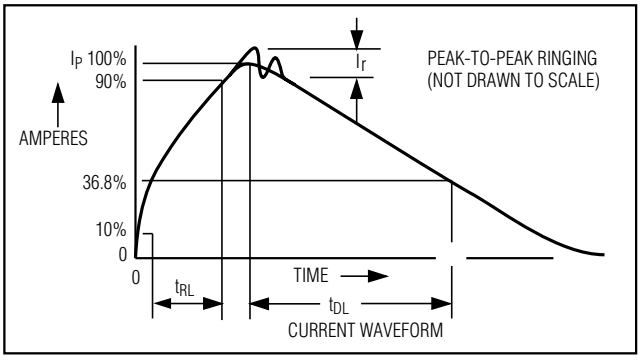


Figure 6b. Human Body Model Current Waveform

IEC 1000-4-2

The IEC 1000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits. The MAX3346E helps to design equipment that meets Level 2 of IEC 1000-4-2, without the need for additional ESD-protection components.

The major difference between tests done using the Human Body Model and IEC 1000-4-2 is a higher peak current in IEC 1000-4-2, because series resistance is lower in the IEC 1000-4-2 model. Hence, the ESD withstand voltage measured to IEC 1000-4-2 is generally lower than that measured using the Human Body Model. Figure 7a shows the IEC 1000-4-2 model.

The Air-Gap Discharge test involves approaching the device with a charged probe. The Contact Discharge method connects the probe to the device before the probe is energized.

Machine Model

The Machine Model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance. Its objective is to emulate the stress caused by contact that occurs with handling and assembly during manufacturing. Of course, all pins require this protection during manufacturing, not just USB inputs and outputs. Therefore, after PC board assembly, the Machine Model is less relevant to I/O ports.

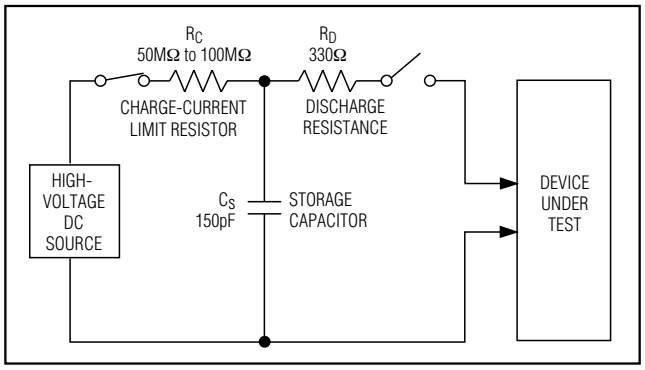


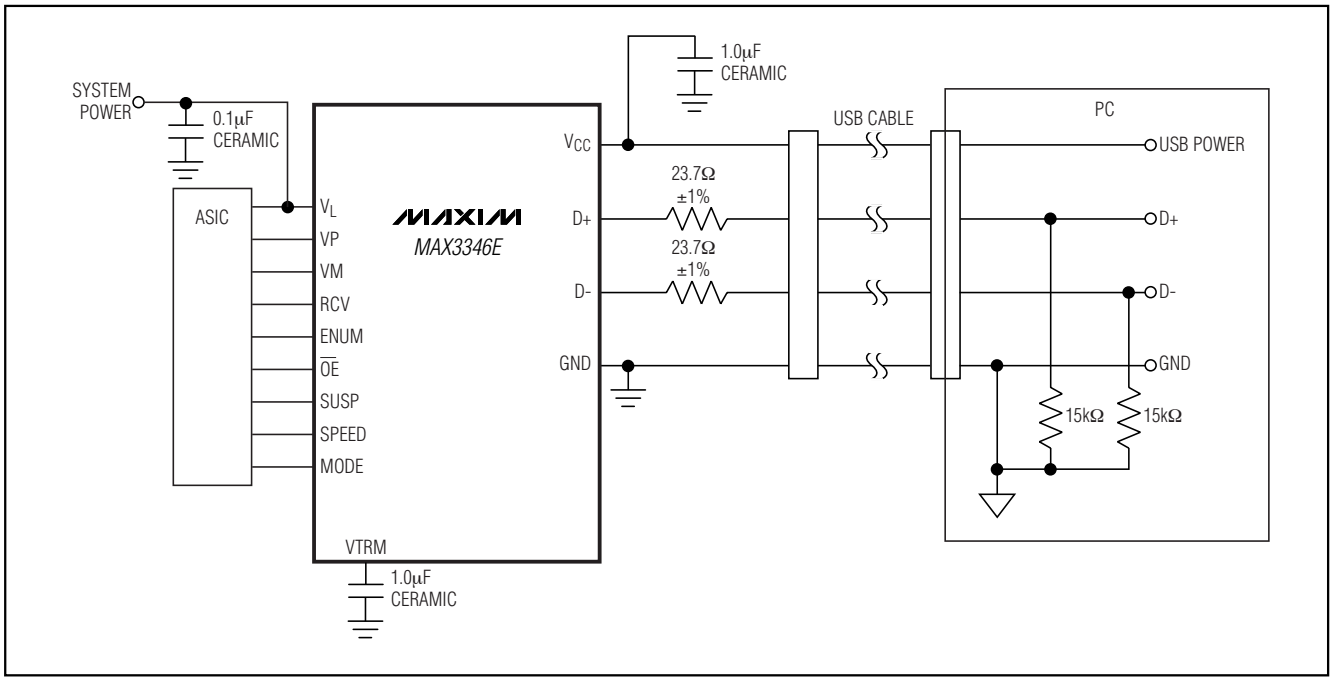
Figure 7a. IEC 1000-4-2 ESD Test Model

UCSP Applications Information

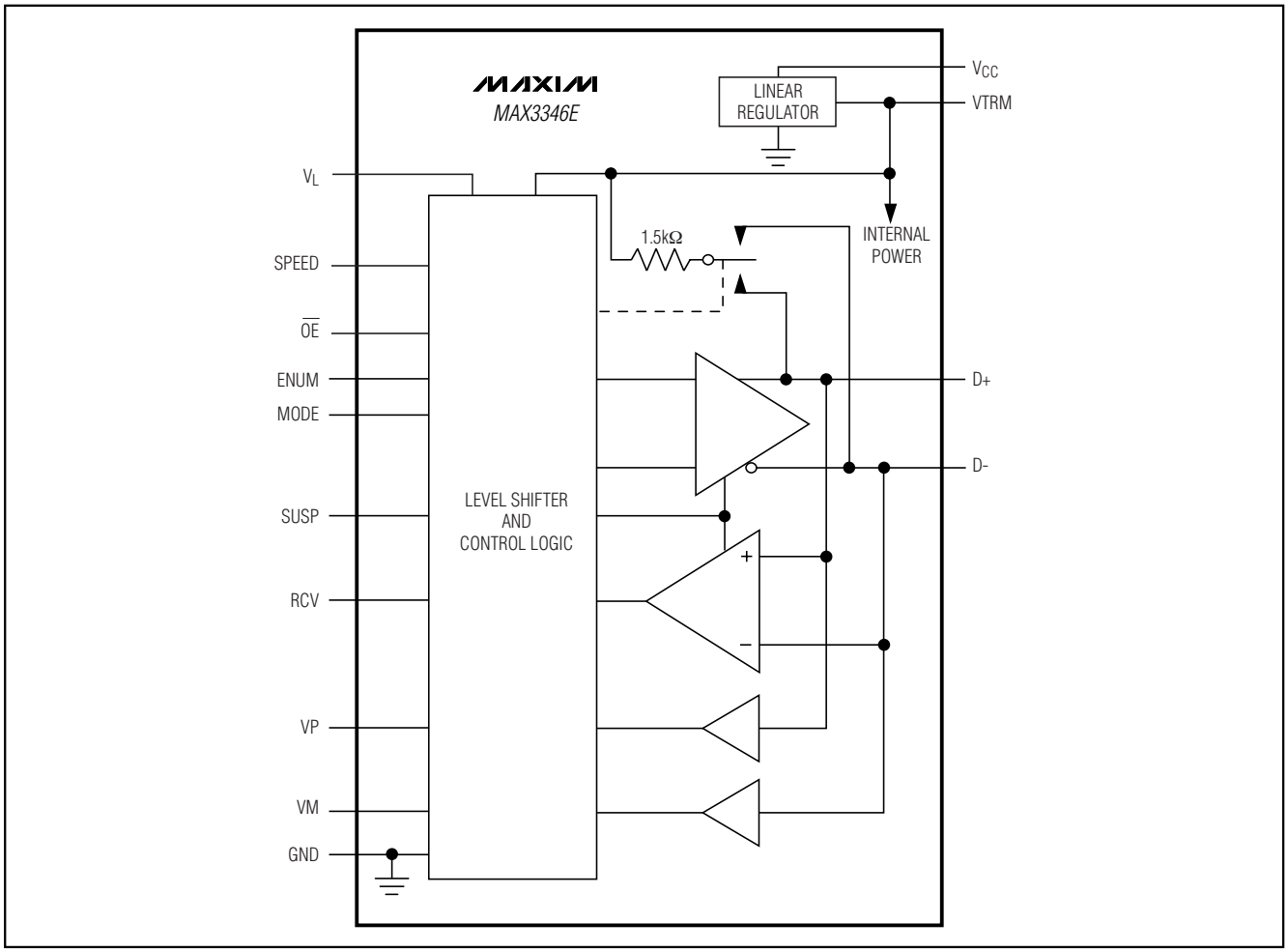
For the latest application details on UCSP construction, dimensions, tape carrier information, printed circuit board techniques, bump-pad layout, and recommended reflow temperature profile as well as the latest information on reliability testing results, go to the Maxim website at www.maxim-ic.com/ucsp for the Application Note, "UCSP—A Wafer-Level Chip-Scale Package."

±15kV ESD-Protected USB Transceiver in UCSP

Typical Operating Circuit



Functional Diagram



Chip Information

TRANSISTOR COUNT: 2162

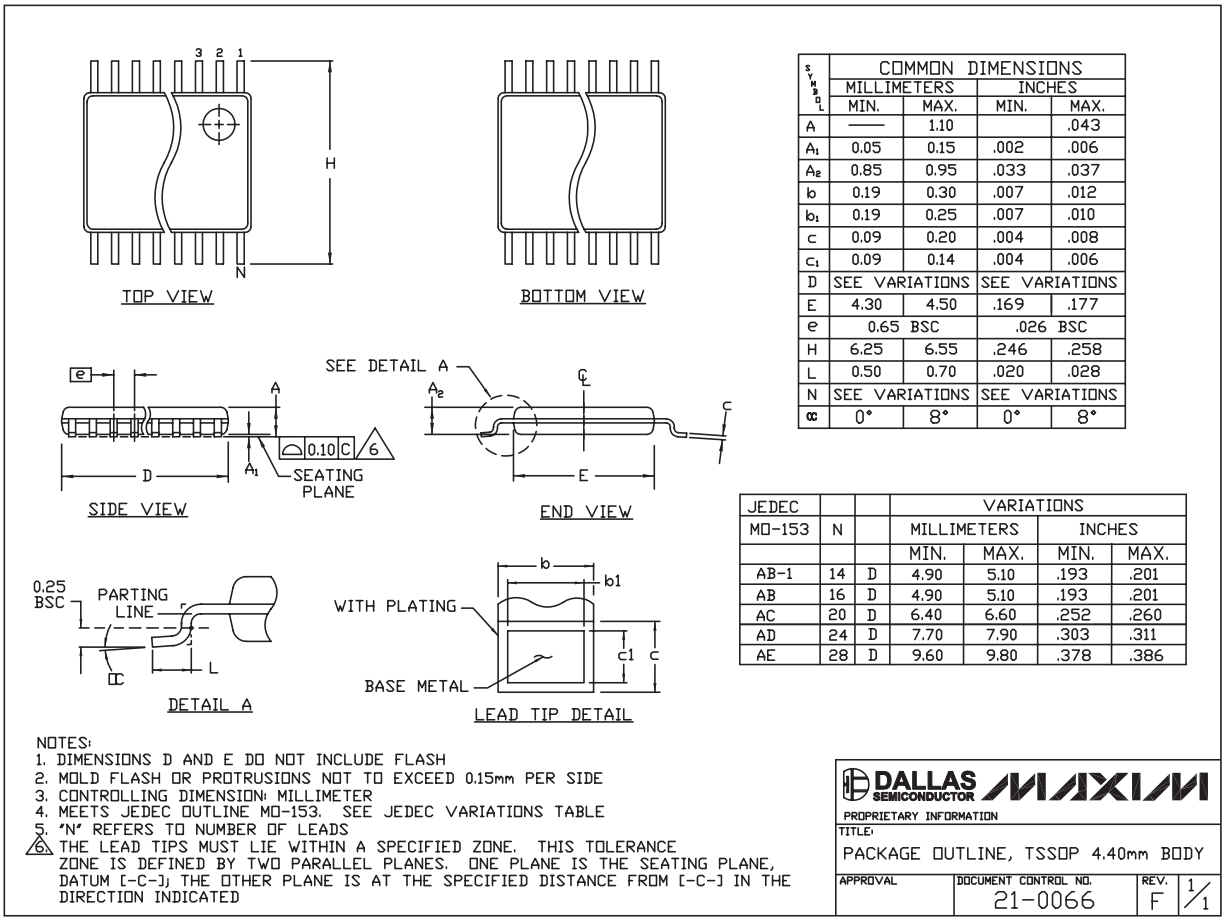
PROCESS: BiCMOS

±15kV ESD-Protected USB Transceiver in UCSP

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

TSSOP4.40mm.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	——	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

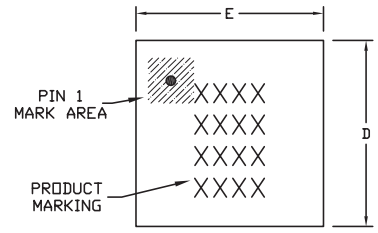
TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0066	F	1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

16L,UCSP.EPS

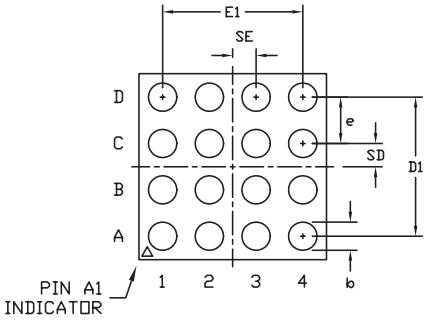


TOP VIEW

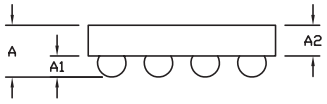
COMMON DIMENSIONS	
A	0.62+0.05-0.08
A1	0.29±0.02
A2	0.33 REF.
b	ø0.35±0.03
D1	1.50 BASIC
E1	1.50 BASIC
e	0.50 BASIC
SD	0.25 BASIC
SE	0.25 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B16-1	2.02±0.05	2.02±0.05	NONE
B16-2	2.02±0.05	2.02±0.05	B3, C3
B16-3	2.02±0.05	2.02±0.05	B3, C2
B16-4	2.02±0.05	2.02±0.05	B2, C3
B16-5	2.02±0.05	2.02±0.05	B2, B3, C2, C3
B16-6	2.02±0.05	2.02±0.05	C3

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. PRODUCT MARKING: NUMBER OF CHARACTERS AND LINES VARY PER PRODUCT.



BOTTOM VIEW



SIDE VIEW

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 4x4 UCSP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0101	H	1/1

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