PRELIMINARY

W48S111-14

Spread Spectrum Desktop/Notebook System Frequency Generator

Features

- **Maximized EMI suppression using Cypress's Spread Spectrum Technology**
- **Reduces measured EMI by as much as 10 dB**
- **I^2C programmable to 133 MHz**
- **Two skew-controlled copies of CPU output**
- **SEL100/66# selects CPU frequency (100 or 66.8 MHz)**
- **Seven copies of PCI output (synchronous w/CPU output)**
- **One copy of 14.31818-MHz IOAPIC output**
- **One copy of 48-MHz USB output**
- **Selectable 24-/48-MHz clock is determined by resistor straps on power-up**
- **One high-drive output buffer that produces a copy of the 14.318-MHz reference**
- **Isolated core VDD pin for noise reduction**

Key Specifications

Supply Voltages: ..... V_{DDQ3} = 3.3V±5%
V_{DDQ2} = 2.5V±5%

CPU Cycle to Cycle Jitter: ..... 200 ps

CPU, PCI Output Edge Rate: ..... ≥1 V/ns

CPU0:1 Output Skew: ..... 175 ps

PCI_F, PCI1:6 Output Skew: ..... 500 ps

CPU to PCI Skew: ..... 1.5 to 4.0 ns (CPU Leads)

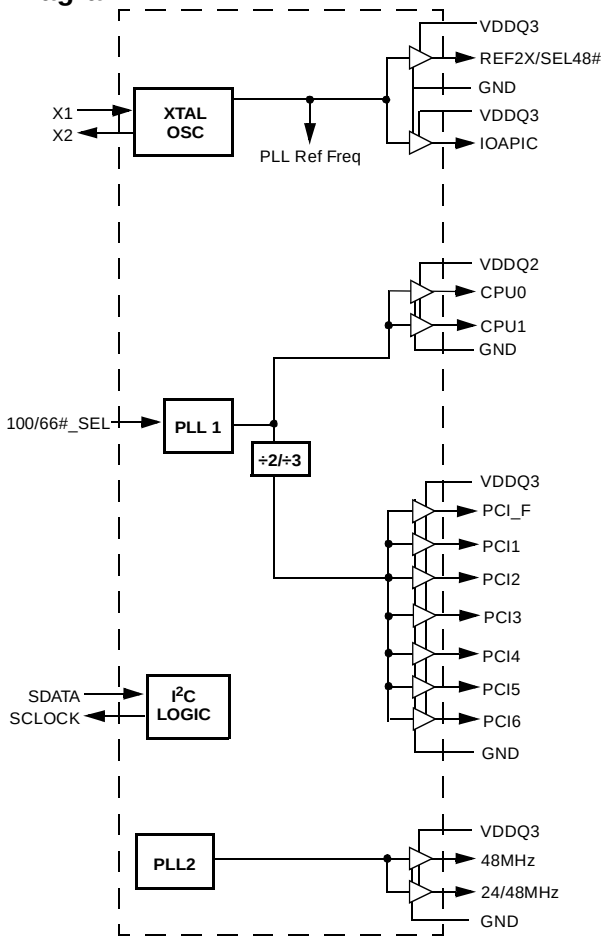
REF2X/SEL48#, SCLOCK, SDATA: ..... 250-kΩ pull-up

Note: Internal pull-up resistors should not be relied upon for setting I/O pins HIGH.

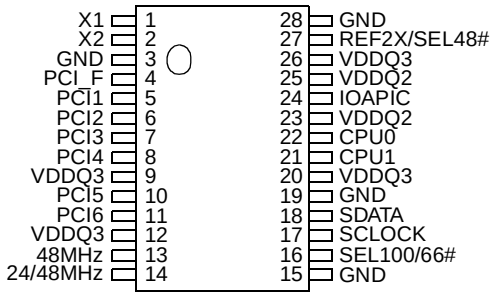
Table 1. Pin Selectable Frequency

SEL100/66#	CPU(0:1)	PCI
1	100 MHz	33.3 MHz
0	66.8 MHz	33.4 MHz

Block Diagram



Pin Configuration



Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
CPU0:1	22, 21	O	***CPU Clock Outputs 0 through 1:*** These two CPU clocks run at a frequency set by SEL100/66#. Output voltage swing is set by the voltage applied to VDDQ2.
PCI1:6 PCI_F	5, 6, 7, 8, 10, 11, 4	O	***PCI Bus Clock Outputs 1 through 6 and PCI_F:*** These seven PCI clock outputs run synchronously to the CPU clock. Voltage swing is set by the power connection to VDDQ3.
IOAPIC	24	O	***I/O APIC Clock Output:*** Provides 14.318-MHz fixed frequency. The output voltage swing is set by the power connection to VDDQ2.
48MHz	13	O	***48-MHz Output:*** Fixed 48-MHz USB clock. Output voltage swing is controlled by voltage applied to VDDQ3.
24/48MHz	14	O	***24-MHz or 48-MHz Output:*** Frequency is set by the state of pin 27 on power-up.
REF2X/SEL48#	27	I/O	***I/O Dual-Function REF2X and SEL48# pin:*** Upon power-up, the state of SEL48# is latched. The initial state is set by either a 10K resistor to GND or to V_{DD}. A 10K resistor to GND causes pin 14 to output 48 MHz. If the pin is strapped to V_{DD}, pin 14 will output 24 MHz. After 2 ms, the pin becomes a high-drive output that produces a copy of 14.318 MHz.
SEL100/66#	16	I	***Frequency Selection Input:*** Selects CPU clock frequency as shown in *Table 1* on page 1.
SDATA	18	I/O	***I^2C Data Pin:*** Data should be presented to this input as described in the I^2C section of this data sheet. Internal 250-kΩ pull-up resistor.
SCLOCK	17	I	***I^2C clock Pin:*** The I^2C data clock should be presented to this input as described in the I^2C section of this data sheet.
X1	1	I	***Crystal Connection or External Reference Frequency Input:*** Connect to either a 14.318-MHz crystal or other reference signal.
X2	2	I	***Crystal Connection:*** An input connection for an external 14.318-MHz crystal. If using an external reference, this pin must be left unconnected.
VDDQ3	9, 12, 20, 26	P	***Power Connection:*** Power supply for core logic and PLL circuitry, PCI, 48/24MHz, and Reference output buffers. Connect to 3.3V supply.
VDDQ2	23, 25	P	***Power Connection:*** Power supply for IOAPIC and CPU output buffers. Connect to 2.5V supply.
GND	3, 15, 19, 28	G	***Ground Connections:*** Connect all ground pins to the common system ground plane.

Functional Description

I/O Pin Operation

Pin 27 is a dual-purpose I/O pin. Upon power-up this pin acts as a logic input, allowing the determination of assigned device functions. A short time after power-up, the logic state of the pin is latched and the pin becomes a clock output. This feature reduces device pin count by combining clock outputs with input select pins.

An external 10-kΩ "strapping" resistor is connected between the I/O pin and ground or V_{DD}. Connection to ground sets a latch to "0," connection to V_{DD} sets a latch to "1." *Figure 1* and *Figure 2* show two suggested methods for strapping resistor connections.

Upon W48S111-14 power-up, the first 2 ms of operation is used for input logic selection. During this period, the Reference clock output buffer is three-stated, allowing the output strapping resistor on the I/O pin to pull the pin and its associated capacitive clock load to either a logic HIGH or LOW state. At the end of the 2-ms period, the established logic "0" or "1" condition of the I/O pin is then latched. Next the output buffer is enabled, which converts the I/O pin into an operating clock output. The 2-ms timer is started when V_{DD} reaches 2.0V. The input bit can only be reset by turning V_{DD} off and then back on again.

It should be noted that the strapping resistor has no significant effect on clock output signal integrity. The drive impedance of clock output is 40Ω (nominal) which is minimally affected by the 10-kΩ strap to ground or V_{DD}. As with the series termination resistor, the output strapping resistor should be placed as close to the I/O pin as possible in order to keep the interconnecting trace short. The trace from the resistor to ground or V_{DD} should be kept less than two inches in length to prevent system noise coupling during input logic sampling.

When the clock output is enabled following the 2-ms input period, a 14.318-MHz output frequency is delivered on the pin, assuming that V_{DD} has stabilized. If V_{DD} has not yet reached full value, output frequency initially may be below target but will increase to target once V_{DD} voltage has stabilized. In either case, a short output clock cycle may be produced from the CPU clock outputs when the outputs are enabled.

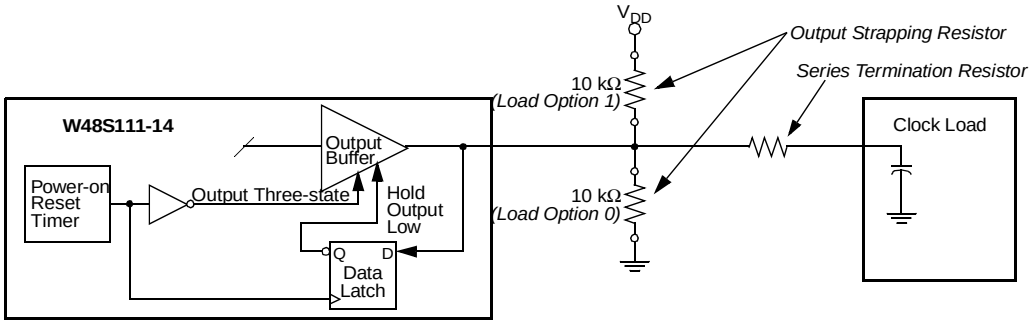


Figure 1. Input Logic Selection Through Resistor Load Option

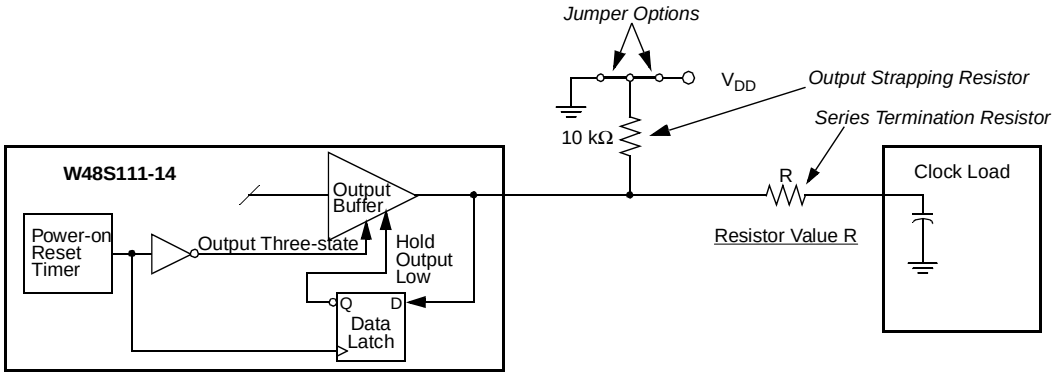


Figure 2. Input Logic Selection Through Jumper Option

Serial Data Interface

The W48S111-14 features a two-pin, serial data interface that can be used to configure internal register settings that control particular device functions. Upon power-up, the W48S111-14 initializes with default register settings. Therefore, the use of this serial data interface is optional. The serial interface is write-only (to the clock chip) and is the dedicated function of device pins SDATA and SCLOCK. In motherboard applications, SDATA and SCLOCK are typically driven by two logic outputs of the chipset. Clock device register changes are normally made upon system initialization, if required. The interface can also be used during system operation for power management functions. *Table 2* summarizes the control functions of the serial data interface.

Operation

Data is written to the W48S111-14 in ten bytes of eight bits each. Bytes are written in the order shown in *Table 3*.

Table 2. Serial Data Interface Control Functions Summary

Control Function	Description	Common Application
Clock Output Disable	Any individual clock output(s) can be disabled. Disabled outputs are actively held LOW.	Unused outputs are disabled to reduce EMI and system power. Examples are clock outputs to unused PCI slots.
CPU Clock Frequency Selection	Provides CPU/PCI frequency selections beyond the 100- and 66.8-MHz selections that are provided by the SEL100/66# pin. Frequency is changed in a smooth and controlled fashion.	For alternate microprocessors and power management options. Smooth frequency transition allows CPU frequency change under normal system operation.
Output Three-state	Puts all clock outputs into a high-impedance state.	Production PCB testing.
Test Mode	All clock outputs toggle in relation to X1 input, internal PLL is bypassed. Refer to *Table 4*.	Production PCB testing.
(Reserved)	Reserved function for future device revision or production device testing.	No user application. Register bit must be written as 0.

Table 3. Byte Writing Sequence

Byte Sequence	Byte Name	Bit Sequence	Byte Description
1	Slave Address	11010010	Commands the W48S111-14 to accept the bits in Data Bytes 3–6 for internal register configuration. Since other devices may exist on the same common serial data bus, it is necessary to have a specific slave address for each potential receiver. The slave receiver address for the W48S111-14 is 11010010. Register setting will not be made if the Slave Address is not correct (or is for an alternate slave receiver).
2	Command Code	Don't Care	Unused by the W48S111-14, therefore bit values are ignored ("don't care"). This byte must be included in the data write sequence to maintain proper byte allocation. The Command Code Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
3	Byte Count	Don't Care	Unused by the W48S111-14, therefore bit values are ignored ("don't care"). This byte must be included in the data write sequence to maintain proper byte allocation. The Byte Count Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
4	Data Byte 0	Don't Care	Refer to Cypress SDRAM drivers.
5	Data Byte 1		
6	Data Byte 2		
7	Data Byte 3	Refer to *Table 4*	The data bits in these bytes set internal W48S111-14 registers that control device operation. The data bits are only accepted when the Address Byte bit sequence is 11010010, as noted above. For description of bit control functions, refer to *Table 4*, Data Byte Serial Configuration Map.
8	Data Byte 4		
9	Data Byte 5		
10	Data Byte 6		

Writing Data Bytes

Each bit in the data bytes control a particular device function except for the “reserved” bits which must be written as a logic 0. Bits are written MSB (most significant bit) first, which is bit 7. *Table 4* gives the bit formats for registers located in Data Bytes 3–6.

Table 5 details additional frequency selections that are available through the serial data interface.

Table 6 details the select functions for Byte 3, bits 1 and 0.

Table 4. Data Bytes 3–6 Serial Configuration Map

Bit(s)	Affected Pin		Control Function	Bit Control		Default
	Pin No.	Pin Name		0	1	
Data Byte 3						
7	--	--	(Reserved)	--	--	0
6	--	--	SEL_2	Refer to *Table 5*		0
5	--	--	SEL_1	Refer to *Table 5*		0
4	--	--	SEL_0	Refer to *Table 5*		0
3	--	--	Frequency Table Selection	Frequency Controlled by external SEL100/ 66# pin (*Table 1*)	Frequency Controlled by BYT3 SEL_(2:0) (*Table 5*)	0
2	--	--	(Reserved)	--	--	0
1–0	--	--	Bit 1 Bit 0 Function (See *Table 6* for function details) 0 0 Normal Operation 0 1 Test Mode 1 0 Spread Spectrum on 1 1 All Outputs Three-stated			00
Data Byte 4						
7	--	--	(Reserved)	--	--	0
6	14	24/48MHz	Clock output disable	Low	Active	1
5	--	--	(Reserved)	--	--	0
4	--	--	(Reserved)	--	--	0
3	--	--	(Reserved)	--	--	0
2	21	CPU1	Clock Output Disable	Low	Active	1
1	--	--	(Reserved)	--	--	0
0	22	CPU0	Clock Output Disable	Low	Active	1
Data Byte 5						
7	4	PCI_F	Clock Output Disable	Low	Active	1
6	11	PCI6	Clock Output Disable	Low	Active	1
5	10	PCI5	Clock Output Disable	Low	Active	1
4	-	--	(Reserved)	--	--	0
3	8	PCI4	Clock Output Disable	Low	Active	1
2	7	PCI3	Clock Output Disable	Low	Active	1
1	6	PCI2	Clock Output Disable	Low	Active	1
0	5	PCI1	Clock Output Disable	Low	Active	1
Data Byte 6						
7	--	--	(Reserved)	--	--	0
6	--	--	(Reserved)	--	--	0
5	24	IOAPIC	Clock Output Disable	Low	Active	1
4	--	--	(Reserved)	--	--	0
3	--	--	(Reserved)	--	--	0
2	--	--	(Reserved)	--	--	0
1	27	REF2X	Clock Output Disable	Low	Active	1[1]
0	27	REF2X	Clock Output Disable	Low	Active	1[1]

Note:
1. Bits 0 and 1 of Data byte 6 in *Table 4* MUST be programmed as the same value.

Table 5. Additional Frequency Selections through Serial Data Interface Data Bytes

Input Conditions			Output Frequency		If Spread Is On
Data Byte 3, Bit 3 = 1					
Bit 6 SEL_2	Bit 5 SEL_1	Bit 4 SEL_0	CPU, SDRAM Clocks (MHz)	PCI Clocks (MHz)	Spread Percentage
0	0	0	68.5	34.25	± 0.5% Center
0	0	1	75	37.5	± 0.5% Center
0	1	0	83.3	41.6	± 0.5% Center
0	1	1	66.8	33.4	± 0.5% Center
1	0	0	103	34.25	± 0.5% Center
1	0	1	112	37.3	± 0.5% Center
1	1	0	133.3	44.43	± 0.5% Center
1	1	1	100	33.3	± 0.5% Center

Table 6. Select Function for Data Byte 3, Bits 0:1

Function	Input Conditions		Output Conditions				
	Data Byte 3						
	Bit 1	Bit 0	CPU0:1	PCI_F, PCI1:6	REF2X, IOAPIC	48MHZ	24MHZ
Normal Operation	0	0	Note 2	Note 2	14.318 MHz	48 MHz	24 MHz
Test Mode	0	1	X1/2	CPU/2, 3, or 4	X1	X1/2	X1/4
Spread Spectrum On	1	0	±0.5%	±0.5%	14.318 MHz	48 MHz	24 MHz
Three-state	1	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

Note:

2. CPU and PCI frequency selections are listed in *Table 1* and *Table 5*.

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Operating Temperature	0 to +70	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C
ESD_{PROT}	Input ESD Protection	2 (min.)	kV

DC Electrical Characteristics: T_A = 0°C to +70°C, V_{DDQ3} = 3.3V±5%, V_{DDQ2} = 2.5V±5%

Parameter	Description		Test Condition	Min.	Typ.	Max.	Unit
Supply Current							
I_{DDQ3}	Combined 3.3V Supply Current		CPUCLK =100 MHz Outputs Loaded[3]		85		mA
I_{DDQ3}	Combined 2.5V Supply Current		CPUCLK =100 MHz Outputs Loaded[3]		30		mA
Logic Inputs							
V_{IL}	Input Low Voltage			GND – 0.3		0.8	V
V_{IH}	Input High Voltage			2.0		V_{DD} + 0.3	V
I_{IL}	Input Low Current[4]					–25	µA
I_{IH}	Input High Current[4]					10	µA
I_{IL}	Input Low Current (SEL100/66#)					–5	µA
I_{IH}	Input High Current (SEL100/66#)					5	µA
Clock Outputs							
V_{OL}	Output Low Voltage		I_{OL} = 1 mA			50	mV
V_{OH}	Output High Voltage		I_{OH} = –1 mA	3.1			V
V_{OH}	Output High Voltage	CPU0:1, IOAPIC	I_{OH} = –1 mA	2.2			V
I_{OL}	Output Low Current	CPU0:1	V_{OL} = 1.25V	50	70	100	mA
		PCI_F, PCI1:6	V_{OL} = 1.5V	60	80	120	mA
		IOAPIC	V_{OL} = 1.25V	40	85	140	mA
		REF2X	V_{OL} = 1.5V	100	130	152	mA
		48MHz, 24MHz	V_{OL} = 1.5V	40	50	76	mA
I_{OH}	Output High Current	CPU0:1	V_{OL} = 1.25V	50	70	100	mA
		PCI_F, PCI1:6	V_{OL} = 1.5V	60	70	120	mA
		IOAPIC	V_{OL} = 1.25V	40	87	155	mA
		REF2X	V_{OL} = 1.5V	100	130	150	mA
		48MHz, 24MHz	V_{OL} = 1.5V	40	50	94	mA

Notes:

3. All clock outputs loaded with maximum lump capacitance test load specified in the AC Electrical Characteristics section.
4. W48S111-14 logic inputs have internal pull-up devices, except SEL100/66# (pull-ups not full CMOS level).

DC Electrical Characteristics: T_A = 0°C to +70°C, V_{DDQ3} = 3.3V±5%, V_{DDQ2} = 2.5V±5% (continued)

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
Crystal Oscillator						
V_{TH}	X1 Input Threshold Voltage[5]	V_{DDQ3} = 3.3V		1.65		V
C_{LOAD}	Load Capacitance, as seen by External Crystal[6]			14		pF
$C_{IN,X1}$	X1 Input Capacitance[7]	Pin X2 unconnected		28		pF
Pin Capacitance/Inductance						
C_{IN}	Input Pin Capacitance	Except X1 and X2			5	pF
C_{OUT}	Output Pin Capacitance				6	pF
L_{IN}	Input Pin Inductance				7	nH

AC Electrical Characteristics

T_A = 0°C to +70°C, V_{DDQ3} = 3.3V±5%,V_{DDQ2} = 2.5V± 5%, f_{XTL} = 14.31818 MHz

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output; Spread Spectrum clocking is disabled.

CPU Clock Outputs, CPU0:1 (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	CPU = 66.8 MHz			CPU = 100 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_P	Period	Measured on rising edge at 1.25V	15		15.5	10		10.5	ns
t_H	High Time	Duration of clock cycle above 2.0V	5.2			3.0			ns
t_L	Low Time	Duration of clock cycle below 0.4V	5.0			2.8			ns
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.0V	1		4	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.0V to 0.4V	1		4	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.25V	45		55	45		55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.25V. Maximum difference of cycle time between two adjacent cycles.			200			200	ps
t_{SK}	Output Skew	Measured on rising edge at 1.25V			175			175	ps
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		20			20		Ω

Notes:

5. X1 input threshold voltage (typical) is $V_{DD}/2$.
6. The W48S111-14 contains an internal crystal load capacitor between pin X1 and ground and another between pin X2 and ground. Total load placed on crystal is 14 pF; this includes typical stray capacitance of short PCB traces to crystal.
7. X1 input capacitance is applicable when driving X1 with an external clock source (X2 is left unconnected).

PCI Clock Outputs, PCI1:6 and PCI_F (Lump Capacitance Test Load = 30 pF

Parameter	Description	Test Condition/Comments	CPU = 66.8/100 MHz			Unit
			Min.	Typ.	Max.	
t_P	Period	Measured on rising edge at 1.5V	30			ns
t_H	High Time	Duration of clock cycle above 2.4V	12			ns
t_L	Low Time	Duration of clock cycle below 0.4V	12			ns
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.			250	ps
t_{SK}	Output Skew	Measured on rising edge at 1.5V			500	ps
t_O	CPU to PCI Clock Skew	Covers all CPU/PCI outputs. Measured on rising edge at 1.5V. CPU leads PCI output.	1.5		4	ns
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		20		Ω

IOAPIC Clock Output (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	CPU = 66.8/100 MHz			Unit
			Min.	Typ.	Max.	
f	Frequency, Actual	Frequency generated by crystal oscillator	14.31818			MHz
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.0V	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.0V to 0.4V	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.25V	45		55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			1.5	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		15		Ω

REF2X Clock Output (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	CPU = 66.8/100 MHz			Unit
			Min.	Typ.	Max.	
f	Frequency, Actual	Frequency generated by crystal oscillator	14.318			MHz
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	0.5		2	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	0.5		2	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		20		Ω

48-MHz and 24-MHz Clock Output (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	CPU = 66.8/100 MHz			Unit
			Min.	Typ.	Max.	
f	Frequency, Actual	Determined by PLL divider ratio (see m/n below)		48.008 24.004		MHz
f_D	Deviation from 48 MHz	(48.008 – 48)/48		+167		ppm
m/n	PLL Ratio	(14.31818 MHz x 57/17 = 48.008 MHz)		57/17, 57/34		
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	0.5		2	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	0.5		2	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		25		Ω

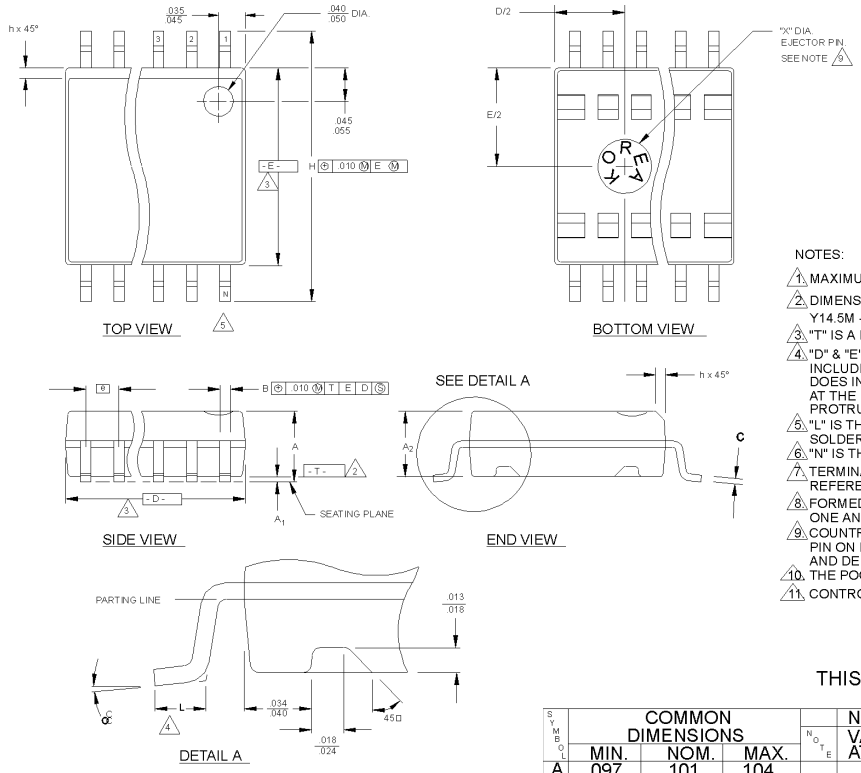
Ordering Information

Ordering Code	Freq. Mask Code	Package Name	Package Type
W48S111	-04	G	28-pin SOIC (300 mils)

Document #: 38-00854

Package Diagram

28-Pin Small Outline Integrated Circuit (SOIC, 300 mils)



NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS .025.
2. DIMENSIONING & TOLERANCES PER ANSI. Y14.5M - 1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
9. COUNTRY OF ORIGIN LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM IS OPTIONAL AND DEPEND ON ASSEMBLY LOCATION.
10. THE POCKETS ON THE BOTTOM ARE OPTIONAL.
11. CONTROLLING DIMENSION: INCHES.

THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE VARIATIONS	3 D			5 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	.097	.101	.104		AA	.402	.407	.412	16
A_1	.0050	.009	.0115		AB	.451	.456	.461	18
A_2	.090	.092	.094		AC	.500	.505	.510	20
B	.014	.016	.019		AD	.602	.607	.612	24
C	.0091	.010	.0125		AE	.701	.706	.711	28
D	SEE VARIATIONS			3					
E	.292	.296	.299						
e	.050 BSC								
H	.400	.406	.410						
h	.010	.013	.016						
L	.024	.032	.040						
N	SEE VARIATIONS			5					
α	0°	5°	8°						
X	.085	.093	.100						

THIS TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE VARIATIONS	3 D			5 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	2.46	2.56	2.64		AA	10.21	10.34	10.46	16
A_1	0.127	0.22	0.29		AB	11.46	11.58	11.71	18
A_2	2.29	2.34	2.39		AC	12.70	12.83	12.95	20
B	0.35	0.41	0.48		AD	15.29	15.42	15.54	24
C	0.23	0.25	0.32		AE	17.81	17.93	18.06	28
D	SEE VARIATIONS			3					
E	7.42	7.52	7.59						
e	1.27 BSC								
H	10.16	10.31	10.41						
h	0.25	0.33	0.41						
L	0.61	0.81	1.02						
N	SEE VARIATIONS			5					
α	0°	5°	8°						
X	2.16	2.36	2.54						

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