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# FSA644 — 2:1 MIPI D-PHY (1.5Gbps) 4-Data Lane Switch

## Features

Switch Type	SPDT (10x)
<b>Signal Types</b>	<b>MIPI, D-PHY</b>
V <sub>CC</sub>	1.65 to 4.5 V
Input Signals	0 to V <sub>CC</sub>
R <sub>ON</sub>	6 Ω Typical HS MIPI 8 Ω Typical LP MIPI
ΔR <sub>ON</sub>	0.6 Ω Typical HS & LP MIPI
R <sub>ON_FLAT</sub>	0.3 Ω Typical
I <sub>CCZ</sub>	0.5 μA Maximum
I <sub>CC</sub>	32 μA Maximum
O <sub>IRR</sub>	-40 dB Typical
X <sub>TALK</sub>	-25 dB Typical
Bandwidth	1100 MHz Minimum
Channel-to-Channel Skew	6 ps Typical
C <sub>ON</sub>	5.2 pF
Operating Temperature	-40 to +85°C
Package	36-Ball WLCSP
FSA644UCX Top Mark	M7
Ordering Information	FSA644UCX
FSA644BUCX Top Mark	KM
Ordering Information	FSA644BUCX

## Description

The FSA644 is a four-data-lane, MIPI, D-PHY switch. This single-pole, double-throw (SPDT) switch is optimized for switching between two high-speed or low-power MIPI sources. The FSA644 is designed for the MIPI specification and allows connection to a CSI or DSI module.

## Applications

- Cellular Phones, Smart Phones
- Displays

## Related Resources

- FSA644 Demonstration Board

## Typical Application

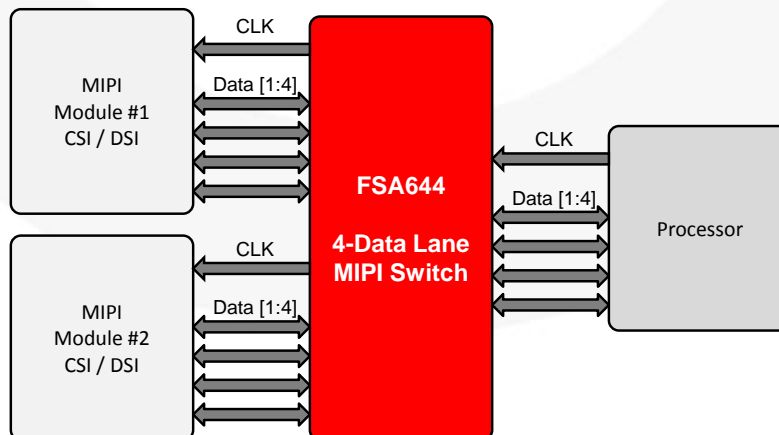


Figure 1. Mobile Phone Example

### Pin Descriptions

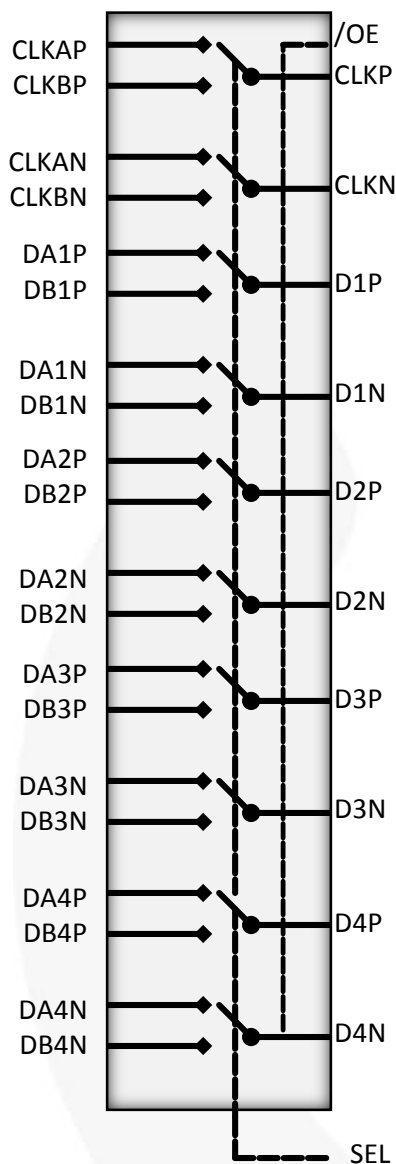


Figure 2. Analog Symbol

Pin Name	Description		
CLK <sub>P/N</sub>	Common Clock Path		
D1 <sub>P/N</sub>	Common Data Path 1		
D2 <sub>P/N</sub>	Common Data Path 2		
D3 <sub>P/N</sub>	Common Data Path 3		
D4 <sub>P/N</sub>	Common Data Path 4		
CLKA <sub>P/N</sub>	A-Side Clock Path		
DA1 <sub>P/N</sub>	A-Side Data Path 1		
DA2 <sub>P/N</sub>	A-Side Data Path 2		
DA3 <sub>P/N</sub>	A-Side Data Path 3		
DA4 <sub>P/N</sub>	A-Side Data Path 4		
CLKB <sub>P/N</sub>	B-Side Clock Path		
DB1 <sub>P/N</sub>	B-Side Data Path 1		
DB2 <sub>P/N</sub>	B-Side Data Path 2		
DB3 <sub>P/N</sub>	B-Side Data Path 3		
DB4 <sub>P/N</sub>	B-Side Data Path 4		
SEL	Control Pin	SEL=0	CLKP=CLKAP, CLKN=CLKAN, Dn(P/N)=DAn(P/N)
		SEL=1	CLKP=CLKBP, CLKN=CLKBN, Dn(P/N)=DBn(P/N)
/OE	Output Enable		
V <sub>CC</sub>	Power		
GND	Ground		
NC	No Connect		

## Pin Definitions

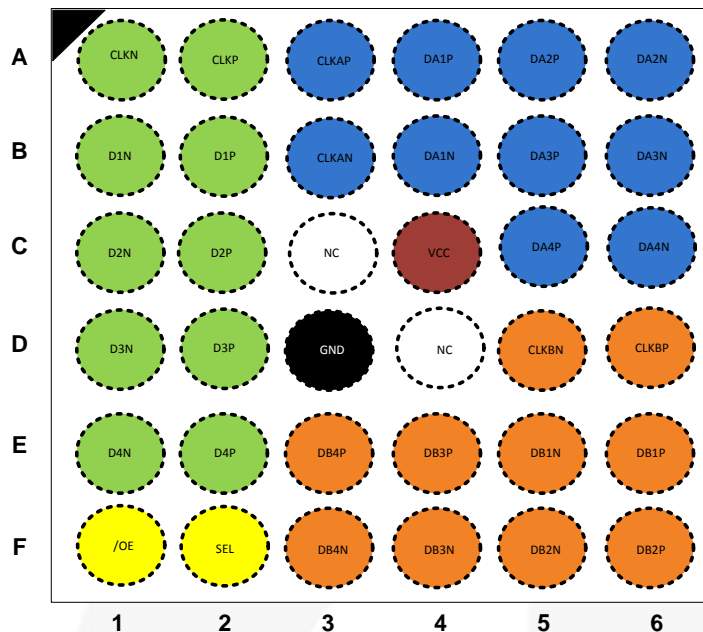


Figure 3. Top Through View

Table 1. Ball-to-Pin Mappings

Ball	Pin Name
A1	CLK <sub>N</sub>
A2	CLK <sub>P</sub>
A3	CLKA <sub>P</sub>
A4	DA1 <sub>P</sub>
A5	DA2 <sub>P</sub>
A6	DA2 <sub>N</sub>
B1	D1 <sub>N</sub>
B2	D1 <sub>P</sub>
B3	CLKA <sub>N</sub>
B4	DA1 <sub>N</sub>
B5	DA3 <sub>P</sub>
B6	DA3 <sub>N</sub>
C1	D2 <sub>N</sub>
C2	D2 <sub>P</sub>
C3	NC
C4	V <sub>CC</sub>
C5	DA4 <sub>P</sub>
C6	DA4 <sub>N</sub>
D1	D3 <sub>N</sub>
D2	D3 <sub>P</sub>
D3	GND
D4	NC
D5	CLKB <sub>N</sub>
D6	CLKB <sub>P</sub>
E1	D4 <sub>N</sub>
E2	D4 <sub>P</sub>
E3	DB4 <sub>P</sub>
E4	DB3 <sub>P</sub>
E5	DB1 <sub>N</sub>
E6	DB1 <sub>P</sub>
F1	/OE
F2	SEL
F3	DB4 <sub>N</sub>
F4	DB3 <sub>N</sub>
F5	DB2 <sub>N</sub>
F6	DB2 <sub>P</sub>

## Truth Table

SEL	/OE	Function
LOW	LOW	CLK <sub>P</sub> =CLKA <sub>P</sub> , CLK <sub>N</sub> =CLKA <sub>N</sub> , Dn(P/N)=DAn(P/N)
HIGH	LOW	CLK <sub>P</sub> =CLKB <sub>P</sub> , CLK <sub>N</sub> =CLKB <sub>N</sub> , Dn(P/N)=DBn(P/N)
X	HIGH	DAn(P/N), DBn(P/N) Data Ports High Impedance

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit	
V <sub>CC</sub>	Supply Voltage	-0.50	+5.25	V	
V <sub>CNTRL</sub>	DC Input Voltage (/OE) <sup>(1)</sup>	-0.5	V <sub>CC</sub>	V	
V <sub>SW</sub>	DC Switch I/O Voltage <sup>(1)</sup>	-0.50	5.25	V	
I <sub>IK</sub>	DC Input Diode Current	-50		mA	
I <sub>OUT</sub>	DC Output Current		50	mA	
T <sub>STG</sub>	Storage Temperature	-65	+150	°C	
ESD	Human Body Model, JEDEC: JESD22-A114	All Pins		3.5	kV
		I/O to GND		3.5	
		Power to GND		8.0	
	Charged Device Model, JEDEC: JESD22-C101			1.5	
	IEC 61000-4-2 System	Contact		8.0	
		Air Gap		15.0	

### Note:

- The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit	
V <sub>CC</sub>	Supply Voltage	1.65	4.50	V	
V <sub>CNTRL</sub>	Control Input Voltage (S, /OE) <sup>(2)</sup>	0	V <sub>CC</sub>	V	
V <sub>SW</sub>	Switch I/O Voltage (CLKn, CLKAn, CLKBn, Dn, DAn, DBn)	HS Mode	0.1	0.3	V
		LP Mode	0	1.2	
T <sub>A</sub>	Operating Temperature	-40	+85	°C	

### Note:

- The control input must be held HIGH or LOW; it must not float.

## DC Electrical Characteristics

All typical values are at  $T_A=25^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions	$V_{CC}$ (V)	$T_A=-40^\circ\text{C}$ to $+85^\circ\text{C}$			Unit
				Min.	Typ.	Max.	
$V_{IK}$	Clamp Diode Voltage	$I_{IN}=-18\text{ mA}$	2.8			-1.2	V
$V_{IH}$	Input Voltage High		1.65 to 4.50	1.0			V
$V_{IL}$	Input Voltage Low		1.65 to 4.50			0.4	V
$I_{IN}$	Control Input Leakage (SEL,/OE)	$V_{SW}=0$ to $V_{CC}$	1.65 to 4.50	-100		100	nA
$I_{NO(OFF)}, I_{NC(OFF)}$	Off Leakage Current of Port CLKAn, DAN, CLKBn, DBn	CLKn, Dn=0.3 V; $V_{CC}=0.3\text{ V}$ ; CLKAn, DAN, or CLKBn; DBn= $V_{CC}-0.3\text{ V}$ , 0.3 V, or Floating; /OE=0 V	1.65 to 4.50	-100		100	nA
$I_{A(ON)}$	On Leakage Current of Common Ports (CLKn, Dn)	CLKn, Dn = 0.3 V; $V_{CC}=0.3\text{ V}$ ; CLKAn, DAN, or CLKBn; DBn= $V_{CC}-0.3\text{ V}$ , 0.3 V, or Floating; /OE=0 V	1.65 to 4.50	-100		100	nA
$I_{OFF}$	Power-Off Leakage Current	CLKn, Dn, or CLKAn; DAN or CLKBn, DBn; $V_{IN}=0\text{ V}$ to 4.5 V; $V_{CC}=0\text{ V}$	0	-100		100	nA
$I_{OZ}$	Off-State Leakage	$0 \leq \text{CLKn, Dn, CLKAn, CLKBn, DAN, DBn} \leq 3.6\text{ V}$ , /OE=High	4.5	-100		100	nA
$R_{ON\_MIPI\_HS}$	Switch On Resistance for HS MIPI Applications <sup>(3)</sup>	$I_{ON}=-10\text{ mA}$ , /OE=0 V, SEL= $V_{CC}$ or 0V, CLK <sub>A, B</sub> , DBn or DAN=0.1, 0.2, 0.3	1.8		7	12	$\Omega$
			2.5		6	9	
			3.6		6	9	
			4.5		6	9	
$R_{ON\_MIPI\_LP}$	Switch On Resistance for LP MIPI Applications <sup>(3)</sup>	$I_{ON}=-10\text{ mA}$ , /OE=0 V, SEL= $V_{CC}$ or 0V, CLK <sub>A, B</sub> , DBn or DAN=0, 0.6, 1.2 V	1.8		6.7	12.0	$\Omega$
			2.5		6.4	9.0	
			3.6		6.2	9.0	
			4.5		6.0	9.0	
$\Delta R_{ON\_MIPI\_HS}$	On Resistance Matching Between HS MIPI Channels <sup>(4)</sup>	$I_{ON}=-10\text{ mA}$ , /OE=0 V, SEL= $V_{CC}$ or 0 V, CLK <sub>A, B</sub> , DBn or DAN=0.1, 0.2, 0.3	1.8		0.8		$\Omega$
			2.5		0.6		
			3.6		0.5		
			4.5		0.5		
$\Delta R_{ON\_MIPI\_LP}$	On Resistance Matching Between LP MIPI Channels <sup>(4)</sup>	$I_{ON}=-10\text{ mA}$ , /OE=0 V, SEL= $V_{CC}$ or 0 V, CLK <sub>A, B</sub> , DBn or DAN= 0.0, 0.6, 1.2 V	1.8		0.8		$\Omega$
			2.5		0.6		
			3.6		0.5		
			4.5		0.5		
$R_{ON\_FLAT\_MIPI\_HS}$	On Resistance Flatness for HS MIPI Signals <sup>(4)</sup>	$I_{ON}=-10\text{ mA}$ , /OE=0 V, SEL= $V_{CC}$ or 0 V, CLK <sub>A, B</sub> , DBn or DAN=0.1, 0.2, 0.3	1.8		1.5		$\Omega$
			2.5		0.5		
			3.6		0.3		
			4.5		0.2		
$R_{ON\_FLAT\_MIPI\_LP}$	On Resistance Flatness for LP MIPI Signals <sup>(4)</sup>	$I_{ON}=-10\text{ mA}$ , /OE=0 V, SEL= $V_{CC}$ or 0 V, CLK <sub>A, B</sub> , DBn or DAN=0.0, 0.6, 1.2 V	1.8		35		$\Omega$
			2.5		2		
			3.6		1		
			4.5		0.5		

Continued on the following page...

## DC Electrical Characteristics

All typical values are at  $T_A=25^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions	$V_{CC}$ (V)	$T_A=-40^\circ\text{C}$ to $+85^\circ\text{C}$			Unit
				Min.	Typ.	Max.	
$I_{CCZ}$	Quiescent Hi-Z Supply Current	$V_{IN}=0$ or $V_{CC}$ , $I_{OUT}=0$	4.5			0.5	$\mu\text{A}$
$I_{CC}$	Quiescent Supply Current	$V_{IN}=0$ or $V_{CC}$ , $I_{OUT}=0$	2.5 to 4.5			32	$\mu\text{A}$
			1.8			22	
$I_{CCT}$	Increase in $I_{CC}$ Current Per Control Voltage and $V_{CC}$	$V_{SEL}/OE=1.65\text{ V}$	4.5			4	$\mu\text{A}$
			2.5			0.1	

### Notes:

- Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltage on the two (A or B ports).
- Guaranteed by characterization.

## AC Electrical Characteristics

All typical values are for  $V_{CC}=3.3\text{V}$  at  $T_A=25^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions	$V_{CC}$ (V)	$T_A=-40^\circ\text{C}$ to $+85^\circ\text{C}$			Unit
				Min.	Typ.	Max.	
$t_{INIT}$	Initialization Time $V_{CC}$ to Output <sup>(5)</sup>	$R_L=50\ \Omega$ , $C_L=5\ \text{pF}$ , $V_{SW}=1.2\ \text{V}$	2.5 to 4.5			100	$\mu\text{s}$
			1.8			150	
$t_{EN}$	Enable Turn-On Time, /OE to Output	$R_L=50\ \Omega$ , $C_L=5\ \text{pF}$ , $V_{SW}=1.2\ \text{V}$	2.5 to 4.5		120	200	ns
			1.8		250	500	
$t_{DIS}$	Disable Turn-Off Time, /OE to Output	$R_L=50\ \Omega$ , $C_L=5\ \text{pF}$ , $V_{SW}=1.2\ \text{V}$	2.5 to 4.5		25	50	ns
			1.8		50	90	
$t_{ON}$	Turn-On Time, SEL to Output	$R_L=50\ \Omega$ , $C_L=5\ \text{pF}$ , $V_{SW}=1.2\ \text{V}$	2.5 to 4.5		50	100	ns
			1.8		75	125	
$t_{OFF}$	Turn-Off Time SEL to Output	$R_L=50\ \Omega$ , $C_L=5\ \text{pF}$ , $V_{SW}=1.2\ \text{V}$	2.5 to 4.5		50	200	ns
			1.8		200	325	
$t_{BBM}$	Break-Before-Make Time	$R_L=50\ \Omega$ , $C_L=5\ \text{pF}$ , $V_{SW}=1.2\ \text{V}$		10	50		ns
$O_{IRR}$	Off Isolation for MIPI <sup>(5)</sup>	$R_L=50\ \Omega$ , $f=750\ \text{MHz}$ , /OE= $V_{CC}$ $V_{SW}=-1\ \text{dBm}$ (200 mV <sub>PP</sub> )	1.65 to 4.5		-18		dB
$X_{TALK}$	Crosstalk for MIPI <sup>(5)</sup>	$R_L=50\ \Omega$ , $f=750\ \text{MHz}$ , $V_{SW}=-1\ \text{dBm}$ (200 mV <sub>PP</sub> )	1.65 to 4.5		-25		dB
BW	-3db Bandwidth <sup>(5)</sup>	$R_L=50\ \Omega$ , $C_L=0\ \text{pF}$	3.0	1100	1600		MHz
$S_{DD21}$	Differential Data Rate	Inter-operability Data Rate	3.0		1.5		Gbps

### Note:

- Guaranteed by characterization.

## High-Speed-Related AC Electrical Characteristics

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> =- 40°C to +85°C			Unit
				Min.	Typ.	Max.	
t <sub>SK(O)</sub>	Channel-to-Channel Single-Ended Skew <sup>(6)</sup>	TDR-Based Method (V <sub>SW</sub> =0.2 V <sub>PP</sub> , C <sub>L</sub> =C <sub>ON</sub> )	3.3		6	20	ps
t <sub>SK(P)</sub>	Skew of Opposite Transitions of the Same Output <sup>(6)</sup>	TDR-Based Method (V <sub>SW</sub> =0.2 V <sub>PP</sub> , C <sub>L</sub> =C <sub>ON</sub> )	3.3		6	20	ps

### Note:

6. Guaranteed by characterization.

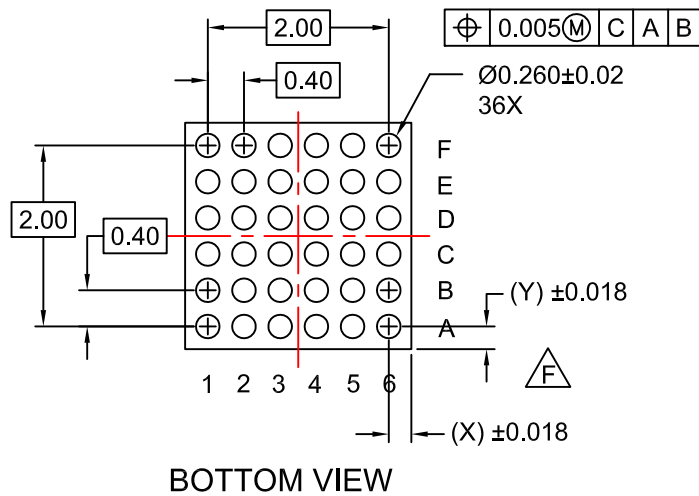
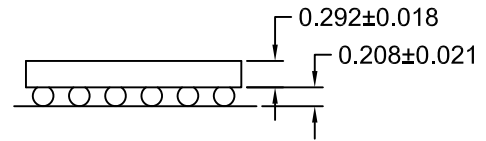
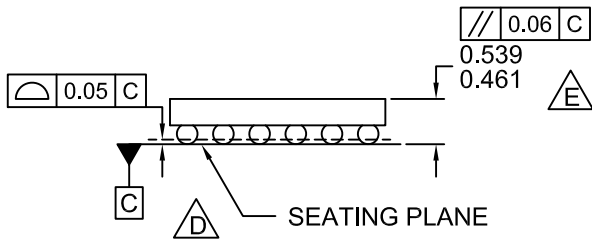
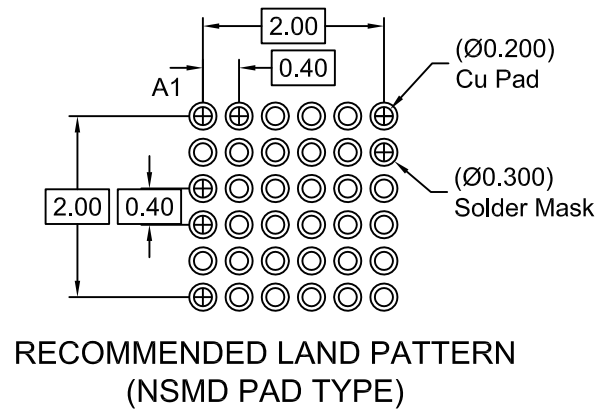
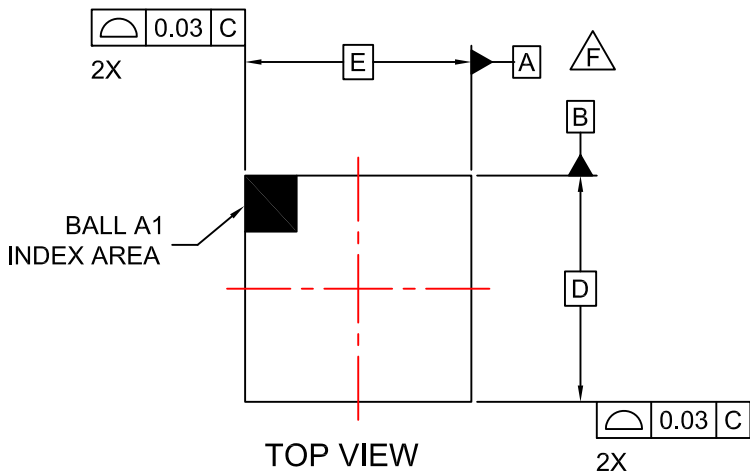
## Capacitance

Symbol	Parameter	Conditions	T <sub>A</sub> =- 40°C to +85°C			Unit
			Min.	Typ.	Max.	
C <sub>IN</sub>	Control Pin Input Capacitance	V <sub>CC</sub> =0 V, f=1 MHz		2.1		pF
C <sub>ON</sub>	Out On Capacitance	V <sub>CC</sub> =3.3 V, /OE=0 V, f=1 MHz		5.2		
C <sub>OFF</sub>	Out Off Capacitance	V <sub>CC</sub> and /OE=3.3 V, f=1 MHz		2.0		

## Ordering Information

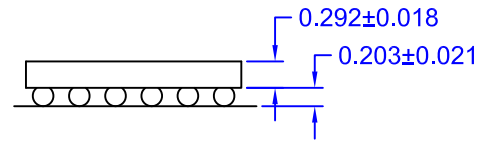
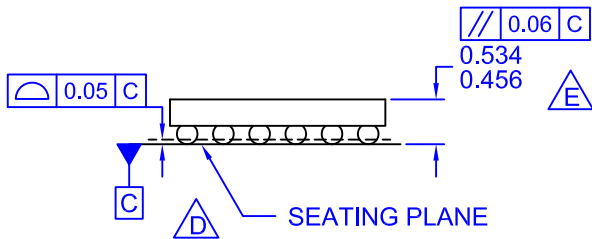
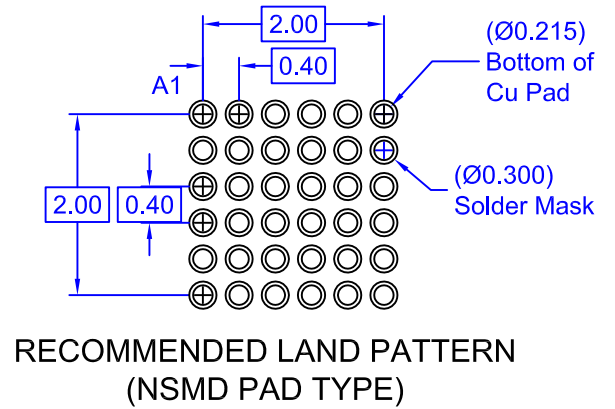
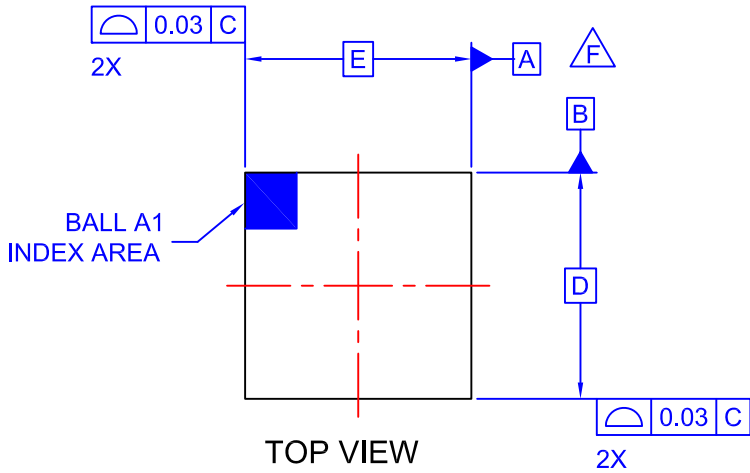
Part Number	Top Mark	Package	D	E	X	Y
FSA644UCX	M7	36-Ball WLCSP, Non-JEDEC 2.36 mm x 2.36 mm, 0.4 mm Pitch	2.36 mm	2.36 mm	0.18 mm	0.18 mm
FSA644BUCX	KM	36-Ball WLCSP, Non-JEDEC 2.415 mm x 2.415 mm, 0.4 mm Pitch	2.415 mm	2.415 mm	0.208 mm	0.208 mm



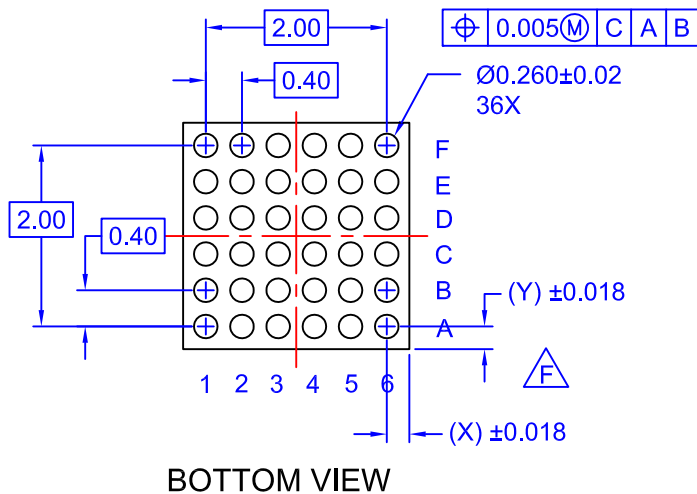


## NOTES

- A. NO JEDEC REGISTRATION APPLIES.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCE PER ASMEY14.5M, 1994.
- D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
- E. PACKAGE NOMINAL HEIGHT IS  $500 \pm 39$  MICRONS (461-539 MICRONS).
- F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.
- G. DRAWING FILNAME: MKT-UC036AArev1.



SIDE VIEWS



NOTES

- A. NO JEDEC REGISTRATION APPLIES.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCE PER ASMEY14.5M, 2009.
- D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
- E. PACKAGE NOMINAL HEIGHT IS  $495 \pm 39$  MICRONS (456-534 MICRONS).
- F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.
- G. DRAWING FILNAME: MKT-UC036AB REV1.



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