High-Efficiency Notebook Computer Power Supply Controller

ADP3020

FEATURES

Wide Input Voltage Range: 4.5 V to 25 V
High Conversion Efficiency > 96%
Integrated Current Sense—No External Resistor Required
Low Shutdown Current: 7 μA (Typical)
Dual Synchronous Buck Controllers with Selectable PWM/Power-Saving Mode Operation
Built-In Gate Drive Boost Circuit for Driving External N-Channel MOSFETs
Two Independently Programmable Output Voltages
Fixed 3.3 V or Adjustable (1.25 V to VIN–0.5 V)
Fixed 5 V or Adjustable (1.25 V to VIN–0.5 V)
Programmable PWM Frequency
Integrated Linear Regulator Controller
Extensive Circuit Protection Functions
38-Lead TSSOP Package

APPLICATIONS

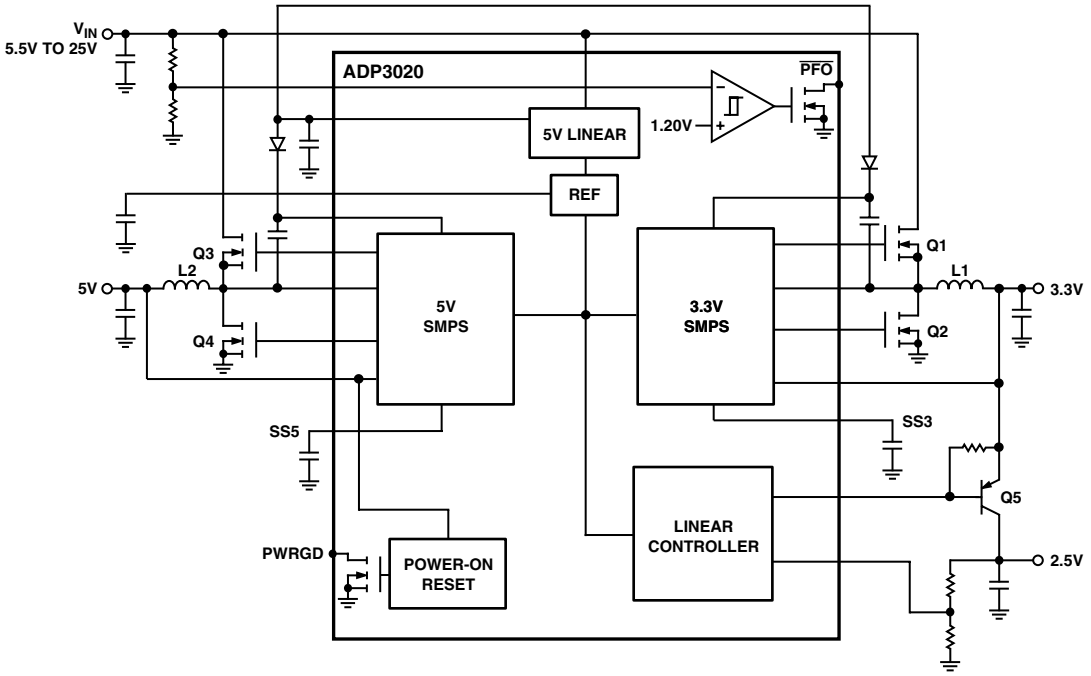
Notebook Computers and PDAs
Portable Instruments
General Purpose DC-DC Converters

GENERAL DESCRIPTION

The ADP3020 is a highly efficient dual synchronous buck switching regulator controller optimized for converting the battery or adapter input into the system supply voltages required in notebook computers. The ADP3020 uses a dual-mode PWM/Power Saving Mode architecture to maintain efficiency over a wide load range. The oscillator frequency can be programmed for 200 kHz, 300 kHz, or 400 kHz operation, or it can be synchronized to an external clock signal of up to 600 kHz.

The ADP3020 provides accurate and reliable short circuit protection using an internal current sense circuit, which reduces cost and increases overall efficiency. Other protection features include programmable soft-start, UVLO, and integrated output undervoltage/overvoltage protection. The ADP3020 contains a linear regulator controller that is designed to drive an external P-channel MOSFET or PNP transistor. The linear regulator output is adjustable, and can be used to generate the auxiliary voltages required in many laptop designs.

FUNCTIONAL BLOCK DIAGRAM



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ADP3020—SPECIFICATIONS (@ T_A = –40°C to +85°C, VIN = 12 V, SS5 = SS3 = INTVCC, INTVCC Load = 0 mA, REF Load = 0 mA, MODE = 0 V, SYNC = 0 V, $\overline{SD}$ = 5 V, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INTERNAL 5 V REGULATOR	INTVCC					
Input Voltage Range			5.5		25	V
5 V Voltage		T_A = 25°C	4.95	5.025	5.15	V
Line Regulation		5.5 V ≤ VIN ≤ 25 V		0.3		mV/V
Total Variation		Line, Temp	4.8		5.2	V
Switchover Voltage		AUXVCC from Low to High	4.65	4.75	4.85	V
Switchover Hysteresis		AUXVCC from High to Low		100		mV
Undervoltage Lockout Threshold Voltage		INTVCC Falling	3.6	3.8	4.2	V
Undervoltage Lockout Hysteresis				120		mV
REFERENCE						
Output Voltage[2]	REF	5.5 V ≤ VIN ≤ 25 V	1.185	1.197	1.209	V
SUPPLY CURRENT	I_Q					
Shutdown Current		$\overline{SD}$ = 0 V		7	15	µA
Standby Current		SS3 = SS5 = $\overline{SD2}$ = 0 V $\overline{SD}$ = 5 V		250	400	µA
Quiescent Current (PWM Mode)		No Loads, MODE = 5 V SS3 = SS5 = $\overline{SD2}$ = 5 V FB5 = FB3 = FB2 = 1.25 V, ADJ/$\overline{FX5}$ = ADJ/$\overline{FX3}$ = 5 V		0.95	1.8	mA
Quiescent Current (Power-Saving Mode)		No Loads, MODE = 0 V SS3 = SS5 = SD2 = 5 V FB5 = FB3 = FB2 = 1.25 V, ADJ/$\overline{FX5}$ = ADJ/$\overline{FX3}$ = 5 V		650		µA
OSCILLATOR						
Frequency	f_{OSC}	SYNC = AGND	176	200	224	kHz
		SYNC = REF	264	300	336	kHz
		SYNC = INTVCC	352	400	448	kHz
SYNC Input						
Frequency Range			230		600	kHz
Input Low Voltage[3]		t_F ≤ 200 ns			0.4	V
Input High Voltage[3]		t_R ≤ 200 ns	4.6			V
Input Current		SYNC = REF		1.2		µA
POWER GOOD	PWRGD					
Output Voltage In Regulation		10 kΩ Pull-Up to 5 V	4.8			V
Output Voltage Out of Regulation		10 kΩ Pull-Up to 5 V FB5 < 90% of Nominal Output Value			0.4	V
PWRGD Trip Threshold		FB5 Rising	–8	–4	–2	%
PWRGD Hysteresis		FB5 Falling		4		%
CPOR Pull-Up Current		CPOR = 1.2 V		2.5		µA
ERROR AMPLIFIER						
DC Gain				67		dB
Gain-Bandwidth Product	GBW			10		MHz
Input Leakage Current	I_{EAN}	ADJ/$\overline{FX5}$ = ADJ/$\overline{FX3}$ = 5 V			200	nA
MAIN SMPS CONTROLLERS						
Fixed 5 V Output Voltage	FB5					
PWM Mode		5.5 V ≤ VIN ≤ 25 V, ADJ/$\overline{FX5}$ = 0 V	4.90	5.0	5.10	V
Power-Saving Mode		5.5 V ≤ VIN ≤ 25 V, ADJ/$\overline{FX5}$ = 0 V	4.925	5.025	5.125	V
Fixed 3.3 V Output Voltage	FB3					
PWM Mode		5.5 V ≤ VIN ≤ 25 V, ADJ/$\overline{FX3}$ = 0 V	3.234	3.3	3.366	V
Power-Saving Mode		5.5 V ≤ VIN ≤ 25 V, ADJ/$\overline{FX3}$ = 0 V	3.250	3.316	3.382	V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Adjustable Output Voltage						
PWM Mode	EAN5, EAN3	5.5 V ≤ VIN ≤ 25 V, ADJ/$\overline{FX5}$ = ADJ/$\overline{FX3}$ = 5 V	1.173	1.197	1.221	V
Power-Saving Mode	FB5, FB3	5.5 V ≤ VIN ≤ 25 V, ADJ/$\overline{FX5}$ = ADJ/$\overline{FX3}$ = 5 V	1.179	1.203	1.227	V
Output Voltage Adjustment Range[3]	FB5, FB3	ADJ/$\overline{FX5}$ = ADJ/$\overline{FX3}$ = 5 V	1.25		VIN–0.5	V
Current Limit Threshold (PWM Mode)						
CLSET5 = CLSET3 = Floating		5.5 V ≤ VIN ≤ 25 V, T_A = 25°C	54	72	90	mV
CLSET5 = CLSET3 = 0 V		5.5 V ≤ VIN ≤ 25 V, T_A = 25°C	115	144	173	mV
Current Limit Threshold (Power-Saving Mode)						
CLSET5 = CLSET3 = Floating		5.5 V ≤ VIN ≤ 25 V, T_A = 25°C		16		mV
CLSET5 = CLSET3 = 0 V		5.5 V ≤ VIN ≤ 25 V, T_A = 25°C		35		mV
Power-Saving Mode Trip Threshold		CLSET5 = CLSET3 = 0 V, T_A = 25°C		28		mV
Soft-Start Current		SS3 = SS5 = 3 V		4		µA
Soft-Start Turn-On Threshold	SS5, SS3		0.7	1.2	1.8	V
Feedback Input Leakage Current	I_{FB}	ADJ/$\overline{FX5}$ = ADJ/$\overline{FX3}$ = 5 V, FB = 1.2 V			200	nA
Maximum Duty Cycle[3]	D_{MAX}	VIN = 5.5 V, SYNC = AGND	94	99		%
Transition Time (DRVH/DRVL)						
Rise	t_R	C_{LOAD} = 3000 pF, 10%–90%		40	70	ns
Fall	t_F	C_{LOAD} = 3000 pF, 90%–10%		40	70	ns
Logic Input Low Voltage		MODE, $\overline{SD}$, ADJ/$\overline{FX3}$, ADJ/$\overline{FX5}$			0.6	V
Logic Input High Voltage		MODE, $\overline{SD}$, ADJ/$\overline{FX3}$, ADJ/$\overline{FX5}$	2.4			V
LINEAR REGULATOR CONTROLLER						
Feedback Threshold	FB2		1.176	1.20	1.224	V
$\overline{SD2}$ Pull-Up Current	$\overline{SD2}$	$\overline{SD2}$ = 1.2 V		4		µA
$\overline{SD2}$ Threshold			0.7	1.2	1.8	V
Current Sinking Capability	DRV2	DRV2 = 2 V, FB2 = 1 V, $\overline{SD2}$ = 5 V	20	45		mA
FB2 Input Leakage Current	I_{FB}	FB2 = 1.2 V		50		nA
POWER-FAIL COMPARATOR						
PFI Input Threshold		$\overline{PFO}$ from High to Low	1.176	1.20	1.224	V
PFI Input Hysteresis				24		mV
PFI Input Current					200	nA
$\overline{PFO}$ High Voltage		10 kΩ Pull-Up to 5 V	4.8			V
$\overline{PFO}$ Low Voltage		10 kΩ Pull-Up to 5 V			0.4	V
FAULT PROTECTION						
Output Overvoltage Trip Threshold		With Respect to Nominal Output	115	120	125	%
Output Undervoltage Lockout Threshold		With Respect to Nominal Output	75	80	85	%

NOTES
[1]All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.
[2]The reference's line-regulation error is insignificant. The reference cannot be used for external load.
[3]Guaranteed by design, not tested in production.

Specifications subject to change without notice.

PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1	CS5	Current Sense Input for top N-Channel MOSFET of the 5 V Buck Converter. Connect to the drain of the top N-channel MOSFET.
2	FB5	Feedback Input for the 5 V Buck Converter. Connect to the output sense point in fixed output mode. Connect to an external resistor divider in adjustable output mode.
3	EAN5	Inverting Input of the Error Amplifier of the 5 V Buck Converter. Use for external loop compensation only in fixed output mode. In adjustable output mode, connect to an external resistor divider.
4	EAO5	Error Amplifier Output for the 5 V Buck Converter.
5	ADJ/$\overline{\text{FX5}}$	TTL Logic Input. When ADJ/$\overline{\text{FX5}}$ = 0 V, fixed output mode, connect FB5 to the output sense point. When ADJ/$\overline{\text{FX5}}$ = 5 V, adjustable output mode, connect FB5 to the external resistor divider.
6	SS5	Soft Start for the 5 V Buck Converter. Also used as an ON/OFF Pin.
7	CLSET5	Current Limit Setting. A resistor can be connected from AGND to CLSET5. A minimum current limit is obtained by leaving it unconnected. A max current limit is obtained by connecting it to AGND.
8	REF	1.2 V Bandgap Reference. Bypass it with a capacitor (1 nF typical) to AGND. REF cannot be used directly with an external load.
9	AGND	Analog Signal Ground.
10	CLSET3	Current Limit Setting. A resistor can be connected from AGND to CLSET3. A minimum current limit is obtained by leaving it unconnected. A max current limit is obtained by connecting it to AGND.
11	MODE	TTL Logic Input. MODE = 5 V, always in constant frequency PWM mode; MODE = 0 V, PWM mode at moderate and heavy loads, and Power Saving (PSV) Mode at light load.
12	SYNC	Oscillator Synchronization and Frequency Select. f_{OSC} = 200 kHz, when SYNC = 0 V; f_{OSC} = 300 kHz, if SYNC is tied to the REF Pin; f_{OSC} = 400 kHz, when SYNC = 5 V. Oscillator can be synchronized with an external source through the SYNC Pin.
13	SS3	Soft Start for the 3.3 V Buck Converter. Also used as an ON/OFF Pin
14	ADJ/$\overline{\text{FX3}}$	TTL Logic Input. When ADJ/$\overline{\text{FX3}}$ = 0 V, fixed output mode, connect FB3 to the output sense point. When ADJ/$\overline{\text{FX3}}$ = 5 V, adjustable output mode, connect FB3 to external resistor divider.
15	EAO3	Error Amplifier Output for the 3.3 V Buck Converter.
16	EAN3	Error Amplifier Inverting Input of the 3.3 V Buck Converter. Use for external loop compensation only in fixed output mode. In adjustable output mode, connect to an external resistor divider.
17	FB3	Feedback Input for the 3.3 V Buck Converter. Connect to output sense point in fixed output mode. Connect to an external resistor divider in adjustable output mode.
18	CS3	Current Sense Input for Top N-Channel MOSFET of the 3.3 V Buck Converter. It should be connected to the drain of the N-channel MOSFET.
19	PFI	The (–) Input of a comparator that can be used as a power fail detector. The positive input is connected to the 1.20 V reference. There is a 24 mV hysteresis for this comparator.
20	$\overline{\text{PFO}}$	Open Drain Output. This pin will sink current when the PFI pin is lower than 1.20 V. Otherwise, $\overline{\text{PFO}}$ is floating.
21	PWRGD	Power Good Output. PWRGD goes low with no delay, whenever the 5 V output drops 8% below its nominal value. When the 5 V output is within –4% of its nominal value, PWRGD will be released after a time delay determined by the timing capacitor on the CPOR pin.
22	CPOR	Connect a capacitor between CPOR and AGND to set the delay time for the PWRGD pin. A 2.5 µA pull-up current is used to charge the capacitor. A manual reset ($\overline{\text{MR}}$) function can also be implemented by grounding this pin.
23	$\overline{\text{SD2}}$	Shutdown input for the Linear Regulator Controller.
24	FB2	Feedback for the Linear Regulator Controller.
25	DRV2	Open Collector Output for the Linear Regulator Controller.
26	BST3	Boost Capacitor Connection for High Side Gate Driver of the 3.3 V Buck Converter.
27	DRVH3	High Side Gate Driver for 3.3 V Buck Converter.
28	SW3	Switching Node (Inductor) Connection of the 3.3 V Buck Converter.
29	DRVL3	Low Side Gate Driver of 3.3 V Buck Converter.
30	VIN	Main Supply Input (4.5 V to 25 V).

PIN FUNCTION DESCRIPTIONS (Continued)

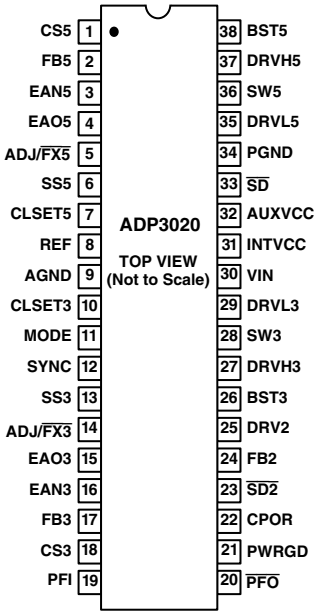
Pin No.	Mnemonic	Function
31	INTVCC	Linear Regulator Bypass for the internal 5 V LDO. Bypass this pin with a 4.7 µF capacitor to AGND.
32	AUXVCC	Supply Switch Over. When AUXVCC > 4.75 V, and both of the switchers are in Power Saving mode, the internal 5 V LDO is turned off. The chip is powered by AUXVCC pin. There is a 2% hysteresis for this pin.
33	$\overline{SD}$	Shutdown Control Input, Active Low. If $\overline{SD}$ = 0 V, the chip is in shutdown with very low quiescent current. For automatic start-up, connect $\overline{SD}$ to V_{IN} directly.
34	PGND	Power Ground.
35	DRVL5	Low Side Driver for 5 V Buck Converter.
36	SW5	Switching Node (Inductor) Connection for 5 V Buck Converter.
37	DRVH5	High Side Gate Driver for 5 V Buck Converter.
38	BST5	Boost Capacitor Connection for High Side Gate Driver of the 5 V Buck Converter.

ABSOLUTE MAXIMUM RATINGS*

VIN to AGND . . . . . –0.3 V to +27 V
AGND to PGND . . . . . ±0.3 V
INTVCC . . . . . AGND – 0.3 V to +6 V
BST5, BST3 to PGND . . . . . –0.3 V to +32 V
BST5 to SW5 . . . . . –0.3 V to +6 V
BST3 to SW3 . . . . . –0.3 V to +6 V
CS5, CS3 . . . . . AGND – 0.3 V to VIN
SW3, SW5 to PGND . . . . . –0.3 V to VIN + 0.3 V
$\overline{SD}$ . . . . . AGND – 0.3 V to +27 V
DRVL5/3 to PGND . . . . . –0.3 V to (INTVCC + 0.3 V)
DRVH5/3 to SW5/3 . . . . . –0.3 V to (INTVCC + 0.3 V)
All Other Inputs and Outputs
. . . . . AGND – 0.3 V to INTVCC + 0.3 V
θ_{JA} . . . . . 98°C/W
Operating Ambient Temperature Range . . . . –40°C to +85°C
Junction Temperature Range . . . . . –40°C to +150°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 10 sec) . . . . . 300°C

*This is a stress rating only; operation beyond these limits can cause the device to be permanently damaged.

PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADP3020ARU	–40°C to +85°C	Thin Shrink Small Outline	RU-38

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADP3020 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

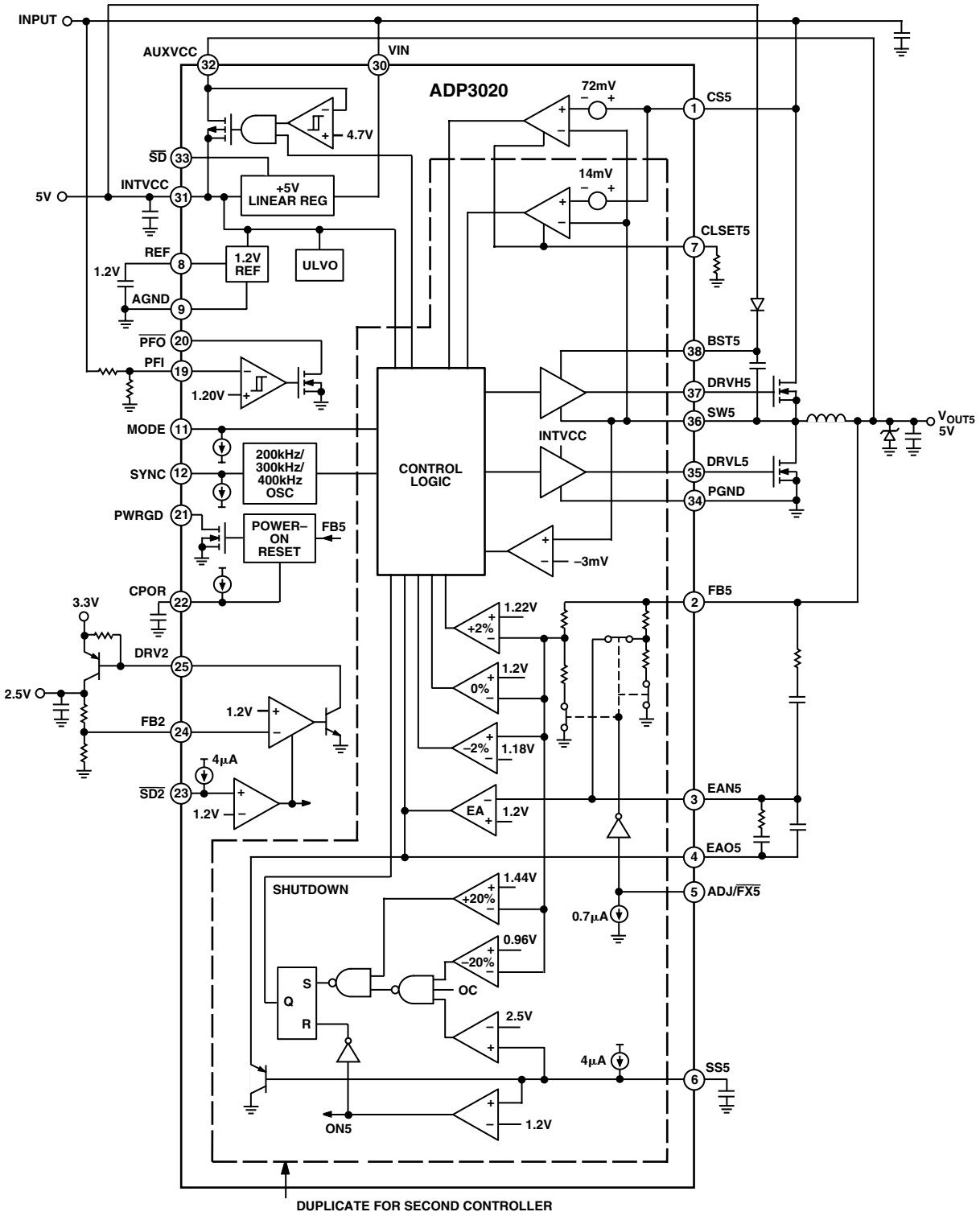


Figure 1. Block Diagram (All Switches and Components Are Shown for Fixed Output Operation)

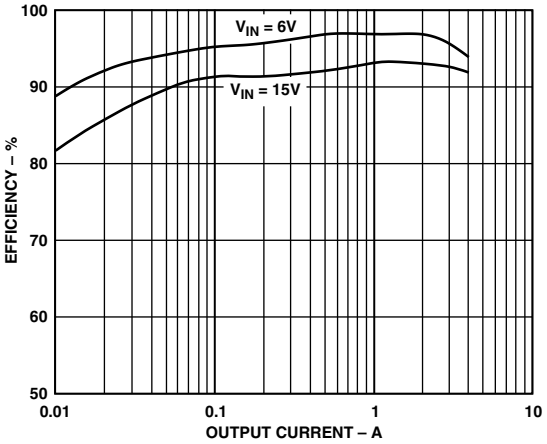


Figure 2. Efficiency vs. 5 V Output Current

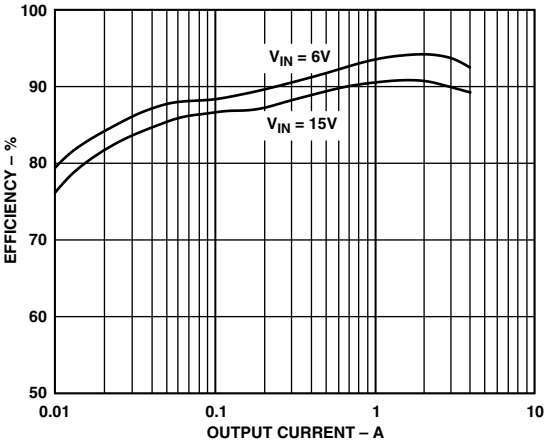


Figure 3. Efficiency vs. 3.3 V Output Current

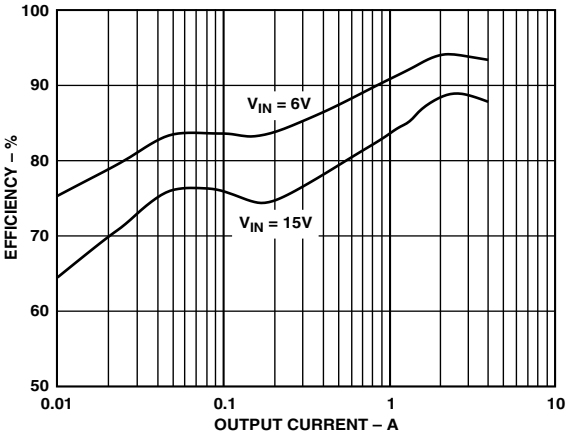


Figure 4. Efficiency vs. 2.5 V Output Current

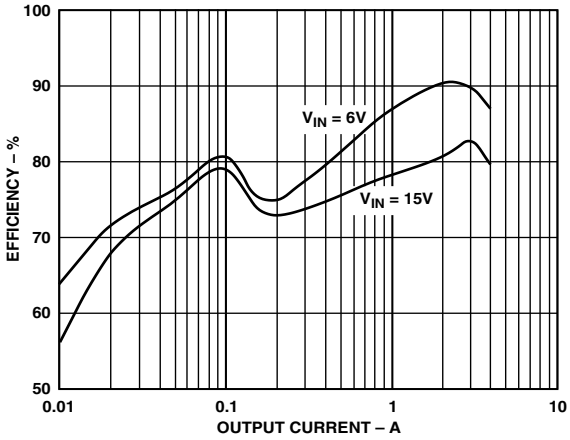


Figure 5. Efficiency, 1.5 V Output Current

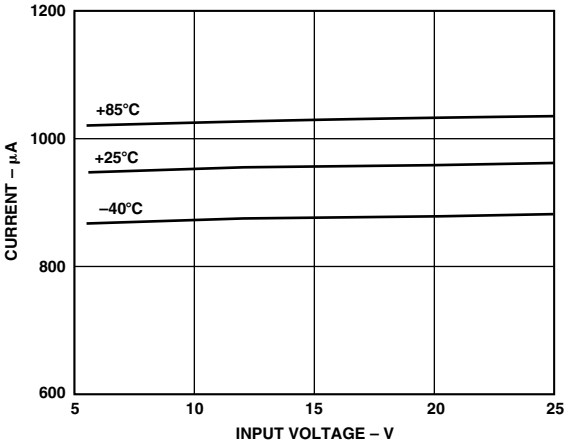


Figure 6. PWM Mode Input Current vs. Input Voltage

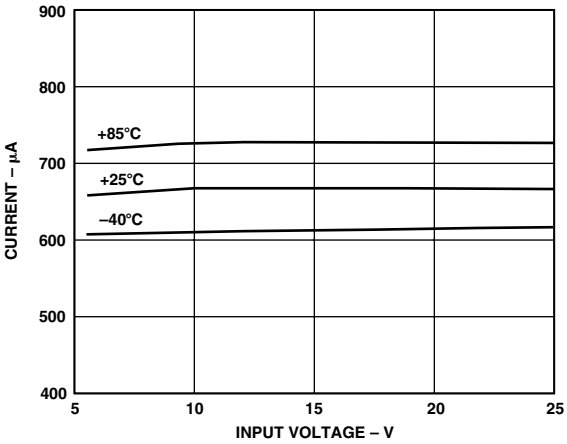


Figure 7. PSV Mode Input Current vs. Input Voltage

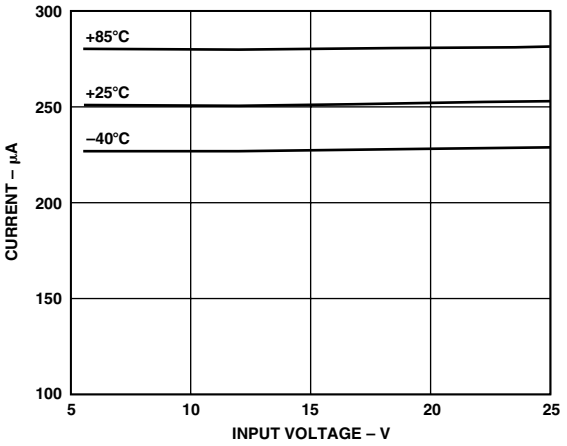


Figure 8. Input Standby Current vs. Input Voltage

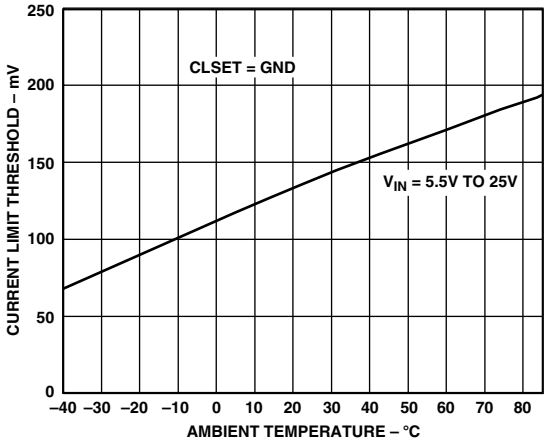


Figure 11. Current Limit Threshold vs. Temperature

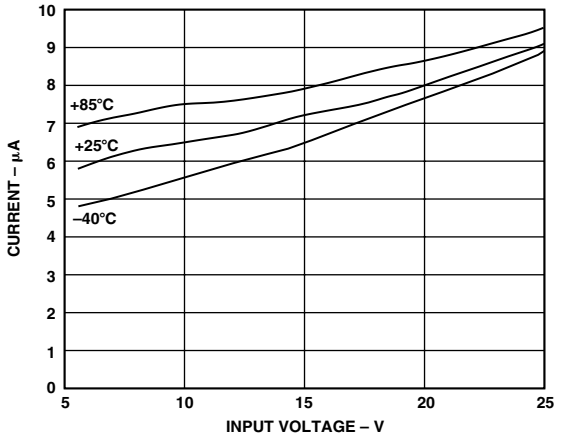


Figure 9. Input Shutdown Current vs. Input Voltage

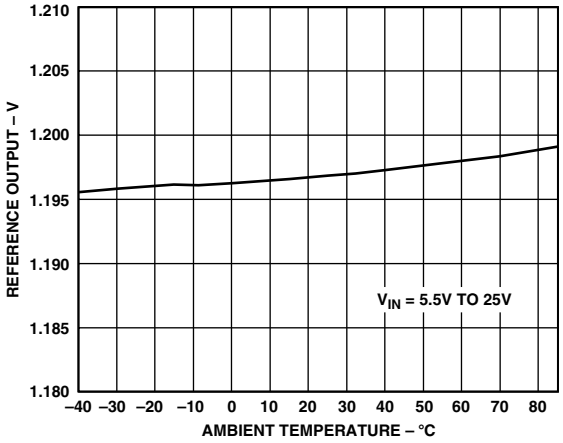


Figure 12. Reference Output vs. Temperature

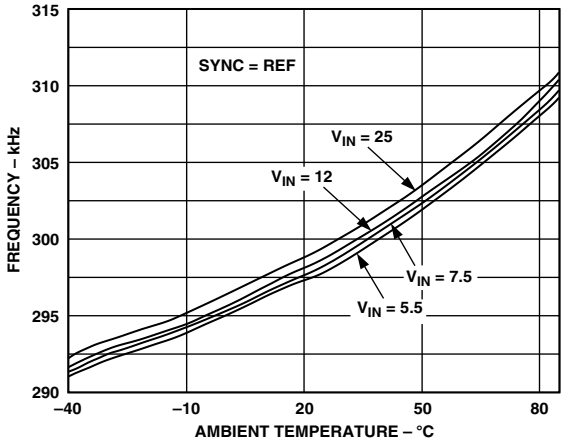


Figure 10. PWM Mode Oscillator Frequency vs. Temperature

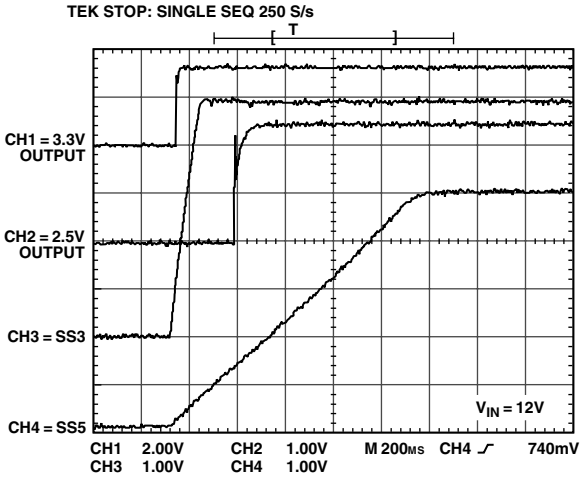


Figure 13. Soft-Start Sequencing

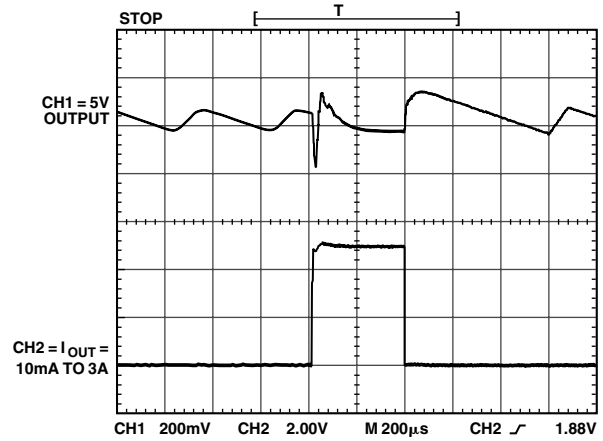


Figure 14. Power-Saving Mode, Transient Response

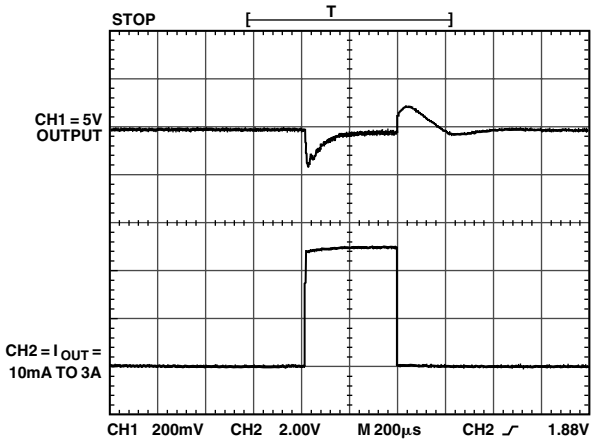


Figure 16. PWM Mode, Transient Response

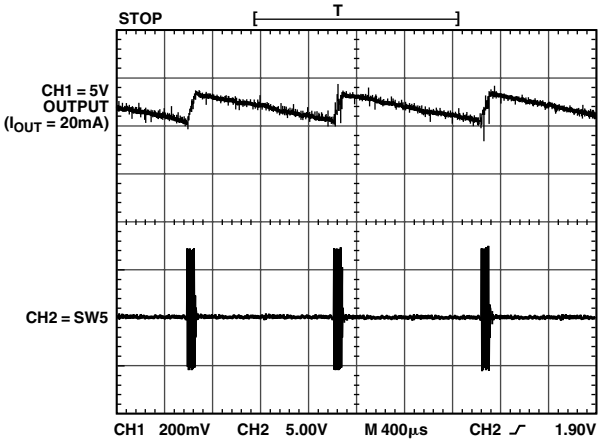


Figure 15. Power-Saving Mode, Waveforms

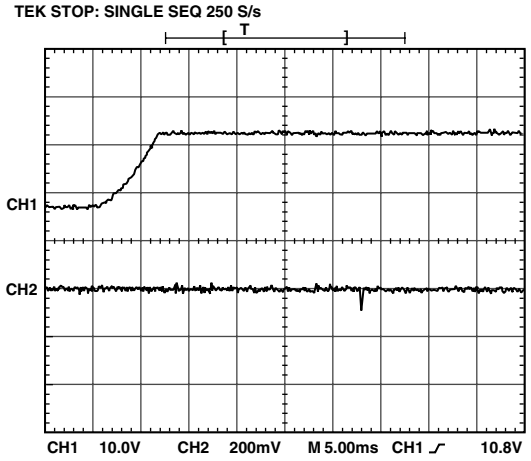


Figure 17. V_{IN} = 7.5 V to 22 V Transient, 2.5 V Output, CH1 – Input Voltage, CH2 – Output Voltage

THEORY OF OPERATION

The ADP3020 is a dual-mode, step-down power supply controller for notebook computers or similar battery-powered applications. The device contains two synchronous step-down buck controllers and a linear regulator controller. The buck controllers in the ADP3020 have the ability to provide either fixed 3.3 V and 5 V outputs or independently adjustable (1.25 V to VIN–0.5 V) outputs. High efficiency over a broad load range is achieved by using a proprietary dual-mode PWM/power-saving (PSV) mode architecture. Efficiency is further improved by deleting the external current sense resistor, which is the main contributor to loss during high current, low output voltage conditions.

CIRCUIT DESCRIPTION

Dual-Mode Architecture

The ADP3020 contains two independent dual-mode, synchronous buck controllers. Traditional constant frequency PWM buck converters suffer from relatively low efficiency under light load conditions. In order to maintain high efficiency over a wide load range, the ADP3020 uses a proprietary dual-mode architecture. At moderate to heavy loads, the buck converter operates in the traditional Pulsewidth Modulation (PWM) mode. At light loads, PSV mode is used to increase system efficiency. A proprietary detection scheme is used for transition from one mode to the other. Input current to the high-side MOSFET is detected when going from PWM mode to PSV mode, and output voltage information is used when changing from PSV mode to PWM mode.

When the high-side N-channel MOSFET is turned on, the current going through the N-channel MOSFET is measured as a voltage between CS and SW. If the peak current through the MOSFET is less than 20% of the current limit value set by CLSET, an internal counter that is based on the oscillator frequency will be started. If the current stays below this threshold for 16 PWM cycles, the buck converter will enter power-saving mode. The counter will automatically reset if the peak current is higher than 20% of the current limit value any time prior to when the counter reaches 16.

In PSV mode, the buck converter works like a window regulator. If the output voltage drops below the PWM mode nominal output voltage, the high-side MOSFET will be turned on. It will remain on until the output capacitors are charged up to 2% above the PWM mode nominal output voltage. The high-side MOSFET will then be latched off until the output capacitors are discharged to the lower threshold. The discharge rate is dependent on the output capacitor value and load current.

It is important to note that the current limit threshold when in PSV mode is approximately 1/4 of the current limit threshold when in PWM mode. If a large load is applied to the converter when in PSV mode (for example, larger than the current limit in PSV mode), the output will continue to drop due to the lower current limit threshold of PSV mode. When the output voltage drops to 2% below the PWM mode nominal voltage, the converter will automatically return to PWM mode. Once in PWM mode, the current limit is quadrupled, and the output will be charged up to the nominal level, as long as the load does not exceed the higher PWM current limit.

PWM/PSV Operation (MODE)

Table I shows the summary of the operating modes of the synchronous buck controllers. The MODE pin determines whether or not the controllers remain in PWM mode under all load conditions. MODE can be driven by an external TTL logic signal. When MODE is pulled HIGH, PSV mode operation is disabled, and the system is always in constant frequency PWM mode. In order to enable PSV mode at light loads, the MODE pin needs to be pulled LOW.

Table I. PWM Mode and PSV Mode

Mode	Load Current	Operating Mode	Description
High	X	PWM	Constant-Frequency PWM
Low	Heavy	PWM	Constant-Frequency PWM
Low	Moderate	PWM	Constant-Frequency PWM
Low	Light	PSV	Variable-Frequency, Burst Mode

X = Don't Care.

Forcing the ADP3020 to always remain in constant frequency PWM mode can be used to reduce interference, as this allows filtering of the fixed fundamental frequency and its harmonics. The operating frequency should be carefully chosen so that both the fundamental and harmonic frequencies are not within sensitive audio or IF bands. This is particularly important in noise-sensitive applications such as multimedia systems, cellular phones, computers with built-in RF communications, and PDAs. If two or more switching regulators are used in a system, it is best to synchronize all the switching regulators to a single master regulator or an external clock signal.

Internal 5 V Supply (INTVCC)

An internal low dropout regulator (LDO) generates a 5 V supply (INTVCC) that powers all of the functional blocks within the IC. The total current rating of this LDO is 50 mA. However, this current is used for supplying gate-drive power, and it is not recommended that current be drawn from this pin for other purposes. Bypass INTVCC to AGND with a 4.7 µF capacitor. A UVLO circuit is also included in the regulator. When INTVCC < 3.8 V, the two switching regulators and the linear regulator controller are shut down. The UVLO hysteresis voltage is about 120 mV. The internal LDO has a built-in fold-back current limit, so that it will be protected if a short circuit is applied to the 5 V output.

If AUXVCC is higher than 4.75 V, and both the 5 V and 3.3 V switching regulators are in PSV mode, an internal switch will connect INTVCC to AUXVCC, while simultaneously turning off the internal LDO. AUXVCC can be tied to either the 5 V switching regulator output or a separate 5 V voltage source. By doing this, the power loss across the internal LDO is eliminated, and the total efficiency in PSV mode is improved.

When AUXVCC = GND, this automatic power switchover feature will be disabled.

Internal Reference (REF)

The ADP3020 contains a precision 1.2 V bandgap reference. Bypass REF to AGND with a 1 nF ceramic capacitor. The reference is intended for internal use only. An external voltage buffer is needed if the reference is used for another purpose.

Boost High Side Gate Drive Supply (BST)

The gate drive voltage for the high-side N-channel MOSFETs is generated by a flying-capacitor boost circuit. The boost capacitor connected between BST and SW is charged from the INTVCC supply. Use only small-signal diodes for the boost circuit.

Synchronous Rectifier (DRVL)
Synchronous rectification is used to reduce conduction losses and to ensure proper start-up of the boost gate driver circuit. Antishoot-through protection has been included to prevent cross conduction during switch transitions. The low side driver must be turned off before the high side driver is turned on. For typical N-channel MOSFETs, the dead time is about 50 ns. On the other edge, a dead time of about 50 ns is achieved by an internal delay circuit. The synchronous rectifier is turned off when the current flowing through the low-side MOSFET falls to zero when in Discontinuous Conduction (DCM) PWM mode and PSV mode. In Continuous Conduction (CCM) PWM mode, the current flowing through the low-side MOSFET never reaches zero, so the synchronous rectifier is turned off by the next clock cycle.

Oscillator Frequency and Synchronization (SYNC)
The SYNC pin controls the oscillator frequency. When SYNC = 0 V, f_{OSC} = 200 kHz ; when SYNC = REF, f_{OSC} = 300 kHz; when SYNC = 5 V, f_{OSC} = 400 kHz. 400 kHz operation will minimize external component size and cost while 200 kHz operation provides better efficiency and lower dropout. The SYNC pin can also be used to synchronize the oscillator with an external 5 V clock signal. A low-to-high transition on SYNC initiates a new cycle. Synchronization range is 230 kHz to 600 kHz.

Shutdown ($\overline{SD}$)
Holding $\overline{SD}$ = GND low will put the ADP3020 into ultralow current shutdown mode. For automatic start-up, $\overline{SD}$ can be tied directly to VIN.

Soft-Start and Power-Up Sequencing (SS)
SS3 and SS5 are soft start pins for the two controllers. A 4 µA pull-up current is used to charge an external soft start capacitor. Power-up sequencing can be easily done by choosing different size external capacitors. When SS3/SS5 < 1.2 V, the two switching regulators are turned off. When 1.2 V < SS5/SS3 < 2.6 V, the regulators start working in soft start mode. When SS3/SS5 > 2.6 V, the regulators are in normal operating mode. The controllers are forced to stay in PWM mode during the soft-start period. The minimum soft-start time (~20 µs) is set by an internal capacitor. Table II shows the ADP3020 operating modes.

Current Limiting (CLSET)
A cycle-by-cycle current limiting scheme is used by monitoring current through the top N-channel MOSFET when it is turned on. By measuring the voltage drop across the high-side MOSFET $V_{DS(ON)}$, the external sense resistor can be deleted. The current limit value can be set by CLSET. When CLSET = Floating, the maximum $V_{DS(ON)}$ = 72 mV at room temperature; when CLSET = 0 V, the maximum $V_{DS(ON)}$ = 144 mV at room temperature. An external resistor can be connected between CLSET and AGND to choose a value between 72 mV and 144 mV. The temperature coefficient of $R_{DS(ON)}$ of the N-channel MOSFET is canceled by the internal current limit circuitry, so that an accurate current limit value can be obtained over a wide temperature range. In PSV mode, the current limit value is reduced to about 1/4 of the value in PWM mode to reduce the interference noise to other components on the PC board.

Output Undervoltage Protection
Each switching controller has an undervoltage protection circuit. When the current flowing through the high-side MOSFET reaches the current limit continuously for eight clock cycles, and the output voltage is below 20% of the nominal output voltage, both controllers will be latched off and will not restart until $\overline{SD}$ or SS3/SS5 is toggled, or until VIN is cycled below 4 V. This feature is disabled during soft start.

Output Overvoltage Protection
Both converter outputs are continuously monitored for overvoltage. If either output voltage is higher than the nominal output voltage by more than 20%, both converter's high-side gate drivers (DRVH5/3) will be latched off, and the low-side gate drivers will be latched on, and will not restart until $\overline{SD}$ or SS5/SS3 are toggled, or until VIN is cycled below 4 V. The low-side gate driver (DRVL) is kept high when the controller is in off-state and the output voltage is less than 93% of the nominal output voltage. Discharging the output capacitors through the main inductor and low-side N-channel MOSFET will cause the output to ring. This will make the output momentarily go below GND. To prevent damage to the circuit, use a reverse-biased 1 A Schottky diode across the output capacitors to clamp the negative surge.

Power Good Output (PWRGD)
The ADP3020 also provides a PWRGD signal for the microprocessor. During start-up, the PWRGD pin is held low until 5 V output is within –4% of its preset voltage. Then, after a time delay determined by an external timing capacitor connected from CPOR to GND, PWRGD will be actively pulled up to INTVCC by an external pull-up resistor. CPOR can also be used as a manual reset ($\overline{MR}$) function. When the 5 V output is lower than the preset voltage by more than 8%, PWRGD is immediately pulled low.

Linear Regulator Controller
The ADP3020 includes an onboard linear regulator controller. An external PNP transistor can be used for operation up to 1 A. For higher output current applications, a low threshold PMOS can be used as the pass transistor. The output voltage can be set by a resistor divider. The minimum output voltage of the LDO is 1.25 V, while the maximum output voltage depends on where the LDO input is connected and the dropout voltage of the external pass transistor.

Table II. Operating Modes

$\overline{SD}$	SS5	SS3	Mode	Description
Low	X	X	Shutdown	All Circuits Turned Off
High	SS5 < 1.2 V	SS3 < 1.2 V	Standby	5 V and 3.3 V Off; INTVCC = 5 V, REF = 1.2 V
High	1.2 V < SS5 < 2.6 V	X	Run	5 V in Soft Start
High	2.6 V < SS5	X	Run	5 V in Normal Operation
High	X	1.2 V < SS3 < 2.6 V	Run	3.3 V in Soft Start
High	X	2.6 V < SS3	Run	3.3 V in Normal Operation

Output Voltage Adjustment

Fixed output voltages (5 V and 3.3 V) are selected when ADJ/$\overline{FX5}$ = ADJ/$\overline{FX3}$ = 0 V. The output voltage of each controller can also be set by an external feedback resistor network when ADJ/FX5 = ADJ/FX3 = 5 V as shown in Figure 18. There should be two external feedback resistor dividers for each controller, one for the voltage feedback loop, and one for output voltage monitor. Both resistor dividers need to be identical. The minimum output voltage is 1.25 V. The maximum output voltage is limited only by the minimum supply voltage. Remote output voltage sensing can be done for both fixed and adjustable output voltage modes.

The output voltage can be calculated using the following formula:

$$V_{OUT} = REF \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

where REF = 1.2 V, and $R1/R2$ = R3/R4.

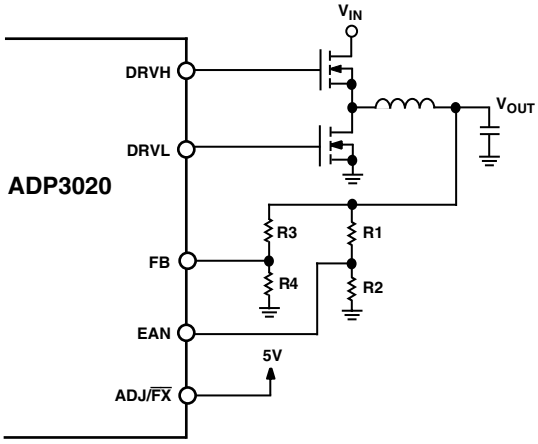


Figure 18. Adjustable Output Mode

If the loop is carefully compensated, R3 and R4 can be, removed, and FB and EAN can be tied together.

APPLICATION INFORMATION

A typical notebook PC application circuit using the ADP3020 is shown in Figure 19. Although the component values given in Figure 19 are based on a 5 V @ 4 A /3.3 V @ 4 A/2.5 V @ 1.5 A design, the ADP3020 output drivers are capable of handling output currents anywhere from <1 A to over 10 A. Throughout this section, design examples and component values will be given for three different power levels. For simplicity, these levels will be referred to as low power, basic, and extended power. Table III shows the input/output specifications for these three levels.

Table III. Typical Power Level Examples

	Low Power	Basic	Extended Power
Input Voltage Range	5.5 V to 25 V	5.5 V to 25 V	5.5 V to 25 V
Switching Output 1	3.3 V/2 A	3.3 V/4 A	3.3 V/10 A
Switching Output 2	5 V/2 A	5 V/4 A	5 V/10 A
Linear Output	2.5 V/1 A	2.5 V/1.5 A	2.5 V/2 A

Input Voltage Range

The input voltage range of the ADP3020 is 5.5 V to 25 V when 5 V output is desired, and 4.5 V to 25 V when neither switcher output is >4.0 V. This converter design is optimized to deliver the best performance within a 7.5 V to 18 V range, which is the nominal voltage for three to four cell Li-Ion battery stacks. Voltages above 18 V may occur under light loads and when the system is powered from an ac adapter with no battery installed.

Maximum Output Current and MOSFET Selection

The maximum output current for each switching regulator is limited by sensing the voltage drop between the drain and source of the high-side MOSFET when it is turned on. A current sense comparator senses voltage drop between CS5 and SW5 for the 5 V converter and between CS3 and SW3 for the 3.3 V converter. The sense comparator threshold is 72 mV when the programming pin, CLSET, is floating, and is 144 mV when CLSET is connected to ground. Current-limiting is based on sensing the peak current. Peak current varies with input voltage and depends on the inductor value. The higher the ripple current or input voltage, the lower the converter maximum output current at the set current sense amplifier threshold. The relation between peak and dc output current is given by:

$$I_{PEAK} = I_{OUT} + V_{OUT} \times \left(\frac{V_{IN(MAX)} - V_{OUT}}{2 \times f \times L \times V_{IN(MAX)}}\right) \quad (2)$$

At a given current comparator threshold V_{TH} and MOSFET $R_{DS(ON)}$, the maximum inductor peak current is:

$$I_{PEAK} = \frac{V_{TH}}{R_{DS(ON)}} \quad (3)$$

Rearranging Equation 2 to solve for $I_{OUT(MAX)}$ gives:

$$I_{OUT(MAX)} = \frac{V_{TH}}{R_{DS(ON)}} - V_{OUT} \times \left(\frac{V_{IN(MAX)} - V_{OUT}}{2 \times f \times L \times V_{IN(MAX)}}\right) \quad (4)$$

Normally, V_{TH} should be set to its maximum value of 144 mV. For example, in the circuit of Figure 19, an Si4410, which has an $R_{DS(ON)}$ of 13.5 mΩ would have a maximum peak current limit of around 10 A. A less efficient way to achieve maximum power from the converter is to design the inductor with a larger inductance, (i.e., a lower ripple current). This helps reduce the peak-to-dc current ratio and increases maximum converter output, but may also increase the inductor value and its size. It is important to remember that this current limit circuit is designed to protect against high current or short circuit conditions only. This will protect the IC and MOSFETs long enough to allow the output undervoltage protection circuitry to latch off the supply.

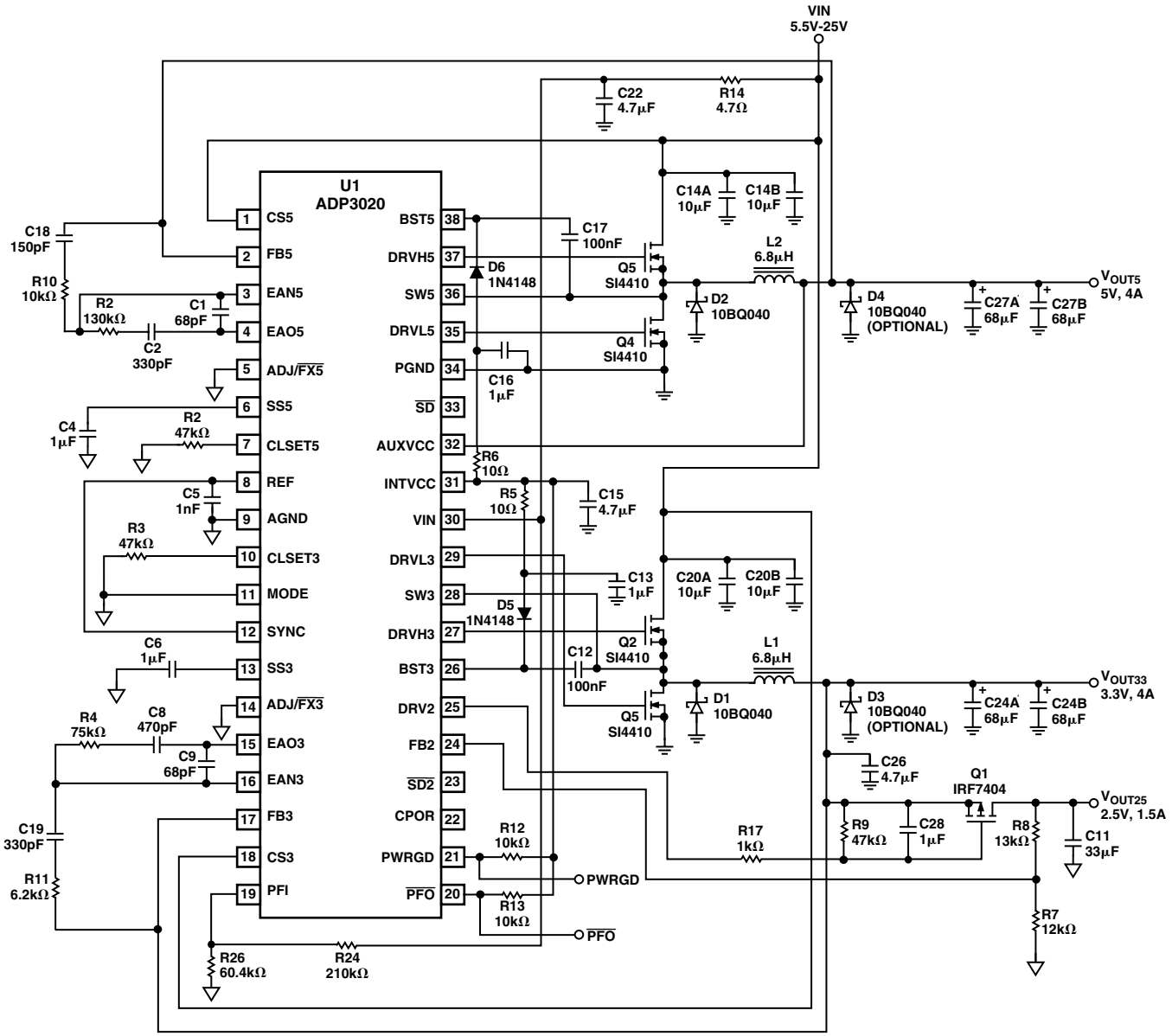


Figure 19. 45 W, Triple Output DC-DC Converter

Nominal Inductor Value

The inductor design is based on the assumption that the inductor ripple current is 30% of the maximum output dc current at nominal 12 V input voltage. The inductor ripple current and inductance value are not critical, but this choice is quite important in analyzing the trade-offs between cost, size, efficiency, and volume. The higher the ripple current, the lower the inductor size and volume. However, this will lead to higher ac losses in the windings. Conversely, a higher inductor value means lower ripple current and smaller output filter capacitors, but transient response will be slower.

The design of the inductor should be based on the maximum output current plus 15% (1/2 of the 30% ripple allowance) at the nominal input voltage:

$$L \geq 3 \times \left(V_{IN(NOM)} - V_{OUT}\right) \times \frac{V_{OUT}}{V_{IN(NOM)} \times I_{OUT} \times f} \qquad (5)$$

Optimum standard inductor values for the three power levels are shown in Table IV.

Table IV. Standard Inductor Values

Freq.	3.3 V/2 A	3.3 V/4 A	3.3 V/10 A	5 V/2 A	5 V/4 A	5 V/10 A
200 kHz	20 µH	8.2 µH	3.3 µH	22 µH	10 µH	4.7 µH
300 kHz	12 µH	6.8 µH	2.2 µH	15 µH	8.2 µH	3.3 µH
400 kHz	10 µH	4.7 µH	1.5 µH	10 µH	6.8 µH	2.2 µH

Inductor Selection

Once the value for the inductor is known, there are two ways to proceed; either to design the inductor in-house or to buy the closest inductor that meets the overall design goals.

Standard Inductors

Buying a standard inductor will provide the fastest, easiest solution, and many companies offer suitable power inductor solutions. A list of power inductor manufacturers is given in Table V.

DESIGNING THE INDUCTOR IN-HOUSE

Core Material Concerns

There are several good choices for low core loss materials at high frequency. Two examples are distributed gap Kool Mu powdered cores from Magnetics and soft ferrite cores, material 3F3, 3F4, 3D3, or 4C4, from Philips. To minimize the ac core loss, especially when the inductor value is relatively low and ripple current is high, the use of low frequency powdered iron cores and low frequency ferrite cores (specified for frequency up to 100 kHz) should be avoided. The ripple current is a key factor for optimization of the converter design and determines core losses to a large extent. Selecting a high ripple current means a relatively low inductor value. This, for a given core size, reflects a lower number of turns and higher core loss.

Core Geometry

There are two main categories of ferromagnetic cores that could be used in this type of application. Open magnetic loop types such as beads, beads on leads, rods, and slugs provide the lowest cost, but do not have focused magnetic fields in the core. The radiated EMI distributed around the magnetic field may create problems with noise interference in electronic circuits surrounding the choke. Other types are cores with closed magnetic paths, such as pot cores, PQ, U, and E cores, toroids, etc. The cost of these cores is higher, but EMI and RFI performance is better. A good compromise between price and performance are cores with a toroidal shape, used primarily in through-hole printing board designs. A very cost-effective solution based, not on closed-loop core, but on good shielded open-loop core, are surface-mount power inductors, DO, DT, and DS Series from Coilcraft.

Table V. Recommended Inductor Manufacturers

Coilcraft	Coiltronics	Murata Electronics North America Inc.
Phone: 847/639-6400 Fax: 847/639-1469 Web: www.coilcraft.com	Phone: 561/241-7876 Fax: 561/241-9339 Web: www.coiltronics.com	Phone: 770/436-1300 Fax: 770/436-3030 Web: www.murata.com
SMT Power Inductors, Series 1608, 3308, 3316, 5022, 5022HC, DO3340, Low Cost Solution SMT Shielded Power Inductors, Series DS5022, DS3316, DT3316, Best for Low EMI/RFI	SMT Power Inductors, Series UNI-PAC2, UNI-PAC3 and UNI-PAC4, Low Cost Solution SMT Power Inductors, Series, ECONO-PAC, VERSA-PAC, Best for Low Profile or Flexible Design.	SMT Power Inductors, Series LQT2535 Best for Low EMI/RFI
Power Inductors and Chokes, Series DC1012, PCV-0, PCV-1, PCV-2, PCH-27, PCH-45, Low Cost	Power Inductors CTX Series, Low EMI/RFI, Low Cost Toroidal Inductors but Not Miniature.	Chip Inductors LQN6C, LQS66C

The Design

The details of designing the power inductor are covered in many reference texts, and will not be covered here. Examples of software and reference books that can be used for quick design of the power inductor are given below:

Software—Magnetic Designer from Intusoft, www.intusoft.com

"Designing Magnetic Components for High Frequency DC-DC Converters," McLyman, Kg Magnetics Inc., ISBN 1-883107-00-08 (for advanced users)

"Power Supply Cookbook," Marty Brown, EDN Series for Design Engineers, ISBN 0-7506-9442-4 (for beginners and intermediate users)

C_{IN} and C_{OUT} Selection

In continuous conduction mode, the source current of the upper MOSFET is approximately a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum rms current must be used. The maximum rms capacitor current is given by:

$$I_{RMS} \approx \sqrt{V_{OUT} \times \left(V_{IN} - V_{OUT}\right)} \times \frac{I_{MAX}}{V_{IN}} \quad (6)$$

This formula has a maximum at $V_{IN} = 2 \times V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. Note that the capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. If electrolytic or tantalum capacitors are used, an additional 0.1 µF–1 µF ceramic bypass capacitor should be placed in parallel with C_{IN}.

The selection of C_{OUT} is driven by the required effective series resistance (ESR) and the desired output ripple. A good rule of thumb is to limit the ripple voltage to 1% of the nominal output voltage. It is assumed that the total ripple is caused by two factors: 25% comes from the C_{OUT} bulk capacitance value, and 75% comes from the capacitor ESR. The value of C_{OUT} can be determined by:

$$C_{OUT} = \frac{I_{RIPPLE}}{2 \times f \times V_{RIPPLE}} \quad (7)$$

where $I_{RIPPLE} = 0.3 \times I_{OUT}$ and $V_{RIPPLE} = 0.01 \times V_{OUT}$. The maximum acceptable ESR of C_{OUT} can then be found using:

$$ESR \leq 0.75 \times \frac{V_{RIPPLE}}{I_{RIPPLE}} \quad (8)$$

Manufacturers such as Vishay, AVX, Elna, WIMA and Sanyo provide good high-performance capacitors. Sanyo's OSCON semiconductor dielectric capacitors have lower ESR for a given size, at a somewhat higher price. Choosing sufficient capacitors to meet the ESR requirement for C_{OUT} will normally exceed the amount of capacitance needed to meet the ripple current requirement.

In surface-mount applications, multiple capacitors may have to be paralleled to meet the capacitance, ESR, or RMS current handling requirements. Aluminum electrolytic and dry tantalum capacitors are available in surface-mount configurations. In the case of tantalum, it is critical that capacitors are surge tested for use in switching power supplies. Recommendations for output capacitors are shown in Table VI.

Power MOSFET Selection

N-channel power MOSFETs must be selected for use with the ADP3020 for both the main and synchronous switch. The main selection parameters for the power MOSFETs are the threshold voltage ($V_{GS(TH)}$) and ON-resistance ($R_{DS(ON)}$). An internal LDO generates a 5 V supply that is boosted above the input voltage using a bootstrap circuit. This floating 5 V supply is used for the upper MOSFET gate drive. Logic-level threshold MOSFETs must be used for both the main and synchronous switches.

Maximum output current (I_{MAX}) determines the $R_{DS(ON)}$ requirement for the two power MOSFETs. When the ADP3020 is operating in continuous mode, the simplifying assumption can be made that one of the two MOSFETs is always conducting the load current. The duty cycles for the MOSFETs are given by:

$$Upper\ MOSFET\ Duty\ Cycle = \frac{V_{OUT}}{V_{IN}} \quad (9)$$

$$Lower\ MOSFET\ Duty\ Cycle = \frac{V_{IN} - V_{OUT}}{V_{IN}} \quad (10)$$

Table VI. Recommended Capacitor Manufacturers

Maximum Output Current	2 A	4 A	10 A
Input Capacitors	TOKIN Multilayer Ceramic Caps, 22 µF/25 V P/N: C55Y5U1E226Z TAIYO YUDEN INC. Ceramic Caps, Y5V Series 10 µF/25 V P/N: TMK432BJ106KM	TOKIN Multilayer Ceramic Caps, 2 × 22 µF/25 V P/N: C55Y5U1E226Z TAIYO YUDEN INC. Ceramic Caps, Y5V Series 2 ×10 µF/25 V P/N: TMK432BJ106KM	TOKIN Multilayer Ceramic Caps, 2 × 22 µF/25 V P/N: C55Y5U1E226Z VISHEY Ceramic Caps, Z5U Series, 2 × 15 µF/25 V
Output Capacitors +3.3 V Output	SANYO POSCAP TPC Series, 68 µF/10 V	SANYO POSCAP TPC Series, 2 × 68 µF/10 V	SANYO POSCAP TPB Series, 2 × 220 µF/4.0 V
Output Capacitors +5 V Output	SANYO POSCAP TPC Series, 68 µF/10 V	SANYO POSCAP TPC Series, 2 × 68 µF/10 V	SANYO POSCAP TPB Series, 2 × 330 µF/6.3 V

From the duty cycle, the required minimum $R_{DS(ON)}$ for each MOSFET can be derived by the following equations:

Upper MOSFET:

$$R_{DS(ON)}(Upper) = \frac{V_{IN} \times P_D}{V_{OUT} \times I_{MAX}^2 \times (1 + \alpha\Delta T)} \quad (11)$$

Lower MOSFET:

$$R_{DS(ON)}(Lower) = \frac{V_{IN} \times P_D}{(V_{IN} - V_{OUT}) \times I_{MAX}^2 \times (1 + \alpha\Delta T)} \quad (12)$$

where P_D is the allowable power dissipation and α is the temperature dependency of $R_{DS(ON)}$. P_D will be determined by efficiency and/or thermal requirements (see Efficiency). $(1 + \alpha\Delta T)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs. temperature curve, but α = 0.007/°C can be used as an approximation for low voltage MOSFETs.

Maximum MOSFET power dissipation occurs at maximum output current, and can be calculated as follows:

Upper MOSFET:

$$P_D(Upper) = \frac{V_{OUT}}{V_{IN}} \times I_{MAX}^2 \times R_{DS(ON)} \times (1 + \alpha\Delta T) \quad (13)$$

Lower MOSFET:

$$P_D(Lower) = \frac{V_{IN} - V_{OUT}}{V_{IN}} \times I_{MAX}^2 \times R_{DS(ON)} \times (1 + \alpha\Delta T) \quad (14)$$

The Schottky diode, D1 shown in Figure 19, conducts only during the dead time between conduction of the two power MOSFETs. D1's purpose is to prevent the body-diode of the lower N-channel MOSFET from turning on and storing charge during the dead time, which could cost as much as 1% in efficiency. D1 should be selected for forward voltage of less than 0.5 V when conducting I_{MAX}. Recommended transistors for upper and lower MOSFET's are given in Table VII.

Table VII. Recommended MOSFETs

Maximum Output	2 A	4 A	10 A
Vishay/ Siliconix	Si4412DY, 28 mΩ	Si4410DY, 13.5 mΩ	Si4874DY, 7.5 mΩ
International Rectifier	IRF7805, 11 mΩ	IRF7811, 8.9 mΩ IRF7805, 11 mΩ	IRFBA3803, 5.5 mΩ IRF7809, 7.5 mΩ

Soft Start

The soft-start time of each of switching regulator can be programmed by connecting a soft-start capacitor to the corresponding soft-start pin (SS3 or SS5). The time it takes each regulator to ramp up to its full duty ratio depends proportionally on the values of the soft-start capacitors. The charging current is 4 µA ±20%. The capacitor value to set a given soft-start time, t_{SS}, is given by:

$$C_{SS} \cong 4\,\mu A \times \frac{(t_{SS})}{2.6\,V}(pF) \quad (15)$$

Fixed or Adjustable Output Voltage

Each switching controller of the ADP3020 can be programmed to operate with a fixed or adjustable output voltage. As shown by the general application schematic in Figure 19, putting the ADP3020 into fixed mode gives a nominal output of 3.3 V and 5 V for the two switching buck converters. By using two identical resistor dividers per converter, any output voltage between 1.25 V and VIN–0.5 V can be set. The center point of one divider is connected to the feedback pin, FB, and the center point of the other identical divider is connected to EAN. It is important to use 1% resistors. A good value for the lower leg resistors is 10 kΩ, 1%, then the upper leg resistors for a given output voltage can be determined by:

$$R_{UPPER} = \frac{V_{OUT} - 1.2\,V}{0.12}(k\Omega) \quad (16)$$

Table VIII shows the resistor values for the most common output voltages.

Table VIII. Typical Feedback Resistor Values

V_{OUT}	1.25 V	1.3 V	1.5 V	1.8 V	2.0 V	2.5 V	3.0 V	3.3 V	5.0 V
R_{UPPER}	412 Ω	825 Ω	2.49 kΩ	4.99 kΩ	6.65 kΩ	10.7 kΩ	15.0 kΩ	17.4 kΩ	31.6 kΩ
R_{LOWER}	10 kΩ	10 kΩ	10 kΩ	10 kΩ	10 kΩ	10 kΩ	10 kΩ	10 kΩ	10 kΩ

PWM Mode/Power-Saving (PSV) Mode Operation

The mode of operation for both switching regulators can be preset using the MODE pin. When MODE is HIGH, or connected to INTVCC, both converters work only in PWM mode, regardless of output current. MODE connected to GND makes both converters operate in a dual PWM/PSV mode of operation. In dual mode, each converter has its own boundary output current when the converter switches from PSV mode to PWM mode and vice versa. There is an output current hysteresis for each mode transition to avoid improper operation.

There are several design recommendations regarding dual mode operation. The trip output current level for switching between PWM mode and PSV mode is a percentage of the peak current sensed via the internal current sense comparator. However, the value of that current depends on the $R_{DS(ON)}$ of the upper MOSFET. For example, if the design uses an Si4420 versus an Si4410 power MOSFET (9 mΩ vs. 13.5 mΩ) the maximum output power of the converter and the mode trip output current will both be 50% higher.

Efficiency Enhancement

The efficiency of each switching regulator is inversely proportional to the losses during the switching conversion. The main factors to consider when attempting to maximize efficiency are:

1. Resistive losses, which include the $R_{DS(ON)}$ of upper and lower MOSFETs, trace resistances and output choke wire resistance.

   These losses contribute a major part of the overall power loss in low voltage battery-powered applications. However, trying to reduce these resistive losses by using multiple MOSFETs and thick traces may tend to lead to lower efficiency and higher price. This is due to the trade-off between reduced resistive loss and increased gate drive loss that must be considered when optimizing efficiency.

2. Switching losses due to the limited time of switching transitions.

   This occurs due to gate drive losses of both upper and lower MOSFETs, and switching node capacitive losses, as well as through hysteresis and eddy-current losses in power choke. Input and output capacitor ripple current losses should also be considered as switching losses. These losses are input-voltage-dependent and can be estimated as follows:

$$P_{SWLOSS} = 2.5 \times V_{IN}^{1.85} \times I_{MAX} \times C_{SN} \times f \qquad (17)$$

   where C_{SN} is the overall capacitance of the switching node related to loss.

3. Supply current of the switching controller (independent of the input current redirected to supply the MOSFETs' gates).

   This is a very small portion of the overall loss, but it does increase with input voltage.

Transient Response Considerations

Both stability and regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in output load current. When a load step occurs, output voltage shifts by an amount equal to the current step multiplied by the total ESR of the summed output capacitor array. Output overshoot or ringing during the recovery time (in both directions of the current step change) indicates a stability problem. The external feedback compensation components shown in Figure 18 should provide adequate compensation for most applications.

Feedback Loop Compensation

The ADP3020 uses Voltage Mode control to stabilize the switching controller outputs. Figure 20 shows the voltage mode control loop for one of the buck switching regulators. The internal reference voltage V_{REF} is applied to the positive input of the internal error amplifier. The other input of the error amplifier is EAN, and is internally connected to the feedback sensing pin FB via an internal resistor. The error amplifier creates the closed-loop voltage level for the pulsewidth modulator that drives the external power MOSFETs. The output LC filter smooths the pulsewidth modulated input voltage to a dc output voltage.

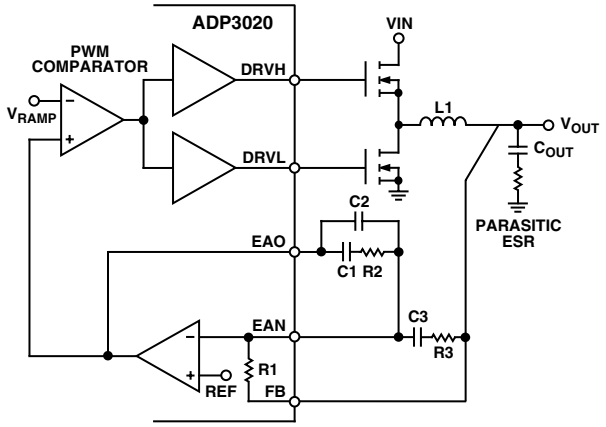


Figure 20. Buck Regulator Voltage Control Loop

The pulsewidth modulator transfer function is V_{OUT}/VEA_{OUT}, where VEA_{OUT} is the output voltage of the error amplifier. That function is dominated by the impedance of the output filter with its double-pole resonance frequency (f_{LC}) and a single zero at output capacitor (f_{ESR}) and the dc gain of the modulator, equal to the input voltage divided by the peak ramp height (V_{RAMP}), which is equal to V_{REF} (1.2 V):

$$f_{LC} = \frac{1}{2\pi \times \sqrt{L_F \times C_{OUT}}} \qquad (18)$$

$$F_{ESR} = \frac{1}{2\pi \times ESR \times C_{OUT}} \qquad (19)$$

The compensation network consists of the internal error amplifier and two external impedance networks Z_{IN} and Z_{FB}. Once the application and the output filter capacitance and ESR are chosen, the specific component values of the external impedance networks Z_{IN} and Z_{FB} can be determined. There are two design criteria for achieving stable switching regulator behavior within the line and load range. One is the maximum bandwidth of the loop, which affects fast transient response, if needed, and the other is the minimum accepted by the design phase margin.

The phase margin is the difference between the closed-loop phase and 180 degrees. Recommended phase margin is 45 to 60 degrees for most applications.

The equations for calculating the compensation Poles and Zeros are:

$$f_{P1} = \frac{1}{2\pi \times R2 \times \frac{C1 \times C2}{C1 + C2}} \quad (20)$$

$$f_{P2} = \frac{1}{2\pi \times R3 \times C3} \quad (21)$$

$$f_{Z1} = \frac{1}{2\pi \times R2 \times C1} \quad (22)$$

$$f_{Z2} = \frac{1}{2\pi \times (R1 + R3) \times C3} \quad (23)$$

The value of the internal resistor $R1$ is 71 kΩ for the 3.3 V switching regulator, and 128 kΩ for the 5 V switching regulator.

Compensation Loop Design and Test Method

1. Choose the gain (R2/R1) for the desired bandwidth.
2. Place f_{Z1} 20%–30% below f_{LC}.
3. Place f_{Z2} 20%–30% above f_{LC}.
4. Place f_{P1} at f_{ESR}, check the output capacitor for worst-case ESR tolerances.
5. Place f_{P2} at 40%–60% of oscillator frequency.
6. Estimate phase margins in full frequency range (zero frequency to zero gain crossing frequency).
7. Apply the designed compensation and test the transient response under a moderate step load change (30%–60%) and various input voltages. Monitor the output voltage via oscilloscope. The voltage overshoot or undershoot should be within 1%–3% of the nominal output, without ringing and abnormal oscillation.

Additional Application Circuits

The multiple outputs and wide input voltage range of the ADP3020 make it a very flexible IC for use in a wide variety of applications. For example, the ADP3020 can be used to generate low voltage (<4.0 V) outputs from a 5 V supply. The circuit shown in Figure 21 converts the 5 V input into a 3.3 V and a 2.5 V output. The circuit of Figure 22 uses a secondary winding on the 5 V output to generate an unregulated 15 V rail which is then regulated to 12 V by the LDO output of the ADP3020.

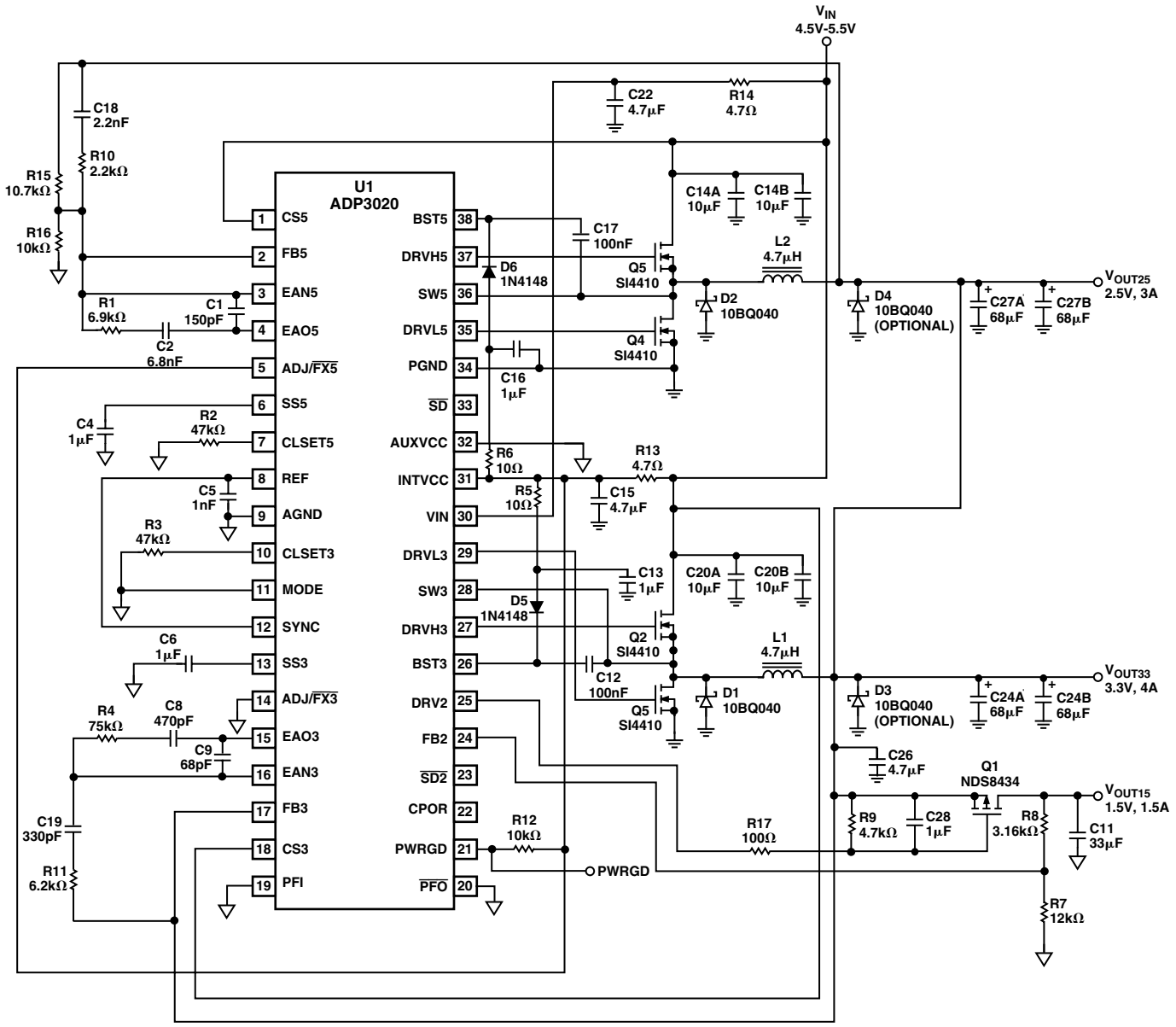


Figure 21. 5 V to 2.5 V/3.3 V DC-DC Converter

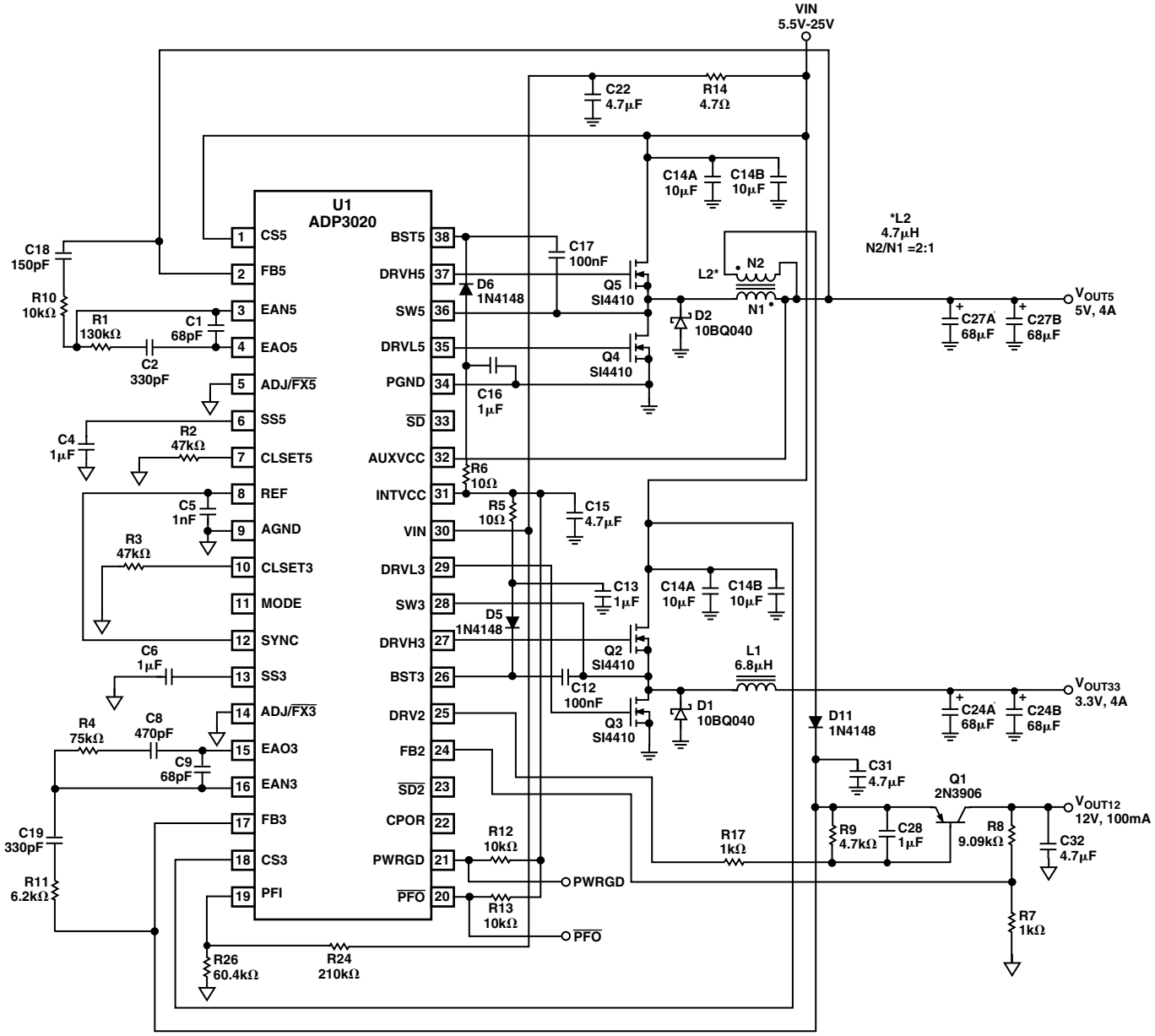


Figure 22. Using a Secondary Winding and an LDO Post Regulator to Generate 12 V

Layout Considerations

The following guidelines are recommended for optimal performance of a switching regulator in a portable PC system:

General Recommendations

1. For best results, a four-layer (minimum) PCB is recommended. This should allow the needed versatility for control circuitry interconnections with optimal placement, a signal ground plane, power planes for both power ground and the input power, and wide interconnection traces in the rest of the power delivery current paths. Each square unit of 1 ounce copper trace has a resistance of ~ 0.53 mΩ at room temperature.
2. Whenever high currents must be routed between PCB layers, vias should be used liberally to create several parallel current paths so that the resistance and inductance introduced by these current paths is minimized and the via current rating is not exceeded.
3. The power and ground planes should overlap each other as little as possible. It is generally easiest (although not necessary) to have the power and signal ground planes on the same PCB layer. The planes should be connected nearest to the first input capacitor where the input ground current flows from the converter back to the battery.

4. If critical signal lines (including the voltage and current sense lines of the ADP3020) must cross through power circuitry, it is best if a signal ground plane can be interposed between those signal lines and the traces of the power circuitry. This serves as a shield to minimize noise injection into the signals at the expense of making signal ground a bit noisier.
5. The PGND pin of the ADP3020 should connect first to a ceramic bypass capacitor on the VIN pin, and then into the power ground plane using the shortest possible trace. However, the power ground plane should not extend under other signal components, including the ADP3020 itself. If necessary, follow the preceding guideline to use the signal plane as a shield between the power ground plane and the signal circuitry.
6. The AGND pin of the ADP3020 should connect first to the REF capacitor, and then into the signal ground plane. In cases where no signal ground plane can be used, short interconnections to other signal ground circuitry in the power converter should be used.
7. The output capacitors of the power converter should be connected to the signal ground plane even though power current flows in the ground of these capacitors. For this reason, it is advised to avoid critical ground connections (e.g., the signal circuitry of the power converter) in the signal ground plane between the input and output capacitors. It is also advised to keep the planar interconnection path short (i.e., have input and output capacitors close together).
8. The output capacitors should also be connected as closely as possible to the load (or connector) that receives the power. If the load is distributed, the capacitors should also be distributed, and generally in proportion to where the load tends to be more dynamic.
9. Absolutely avoid crossing any signal lines over the switching power path loop, described below.

Power Circuitry

10. The switching power path should be routed on the PCB to encompass the smallest possible area in order to minimize radiated switching noise energy (i.e., EMI). Failure to take proper precaution often results in EMI problems for the entire PC system as well as noise-related operational problems in the power converter control circuitry. The switching power path is the loop formed by the current path through the input capacitors, the two FETs (and the power Schottky diode if used), including all interconnecting PCB traces and planes. The use of short and wide interconnection traces is especially critical in this path for two reasons: it minimizes the inductance in the switching loop, which can cause high-energy ringing, and it accommodates the high current demand with minimal voltage loss.
11. A power Schottky diode (1 ~ 2 A dc rating) placed from the lower FET's source (anode) to drain (cathode) will help to minimize switching power dissipation in the upper FET. In the absence of an effective Schottky diode, this dissipation occurs through the following sequence of switching events. The lower FET turns off in advance of the upper FET turning on (necessary to prevent cross-conduction). The circulating current in the power converter, no longer finding a path for current through the channel of the lower FET, draws current through the inherent body-drain diode of the FET. The upper FET turns on, and the reverse recovery characteristic of the lower FET's body-drain diode prevents the drain voltage from being pulled high quickly.

    The upper FET then conducts very large current while it momentarily has a high voltage forced across it, which translates into added power dissipation in the upper FET. The Schottky diode minimizes this problem by carrying a majority of the circulating current when the lower FET is turned off, and by virtue of its essentially nonexistent reverse recovery time.
12. Whenever a power-dissipating component (e.g., a power MOSFET) is soldered to a PCB, the liberal use of vias, both directly on the mounting pad and immediately surrounding it, is recommended. Two important reasons for this are: improved current rating through the vias (if it is a current path), and improved thermal performance, especially if the vias are extended to the opposite side of the PCB where a plane can more readily transfer the heat to the air.
13. The output power path, though not as critical as the switching power path, should also be routed to encompass a small area. The output power path is formed by the current path through the inductor, the output capacitors, and back to the input capacitors.
14. For best EMI containment, the power ground plane should extend fully under all the power components except the output capacitors. These are: the input capacitors, the power MOSFETs and Schottky diode, the inductor, and any snubbing elements that might be added to dampen ringing. Avoid extending the power ground under any other circuitry or signal lines, including the voltage and current sense lines.

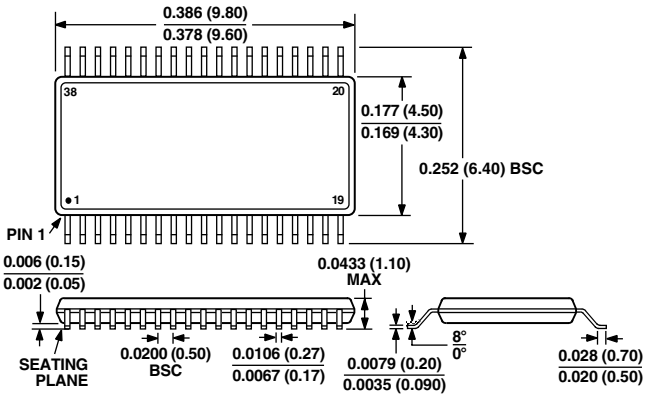
Signal Circuitry

15. The CS and SW traces should be Kelvin-connected to the upper MOSFET drain and source so that the additional voltage drop due to current flow on the PCB at the current sense comparator connections does not affect the sensed voltage. It is desirable to have the ADP3020 close to the output capacitor bank and not in the output power path, so that any voltage drop between the output capacitors and the AGND pin is minimized, and voltage regulation is not compromised.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

38-Lead TSSOP (RU-38)



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