### SN74HC4066 QUADRUPLE BILATERAL ANALOG SWITCH

SCLS325G - MARCH 1996 - REVISED JULY 2003

- Wide Operating Voltage Range of 2 V to 6 V
- Typical Switch Enable Time of 18 ns
- Low Power Consumption, 20-μA Max I<sub>CC</sub>
- Low Input Current of 1 μA Max
- High Degree of Linearity
- High On-Off Output-Voltage Ratio
- Low Crosstalk Between Switches
- Low On-State Impedance . . .
   50-Ω TYP at V<sub>CC</sub> = 6 V
- Individual Switch Controls

#### D, DB, N, NS, OR PW PACKAGE (TOP VIEW) 14 🛮 V<sub>CC</sub> 1A 1B 🛛 13 1 1C 2B **∏** 3 12 AC 11 4A 2A 🛮 4 2C 3C [6 9 3B GND [ 8∏ 3A

### description/ordering information

The SN74HC4066 is a silicon-gate CMOS quadruple analog switch designed to handle both analog and digital signals. Each switch permits signals with amplitudes of up to 6 V (peak) to be transmitted in either direction.

Each switch section has its own enable input control (C). A high-level voltage applied to C turns on the associated switch section.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

#### ORDERING INFORMATION

TA	PACK	AGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
	PDIP – N	Tube of 25	SN74HC4066N	SN74HC4066N	
		Tube of 50	SN74HC4066D		
	SOIC - D	Reel of 2500	SN74HC4066DR	HC4066	
		Reel of 250	SN74HC4066DT		
-40°C to 85°C	SOP – NS	Reel of 2000	SN74HC4066NSR	HC4066	
	SSOP – DB	Reel of 2000	SN74HC4066DBR	HC4066	
		Tube of 90	SN74HC4066PW	HC4066	
	TSSOP – PW	Reel of 2000	SN74HC4066PWR		
		Reel of 250	SN74HC4066PWT		

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

## FUNCTION TABLE (each switch)

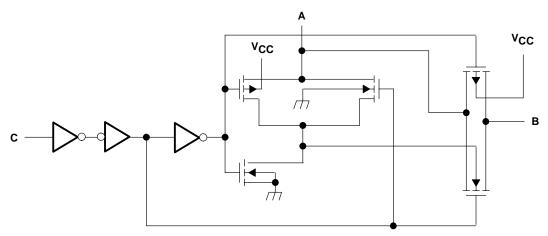
INPUT CONTROL (C)	SWITCH
L	OFF
Н	ON



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#### logic diagram, each switch (positive logic)



One of Four Switches

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub> (see Note 1)		–0.5 V to 7 V
Control-input diode current, $I_1$ ( $V_1 < 0$ or $V_1 > V_0$	cc)	±20 mA
I/O port diode current, $I_1$ ( $V_1 < 0$ or $V_{1/O} > V_{CC}$ )		
On-state switch current ( $V_{I/O} = 0$ to $V_{CC}$ )		±25 mA
Continuous current through V <sub>CC</sub> or GND		±50 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 2)	: D package	86°C/W
	DB package	96°C/W
	N package	80°C/W
	NS package	76°C/W
	PW package	113°C/W
Storage temperature range, T <sub>stq</sub>		. −65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltages are with respect to ground unless otherwise specified.
  - 2. The package thermal impedance is calculated in accordance with JESD 51-7.



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#### recommended operating conditions (see Note 3)

			MIN	NOM	MAX	UNIT
Vcc	Supply voltage		2†	5	6	V
V <sub>I/O</sub>	I/O port voltage		0		VCC	V
		V <sub>CC</sub> = 2 V	1.5		VCC	
VIH	High-level input voltage, control inputs $V_{CC} = 4.5 \text{ V}$				VCC	V
		VCC = 6 V	4.2		Vcc	
		V <sub>CC</sub> = 2 V	0		0.3	0.3 0.9 V
VIL	Low-level input voltage, control inputs	V <sub>CC</sub> = 4.5 V	0		0.9	
		V <sub>CC</sub> = 6 V	0		1.2	
		V <sub>CC</sub> = 2 V			1000	
Δt/Δν	Input transition rise/fall time	V <sub>CC</sub> = 4.5 V			500	ns
				400		
TA	Operating free-air temperature		-40		85	°C

T With supply voltages at or near 2 V, the analog switch on-state resistance becomes very nonlinear. It is recommended that only digital signals be transmitted at these low supply voltages.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		TEST CONDITIONS	\ , \	T	\ = 25°C	;	MIN	MAX	UNIT
	PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	IVIIIN	WAX	UNIT
				2 V		150				
ron	r <sub>on</sub> On-state switch resistance		$I_T = -1$ mA, $V_I = 0$ to $V_{CC}$ , $V_C = V_{IH}$ (see Figure 1)	4.5 V		50	85		106	Ω
			VC = VIH (See Figure 1)	6 V		30				
				2 V		320				
r <sub>on(p)</sub>	Peak on-state resistar	ice	$V_I = V_{CC}$ or GND, $V_C = V_{IH}$ , $I_T = -1$ mA	4.5 V		70	170		215	Ω
				6 V		50				
Ц	Control input current		$V_C = 0$ or $V_{CC}$	6 V		±0.1	±100		±1000	nA
I <sub>soff</sub>	Off-state switch leakage current		$V_I = V_{CC}$ or 0, $V_O = V_{CC}$ or 0, $V_C = V_{IL}$ (see Figure 2)	6 V			±0.1		±5	μΑ
I <sub>son</sub>	On-state switch leaka	ge current	V <sub>I</sub> = V <sub>CC</sub> or 0, V <sub>C</sub> = V <sub>IH</sub> (see Figure 3)	6 V			±0.1		±5	μΑ
Icc	Supply current		$V_I = 0$ or $V_{CC}$ , $I_O = 0$	6 V			2		20	μΑ
C.	lanut conscitores	A or B		5 V		9				~F
Ci	Input capacitance	С	]	o v		3	10		10	pF
Cf	Feed-through capacitance	A to B	V <sub>I</sub> = 0			0.5				pF
Со	Output capacitance	A or B		5 V		9				pF

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## SN74HC4066 QUADRUPLE BILATERAL ANALOG SWITCH

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### switching characteristics over recommended operating free-air temperature range

BA	RAMETER	FROM	то	TEST	Vaa	Τ <sub>Δ</sub>	( = 25°C	;	MIN	MAX	UNIT				
FA	RAMETER	(INPUT)	(OUTPUT)	CONDITIONS	Vcc	MIN	TYP	MAX	IVIIIN	IVIAA	UNIT				
Ι.					2 V		10	60		75					
t <sub>PLH</sub> ,	Propagation delay time	A or B	B or A	C <sub>L</sub> = 50 pF (see Figure 4)	4.5 V		4	12		15	ns				
'PHL	dolay iiiilo			(See Figure 1)	6 V		3	10		13					
				$R_1 = 1 k\Omega$	2 V		70	180		225					
tPZH, tPZL	Switch turn-on time	С	A or B	$C_{L} = 50  pF$	4.5 V		21	36		45	ns				
, PZL	tarri ori timo			(see Figure 5)	6 V		18	31		38					
				$R_L = 1 k\Omega$ ,	2 V		50	200		250					
<sup>t</sup> PLZ <sup>,</sup> <sup>t</sup> PHZ	Switch turn-off time	С	A or B	C <sub>L</sub> = 50 pF (see Figure 5)	4.5 V		25	40		50	ns				
, PRZ	tarri on time				6 V		22	34		43					
	Control			$C_L = 15 \text{ pF},$ $R_I = 1 \text{ k}\Omega,$	2 V		15								
fĮ	input	С	A or B $V_C = V_{CC}$ or Gf	A or B	A or B $V_C =$	A or B	A or B $V_C = V_{CC}$ or GNI	$V_C = V_{CC}$ or GND,	4.5 V		30				MHz
	frequency			VO = VCC/2 (see Figure 6)	6 V		30								
	Control feed-through	С	A or B	$R_{in} = RL = 600 \Omega$	4.5 V		15				mV				
	noise	J	AUID	$V_C = V_{CC}$ or GND, $f_{in} = 1$ MHz (see Figure 7)	6 V		20	·		·	(rms)				

## operating characteristics, $V_{CC}$ = 4.5 V, $T_A$ = 25°C

	PARAMETER	TEST C	TYP	UNIT	
C <sub>pd</sub>	Power dissipation capacitance per gate	$C_L = 50 \text{ pF},$	f = 1 MHz	45	pF
	Minimum through bandwidth, A to B or B to A $^{\dagger}$ [20 log (VO/VI)] = -3 dB	$C_L = 50 \text{ pF},$ $V_C = V_{CC}$	$R_L = 600 \Omega$ , (see Figure 8)	30	MHz
	Crosstalk between any switches‡	$C_L = 10 \text{ pF},$ $f_{in} = 1 \text{ MHz}$	$R_L = 50 \Omega$ , (see Figure 9)	45	dB
	Feed through, switch off, A to B or B to A <sup>‡</sup>	C <sub>L</sub> = 50 pF, f <sub>in</sub> = 1 MHz	$R_L = 600 \Omega$ , (see Figure 10)	42	dB
	Amplitude distortion rate, A to B or B to A	C <sub>L</sub> = 50 pF, f <sub>in</sub> = 1 kHz	$R_L$ = 10 kΩ, (see Figure 11)	0.05%	

 $<sup>\</sup>uparrow$  Adjust the input amplitude for output = 0 dBm at f = 1 MHz. Input signal must be a sine wave.

 $<sup>\</sup>ddagger$  Adjust the input amplitude for input = 0 dBm at f = 1 MHz. Input signal must be a sine wave.

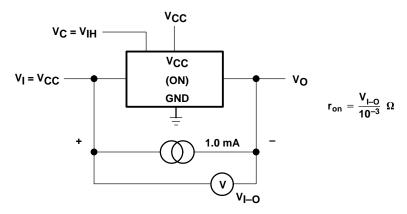


Figure 1. On-State Resistance Test Circuit

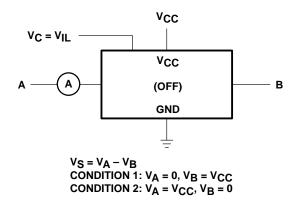


Figure 2. Off-State Switch Leakage-Current Test Circuit

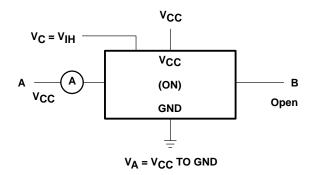


Figure 3. On-State Leakage-Current Test Circuit

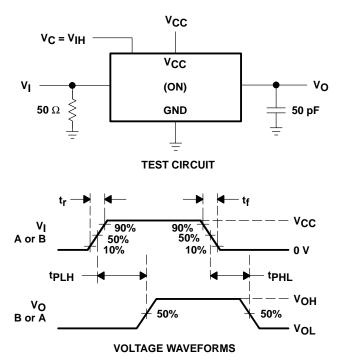
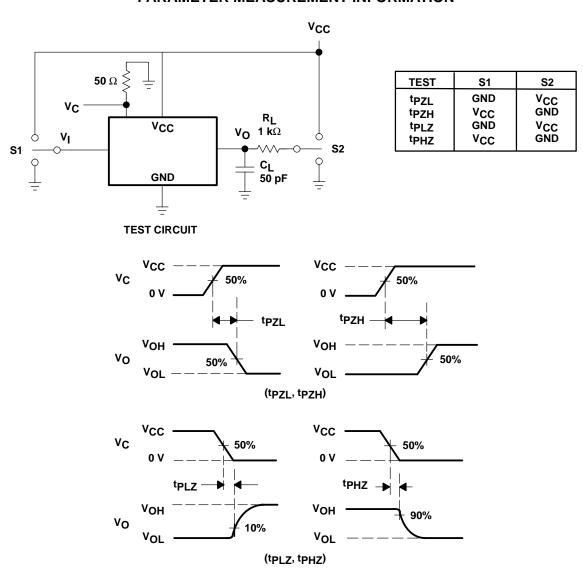


Figure 4. Propagation Delay Time, Signal Input to Signal Output



**VOLTAGE WAVEFORMS** 

Figure 5. Switching Time ( $t_{PZL}$ ,  $t_{PLZ}$ ,  $t_{PZH}$ ,  $t_{PHZ}$ ), Control to Signal Output

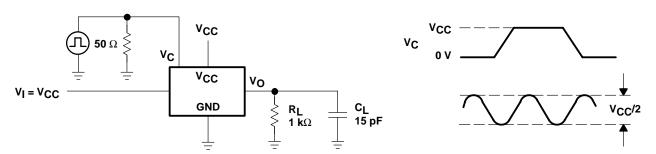


Figure 6. Control-Input Frequency

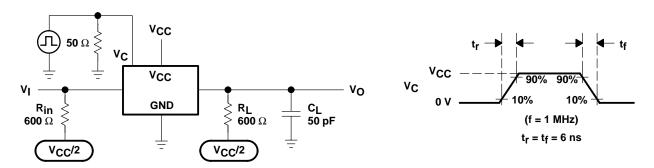


Figure 7. Control Feed-Through Noise

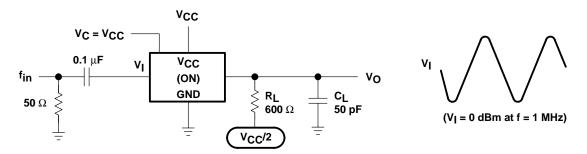


Figure 8. Minimum Through Bandwidth

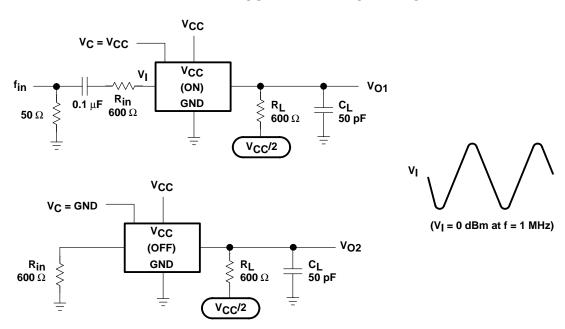


Figure 9. Crosstalk Between Any Two Switches

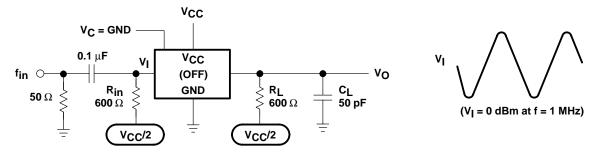


Figure 10. Feed Through, Switch Off

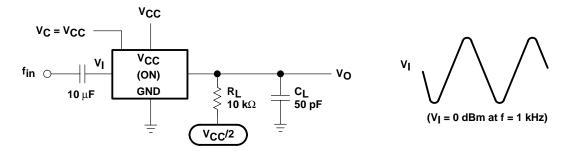


Figure 11. Amplitude-Distortion Rate

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logic.ti.com	Military	www.ti.com/military
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www.ti.com/lpw	Telephony	www.ti.com/telephony
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#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74HC4066D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4066DBLE	OBSOLETE	SSOP	DB	14		TBD	Call TI	Call TI
SN74HC4066DBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4066DBRE4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4066DBRG4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4066DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4066DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4066DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4066DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4066DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4066DT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4066DTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4066DTG4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4066N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74HC4066NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74HC4066NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4066NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4066PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4066PWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4066PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4066PWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI
SN74HC4066PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4066PWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4066PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4066PWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4066PWTE4	ACTIVE	TSSOP	PW	14	250	Green (RoHS &	CU NIPDAU	Level-1-260C-UNLIM



#### PACKAGE OPTION ADDENDUM

28-May-2007

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
					no Sb/Br)		
SN74HC4066PWTG4	ACTIVE	TSSOP	PW	14 250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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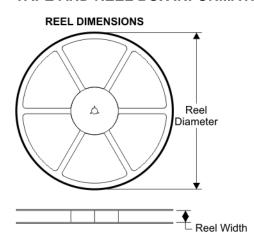
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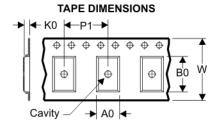




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#### TAPE AND REEL BOX INFORMATION





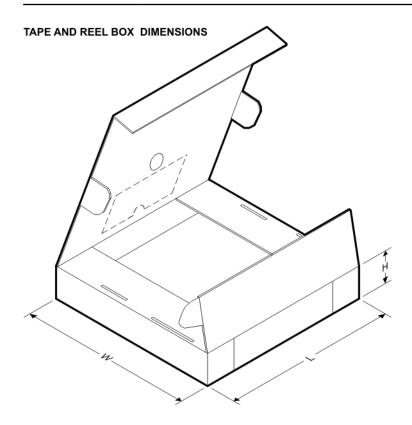
	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC4066DBR	DB	14	SITE 41	330	16	8.2	6.6	2.5	12	16	Q1
SN74HC4066DR	D	14	SITE 41	330	16	6.5	9.0	2.1	8	16	Q1
SN74HC4066NSR	NS	14	SITE 41	330	16	8.2	10.5	2.5	12	16	Q1
SN74HC4066PWR	PW	14	SITE 41	330	12	7.0	5.6	1.6	8	12	Q1





Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN74HC4066DBR	DB	14	SITE 41	346.0	346.0	33.0
SN74HC4066DR	D	14	SITE 41	346.0	346.0	33.0
SN74HC4066NSR	NS	14	SITE 41	346.0	346.0	33.0
SN74HC4066PWR	PW	14	SITE 41	346.0	346.0	29.0

## N (R-PDIP-T\*\*)

## PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



## D (R-PDSO-G14)

## PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AB.



#### **MECHANICAL DATA**

## NS (R-PDSO-G\*\*)

## 14-PINS SHOWN

#### PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



#### DB (R-PDSO-G\*\*)

#### PLASTIC SMALL-OUTLINE

#### **28 PINS SHOWN**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

#### PW (R-PDSO-G\*\*)

#### 14 PINS SHOWN

#### PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

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