19-5875; Rev 0; 5/11

EVALUATION KIT AVAILABLE

MAX2769B

Universal GPS Receiver

General Description

The MAX2769B is a next-generation Global Navigation Satellite System (GNSS) receiver covering GPS, GLONASS, Galileo, and Compass navigation satellite systems on a single chip. This single-conversion GNSS receiver is designed to provide high performance for industrial and automotive applications.

Designed on Maxim's advanced, low-power SiGe BiCMOS process technology, the MAX2769B offers the highest performance and integration at a low cost. Incorporated on the chip is the complete receiver chain, including a dual-input LNA and mixer, followed by the image-rejected filter, PGA, VCO, fractional-N frequency synthesizer, crystal oscillator, and a multibit ADC. The total cascaded noise figure of this receiver is as low as 1.4dB.

The MAX2769B completely eliminates the need for external IF filters by implementing on-chip monolithic filters and requires only a few external components to form a complete low-cost GPS RF receiver solution.

The MAX2769B is the most flexible receiver on the market. The integrated delta-sigma fractional-N frequency synthesizer allows programming of the IF frequency within a ±30Hz (f_{XTAL} = 32MHz) accuracy while operating with any reference or crystal frequencies that are available in the host system. The ADC outputs CMOS logic levels with 1 or 2 quantized bits for both I and Q channels, or up to 3 quantized bits for the I channel. I and Q analog outputs are also available.

The MAX2769B is packaged in a 5mm x 5mm, 28-pin thin QFN package with an exposed paddle.

Applications

- Automotive Navigation Systems
- Location-Enabled Mobile Handsets
- PNDs (Personal Navigation Devices)
- Telematics (Asset Tracking, Inventory Management)
- Marine/Avionics Navigation
- Software GPS
- Laptops and Netbooks

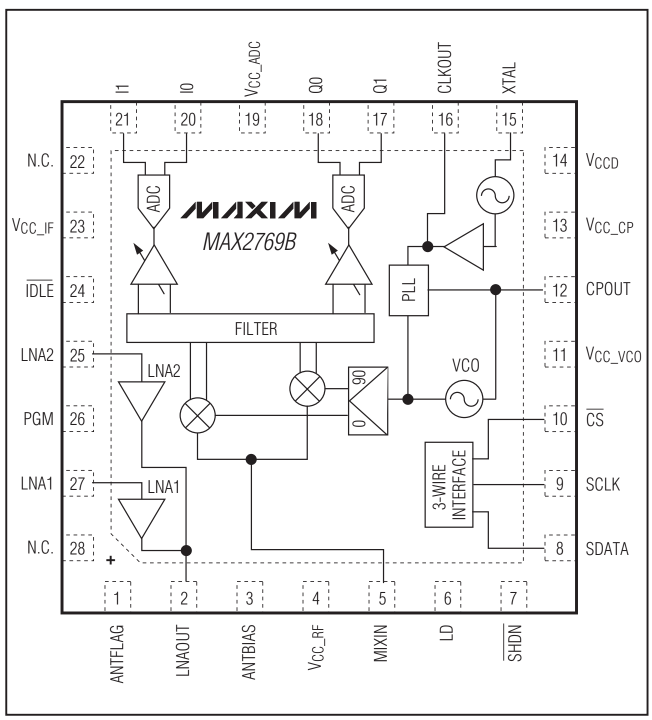
For related parts and recommended products to use with this part, refer to ***www.maxim-ic.com/MAX2769B.related****.*

Features

- ♦ **AEC-Q100 Automotive Qualified**
- ♦ **GPS/GLONASS/Galileo/Compass Systems**
- ♦ **40pF Output Clock Drive Capability**
- ♦ **No External IF SAW or Discrete Filters Required**
- ♦ **Programmable IF Frequency**
- ♦ **Fractional-N Synthesizer with Integrated VCO Supports Wide Range of Reference Frequencies**
- ♦ **Dual-Input Uncommitted LNA for Separate Passive and Active Antenna Inputs**
- ♦ **1.4dB Cascade Noise Figure**
- ♦ **Integrated Crystal Oscillator**
- ♦ **Integrated Active Antenna Sensor**
- ♦ **2.7V to 3.3V Supply Voltage**
- ♦ **Small, 28-Pin, RoHS-Compliant, Thin QFN Lead-Free Package (5mm x 5mm)**

Ordering Information ***appears at end of data sheet.***

Block Diagram



ABSOLUTE MAXIMUM RATINGS

$V_{CC\_}$ to Ground..-0.3V to +4.2V
Other Pins Except LNA_, MIXIN, XTAL, and LNAOUT to
Ground............................ -0.3V to +(Operating $V_{CC\_}$ + 0.3V)
Maximum RF Input Power ....+15dBm
Continuous Power Dissipation (T_A = +70°C)
TQFN (derates 27mW/°C above +70°C) 2500mW

Operating Temperature Range.......................... -40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range........................... -65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION! ESD SENSITIVE DEVICE

DC ELECTRICAL CHARACTERISTICS*

(MAX2769B EV kit, $V_{CC\_}$ = 2.7V to 3.3V, T_A = -40°C to +85°C, PGM = Ground. Registers are set to the default power-up states. Typical values are at $V_{CC\_}$ = 2.85V and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage		2.7	2.85	3.3	V
Supply Current	Default mode, LNA1 is active (Note 2)	18	27	31	mA
	Default mode, LNA2 is active (Note 2)	15	25	30.5	
	Idle Mode™, $\overline{\text{IDLE}}$ = low, $\overline{\text{SHDN}}$ = high		5		
	Shutdown mode, $\overline{\text{SHDN}}$ = low		200		µA
Voltage Drop at ANTBIAS from V_{CC_RF}	Sourcing 20mA at ANTBIAS		0.2		V
Short-Circuit Protection Current at ANTBIAS	ANTBIAS is shorted to ground		57		mA
Active Antenna Detection Current	To assert logic-high at ANTFLAG		1.1		mA
DIGITAL INPUT AND OUTPUT					
Digital Input Logic-High	Measure at the $\overline{\text{SHDN}}$ pin	1.5			V
Digital Input Logic-Low	Measure at the $\overline{\text{SHDN}}$ pin			0.4	V

Idle Mode is a trademark of Maxim Integrated Products, Inc.

**The parametric values (min, typ, max limits) shown in the Electrical Characteristics table supersede values quoted elsewhere in this data sheet.*

AC ELECTRICAL CHARACTERISTICS*

(MAX2769B EV kit, $V_{CC\_}$ = 2.7V to 3.3V, T_A = -40°C to +85°C, PGM = Ground. Registers are set to the default power-up states. LNA input is driven from a 50Ω source. All RF measurements are done in the analog output mode with ADC bypassed. PGA gain is set to 51dB gain by serial-interface word GAININ = 111010. Maximum IF output load is not to exceed 10kΩll7.5pF on each pin. Typical values are at $V_{CC\_}$ = 2.85V and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CASCADED RF PERFORMANCE					
RF Frequency	L1 band		1575.42		MHz
Noise Figure	LNA1 input active, default mode (Note 3)		1.4		dB
	LNA2 input active, default mode (Note 3)		2.7		
	Measured at the mixer input		10.3		
Out-of-Band 3rd-Order Input Intercept Point	Measured at the mixer input (Note 4)		-7		dBm
In-Band Mixer Input Referred 1dB Compression Point	Measured at the mixer input		-85		dBm
Mixer Input Return Loss			10		dB
Image Rejection			25		dB
Spurs at LNA1 Input	LO leakage		-101		dBm
	Reference harmonics leakage		-103		
Maximum Voltage Gain	Measured from the mixer to the baseband analog output	91	96	103	dB
Variable Gain Range		55	59		dB
FILTER RESPONSE					
Passband Center Frequency	FBW = 00		4		MHz
	FBW = 10		4		
	FBW = 01		9.27		
Passband 3dB Bandwidth	FBW = 00		2.5		MHz
	FBW = 10		4.2		
	FBW = 01		9.66		
Lowpass 3dB Bandwidth	FBW = 11		9		MHz
Stopband Attenuation	3rd-order filter, bandwidth = 2.5MHz, measured at 4MHz offset		30		dB
	5th-order filter, bandwidth = 2.5MHz, measured at 4MHz offset	40	49.5		
LNA					
LNA1 INPUT					
Power Gain			19		dB
Noise Figure			0.83		dB
Input IP3	(Note 5)		-1.1		dBm
Output Return Loss			10		dB
Intput Return Loss			8		dB

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AC ELECTRICAL CHARACTERISTICS* (continued)

(MAX2769B EV kit, $V_{CC\_}$ = 2.7V to 3.3V, T_A = -40°C to +85°C, PGM = Ground. Registers are set to the default power-up states. LNA input is driven from a 50Ω source. All RF measurements are done in the analog output mode with ADC bypassed. PGA gain is set to 51dB gain by serial-interface word GAININ = 111010. Maximum IF output load is not to exceed 10kΩll7.5pF on each pin. Typical values are at $V_{CC\_}$ = 2.85V and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LNA2 INPUT					
Power Gain			13		dB
Noise Figure			1.14		dB
Input IP3	(Note 5)		1		dBm
Output Return Loss			19		dB
Input Return Loss			11		dB
FREQUENCY SYNTHESIZER					
LO Frequency Range	0.2V < V_{TUNE} < ($V_{CC\_}$ - 0.3V)	1550		1610	MHz
LO Tuning Gain			57		MHz/V
Reference Input Frequency		8		44	MHz
Main Divider Ratio		36		32,767	—
Reference Divider Ratio		1		1023	—
Charge-Pump Current	ICP = 0		0.5		mA
	ICP = 1		1		
TCXO INPUT BUFFER/OUTPUT CLOCK BUFFER					
Frequency Range		8		32	MHz
Output Logic-Level High (V_{OH})	With respect to ground, I_{OH} = 10µA (DC-coupled)	2			V
Output Logic-Level Low (V_{OL})	With respect to ground, I_{OL} = 10µA (DC-coupled)			0.8	V
Capacitive Slew Current	Load = 10kΩ + 40pF, f_{CLKOUT} = 32MHz		11		mA
Output Load			10ll40		kΩllpF
Reference Input Level	Sine wave	0.5			V_{P-P}
Clock Output Multiply/Divide Range	/4, /2, /1 (x2, max input frequency of 16MHz)	÷4		x2	—
ADC					
ADC Differential Nonlinearity	AGC enabled, 3-bit output		±0.1		LSB
ADC Integral Nonlinearity	AGC enabled, 3-bit output		±0.1		LSB

Note 1: MAX2769B is production tested at T_A = +25°C and +85°C. All min/max specifications are guaranteed by design and characterization from -40°C to +85°C, unless otherwise noted. Default register settings are not production tested or guaranteed. User must program the registers upon power-up.

Note 2: Default, low-NF mode of the IC. LNA choice is gated by the ANT_FLAG signal. In the normal mode of operation without an active antenna, LNA1 is active. If an active antenna is connected and ANT_FLAG switches to 1, LNA1 is automatically disabled and LNA2 becomes active. PLL is in an integer-N mode with f_{COMP} = f_{TCXO}/16 = 1.023MHz and ICP = 0.5mA. The complex IF filter is configured as a 5th-order Butterworth filter with a center frequency of 4MHz and bandwidth of 2.5MHz. Output data is in a 2-bit sign/magnitude format at CMOS logic levels in the I channel only.

Note 3: The LNA output connects to the mixer input without a SAW filter between them.

Note 4: Two tones are located at 12MHz and 24MHz offset frequencies from the GPS center frequency of 1575.42MHz at -60dBm/tone. Passive pole at the mixer output is programmed to be 13MHz.

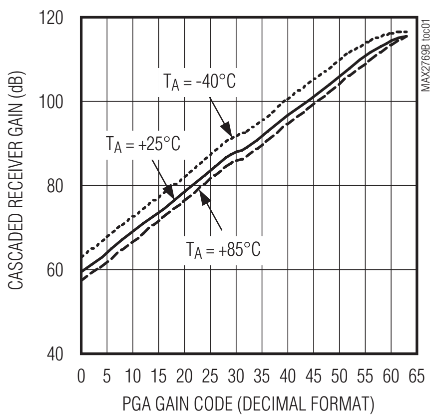
Note 5: Measured from the LNA input to the LNA output. Two tones are located at 12MHz and 24MHz offset frequencies from the GPS center frequency of 1575.42MHz at -60dBm per tone.

*The parametric values (min, typ, max limits) shown in the Electrical Characteristics table supersede values quoted elsewhere in this data sheet.

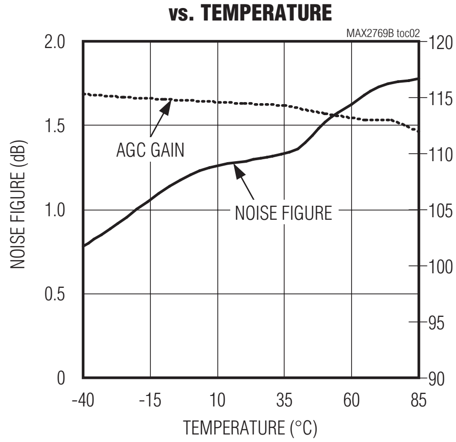
Typical Operating Characteristics

(MAX2769B EV kit, $V_{CC\_}$ = 2.7V to 3.3V, T_A = -40°C to +85°C, PGM = Ground. Registers are set to the default power-up states. LNA input is driven from a 50Ω source. All RF measurements are done in the analog output mode with ADC bypassed. PGA gain is set to 51dB gain by serial-interface word GAININ = 111010. Maximum IF output load is not to exceed 10kΩll7.5pF on each pin. Typical values are at $V_{CC\_}$ = 2.85V and T_A = +25°C, unless otherwise noted.)

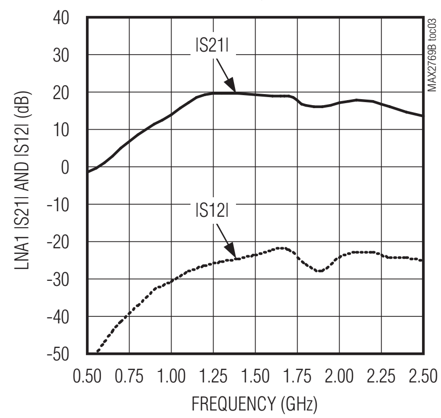
CASCADED RECEIVER GAIN vs. PGA GAIN CODE



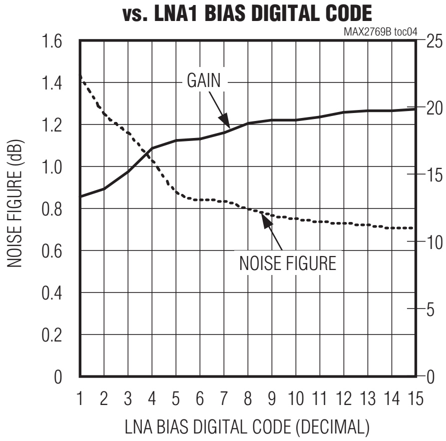
CASCADED GAIN AND NOISE FIGURE vs. TEMPERATURE



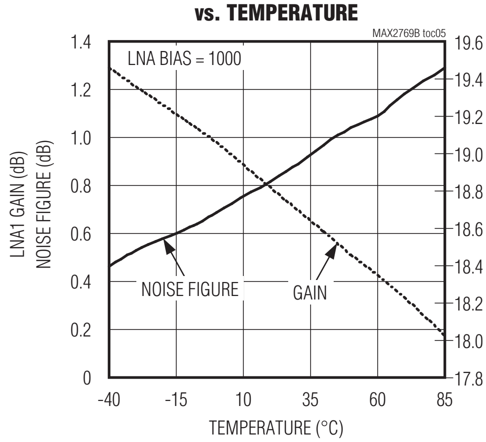
LNA1 IS21I AND IS12I vs. FREQUENCY



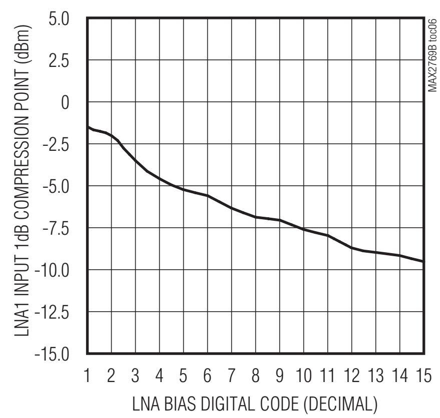
LNA1 GAIN AND NOISE FIGURE vs. LNA1 BIAS DIGITAL CODE



LNA1 GAIN AND NOISE FIGURE vs. TEMPERATURE



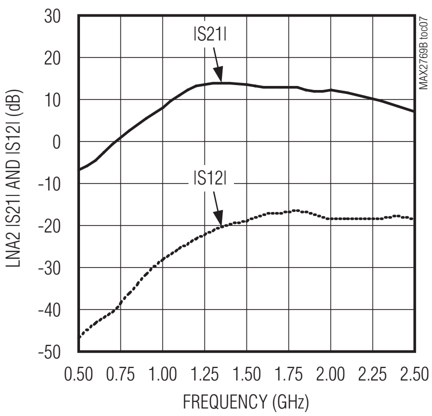
LNA1 INPUT 1dB COMPRESSION POINT vs. LNA1 BIAS DIGITAL CODE



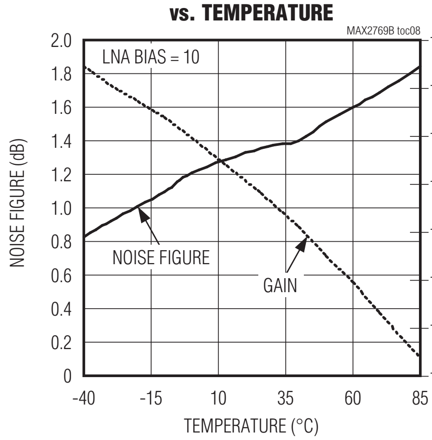
Typical Operating Characteristics (continued)

(MAX2769B EV kit, $V_{CC\_}$ = 2.7V to 3.3V, T_A = -40°C to +85°C, PGM = Ground. Registers are set to the default power-up states. LNA input is driven from a 50Ω source. All RF measurements are done in the analog output mode with ADC bypassed. PGA gain is set to 51dB gain by serial-interface word GAININ = 111010. Maximum IF output load is not to exceed 10kΩ||7.5pF on each pin. Typical values are at $V_{CC\_}$ = 2.85V and T_A = +25°C, unless otherwise noted.)

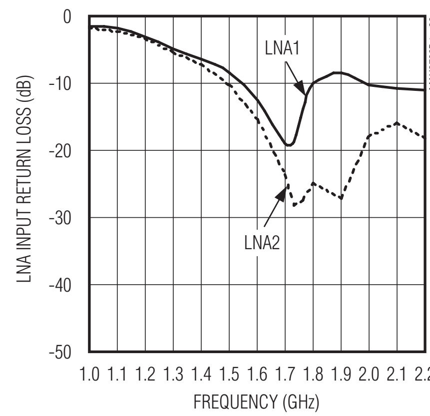
LNA2 |S21| AND |S12| vs. FREQUENCY



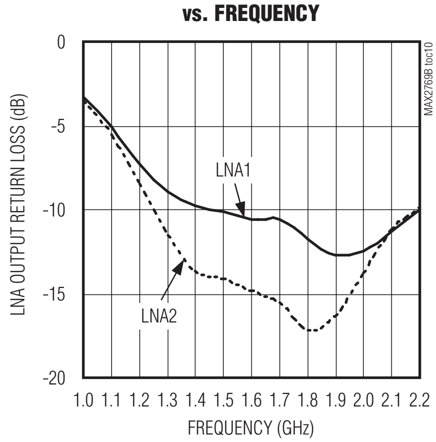
LNA2 GAIN AND NOISE FIGURE vs. TEMPERATURE



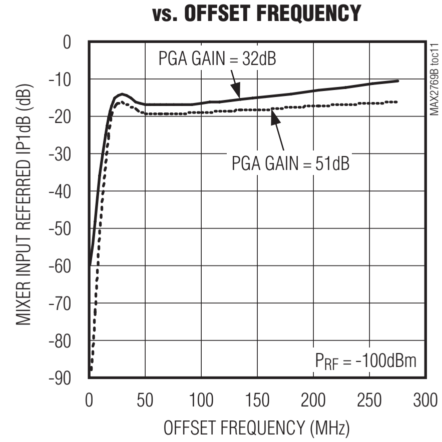
LNA INPUT RETURN LOSS vs. FREQUENCY



LNA OUTPUT RETURN LOSS vs. FREQUENCY



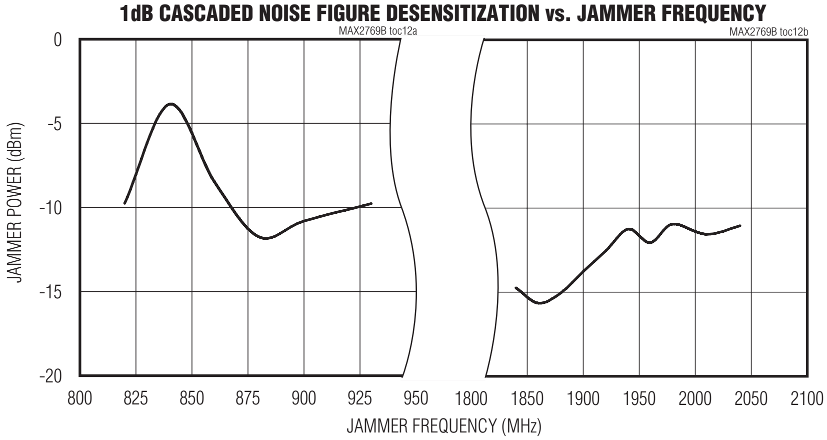
MIXER INPUT REFERRED IP1dB vs. OFFSET FREQUENCY



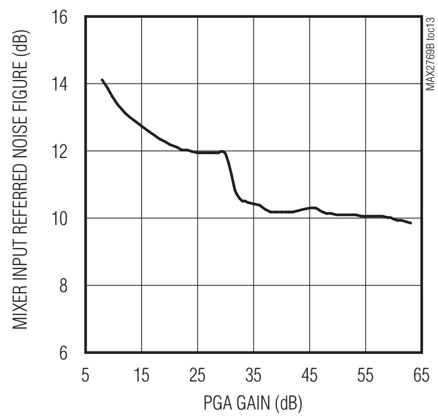
Typical Operating Characteristics (continued)

(MAX2769B EV kit, $V_{CC\_}$ = 2.7V to 3.3V, T_A = -40°C to +85°C, PGM = Ground. Registers are set to the default power-up states. LNA input is driven from a 50Ω source. All RF measurements are done in the analog output mode with ADC bypassed. PGA gain is set to 51dB gain by serial-interface word GAININ = 111010. Maximum IF output load is not to exceed 10kΩ||7.5pF on each pin. Typical values are at $V_{CC\_}$ = 2.85V and T_A = +25°C, unless otherwise noted.)

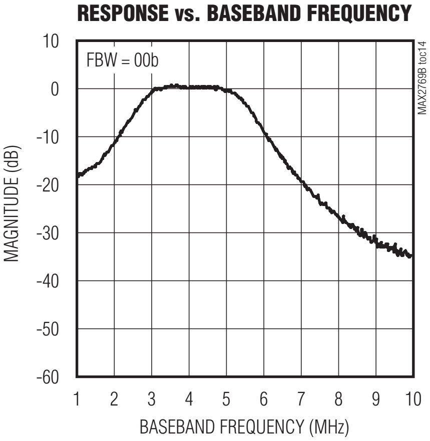
1dB CASCADED NOISE FIGURE DESENSITIZATION vs. JAMMER FREQUENCY



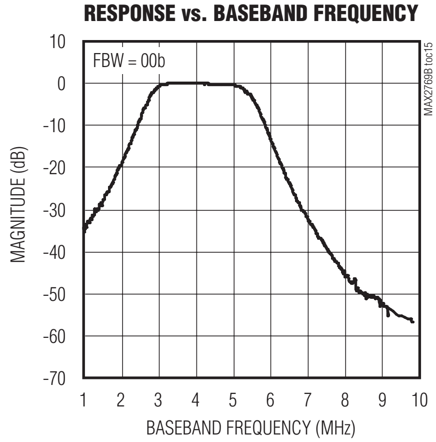
MIXER INPUT REFERRED NOISE FIGURE vs. PGA GAIN



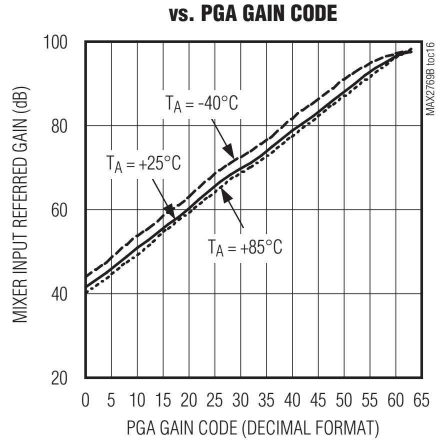
3RD-ORDER POLYPHASE FILTER MAGNITUDE RESPONSE vs. BASEBAND FREQUENCY



5TH-ORDER POLYPHASE FILTER MAGNITUDE RESPONSE vs. BASEBAND FREQUENCY



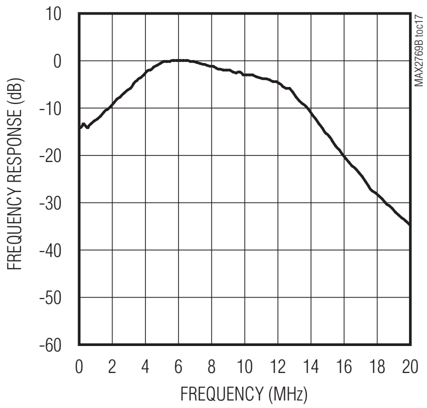
MIXER INPUT REFERRED GAIN vs. PGA GAIN CODE



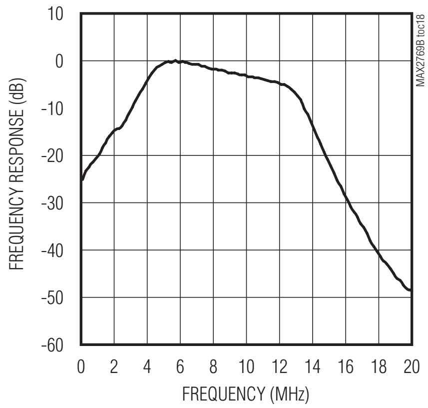
Typical Operating Characteristics (continued)

(MAX2769B EV kit, $V_{CC\_}$ = 2.7V to 3.3V, T_A = -40°C to +85°C, PGM = Ground. Registers are set to the default power-up states. LNA input is driven from a 50Ω source. All RF measurements are done in the analog output mode with ADC bypassed. PGA gain is set to 51dB gain by serial-interface word GAININ = 111010. Maximum IF output load is not to exceed 10kΩll7.5pF on each pin. Typical values are at $V_{CC\_}$ = 2.85V and T_A = +25°C, unless otherwise noted.)

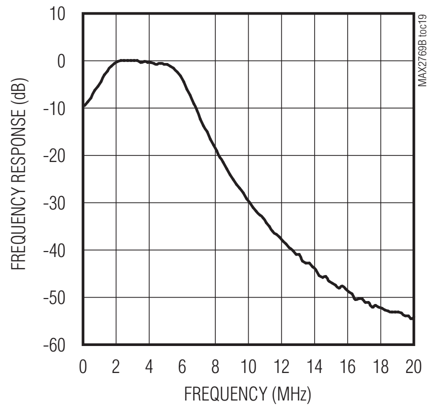
3RD-ORDER POLYPHASE FILTER vs. BASEBAND FREQUENCY (FBW = 01)



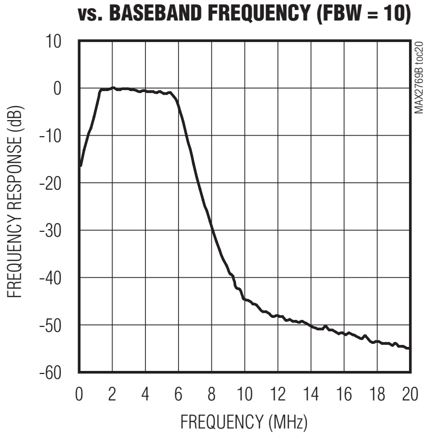
5TH-ORDER POLYPHASE FILTER vs. BASEBAND FREQUENCY (FBW = 01)



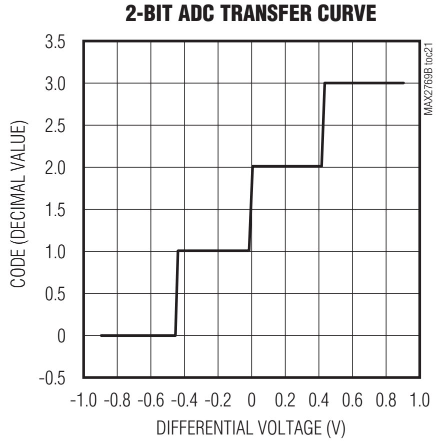
3RD-ORDER POLYPHASE FILTER vs. BASEBAND FREQUENCY (FBW = 10)



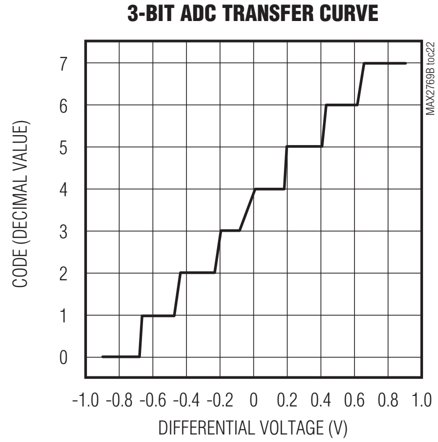
5TH-ORDER POLYPHASE FILTER vs. BASEBAND FREQUENCY (FBW = 10)



2-BIT ADC TRANSFER CURVE



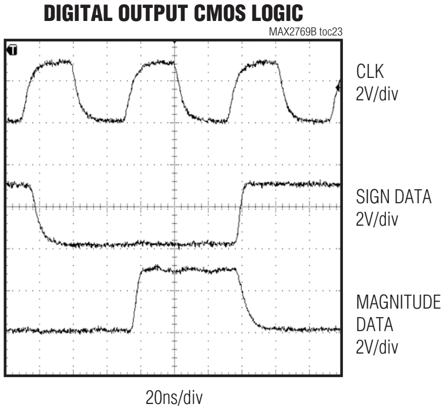
3-BIT ADC TRANSFER CURVE



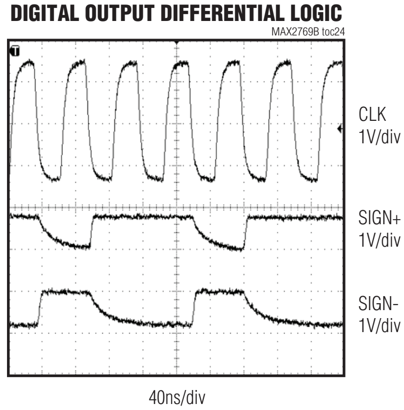
Typical Operating Characteristics (continued)

(MAX2769B EV kit, $V_{CC\_}$ = 2.7V to 3.3V, T_A = -40°C to +85°C, PGM = Ground. Registers are set to the default power-up states. LNA input is driven from a 50Ω source. All RF measurements are done in the analog output mode with ADC bypassed. PGA gain is set to 51dB gain by serial-interface word GAININ = 111010. Maximum IF output load is not to exceed 10kΩ||7.5pF on each pin. Typical values are at $V_{CC\_}$ = 2.85V and T_A = +25°C, unless otherwise noted.)

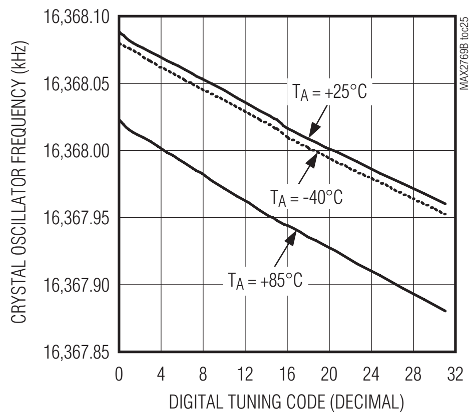
DIGITAL OUTPUT CMOS LOGIC



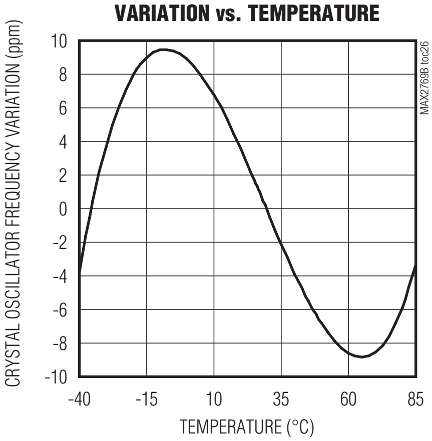
DIGITAL OUTPUT DIFFERENTIAL LOGIC



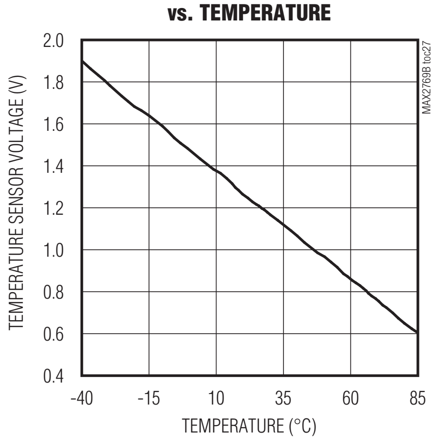
CRYSTAL OSCILLATOR FREQUENCY vs. DIGITAL TUNING CODE



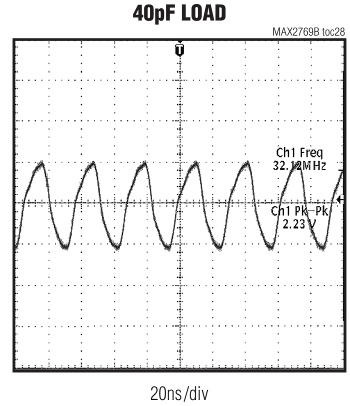
CRYSTAL OSCILLATOR FREQUENCY VARIATION vs. TEMPERATURE



TEMPERATURE SENSOR VOLTAGE vs. TEMPERATURE



CLOCK OUTPUT DRIVER WITH 40pF LOAD



Typical Application Circuit

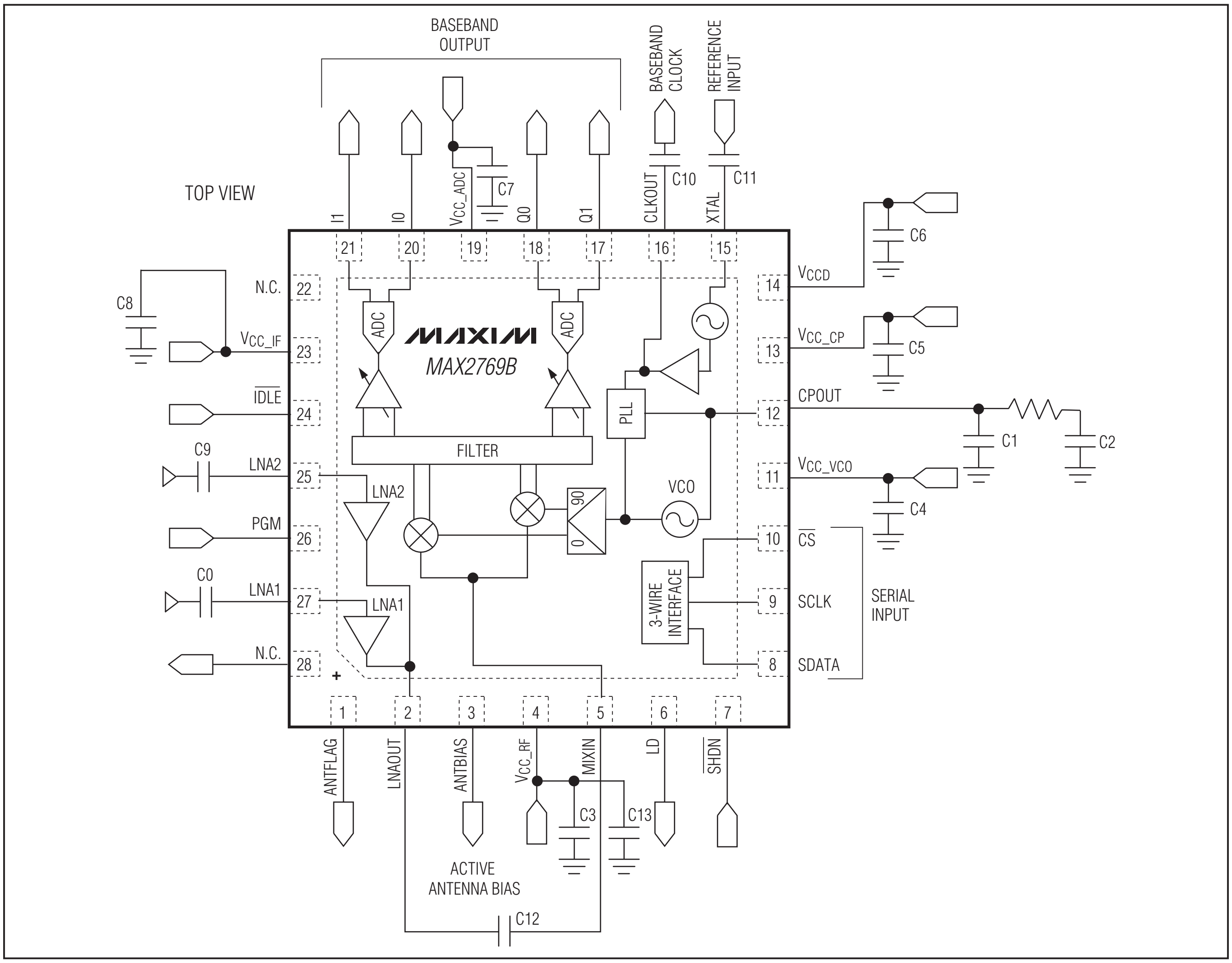
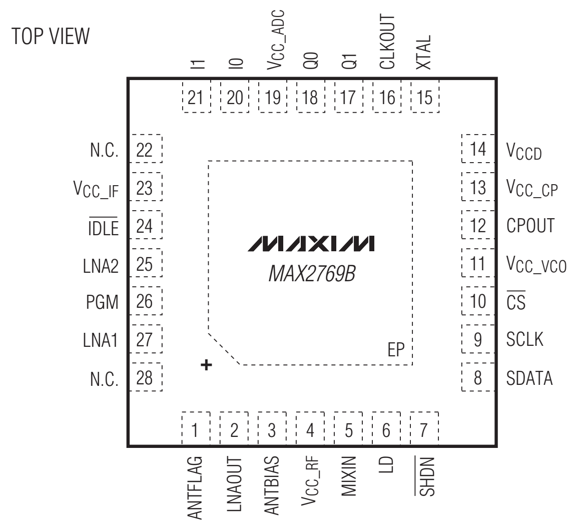


Table 1. Component List

DESIGNATION	QUANTITY	DESCRIPTION
C0, C9	2	0.47nF AC-coupling capacitors
C1	1	27pF PLL loop filter capacitor
C2	1	0.47nF PLL loop filter capacitor
C3–C8	6	0.1µF supply voltage bypass capacitor
C10, C11	2	10nF AC-coupling capacitor
C12	1	0.47nF AC-coupling capacitor
C13	1	0.1nF supply voltage bypass capacitor
R1	1	20kΩ PLL loop filter resistor

Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	ANTFLAG	Active Antenna Flag Logic Output. A logic-high indicates that an active antenna is connected to the ANTBIAS pin.
2	LNAOUT	LNA Output. The LNA output is internally matched to 50Ω.
3	ANTBIAS	Buffered Supply Voltage Output. Provides a supply voltage bias for an external active antenna.
4	V_{CC_RF}	RF Section Supply Voltage. Bypass to ground with 100nF and 100pF capacitors in parallel as close as possible to the pin.
5	MIXIN	Mixer Input. The mixer input is internally matched to 50Ω.
6	LD	Lock-Detector CMOS Logic Output. A logic-high indicates the PLL is locked.
7	$\overline{\text{SHDN}}$	Operation Control Logic Input. A logic-low shuts off the entire device.
8	SDATA	Data Digital Input of 3-Wire Serial Interface
9	SCLK	Clock Digital Input of 3-Wire Serial Interface. Active when $\overline{\text{CS}}$ is low. Data is clocked in on the rising edge of the SCLK.

Pin Description (continued)

PIN	NAME	FUNCTION
10	$\overline{CS}$	Chip-Select Logic Input of 3-Wire Serial Interface. Set $\overline{CS}$ low to allow serial data to shift in. Set $\overline{CS}$ high when the loading action is completed.
11	V_{CC_VCO}	VCO Supply Voltage. Bypass to ground with a 100nF capacitor as close as possible to the pin.
12	CPOUT	Charge-Pump Output. Connect a PLL loop filter as a shunt C and a shunt combination of series R and C (see the *Typical Application Circuit*).
13	V_{CC_CP}	PLL Charge-Pump Supply Voltage. Bypass to ground with a 100nF capacitor as close as possible to the pin.
14	V_{CCD}	Digital Circuitry Supply Voltage. Bypass to ground with a 100nF capacitor as close as possible to the pin.
15	XTAL	XTAL or Reference Oscillator Input. Connect to XTAL or a DC-blocking capacitor if TCXO is used.
16	CLKOUT	Reference Clock Output
17	Q1	Q-Channel Voltage Outputs. Bits 0 and 1 of the Q-channel ADC output or analog differential voltage output.
18	Q0	
19	V_{CC_ADC}	ADC Supply Voltage. Bypass to ground with a 100nF capacitor as close as possible to the pin.
20	I0	I-Channel Voltage Outputs. Bits 0 and 1 of the I-channel ADC output or analog differential voltage output.
21	I1	
22	N.C.	No Connection. Leave this pin unconnected.
23	V_{CC_IF}	IF Section Supply Voltage. Bypass to ground with a 100nF capacitor as close as possible to the pin.
24	$\overline{IDLE}$	Operation Control Logic Input. A logic-low enables the idle mode, in which the XTAL oscillator is active, and all other blocks are off.
25	LNA2	LNA Input Port 2. This port is typically used with an active antenna. Internally matched to 50Ω.
26	PGM	Logic Input. Connect to ground to use the serial interface. A logic-high allows programming to 8 hard-coded by device states connecting SDATA, $\overline{CS}$, and SCLK to supply or ground according to Table 3.
27	LNA1	LNA Input Port 1. This port is typically used with a passive antenna. Internally matched to 50Ω (see the *Typical Application Circuit*).
28	N.C.	No connection. Leave this pin open.
—	EP	Exposed Pad. Ultra-low-inductance connection to ground. Place several vias to the PCB ground plane.

Detailed Description

Integrated Active Antenna Sensor

The MAX2769B includes a low-dropout switch to bias an external active antenna. To activate the antenna switch output, set ANTEN in the Configuration 1 register to logic 1. This closes the switch that connects the antenna bias pin to V_{CC_RF} to achieve a low 200mV dropout for a 20mA load current. A logic-low in ANTEN disables the antenna bias. The active antenna circuit also features short-circuit protection to prevent the output from being shorted to ground.

Low-Noise Amplifier (LNA)

The MAX2769B integrates two low-noise amplifiers. LNA1 is typically used with a passive antenna. This LNA requires an AC-coupling capacitor. In the default mode, the bias current is set to 4mA, the typical noise figure and IIP3 are approximately 0.8dB and -1.1dBm, respectively. LNA2 is typically used with an active antenna. The LNA2 is internally matched to 50. and requires a DC-blocking capacitor. Bits LNAMODE in the Configuration 1 register control the modes of the two LNAs. See Table 6 and Table 7 for the LNA mode settings.

Mixer

The MAX2769B includes a quadrature mixer to output low-IF or zero IF I and Q signals. The quadrature mixer is internally matched to 50Ω and requires a low-side LO injection. The output of the LNA and the input of the mixer are brought off-chip to facilitate the use of a SAW filter.

Programmable Gain Amplifier (PGA)

The MAX2769B integrates a baseband programmable gain amplifier that provides 59dB of gain control range. The PGA gain can be programmed through the serial interface by setting bits GAININ in the Configuration 3 register. Set bits 12 and 11 (AGCMODE) in the Configuration 2 register to 10 to control the gain of the PGA directly from the 3-wire interface.

Automatic Gain Control (AGC)

The MAX2769B provides a control loop that automatically programs PGA gain to provide the ADC with an input power that optimally fills the converter and establishes a desired magnitude bit density at its output. An algorithm operates by counting the number of magnitude bits over 512 ADC clock cycles and comparing the magnitude bit count to the reference value provided through a control word (GAINREF). The desired magnitude bit density is expressed as a value of GAINREF in a decimal format divided by the counter length of 512. For example, to achieve the magnitude bit density of 33%, which is optimal for a 2-bit converter, program the GAINREF to 170, so that 170/512 = 33%.

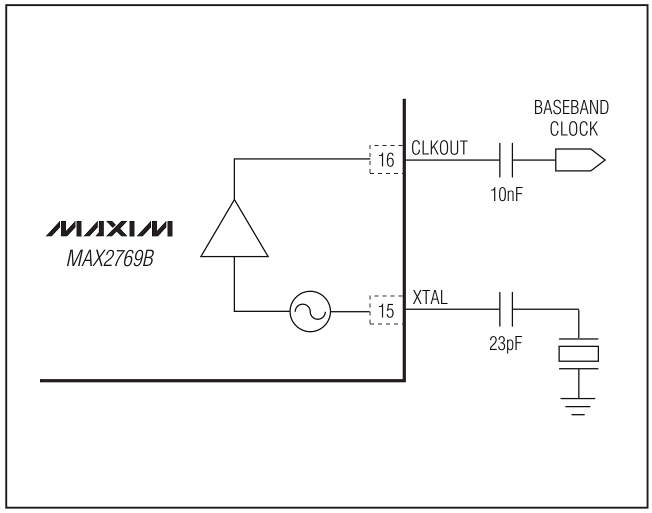


Figure 1. Schematic of the Crystal Oscillator in the MAX2679B EV Kit

Baseband Filter

The baseband filter of the receiver can be programmed to be a lowpass filter or a complex bandpass filter. The lowpass filter can be configured as a 3rd-order Butterworth filter for a reduced group delay by setting bit F3OR5 in the Configuration 1 register to be 1 or a 5th-order Butterworth filter for a steeper out-of-band rejection by setting the same bit to be 0. The two-sided 3dB corner bandwidth can be selected to be 2.5MHz, 4.2MHz, 9.66MHz, or by programming bits FBW in the Configuration 1 register. When the complex filter is enabled by changing bit FCENX in the Configuration 1 register to 1, the lowpass filter becomes a bandpass filter and the center frequency can be programmed by bits FCEN and FCENMSB in the Configuration 1 register.

Table 2. Output Data Format

INTEGER VALUE	SIGN/MAGNITUDE			UNSIGNED BINARY			TWO'S COMPLEMENT BINARY		
	1b	2b	3b	1b	2b	3b	1b	2b	3b
7	0	01	011	1	11	111	0	01	011
5	0	01	010	1	11	110	0	01	010
3	0	00	001	1	10	101	0	00	001
1	0	00	000	1	10	110	0	00	000
-1	1	10	100	0	01	011	1	11	111
-3	1	10	101	0	01	010	1	11	110
-5	1	11	110	0	00	001	1	10	101
-7	1	11	111	0	00	000	1	10	100

Synthesizer

The MAX2769B integrates a 20-bit sigma-delta fractional-N synthesizer allowing the device to tune to a required VCO frequency with an accuracy of approximately ±30Hz. The synthesizer includes a 10-bit reference divider with a divisor range programmable from 1 to 1023, a 15-bit integer portion main divider with a divisor range programmable from 36 to 32767, and also a 20-bit fractional portion main divider. The reference divider is programmable by bits RDIV in the PLL integer division ratio register (see Table 11), and can accommodate reference frequencies from 8MHz to 32MHz. The reference divider needs to be set so the comparison frequency falls between 0.05MHz to 32MHz.

The PLL loop filter is the only external block of the synthesizer. A typical PLL filter is a classic C-R-C network at the charge-pump output. The charge-pump output sink and source current is 0.5mA by default, and the LO tuning gain is 57MHz/V. As an example, see the *Typical Application Circuit* for the recommended loop-filter component values for f_{COMP} = 1.023MHz and loop bandwidth = 50kHz.

The desired integer and fractional divider ratios can be calculated by dividing the LO frequency (f_{LO}) by f_{COMP}. f_{COMP} can be calculated by dividing the TCXO frequency (f_{TCXO}) by the reference division ratio (RDIV). For example, let the TCXO frequency be 20MHz, RDIV be 1, and the nominal LO frequency be 1575.42MHz. The following method can be used when calculating divider ratios supporting various reference and comparison frequencies:

$$\text{Comparison Frequency} = \frac{f_{TCXO}}{RDIV} = \frac{20MHz}{1} = 20MHz$$

$$\text{LO Frequency Divider} = \frac{f_{LO}}{f_{COMP}} = \frac{1575.42MHz}{20MHz} = 78.771$$

Integer Divider = 78(d) = 000 000 0100 1110 (binary)

Fractional Divider = 0.771 x 220 = 808452 (decimal) = 1100 0101 0110 0000 0100

In the fractional mode, the synthesizer should not be operated with integer division ratios greater than 251.

Crystal Oscillator

The MAX2769B includes an on-chip crystal oscillator. A parallel mode crystal is required when the crystal oscillator is being used. It is recommended that an AC-coupling capacitor be used in series with the crystal and the XTAL pin to optimize the desired load capacitance and to center the crystal-oscillator frequency. Take the parasitic loss of interconnect traces on the PCB into account when optimizing the load capacitance. For example, the MAX2769B EV kit utilizes a 16.368MHz crystal that is designed for a 12pF load capacitance. A series capacitor of 23pF is used to center the crystal oscillator frequency, see Figure 1. In addition, the 5-bit serial-interface word, XTALCAP in the PLL Configuration register, can be used to vary the crystal-oscillator frequency electronically. The range of the electronic adjustment depends on how much the chosen crystal frequency can be pulled by the varying capacitor. The frequency of the crystal oscillator used on the MAX2769B EV kit has a range of approximately 200Hz.

The MAX2769B provides a reference clock output. The frequency of the clock can be adjusted to crystal-oscillator frequency, a quarter of the oscillator frequency, a half of the oscillator frequency ($f_{XTAL} \leq$ 16MHz), or twice the oscillator frequency, by programming bits REFDIV in the PLL Configuration register.

ADC

The MAX2769B features an on-chip ADC to digitize the downconverted GPS signal. The maximum sampling rate of the ADC is approximately 50Msps. The sampled output is provided in a 2-bit format (1-bit magnitude and 1-bit sign) by default and also can be configured as a 1-bit or 2-bit in both I and Q channels, or 1-bit, 2-bit, or 3-bit in the I channel only. The ADC supports the digital outputs in three different formats: the unsigned binary, the sign and magnitude, or the two's complement format by setting bits FORMAT in Configuration register 2. MSB bits are output at I1 or Q1 pins and LSB bits are output at I0 or Q0 pins, for I or Q channel, respectively. In the case of 3-bit, output data format is selected in the I channel only, the MSB is output at I1, the second bit is at I0, and the LSB is at Q1.

Figure 2 illustrates the ADC quantization levels for 2-bit and 3-bit cases and also describes the sign/magnitude data mapping. The variable T = 1 designates the location of the magnitude threshold for the 2-bit case.

ADC Fractional Clock Divider

A 12-bit fractional clock divider is located in the clock path prior to the ADC and can be used to generate the ADC clock that is a fraction of the reference input clock. In a fractional divider mode, the instantaneous division ratio alternates between integer division ratios to achieve the required fraction. For example, if the fractional output clock is 4.5 times slower than the input clock, an average division ratio of 4.5 is achieved through an equal series of alternating divide-by-4 and divide-by-5 periods. The fractional division ratio is given by:

$$f_{OUT}/f_{IN} = L_{COUNT}/(4096 - M_{COUNT} + L_{COUNT})$$

where L_{COUNT} and M_{COUNT} are the 12-bit counter values programmed through the serial interface.

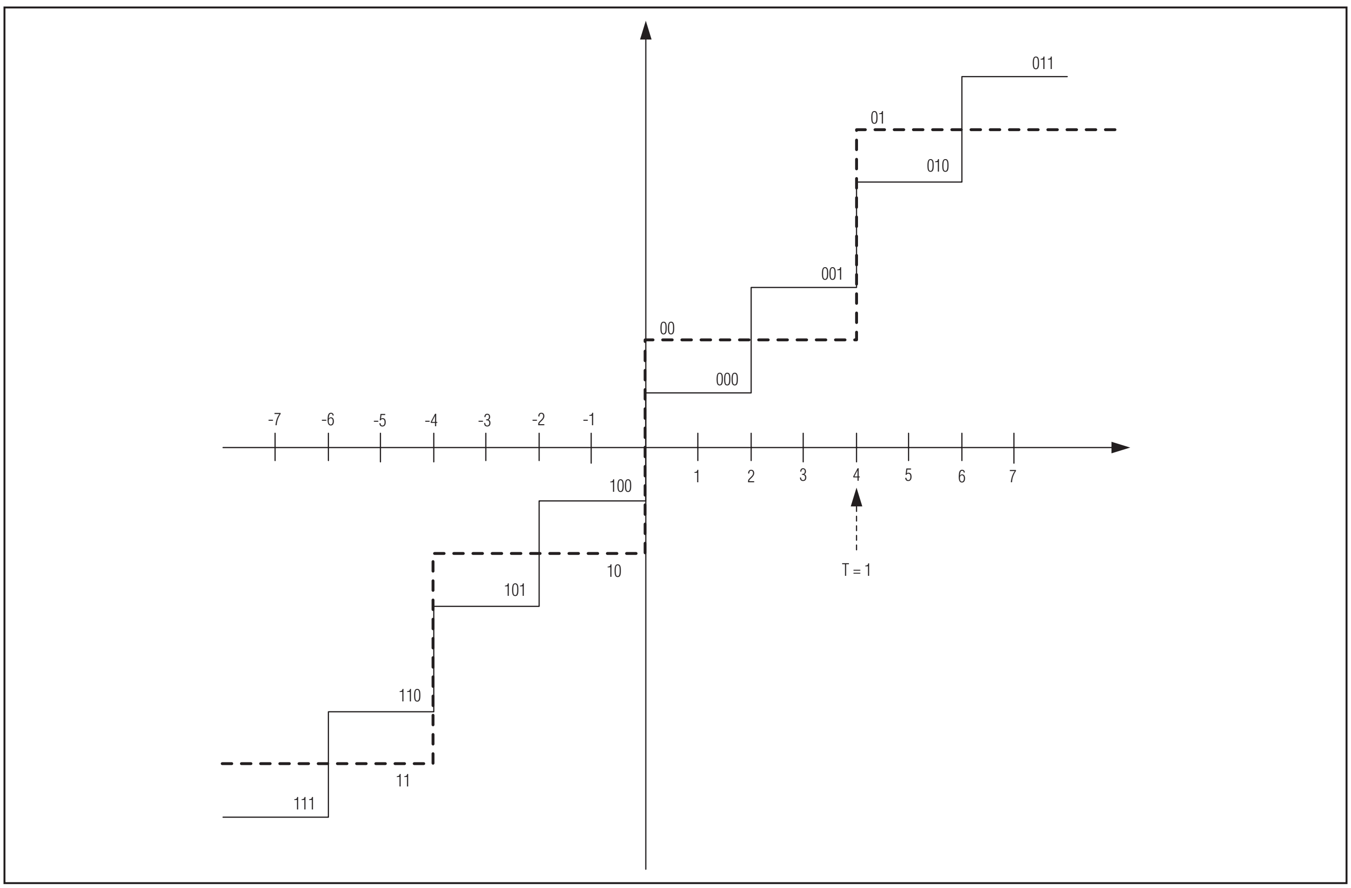


Figure 2. ADC Quantization Levels for 2- and 3-Bit Cases

DSP Interface

GPS data is output from the ADC as the four logic signals (bit_0, bit_1, bit_2, and bit_3) that represent sign/magnitude, unsigned binary, or two's complement binary data in the I (bit_0 and bit_1) and Q (bit_2 and bit_3) channels. The resolution of the ADC can be set up to 3 bits per channel. For example, the 2-bit I and Q data in sign/magnitude format is mapped as follows: $bit_0 = I_{SIGN}$, $bit_1 = I_{MAG}$, $bit_2 = Q_{SIGN}$, and $bit_3 = Q_{MAG}$. The data can be serialized in 16-bit segments of bit_0, followed by bit_1, bit_2, and bit_3. The number of bits to be serialized is controlled by the bits STRMBITS in the Configuration 3 register. This selects between bit_0; bit_0 and bit_1; bit_0 and bit_2; and bit_0, bit_1, bit_2, and bit_3 cases. If only bit_0 is serialized, the data stream consists of bit_0 data only. If a serialization of bit_0 and bit_1 (or bit_2) is selected, the stream data pattern consists of 16 bits of bit_0 data followed by 16 bits of bit_1 (or bit_2) data, which, in turn, is followed by 16 bits of bit_0 data, and so on. In this case, the serial clock must be at least twice as fast as the ADC clock. If a 4-bit serialization of bit_0, bit_1, bit_2, and bit_3 is chosen, the serial clock must be at least four times faster than the ADC clock.

The ADC data is loaded in parallel into four holding registers that correspond to four ADC outputs. Holding registers are 16 bits long and are clocked by the ADC clock. At the end of the 16-bit ADC cycle, the data is transferred into four shift registers and shifted serially to the output during the next 16-bit ADC cycle. Shift registers are clocked by a serial clock that must be chosen fast enough so that all data is shifted out before the next set of data is loaded from the ADC. An all-zero pattern follows the data after all valid ADC data are streamed to the output. A DATASYNC signal is used to signal the beginning of each valid 16-bit data slice. In addition, there is a TIME_SYNC signal that is output every 128 to 16,384 cycles of the ADC clock.

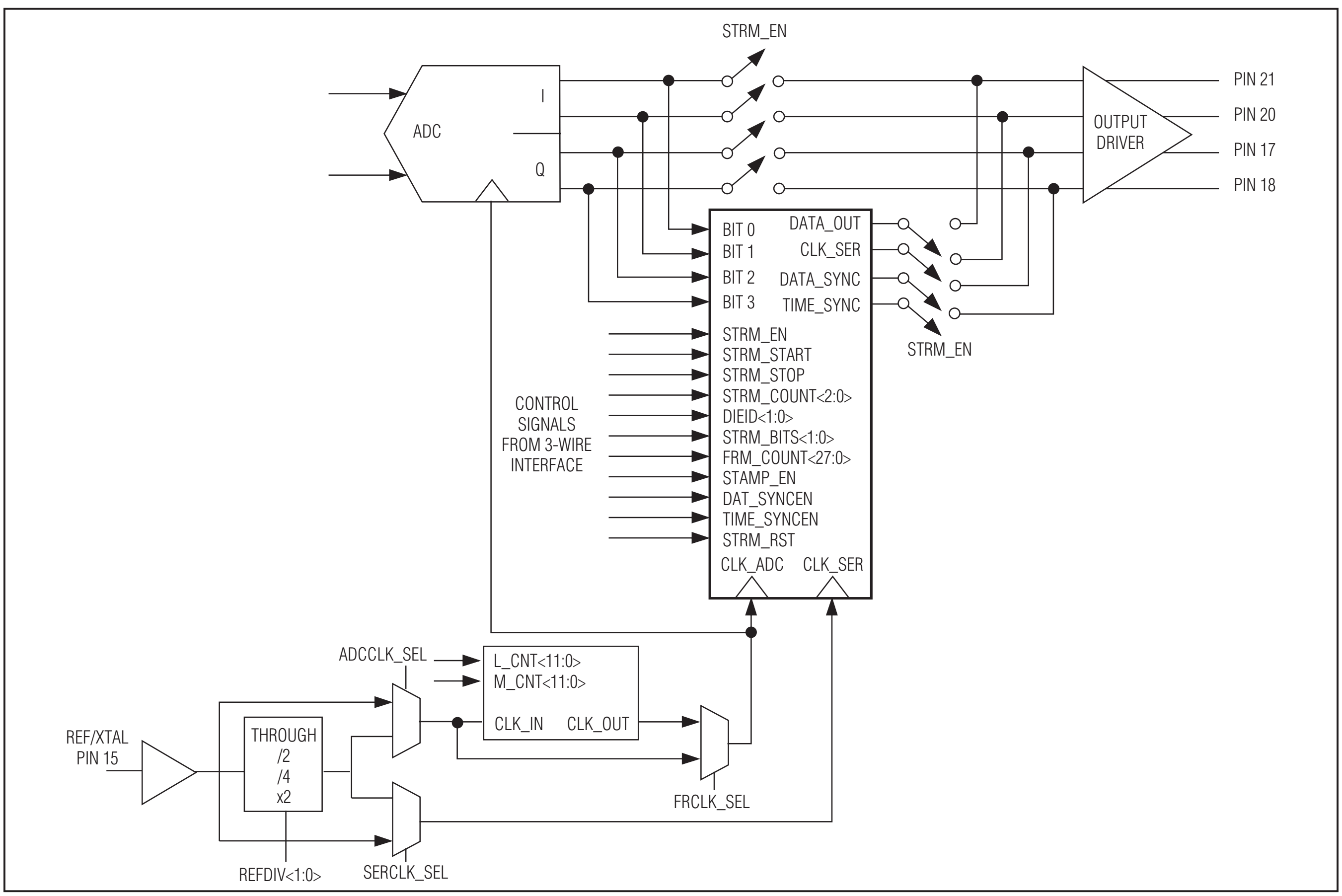


Figure 3. DSP Interface Top-Level Connectivity and Control Signals

Preconfigured Device States

When a serial interface is not available, the device can be used in preconfigured states that don't require programming through the serial interface. Connecting the PGM pin to logic-high and SCLK, SDATA, and $\overline{CS}$ pins to either logic-high or low sets the device in one of the preconfigured states according to Table 3.

Power-On Reset (POR)

The MAX2769B incorporates power-on reset circuitry to ensure that register settings are loaded upon power-up. To ensure proper operation, the rising edge of PGM must occur no sooner than when $V_{CC\_}$ reaches 90% of its final nominal value; see Figure 4 for details.

Serial Interface, Address, and Bit Assignments

A serial interface is used to program the MAX2769B for configuring the different operating modes.

The serial interface is controlled by three signals: SCLK (serial clock), $\overline{CS}$ (chip select), and SDATA (serial data). The control of the PLL, AGC, test, and block selection is performed through the serial-interface bus from the baseband controller. A 32-bit word, with the MSB (D27) being sent first, is clocked into a serial shift register when the chip-select signal is asserted low. The timing of the interface signals is shown in Figure 5 and Table 4 along with typical values for setup and hold time requirements.

Table 3. Preconfigured Device States

DEVICE STATE	DEVICE ELECTRICAL CHARACTERISTICS									3-WIRE CONTROL PINS		
	REFERENCE FREQUENCY (MHz)	REFERENCE DIVISION RATIO	MAIN DIVISION RATIO	I AND Q OR I ONLY	NUMBER OF IQ BITS	I AND Q LOGIC LEVEL	IF CENTER FREQUENCY (MHz)	IF FILTER BW (MHz)	IF FILTER ORDER	SCLK	DATA	$\overline{CS}$
0	16.368	16	1536	I	1	Differential	4.092	2.5	5th	0	0	0
1	16.368	16	1536	I	1	Differential	4.092	2.5	3rd	0	0	1
2	16.368	16	1536	I	2	CMOS	4.092	2.5	5th	0	1	0
3	32.736	32	1536	I	2	CMOS	4.092	2.5	5th	0	1	1
4	19.2	96	7857	I	2	CMOS	4.092	2.5	5th	1	0	0
5	27.456	26	1488	I	3	CMOS	4.092	4.2	5th	1	0	1
6	16.368	16	1536	I	3	CMOS	4.092	4.2	5th	1	1	0
7	27.456	26	1508	I	3	CMOS	9.27075	9.66	5th	1	1	1

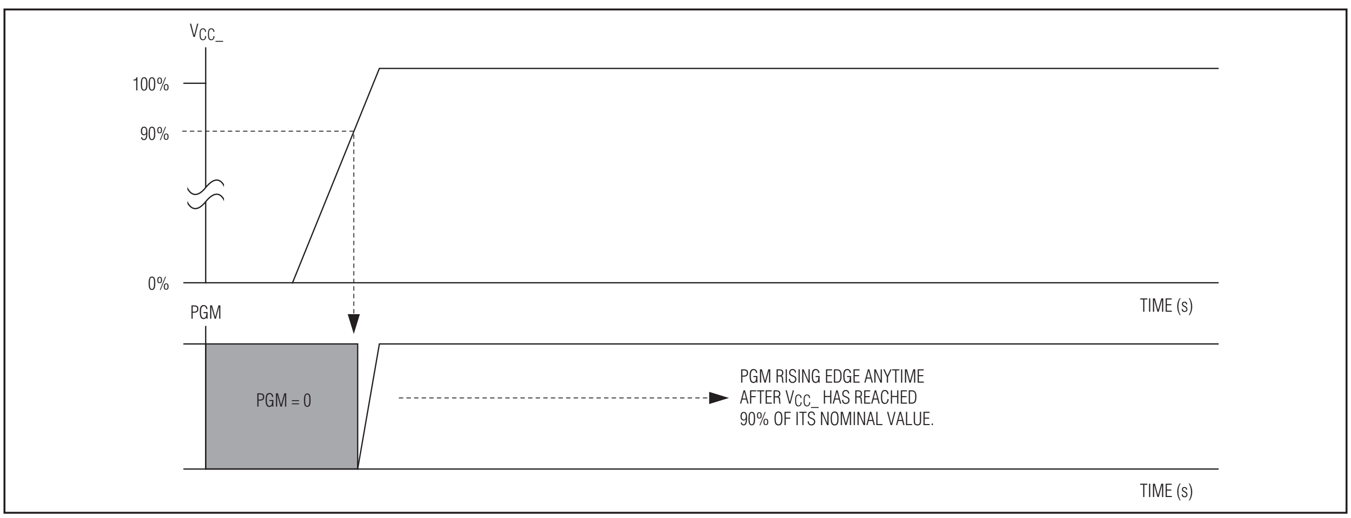


Figure 4. $V_{CC\_}$ Power-On Reset

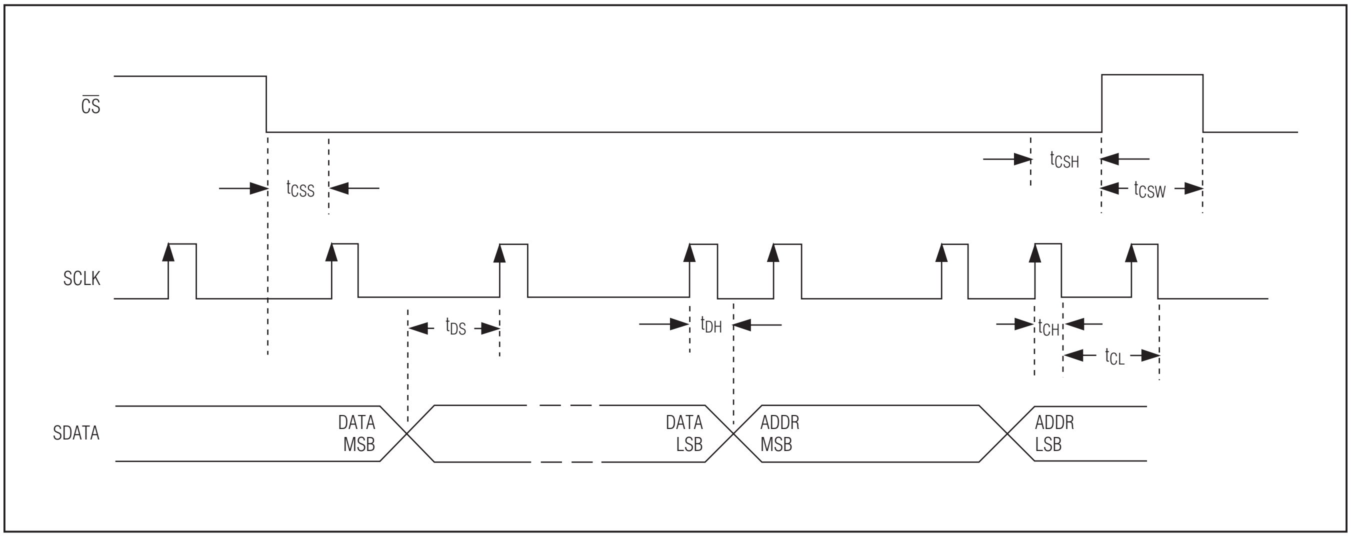


Figure 5. 3-Wire Timing Diagram

Table 4. Serial-Interface Timing Requirements

SYMBOL	PARAMETER	TYP VALUE	UNITS
t_{CSS}	Falling edge of $\overline{CS}$ to rising edge of the first SCLK time.	10	ns
t_{DS}	Data to serial-clock setup time.	10	ns
t_{DH}	Data to clock hold time.	10	ns
t_{CH}	Serial clock pulse-width high.	25	ns
t_{CL}	Clock pulse-width low.	25	ns
t_{CSH}	Last SCLK rising edge to rising edge of $\overline{CS}$.	10	ns
t_{CSW}	$\overline{CS}$ high pulse width.	1	clock

Table 5. Default Register Settings Overview

REGISTER NAME	ADDRESS (A3:A0)	DATA
CONF1	0000	Configures RX and IF sections, bias settings for individual blocks.
CONF2	0001	Configures AGC and output sections.
CONF3	0010	Configures support and test functions for IF filter and AGC.
PLLCONF	0011	PLL, VCO, and CLK settings.
DIV	0100	PLL main and reference division ratios, other controls.
FDIV	0101	PLL fractional division ratio, other controls.
STRM	0110	DSP interface number of frames to stream.
CLK	0111	Fractional clock-divider values.
TEST1	1000	Reserved for test mode.
TEST2	1001	Reserved for test mode.

Table 6. Default Register Settings

REGISTER NAME	ADDRESS (A3:A0)	POWER-ON RESET, PGM = 0 (hex)	PRECONFIGURED DEVICE STATE, PGM = 1 (hex)							
			0	1	2	3	4	5	6	7
CONF1	0000	A2919A3	A2919A3	A2919A3	A2919A7	A2919A3	A2919A3	A293573	A293573	A29B26B
CONF2	0001	055028C	055121C	055028C	055121C	055028C	055028C	855030C	855030C	855030C
CONF3	0010	EAFE1DC	EAFE1DC	EAFE1DC	EAFE1DC	EAFE1DC	EAFE1DC	EAFE1DC	EAFE1DC	EAFE1DC
PLLCONF	0011	9EC0008	9EC0008	9EC0008	9EC0008	9EC0008	9EC0008	9EC0008	9EC0008	9EC0008
DIV	0100	0C00080	0C00080	0C00080	0C00080	0C00100	3D62300	0BA00D0	0C00080	0BC80D0
FDIV	0101	8000070	8000070	8000070	8000070	8000070	8000070	8000070	8000070	8000070
STRM	0110	8000000	8000000	8000000	8000000	8000000	8000000	8000000	8000000	8000000
CLK	0111	10061B2	10061B2	10061B2	10061B2	10061B2	10061B2	10061B2	10061B2	10061B2
TEST1	1000	1E0F401	1E0F401	1E0F401	1E0F401	1E0F401	1E0F401	1E0F401	1E0F401	1E0F401
TEST2	1001	28C0402	28C0402	28C0402	28C0402	28C0402	28C0402	28C0402	28C0402	7CC0403

Detailed Register Definitions

Table 7. Configuration 1 (Address: 0000)

DATA BIT	LOCATION	DEFAULT VALUE (PGM = 0)	DESCRIPTION
CHIPEN	27	1	Chip enable. Set 1 to enable the device and 0 to disable the entire device except the serial bus.
IDLE	26	0	Idle enable. Set 1 to put the chip in the idle mode and 0 for operating mode.
RESERVED	25:22	1000	—
RESERVED	21:20	10	—
RESERVED	19:18	10	—
RESERVED	17:16	01	—
MIXPOLE	15	0	Mixer pole selection. Set 1 to program the passive filter pole at mixer output at 36MHz, or set 0 to program the pole at 13MHz.
LNAMODE	14:13	00	LNA mode selection, D14:D13 = 00: LNA selection gated by the antenna bias circuit, 01: LNA2 is active; 10: LNA1 is active; 11: both LNA1 and LNA2 are off.
MIXEN	12	1	Mixer enable. Set 1 to enable the mixer and 0 to shut down the mixer.
ANTEN	11	1	Antenna bias enable. Set 1 to enable the antenna bias and 0 to shut down the antenna bias.
FCEN	10:5	001101	IF center frequency programming. Default for f_{CENTER} = 3.092MHz, BW = 2.5MHz. The MSB of FCEN is located in Register Test Mode 2 (Table 16). 001101 = 3.092MHz, 001011 = 4.092MHz, 010011 = 10.0MHz
FBW	4:3	00	IF filter center bandwidth selection. D4:D3 = 00: 2.5MHz; 10: 4.2MHz; 01: 9.66MHz; 11: Reserved.
F3OR5	2	0	Filter order selection. Set 0 to select the 5th-order Butterworth filter. Set 1 to select the 3rd-order Butterworth filter.
FCENX	1	1	Polyphase filter selection. Set 1 to select complex bandpass filter mode. Set 0 to select lowpass filter mode.
FGAIN	0	1	IF filter gain setting. Set 0 to reduce the filter gain by 6dB.

Table 8. Configuration 2 (Address: 0001)

DATA BIT	LOCATION	DEFAULT VALUE (PGM = 0)	DESCRIPTION
IQEN	27	0	I and Q channels enable. Set 1 to enable both I and Q channels and 0 to enable I channel only.
GAINREF	26:15	170d	AGC gain reference value expressed by the number of MSB counts (magnitude bit density). 10101010 = 234 magnitude bit density reference, 1010100 = 84 magnitude bit density reference, 100111010 = 314 magnitude bit density reference.
RESERVED	14:13	00	Reserved.
AGCMODE	12:11	00	AGC mode control. Set D12:D11 = 00: independent I and Q; 01: reserved; 10: gain is set directly from the serial interface by GAININ; 11: reserved.
FORMAT	10:9	01	Output data format. Set D10:D9 = 00: unsigned binary; 01: sign and magnitude; 1X: two's complement binary.
BITS	8:6	010	Number of bits in the ADC. Set D8:D6 = 000: 1 bit, 001: reserved; 010: 2 bits; 011: reserved, 100: 3 bits.
DRVCFG	5:4	00	Output driver configuration. Set D5:D4 = 00: CMOS logic, 01: reserved; 1X: analog outputs.
RESERVED	3	1	—
RESERVED	2	0	—
DIEID	1:0	00	Identifies a version of the IC.

Table 9. Configuration 3 (Address: 0010)

DATA BIT	LOCATION	DEFAULT VALUE (PGM = 0)	DESCRIPTION
GAININ	27:22	111010	PGA gain value programming from the serial interface in steps of dB per LSB. 000000 = PGA gain set to 0dB, 101011 = 42dB, 101100 = 43dB, 101110 = 45dB, 111010 = 57dB, 111111 = 62dB.
RESERVED	21	1	—
HILOADEN	20	0	Set 1 to enable the output driver to drive high loads.
RESERVED	19	1	—
RESERVED	18	1	—
RESERVED	17	1	—
RESERVED	16	1	—
FHIPEN	15	1	Highpass coupling enable. Set 1 to enable the highpass coupling between the filter and PGA, or 0 to disable the coupling.
RESERVED	14	1	—
RESERVED	13	1	—
RESERVED	12	0	—
STRMEN	11	0	DSP interface for serial streaming of data enable. This bit configures the IC such that the DSP interface is inserted in the signal path. Set 1 to enable the interface or 0 to disable the interface.

Table 9. Configuration 3 (Address: 0010) (continued)

DATA BIT	LOCATION	DEFAULT VALUE (PGM = 0)	DESCRIPTION
STRMSTART	10	0	The positive edge of this command enables data streaming to the output. It also enables clock, data sync, and frame sync outputs.
STRMSTOP	9	0	The positive edge of this command disables data streaming to the output. It also disables clock, data sync, and frame sync outputs.
RESERVED	8:6	111	—
STRMBITS	5:4	01	Number of bits streamed. D5:D4 = 00: reserved; 01: 1 MSB, 1 LSB; 10: reserved, Q MSB; 11: 1 MSB, 1 LSB, Q MSB, Q LSB.
STAMPEN	3	1	The signal enables the insertion of the frame number at the beginning of each frame. If disabled, only the ADC data is streamed to the output.
TIMESYNCEN	2	1	This signal enables the output of the time sync pulses at all times when streaming is enabled by the STRMEN command. Otherwise, the time sync pulses are available only when data streaming is active at the output, for example, in the time intervals bound by the STRMSTART and STRMSTOP commands.
DATSYNCEN	1	0	This control signal enables the sync pulses at the DATASYNC output. Each pulse is coincident with the beginning of the 16-bit data word that corresponds to a given output bit.
STRMRST	0	0	This command resets all the counters irrespective of the timing within the stream cycle.

Table 10. PLL Configuration (Address: 0011)

DATA BIT	LOCATION	DEFAULT VALUE (PGM = 0)	DESCRIPTION
RESERVED	27	1	—
RESERVED	26	0	—
RESERVED	25	0	—
REFOUTEN	24	1	Clock buffer enable. Set 1 to enable the clock buffer or 0 to disable the clock buffer.
RESERVED	23	1	—
REFDIV	22:21	11	Clock output divider ratio. Set D22:D21 = 00: clock frequency = XTAL frequency x 2; 01: clock frequency = XTAL frequency/4; 10: clock frequency = XTAL frequency/2; 11: clock frequency = XTAL.
IXTAL	20:19	01	Current programming for XTAL oscillator/buffer. Set D20:D19 = 00: reserved; 01: buffer normal current; 10: reserved; 11: oscillator high current.
RESERVED	18:14	10000	—
LDMUX	13:10	0000	PLL lock-detect enable.

Table 10. PLL Configuration (Address: 0011) (continued)

DATA BIT	LOCATION	DEFAULT VALUE (PGM = 0)	DESCRIPTION
ICP	9	0	Charge-pump current selection. Set 1 for 1mA and 0 for 0.5mA.
PFDEN	8	0	Set 0 for normal operation or 1 to disable the PLL phase frequency detector.
RESERVED	7	0	—
RESERVED	6:4	000	—
INT_PLL	3	1	PLL mode control. Set 1 to enable the integer-N PLL or 0 to enable the fractional-N PLL.
PWRSAV	2	0	PLL power-save mode. Set 1 to enable the power-save mode or 0 to disable.
RESERVED	1	0	—
RESERVED	0	0	—

Table 11. PLL Integer Division Ratio (Address 0100)

DATA BIT	LOCATION	DEFAULT VALUE (PGM = 0)	DESCRIPTION
NDIV	27:13	1536d	PLL integer division ratio.
RDIV	12:3	16d	PLL reference division ratio.
RESERVED	2:0	000	—

Table 12. PLL Division Ratio (Address 0101)

DATA BIT	LOCATION	DEFAULT VALUE (PGM = 0)	DESCRIPTION
FDIV	27:8	80000h	PLL fractional divider ratio.
RESERVED	7:0	01110000	—

Table 13. Reserved (Address 0110)

DATA BIT	LOCATION	DEFAULT VALUE (PGM = 0)	DESCRIPTION
RESERVED	27:0	8000000h	—

Table 14. Clock Fractional Division Ratio (Address 0111)

DATA BIT	LOCATION	DEFAULT VALUE (PGM = 0)	DESCRIPTION
L_CNT	27:16	256d	Sets the value for the L counter. 000100000000 = 256 fractional clock divider, 100000000000 = 2048 fractional clock divider.
M_CNT	15:4	1563d	Sets the value for the M counter. 011000011011 = 1563 fractional clock divider, 100000000 = 2048 fractional clock divider.
FCLKIN	3	0	Fractional clock divider. Set 1 to select the ADC clock to come from the fractional clock divider, or 0 to bypass the ADC clock from the fractional clock divider.
ADCCLK	2	0	ADC clock selection. Set 0 to select the ADC and fractional divider clocks to come from the reference divider/multiplier.
RESERVED	1	1	—
MODE	0	0	DSP interface mode selection.

Table 15. Test Mode 1 (Address 1000)

DATA BIT	LOCATION	DEFAULT VALUE (PGM = 0)	DESCRIPTION
RESERVED	27:0	1E0F401	—

Table 16. Test Mode 2 (Address 1001)

DATA BIT	LOCATION	DEFAULT VALUE (PGM = 0)	DESCRIPTION
RESERVED	27:1	28C0402	—
FCENMSB	0	0	When combined with FCEN, this bit represents the MSB of a 7-bit FCEN word.

Applications Information

The LNA and mixer inputs require careful consideration in matching to 50Ω lines. Proper supply bypassing, grounding, and layout are required for reliable performance from any RF circuit.

Layout Issues

The MAX2769B EV kit can be used as a starting point for layout. For best performance, take into consideration grounding and routing of RF, baseband, and power-supply PCB proper line. Make connections from vias to the ground plane as short as possible. On the high-impedance ports, keep traces short to minimize shunt capacitance. EV kit Gerber files can be requested at **www.maxim-ic.com**.

Power-Supply Layout

To minimize coupling between different sections of the IC, a star power-supply routing configuration with a large decoupling capacitor at a central $V_{CC\_}$ node is recommended. The $V_{CC\_}$ traces branch out from this node, each going to a separate $V_{CC\_}$ node in the circuit. Place a bypass capacitor as close as possible to each supply pin This arrangement provides local decoupling at each $V_{CC\_}$ pin. Use at least one via per bypass capacitor for a low-inductance ground connection. Do not share the capacitor ground vias with any other branch.

Refer to **Maxim's Wireless and RF Application Notes** for more information.

Chip Information

PROCESS: SiGe BiCMOS

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX2769ETI/V+	-40°C to +85°C	28 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
/V denotes an automotive qualified part.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
28 TQFN-EP	T2855+3	21-0140	90-0023

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/11	Initial release	—

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