

Operational Amplifiers

Input/Output Full Swing Low Voltage Operating CMOS Operational Amplifiers

BU7261G BU7261SG BU7262xxx BU7262Sxxx BU7264xx BU7264Sxx
General Description

BU7261G, BU7262xxx, BU7264xx are CMOS operational amplifier of the input/output full swing low voltage operation. Also, BU7261SG, BU7262Sxxx, BU7264Sxx which expanded the operating temperature range perform a lineup. It is most suitable for a sensor amplifier and a battery-powered equipment to have a high slew rate, the characteristic of the low input bias current.

Features

- Operable with Low Voltage
- Input-Output Full Swing
- High Slew Rate
- Wide Temperature Range
- Low Input Bias Current

Applications

- Sensor Amplifier
- Battery-powered Equipment
- Portable Equipment
- Consumer Equipment

Key Specifications

- Operating Supply Voltage Range(Single Supply):
+1.8V to +5.5V
- Operating Temperature Range:
BU7261G, BU7262xxx, BU7264xx:
-40°C to +85°C
BU7261SG, BU7262Sxxx, BU7264Sxx:
-40°C to +105°C
- Slew Rate:
1.1 V/μs(Typ)
- Input Offset Current:
1pA (Typ)
- Input Bias Current:
1pA (Typ)

Packages

	W(Typ) x D(Typ) x H(Max)
SSOP5	2.90mm x 2.80mm x 1.25mm
SOP8	5.00mm x 6.20mm x 1.71mm
MSOP8	2.90mm x 4.00mm x 0.90mm
VSON008X2030	2.00mm x 3.00mm x 0.60mm
SOP14	8.70mm x 6.20mm x 1.71mm
SSOP-B14	5.00mm x 6.40mm x 1.35mm

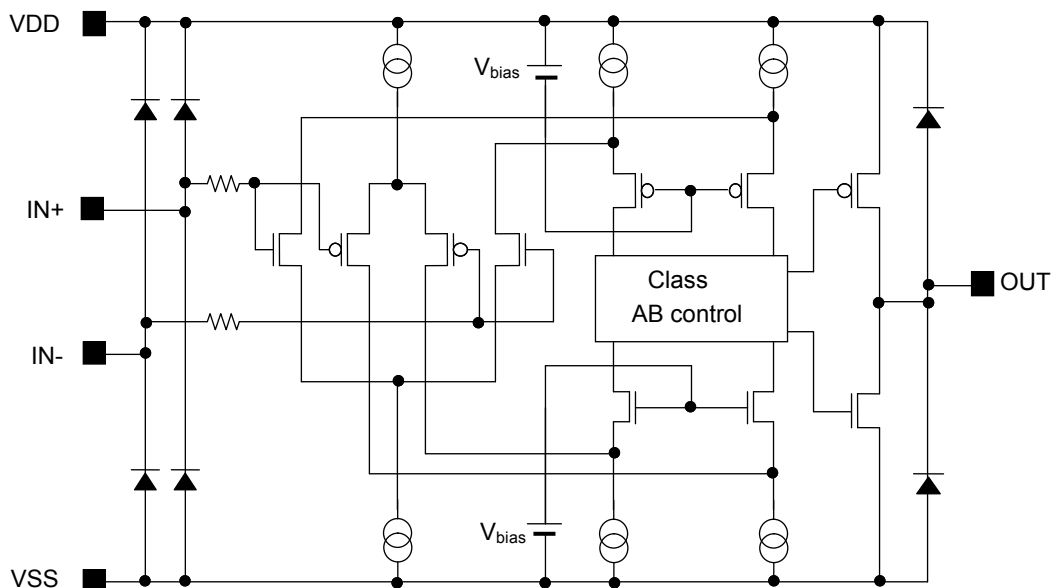
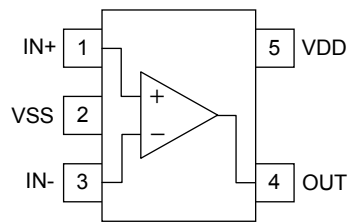


Figure 1. Simplified Schematic (1 channel only)

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays.

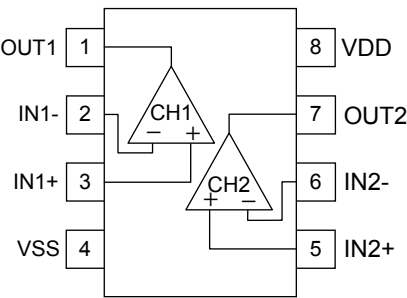
Pin Configuration

BU7261G, BU7261SG : SSOP5



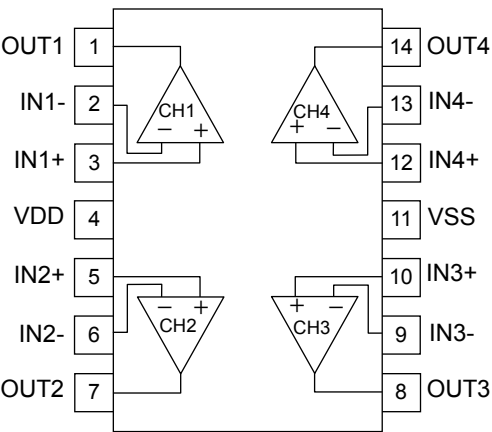
Pin No.	Pin Name
1	IN+
2	VSS
3	IN-
4	OUT
5	VDD

BU7262F, BU7262SF : SOP8
BU7262FVM, BU7262SFVM : MSOP8
BU7262NUX, BU7262SNUX : VSON008X2030



Pin No.	Pin Name
1	OUT1
2	IN1-
3	IN1+
4	VSS
5	IN2+
6	IN2-
7	OUT2
8	VDD

BU7264F, BU7264SF : SOP14
BU7264FV, BU7264SFV : SSOP-B14



Pin No.	Pin Name
1	OUT1
2	IN1-
3	IN1+
4	VDD
5	IN2+
6	IN2-
7	OUT2
8	OUT3
9	IN3-
10	IN3+
11	VSS
12	IN4+
13	IN4-
14	OUT4

Package					
SSOP5	SOP8	VSON008X2030	MSOP8	SOP14	SSOP-B14
BU7261G BU7261SG	BU7262F BU7262SF	BU7262NUX BU7262SNUX	BU7262FVM BU7262SFVM	BU7264F BU7264SF	BU7264FV BU7264SFV

Ordering Information

B U 7 2 6 x x x x x										-	x x	
Part Number					Package					Packaging and forming specification		
BU7261G					G : SSOP5					E2: Embossed tape and reel		
BU7261SG					F : SOP8, SOP14					(SOP8/SOP14/SSOP-B14)		
BU7262xxx					FV : SSOP-B14					TR: Embossed tape and reel		
BU7262Sxxx					FVM: MSOP8					(SSOP5/MSOP8/VSON008X2030)		
BU7264xx					NUX: VSON008X2030							
BU7264Sxx												

Line-up

T _{opr}	Channels	Package		Orderable Part Number
-40°C to +85°C	1ch	SSOP5	Reel of 3000	BU7261G-TR
	2ch	SOP8	Reel of 2500	BU7262F-E2
		MSOP8	Reel of 3000	BU7262FVM-TR
		VSON008X2030	Reel of 4000	BU7262NUX-TR
	4ch	SOP14	Reel of 2500	BU7264F-E2
		SSOP-B14	Reel of 2500	BU7264FV-E2
-40°C to +105°C	1ch	SSOP5	Reel of 3000	BU7261SG-TR
	2ch	SOP8	Reel of 2500	BU7262SF-E2
		MSOP8	Reel of 3000	BU7262SFVM-TR
		VSON008X2030	Reel of 4000	BU7262SNUX-TR
	4ch	SOP14	Reel of 2500	BU7264SF-E2
		SSOP-B14	Reel of 2500	BU7264SFV-E2

Absolute Maximum Ratings ($T_A=25^{\circ}\text{C}$)

OBU7261G, BU7262xxx, BU7264xx

Parameter	Symbol		Rating			Unit
			BU7261G	BU7262xxx	BU7264xx	
Supply Voltage	VDD-VSS		+7			V
Power Dissipation	P_D	SSOP5	0.54 ^(Note 1,7)	-	-	W
		SOP8	-	0.55 ^(Note 2,7)	-	
		MSOP8	-	0.47 ^(Note 3,7)	-	
		VSON008X2030	-	0.41 ^(Note 4,7)	-	
		SOP14	-	-	0.45 ^(Note 5,7)	
		SSOP-B14			0.70 ^(Note 6,7)	
Differential Input Voltage ^(Note 8)	V_{ID}		VDD - VSS			V
Input Common-mode Voltage Range	V_{ICM}		(VSS - 0.3) to (VDD + 0.3)			V
Input Current ^(Note 9)	I_I		± 10			mA
Operating Supply Voltage	V_{opr}		+1.8 to +5.5			V
Operating Temperature	T_{opr}		-40 to +85			$^{\circ}\text{C}$
Storage Temperature	T_{stg}		-55 to +125			$^{\circ}\text{C}$
Maximum Junction Temperature	T_{Jmax}		+125			$^{\circ}\text{C}$

(Note 1) To use at temperature above $T_A=25^{\circ}\text{C}$ reduce 5.4mW/ $^{\circ}\text{C}$.(Note 2) To use at temperature above $T_A=25^{\circ}\text{C}$ reduce 5.5mW/ $^{\circ}\text{C}$.(Note 3) To use at temperature above $T_A=25^{\circ}\text{C}$ reduce 4.7mW/ $^{\circ}\text{C}$.(Note 4) To use at temperature above $T_A=25^{\circ}\text{C}$ reduce 4.1mW/ $^{\circ}\text{C}$.(Note 5) To use at temperature above $T_A=25^{\circ}\text{C}$ reduce 4.5mW/ $^{\circ}\text{C}$.(Note 6) To use at temperature above $T_A=25^{\circ}\text{C}$ reduce 7.0mW/ $^{\circ}\text{C}$.

(Note 7) Mounted on a FR4 glass epoxy PCB 70mm×70mm×1.6mm (Copper foil area less than 3%).

(Note 8) The voltage difference between inverting input and non-inverting input is the differential input voltage. Then input pin voltage is set to more than VSS.

(Note 9) An excessive input current will flow when input voltages of more than VDD+0.6V or less than VSS-0.6V are applied. The input current can be set to less than the rated current by adding a limiting resistor.

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Absolute Maximum Ratings (T_A=25°C)- continued

OBU7261SG, BU7262Sxxx, BU7264Sxx

Parameter	Symbol	Rating			Unit
		BU7261SG	BU7262Sxxx	BU7264Sxx	
Supply Voltage	VDD-VSS	+7			V
Power Dissipation	P _D	SSOP5	0.54 ^(Note 10,16)	-	-
		SOP8	-	0.55 ^(Note 11,16)	-
		MSOP8	-	0.47 ^(Note 12,16)	-
		VSON008X2030	-	0.41 ^(Note 13,16)	-
		SOP14	-	-	0.45 ^(Note 14,16)
		SSOP-B14	-	-	0.70 ^(Note 15,16)
Differential Input Voltage ^(Note 17)	V _{ID}	VDD - VSS			V
Input Common-mode Voltage Range	V _{ICM}	(VSS - 0.3) to (VDD + 0.3)			V
Input Current ^(Note 18)	I _I	±10			mA
Operating Supply Voltage	V _{opr}	+1.8 to +5.5			V
Operating Temperature	T _{opr}	-40 to +105			°C
Storage Temperature	T _{stg}	-55 to +125			°C
Maximum Junction Temperature	T _{Jmax}	+125			°C

(Note 10) To use at temperature above T_A=25°C reduce 5.4mW/°C.

(Note 11) To use at temperature above T_A=25°C reduce 5.5mW/°C.

(Note 12) To use at temperature above T_A=25°C reduce 4.7mW/°C.

(Note 13) To use at temperature above T_A=25°C reduce 4.1mW/°C.

(Note 14) To use at temperature above T_A=25°C reduce 4.5mW/°C.

(Note 15) To use at temperature above T_A=25°C reduce 7.0mW/°C.

(Note 16) Mounted on a FR4 glass epoxy PCB 70mm×70mm×1.6mm (Copper foil area less than 3%).

(Note 17) The voltage difference between inverting input and non-inverting input is the differential input voltage. Then input pin voltage is set to more than VSS.

(Note 18) An excessive input current will flow when input voltages of more than VDD+0.6V or less than VSS-0.6V are applied. The input current can be set to less than the rated current by adding a limiting resistor.

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Electrical Characteristics

OBU7261G, BU7261SG (Unless otherwise specified VDD=+3V, VSS=0V, TA=25°C)

Parameter	Symbol	Temperature Range	Limit			Unit	Conditions
			Min	Typ	Max		
Input Offset Voltage ^(Note 19, 20)	V _{IO}	25°C	-	1	9	mV	VDD=1.8 to 5.5V
		Full range	-	-	10		
Input Offset Current ^(Note 19)	I _{IO}	25°C	-	1	-	pA	-
Input Bias Current ^(Note 19)	I _B	25°C	-	1	-	pA	-
Supply Current ^(Note 20)	I _{DD}	25°C	-	250	550	μA	R _L =∞ A _V =0dB, IN+=1.5V
		Full range	-	-	600		
Maximum Output Voltage(High)	V _{OH}	25°C	VDD-0.1	-	-	V	R _L =10kΩ
Maximum Output Voltage(Low)	V _{OL}	25°C	-	-	VSS+0.1	V	R _L =10kΩ
Large Signal Voltage Gain	A _V	25°C	70	95	-	dB	R _L =10kΩ
Input Common-mode Voltage Range	V _{ICM}	25°C	0	-	3	V	VSS - VDD
Common-mode Rejection Ratio	CMRR	25°C	45	60	-	dB	-
Power Supply Rejection Ratio	PSRR	25°C	60	80	-	dB	-
Output Source Current ^(Note 21)	I _{SOURCE}	25°C	4	10	-	mA	OUT=VDD-0.4V
Output Sink Current ^(Note 21)	I _{SINK}	25°C	5	12	-	mA	OUT=VSS+0.4V
Slew Rate	SR	25°C	-	1.1	-	V/μs	C _L =25pF
Gain Bandwidth	GBW	25°C	-	2	-	MHz	C _L =25pF, A _V =40dB
Phase Margin	θ	25°C	-	50	-	deg	C _L =25pF, A _V =40dB
Total Harmonic Distortion + Noise	THD+N	25°C	-	0.05	-	%	OUT=0.8V _{P-P} , f=1kHz

(Note 19) Absolute value

(Note 20) Full range: BU7261: TA=-40°C to +85°C BU7261S: TA=-40°C to +105°C

(Note 21) Under the high temperature environment, consider the power dissipation of IC when selecting the output current.

When the terminal short circuits are continuously output, the output current is reduced to climb to the temperature inside IC.

Electrical Characteristics - continued

OBU7262xxx, BU7262Sxxx (Unless otherwise specified VDD=+3V, VSS=0V, TA=25°C)

Parameter	Symbol	Temperature Range	Limit			Unit	Conditions
			Min	Typ	Max		
Input Offset Voltage (Note 22, 23)	V _{IO}	25°C	-	1	9	mV	VDD=1.8 to 5.5V
		Full range	-	-	10		
Input Offset Current (Note 22)	I _{IO}	25°C	-	1	-	pA	-
Input Bias Current (Note 22)	I _B	25°C	-	1	-	pA	-
Supply Current (Note 23)	I _{DD}	25°C	-	550	1100	μA	R _L =∞, All Op-Amps A _V =0dB, IN+=1.5V
		Full range	-	-	1200		
Maximum Output Voltage(High)	V _{OH}	25°C	VDD-0.1	-	-	V	R _L =10kΩ
Maximum Output Voltage(Low)	V _{OL}	25°C	-	-	VSS+0.1	V	R _L =10kΩ
Large Signal Voltage Gain	A _V	25°C	70	95	-	dB	R _L =10kΩ
Input Common-mode Voltage Range	V _{ICM}	25°C	0	-	3	V	VSS - VDD
Common-mode Rejection Ratio	CMRR	25°C	45	60	-	dB	-
Power Supply Rejection Ratio	PSRR	25°C	60	80	-	dB	-
Output Source Current (Note 24)	I _{SOURCE}	25°C	4	10	-	mA	OUT=VDD-0.4V
Output Sink Current (Note 24)	I _{SINK}	25°C	5	12	-	mA	OUT=VSS+0.4V
Slew Rate	SR	25°C	-	1.1	-	V/μs	C _L =25pF
Gain Bandwidth	GBW	25°C	-	2	-	MHz	C _L =25pF, A _V =40dB
Phase Margin	θ	25°C	-	50	-	deg	C _L =25pF, A _V =40dB
Total Harmonic Distortion + Noise	THD+N	25°C	-	0.05	-	%	OUT=0.8V _{P-P} , f=1kHz
Channel Separation	CS	25°C	-	100	-	dB	A _V =40dB, OUT=1Vrms

(Note 22) Absolute value

(Note 23) Full range: BU7262: T_A=-40°C to +85°C BU7262S: T_A=-40°C to +105°C

(Note 24) Under the high temperature environment, consider the power dissipation of IC when selecting the output current.

When the terminal short circuits are continuously output, the output current is reduced to climb to the temperature inside IC.

Electrical Characteristics - continued

OBU7264xx, BU7264Sxx (Unless otherwise specified VDD=+3V, VSS=0V, T_A=25°C)

Parameter	Symbol	Temperature Range	Limit			Unit	Conditions
			Min	Typ	Max		
Input Offset Voltage ^(Note 25, 26)	V _{IO}	25°C	-	1	9	mV	VDD=1.8 to 5.5V
		Full range	-	-	10		
Input Offset Current ^(Note 25)	I _{IO}	25°C	-	1	-	pA	-
Input Bias Current ^(Note 25)	I _B	25°C	-	1	-	pA	-
Supply Current ^(Note 26)	I _{DD}	25°C	-	1100	2300	μA	R _L =∞, All Op-Amps A _V =0dB, IN+=1.5V
		Full range	-	-	2800		
Maximum Output Voltage(High)	V _{OH}	25°C	VDD-0.1	-	-	V	R _L =10kΩ
Maximum Output Voltage(Low)	V _{OL}	25°C	-	-	VSS+0.1	V	R _L =10kΩ
Large Signal Voltage Gain	A _V	25°C	70	95	-	dB	R _L =10kΩ
Input Common-mode Voltage Range	V _{ICM}	25°C	0	-	3	V	VSS - VDD
Common-mode Rejection Ratio	CMRR	25°C	45	60	-	dB	-
Power Supply Rejection Ratio	PSRR	25°C	60	80	-	dB	-
Output Source Current ^(Note 27)	I _{SOURCE}	25°C	4	10	-	mA	OUT=VDD-0.4V
Output Sink Current ^(Note 27)	I _{SINK}	25°C	5	12	-	mA	OUT=VSS+0.4V
Slew Rate	SR	25°C	-	1.1	-	V/μs	C _L =25pF
Gain Bandwidth	GBW	25°C	-	2	-	MHz	C _L =25pF, A _V =40dB
Phase Margin	θ	25°C	-	50	-	deg	C _L =25pF, A _V =40dB
Total Harmonic Distortion + Noise	THD+N	25°C	-	0.05	-	%	OUT=0.8V _{P-P} , f=1kHz
Channel Separation	CS	25°C	-	100	-	dB	A _V =40dB, OUT=1V _{rms}

(Note 25) Absolute value

(Note 26) Full range: BU7264: T_A=-40°C to +85°C BU7264S: T_A=-40°C to +105°C

(Note 27) Under the high temperature environment, consider the power dissipation of IC when selecting the output current.

When the terminal short circuits are continuously output, the output current is reduced to climb to the temperature inside IC.

Description of electrical characteristics

Described below are descriptions of the relevant electrical terms used in this datasheet. Items and symbols used are also shown. Note that item name and symbol and their meaning may differ from those on another manufacturer's document or general document.

1. Absolute maximum ratings

Absolute maximum rating items indicate the condition which must not be exceeded. Application of voltage in excess of absolute maximum rating or use out of absolute maximum rated temperature environment may cause deterioration of characteristics.

- (1) Supply Voltage (VDD/VSS)
Indicates the maximum voltage that can be applied between the VDD terminal and VSS terminal without deterioration or destruction of characteristics of internal circuit.
- (2) Differential Input Voltage (V_{ID})
Indicates the maximum voltage that can be applied between non-inverting and inverting terminals without damaging the IC.
- (3) Input Common-mode Voltage Range (V_{ICM})
Indicates the maximum voltage that can be applied to the non-inverting and inverting terminals without deterioration or destruction of electrical characteristics. Input common-mode voltage range of the maximum ratings does not assure normal operation of IC. For normal operation, use the IC within the input common-mode voltage range characteristics.
- (4) Power Dissipation (P_D)
Indicates the power that can be consumed by the IC when mounted on a specific board at the ambient temperature 25°C (normal temperature). As for package product, P_D is determined by the temperature that can be permitted by the IC in the package (maximum junction temperature) and the thermal resistance of the package.

2. Electrical characteristics

- (1) Input Offset Voltage (V_{IO})
Indicates the voltage difference between non-inverting terminal and inverting terminals. It can be translated into the input voltage difference required for setting the output voltage at 0 V.
- (2) Input Offset Current (I_{IO})
Indicates the difference of input bias current between the non-inverting and inverting terminals.
- (3) Input Bias Current (I_B)
Indicates the current that flows into or out of the input terminal. It is defined by the average of input bias currents at the non-inverting and inverting terminals.
- (4) Supply Current (I_{DD})
Indicates the current that flows within the IC under specified no-load conditions.
- (5) Maximum Output Voltage(High) / Maximum Output Voltage(Low) (V_{OH}/V_{OL})
Indicates the voltage range of the output under specified load condition. It is typically divided into maximum output voltage high and low. Maximum output voltage high indicates the upper limit of output voltage. Maximum output voltage low indicates the lower limit.
- (6) Large Signal Voltage Gain (A_V)
Indicates the amplifying rate (gain) of output voltage against the voltage difference between non-inverting terminal and inverting terminal. It is normally the amplifying rate (gain) with reference to DC voltage.
 $A_v = (\text{Output voltage}) / (\text{Differential Input voltage})$
- (7) Input Common-mode Voltage Range (V_{ICM})
Indicates the input voltage range where IC normally operates.
- (8) Common-mode Rejection Ratio (CMRR)
Indicates the ratio of fluctuation of input offset voltage when the input common mode voltage is changed. It is normally the fluctuation of DC.
 $CMRR = (\text{Change of Input common-mode voltage}) / (\text{Input offset fluctuation})$
- (9) Power Supply Rejection Ratio (PSRR)
Indicates the ratio of fluctuation of input offset voltage when supply voltage is changed.
It is normally the fluctuation of DC.
 $PSRR = (\text{Change of power supply voltage}) / (\text{Input offset fluctuation})$
- (10) Output Source Current / Output Sink Current (I_{SOURCE}/I_{SINK})
The maximum current that can be output under specific output conditions, it is divided into output source current and output sink current. The output source current indicates the current flowing out of the IC, and the output sink current the current flowing into the IC.
- (11) Slew Rate (SR)
Indicates the ratio of the change in output voltage with time when a step input signal is applied.
- (12) Gain Bandwidth (GBW)
The product of the open-loop voltage gain and the frequency at which the voltage gain decreases 6dB/octave.

- (13) Phase Margin (θ)
Indicates the margin of phase from 180 degree phase lag at unity gain frequency.
- (14) Total Harmonic Distortion + Noise (THD+N)
Indicates the fluctuation of input offset voltage or that of output voltage with reference to the change of output voltage of driven channel.
- (15) Channel Separation (CS)
Indicates the fluctuation in the output voltage of the driven channel with reference to the change of output voltage of the channel which is not driven.

Typical Performance Curves

OBU7261G, BU7261SG

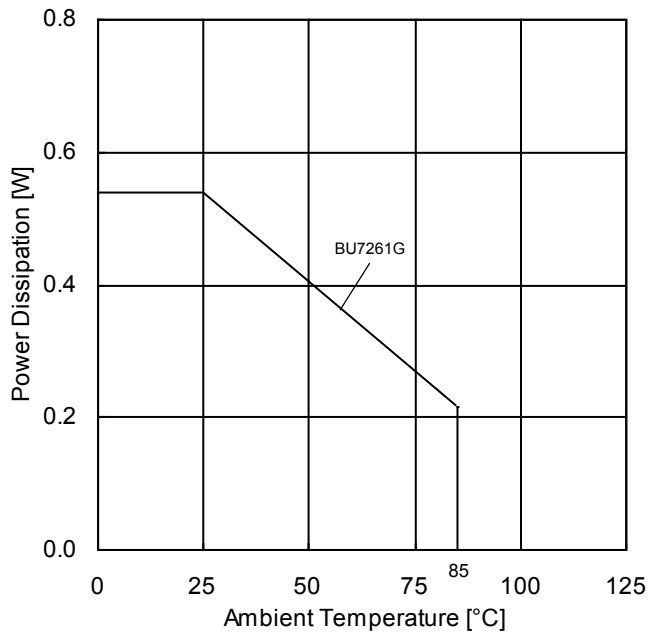


Figure 2.
Power Dissipation vs Ambient Temperature
(Derating Curve)

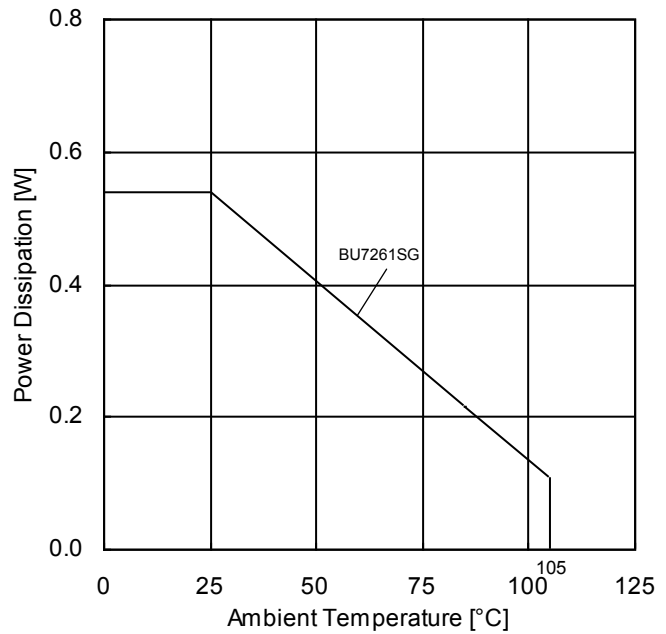


Figure 3.
Power Dissipation vs Ambient Temperature
(Derating Curve)

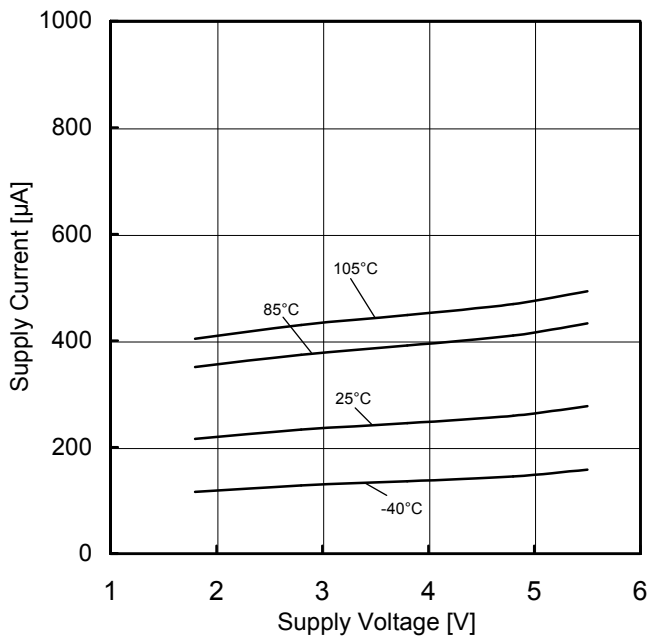


Figure 4.
Supply Current vs Supply Voltage

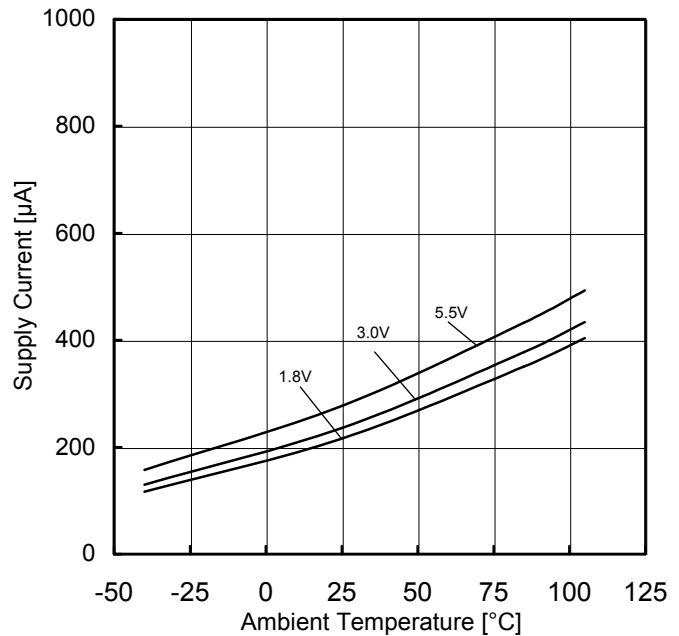


Figure 5.
Supply Current vs Ambient Temperature

(*)The above characteristics are measurements of typical sample, they are not guaranteed.

BU7261G: -40°C to +85°C BU7261SG: -40°C to +105°C

Typical Performance Curves - Continued

OBU7261G, BU7261SG

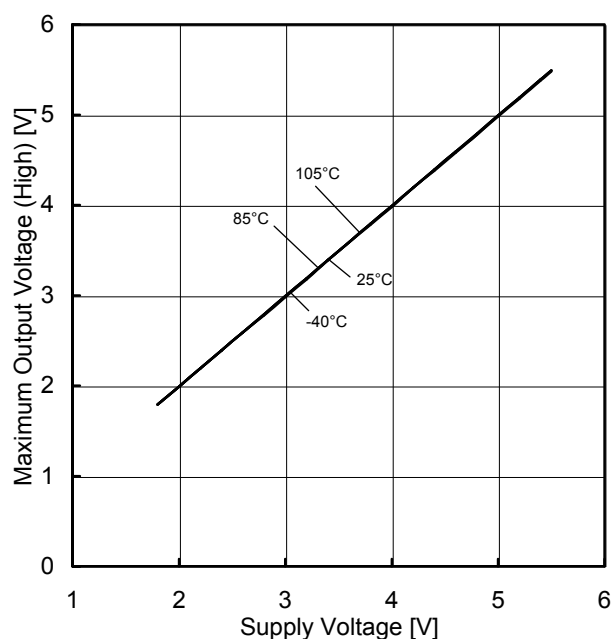


Figure 6.
Maximum Output Voltage (High) vs Supply Voltage
($R_L=10k\Omega$)

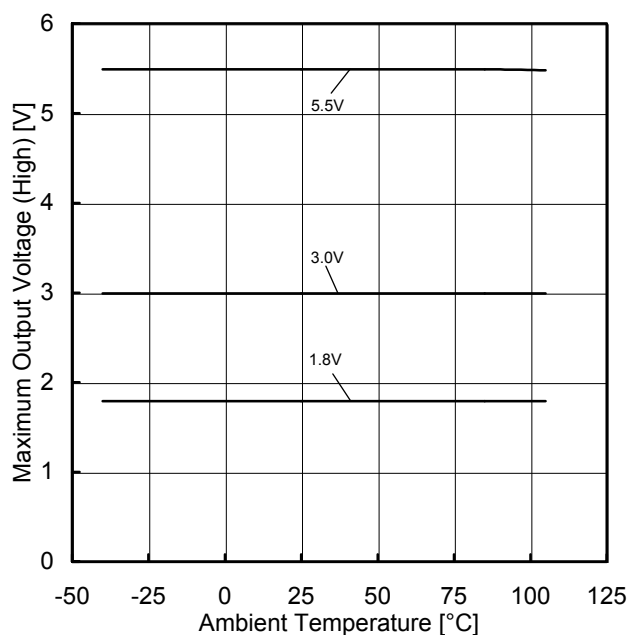


Figure 7.
Maximum Output Voltage (High) vs Ambient Temperature
($R_L=10k\Omega$)

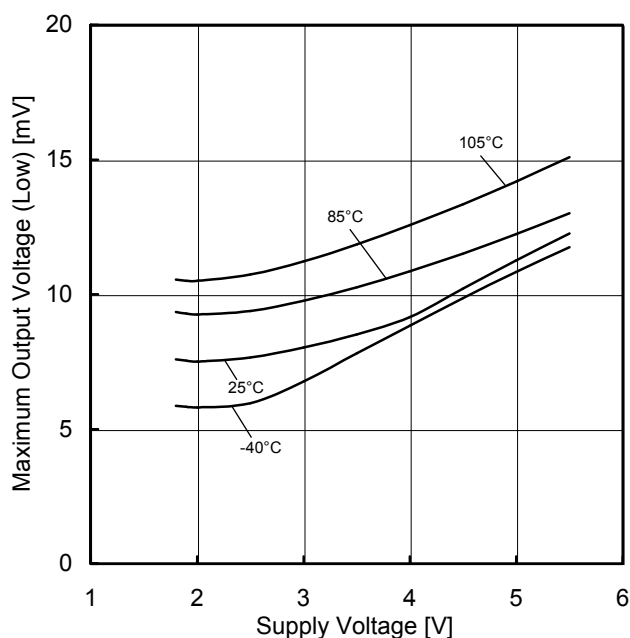


Figure 8.
Maximum Output Voltage (Low) vs Supply Voltage
($R_L=10k\Omega$)

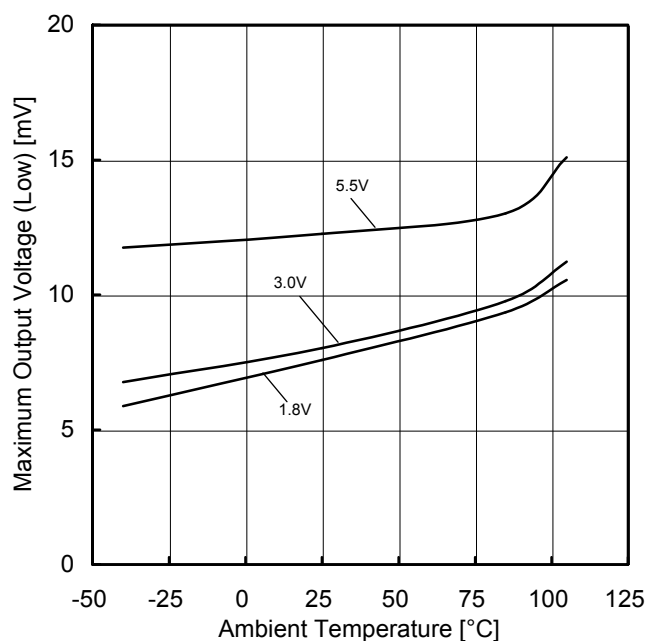


Figure 9.
Maximum Output Voltage (Low) vs Ambient Temperature
($R_L=10k\Omega$)

(*)The above characteristics are measurements of typical sample, they are not guaranteed.

BU7261G: -40°C to +85°C BU7261SG: -40°C to +105°C

Typical Performance Curves - Continued

OBU7261G, BU7261SG

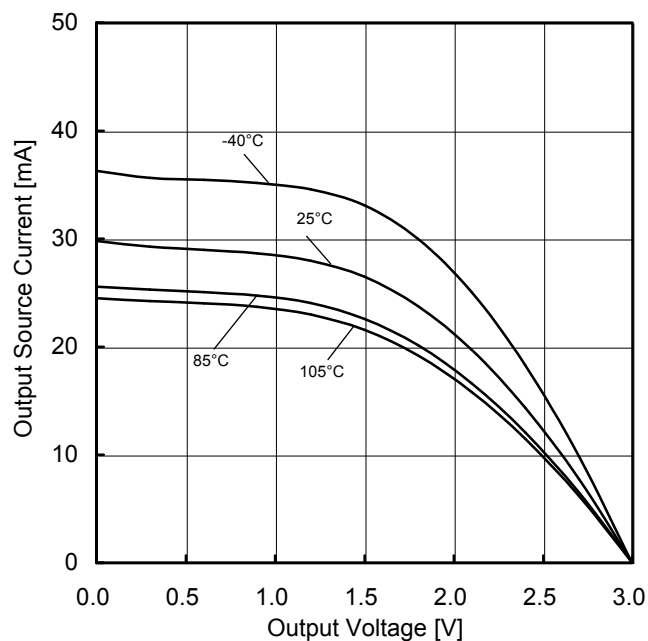


Figure 10.
Output Source Current vs Output Voltage
(VDD=3V)

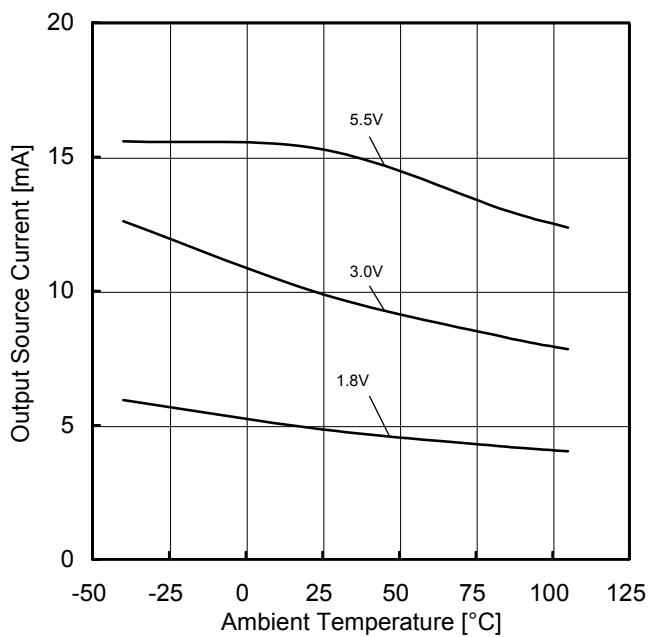


Figure 11.
Output Source Current vs Ambient Temperature
(OUT=VDD-0.4V)

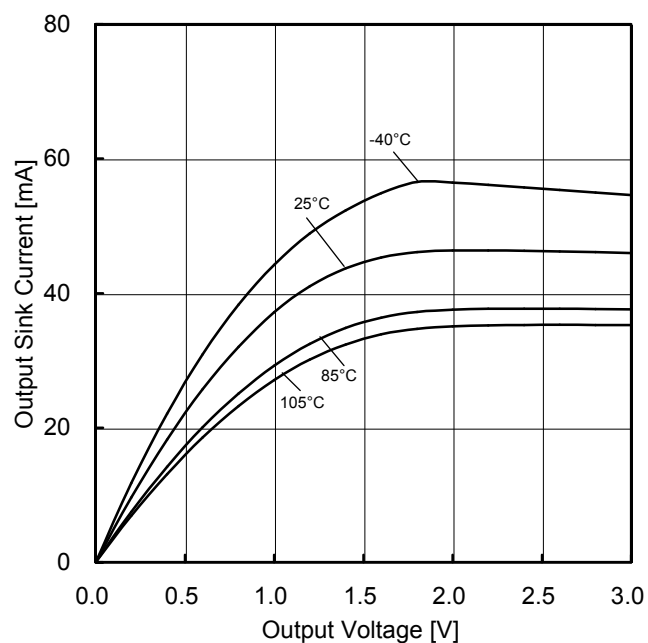


Figure 12.
Output Sink Current vs Output Voltage
(VDD=3V)

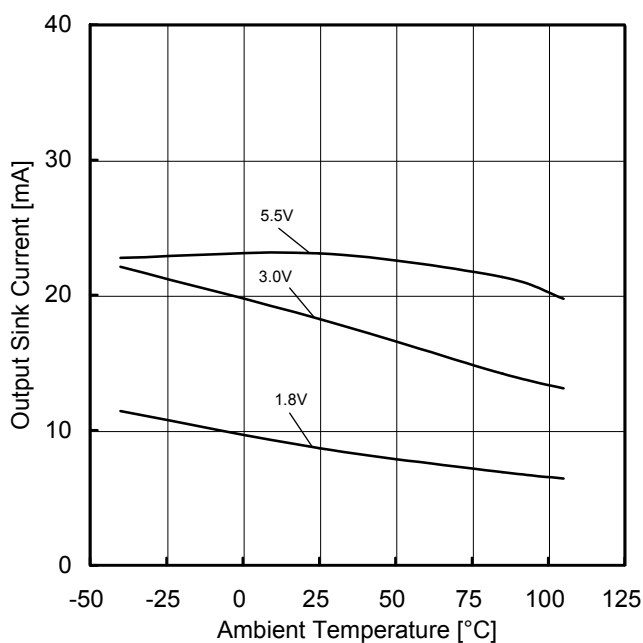


Figure 13.
Output Sink Current vs Ambient Temperature
(OUT=VSS+0.4V)

(*)The above characteristics are measurements of typical sample, they are not guaranteed.

BU7261G: -40°C to +85°C BU7261SG: -40°C to +105°C

Typical Performance Curves - Continued

OBU7261G, BU7261SG

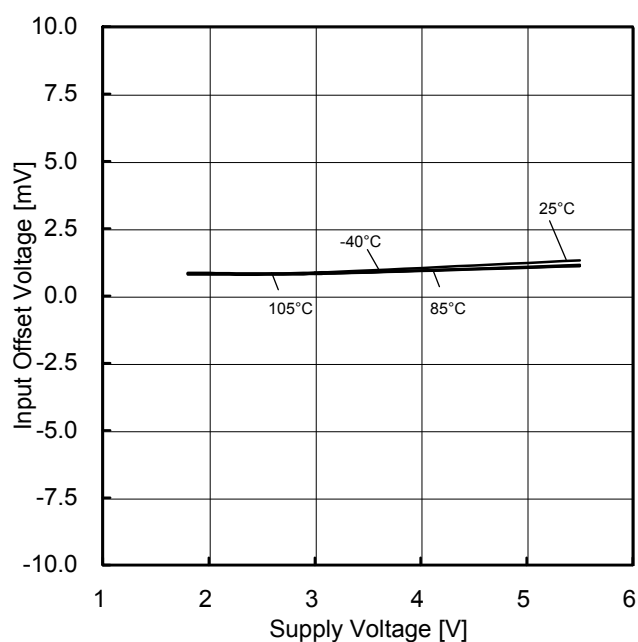


Figure 14.
Input Offset Voltage vs Supply Voltage
($V_{ICM}=V_{DD}$, $E_K=-V_{DD}/2$)

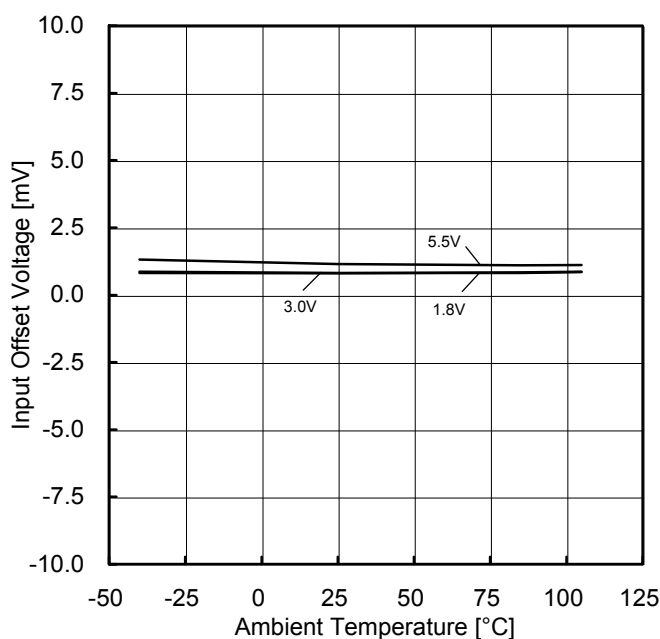


Figure 15.
Input Offset Voltage vs Ambient Temperature
($V_{ICM}=V_{DD}$, $E_K=-V_{DD}/2$)

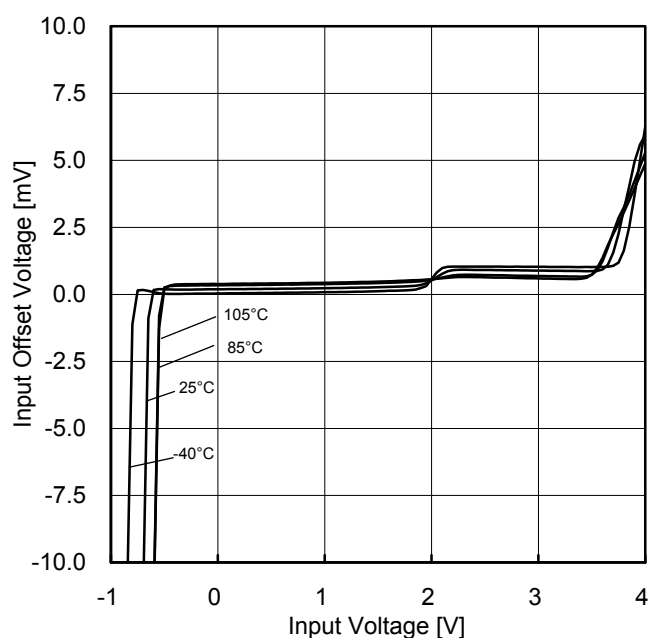


Figure 16.
Input Offset Voltage vs Input Voltage
($V_{DD}=3V$)

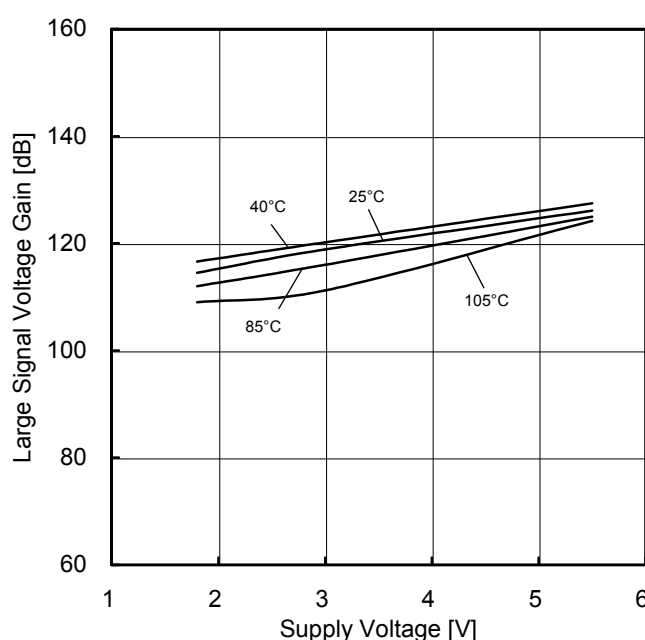


Figure 17.
Large Signal Voltage Gain vs Supply Voltage

(*)The above characteristics are measurements of typical sample, they are not guaranteed.

BU7261G: -40°C to +85°C BU7261SG: -40°C to +105°C

Typical Performance Curves - Continued

OBU7261G, BU7261SG

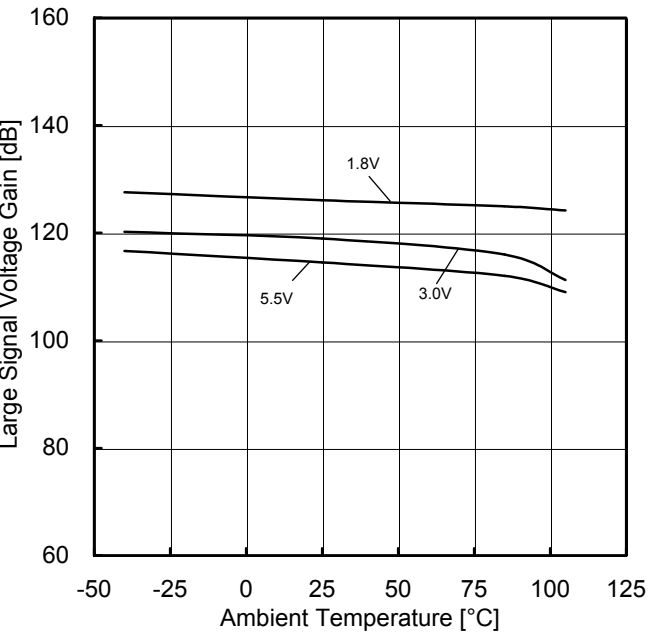


Figure 18.
Large Signal Voltage Gain vs Ambient Temperature

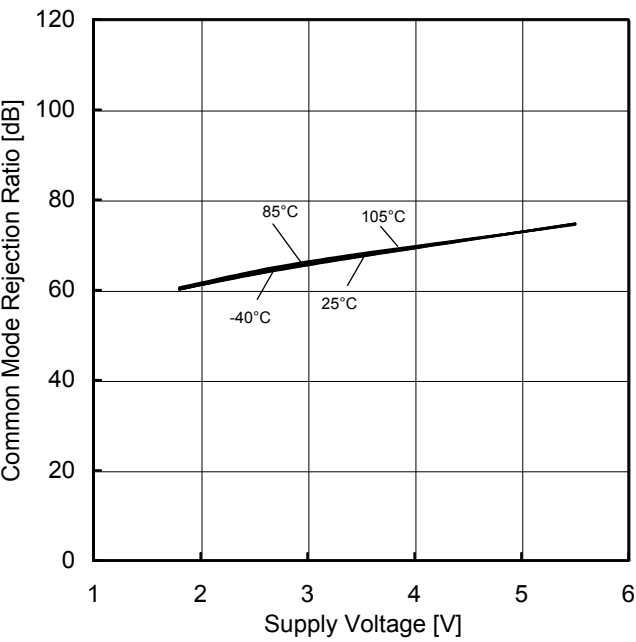


Figure 19.
Common Mode Rejection Ratio vs Supply Voltage

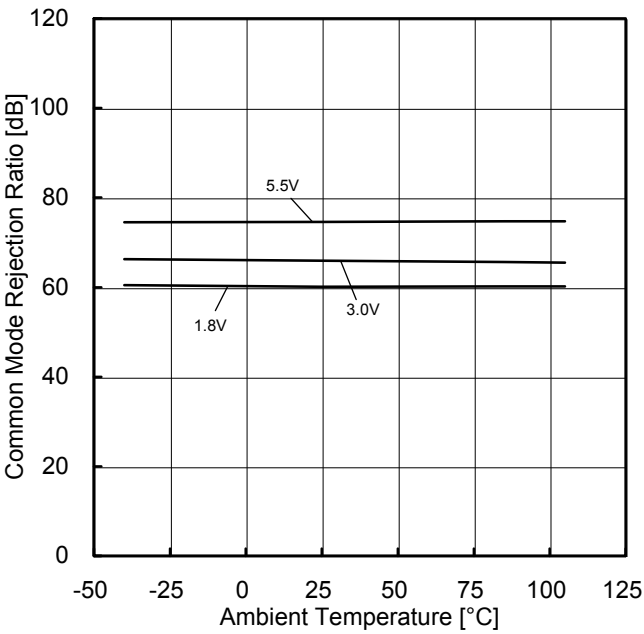


Figure 20.
Common Mode Rejection Ratio vs Ambient Temperature

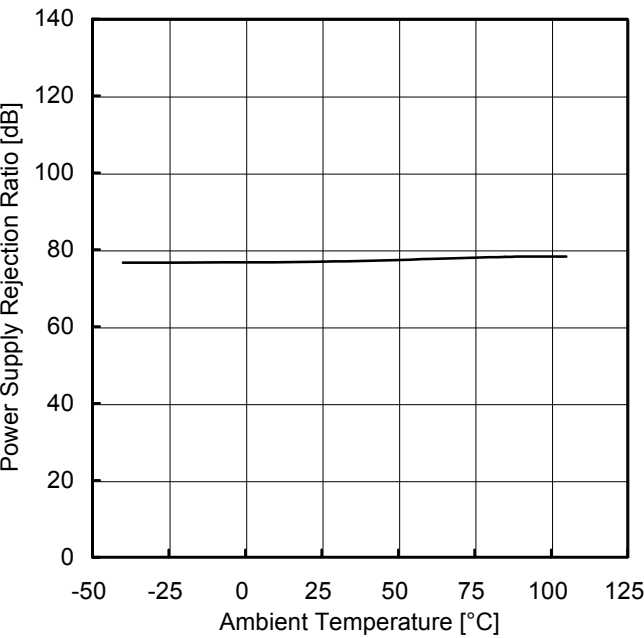


Figure 21.
Power Supply Rejection Ratio vs Ambient Temperature

(*)The above characteristics are measurements of typical sample, they are not guaranteed.
BU7261G: -40°C to +85°C BU7261SG: -40°C to +105°C

Typical Performance Curves - Continued

OBU7261G, BU7261SG

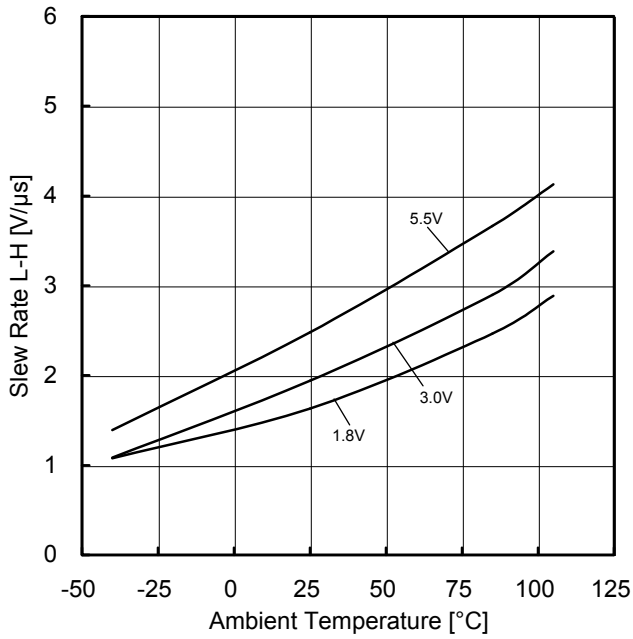


Figure 22.
Slew Rate L-H vs Ambient Temperature

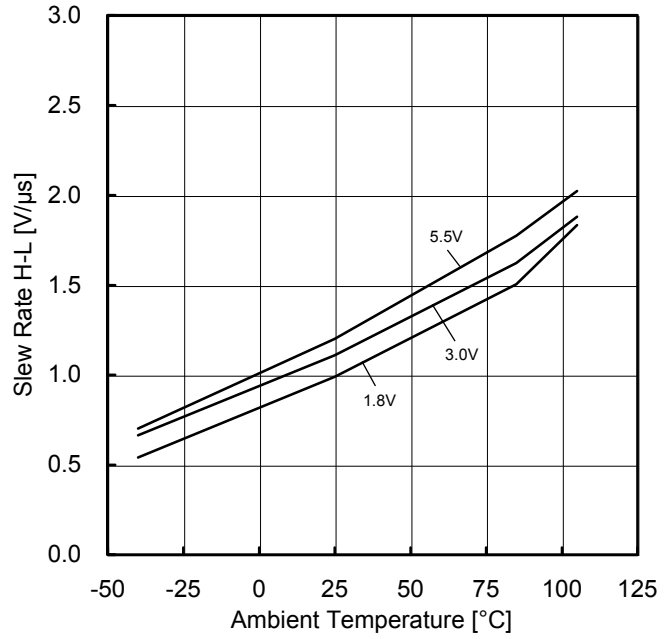


Figure 23.
Slew Rate H-L vs Ambient Temperature

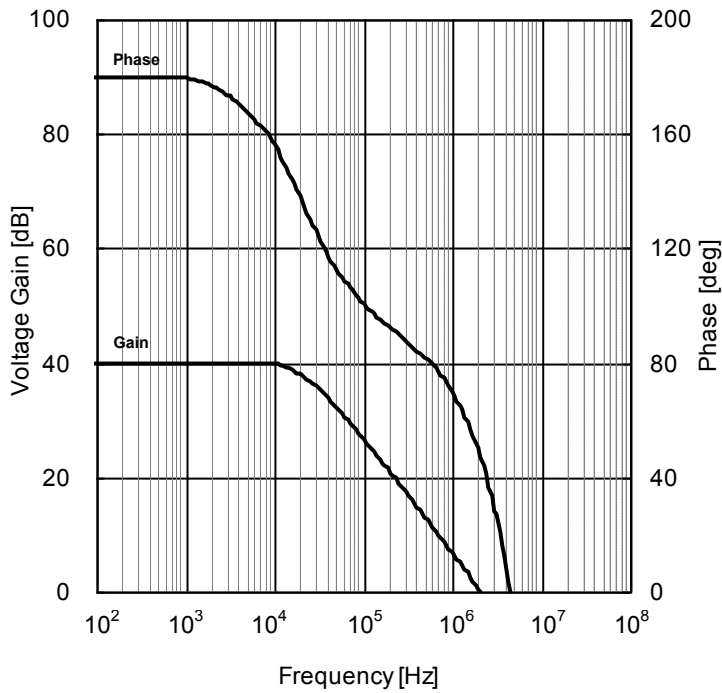


Figure 24.
Voltage Gain • Phase vs Frequency

(*)The above characteristics are measurements of typical sample, they are not guaranteed.
BU7261G: -40°C to +85°C BU7261SG: -40°C to +105°C

Typical Performance Curves – Continued

OBU7262xxx, BU7262Sxxx

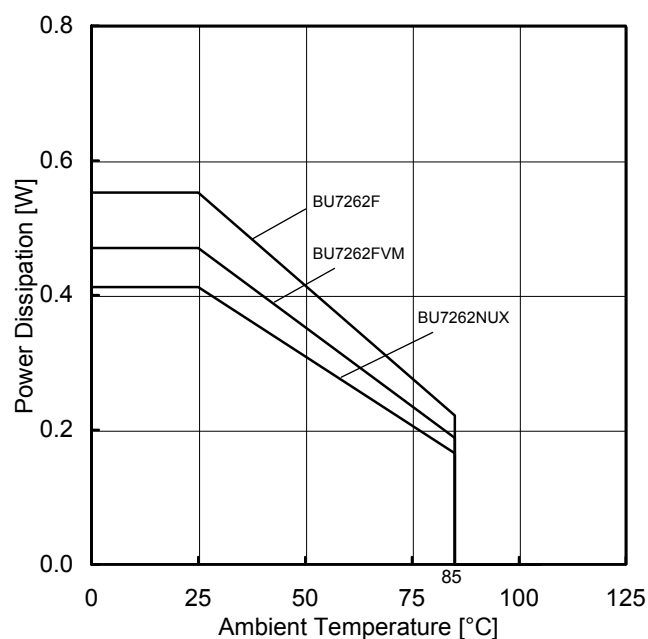


Figure 25.
Power Dissipation vs Ambient Temperature
(Derating Curve)

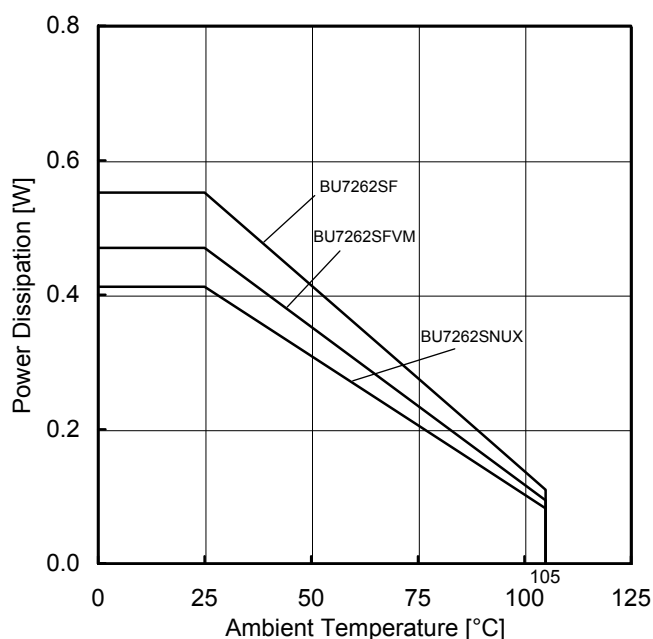


Figure 26.
Power Dissipation vs Ambient Temperature
(Derating Curve)

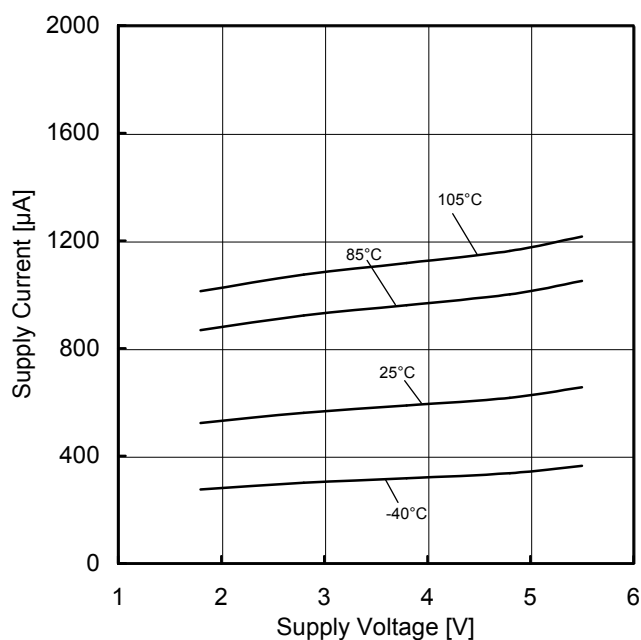


Figure 27.
Supply Current vs Supply Voltage

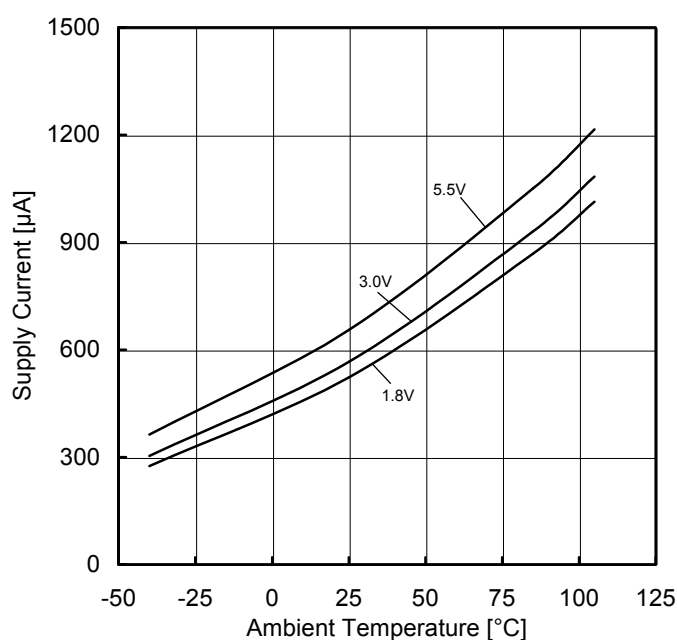


Figure 28.
Supply Current vs Ambient Temperature

(*)The above characteristics are measurements of typical sample, they are not guaranteed.

BU7262xxx: -40°C to +85°C BU7262Sxxx: -40°C to +105°C

Typical Performance Curves – Continued

OBU7262xxx, BU7262Sxxx

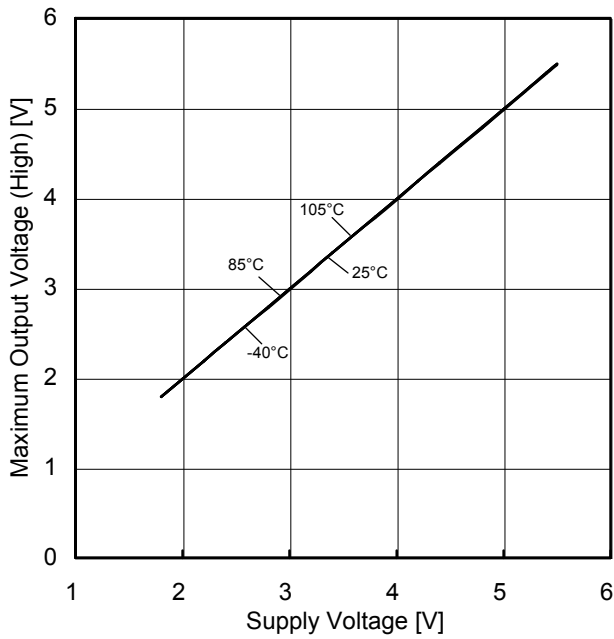


Figure 29.
Maximum Output Voltage (High) vs Supply Voltage
($R_L=10k\Omega$)

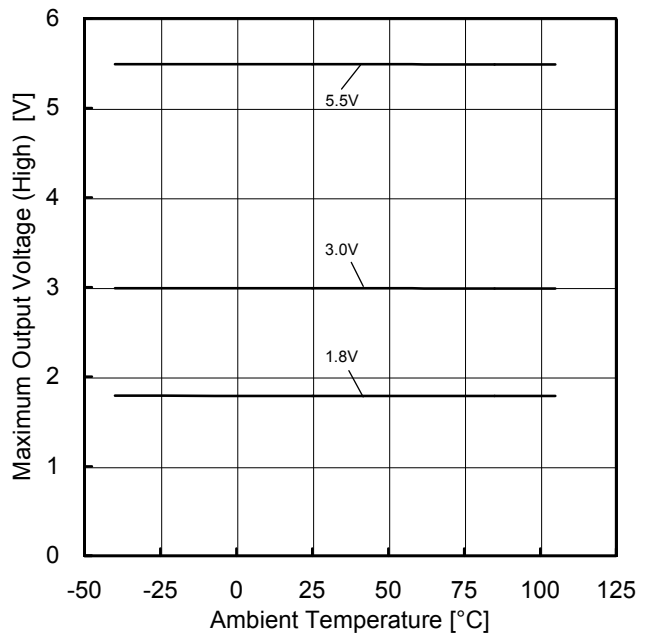


Figure 30.
Maximum Output Voltage (High) vs Ambient Temperature
($R_L=10k\Omega$)

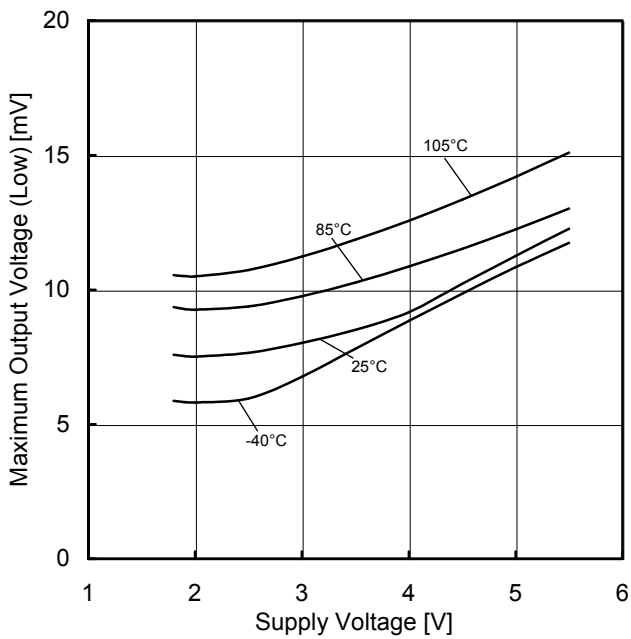


Figure 31.
Maximum Output Voltage (Low) vs Supply Voltage
($R_L=10k\Omega$)

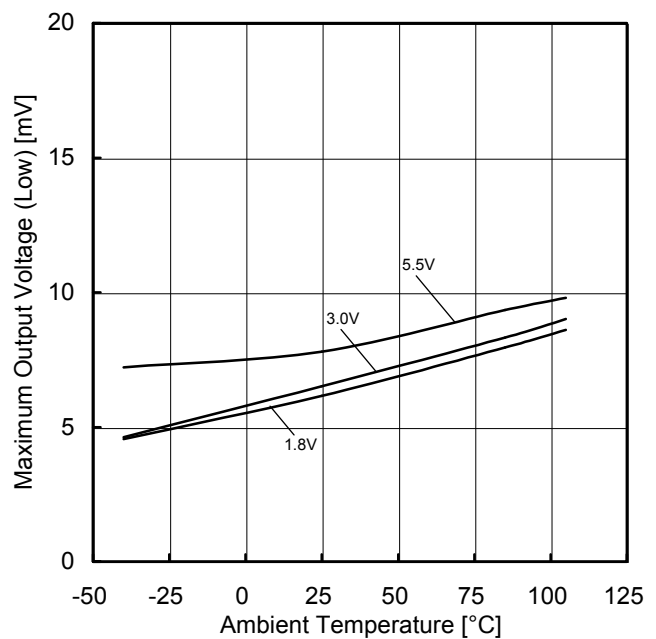


Figure 32.
Maximum Output Voltage (Low) vs Ambient Temperature
($R_L=10k\Omega$)

(*)The above characteristics are measurements of typical sample, they are not guaranteed.

BU7262xxx: -40°C to +85°C BU7262Sxxx: -40°C to +105°C

Typical Performance Curves – Continued

OBU7262xxx, BU7262Sxxx

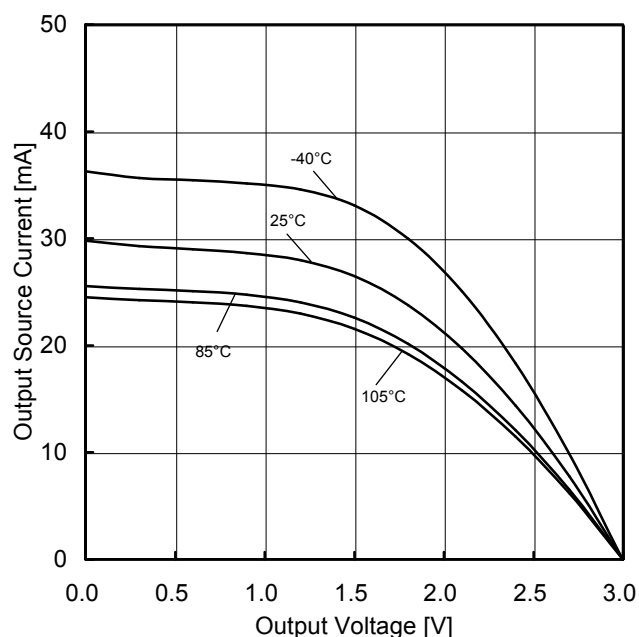


Figure 33.
Output Source Current vs Output Voltage
(VDD=3V)

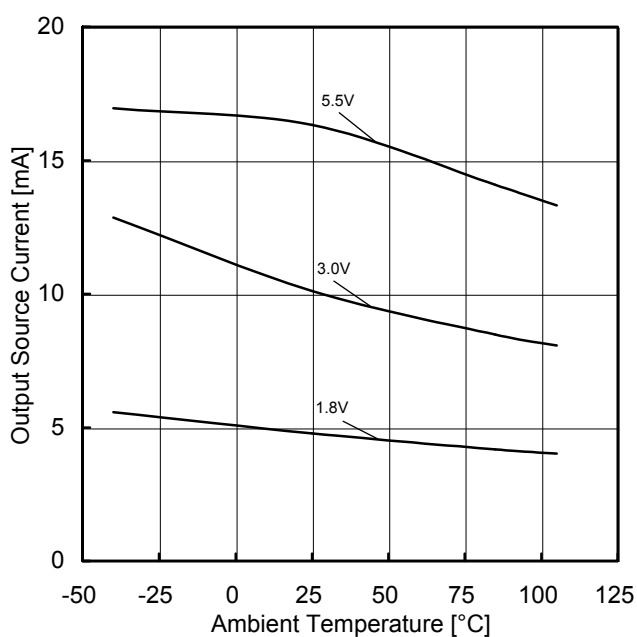


Figure 34.
Output Source Current vs Ambient Temperature
(OUT=VDD-0.4V)

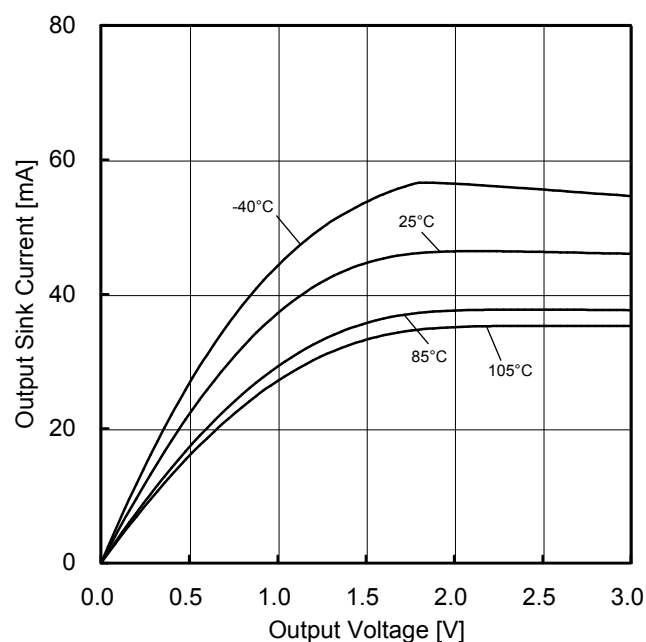


Figure 35.
Output Sink Current vs Output Voltage
(VDD=3V)

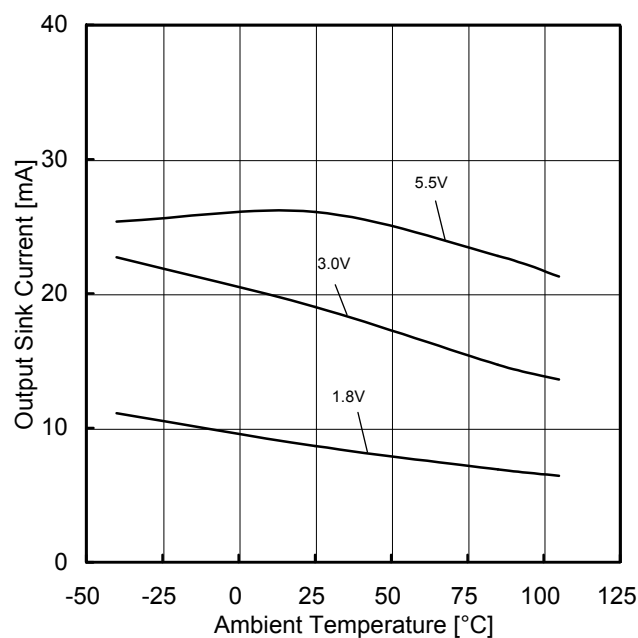


Figure 36.
Output Sink Current vs Ambient Temperature
(OUT=VSS+0.4V)

(*)The above characteristics are measurements of typical sample, they are not guaranteed.
BU7262xxx: -40°C to +85°C BU7262Sxxx: -40°C to +105°C

Typical Performance Curves – Continued

OBU7262xxx, BU7262Sxxx

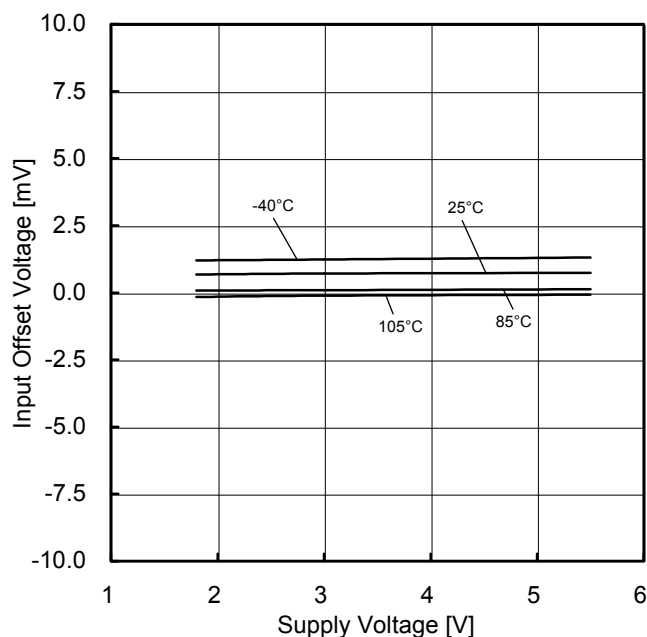


Figure 37.
Input Offset Voltage vs Supply Voltage
($V_{ICM}=V_{DD}$, $E_K=-V_{DD}/2$)

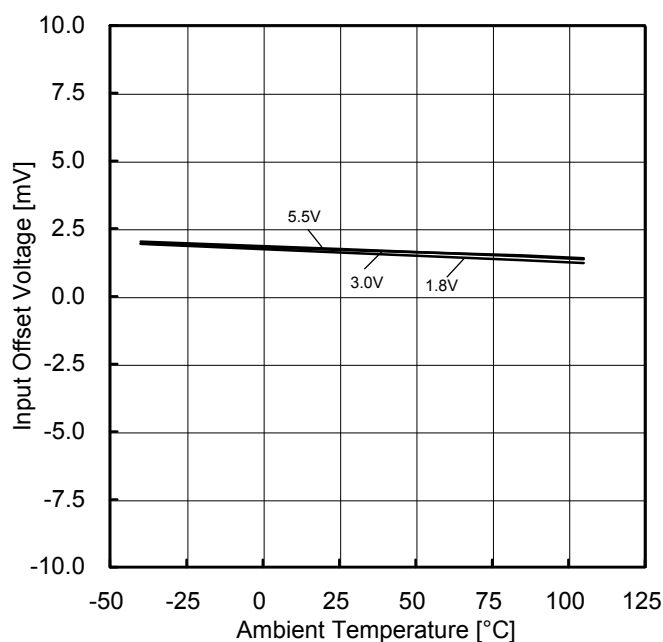


Figure 38.
Input Offset Voltage vs Ambient Temperature
($V_{ICM}=V_{DD}$, $E_K=-V_{DD}/2$)

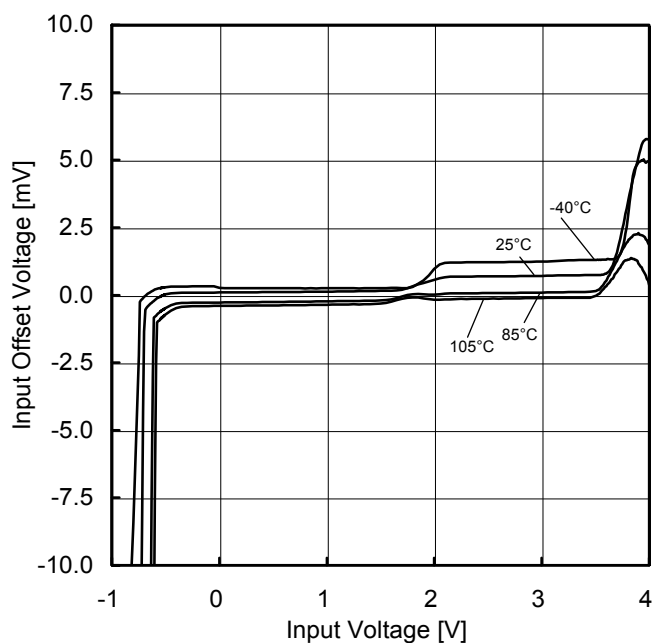


Figure 39.
Input Offset Voltage vs Input Voltage
($V_{DD}=3V$)

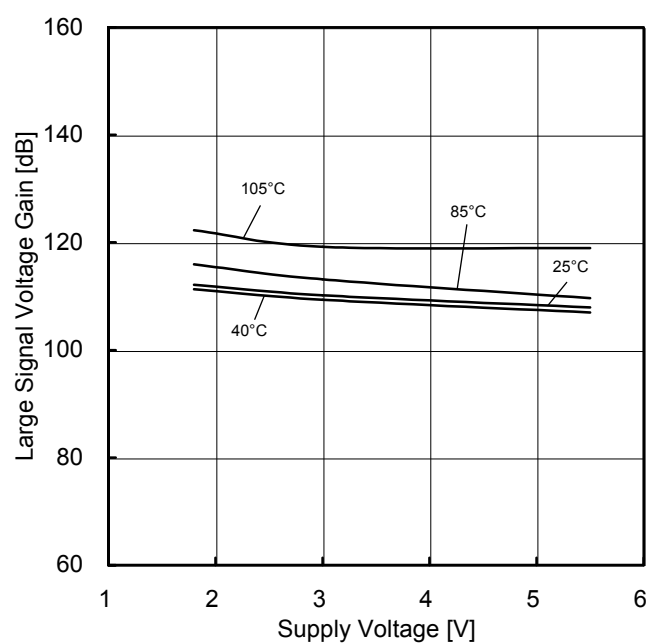


Figure 40.
Large Signal Voltage Gain vs Supply Voltage

(*)The above characteristics are measurements of typical sample, they are not guaranteed.

BU7262xxx: -40°C to +85°C BU7262Sxxx: -40°C to +105°C

Typical Performance Curves – Continued

OBU7262xxx, BU7262Sxxx

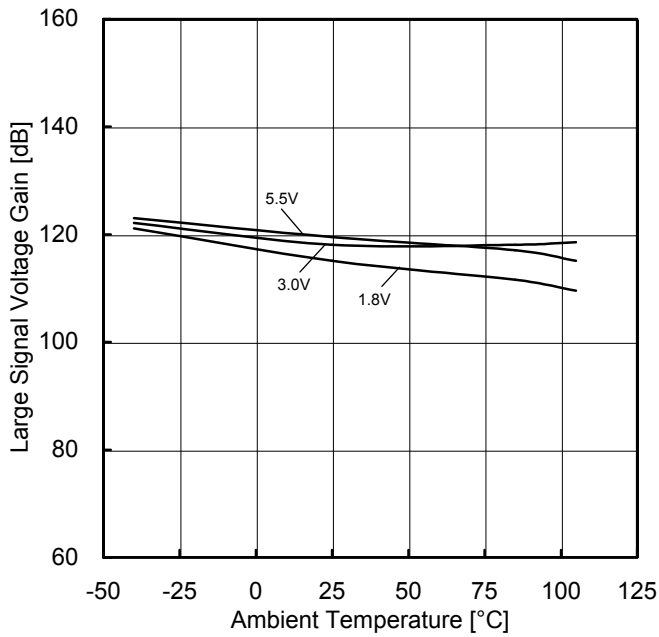


Figure 41.
Large Signal Voltage Gain vs Ambient Temperature

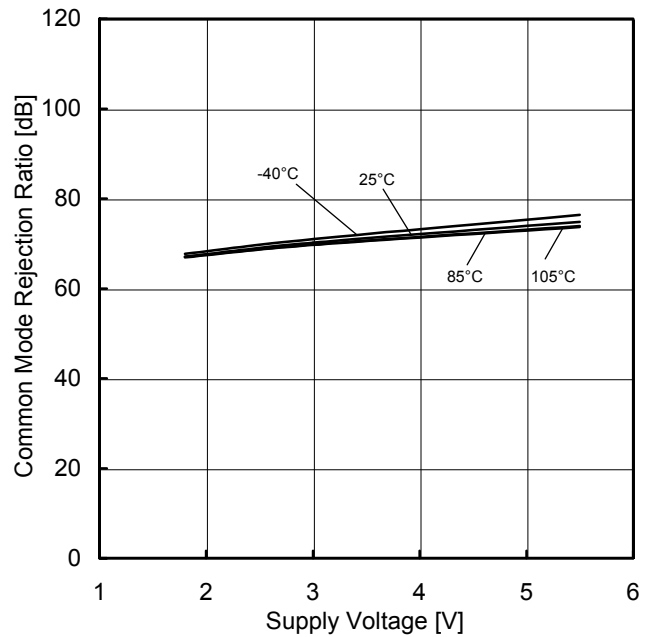


Figure 42.
Common Mode Rejection Ratio vs Supply Voltage
(VDD=3V)

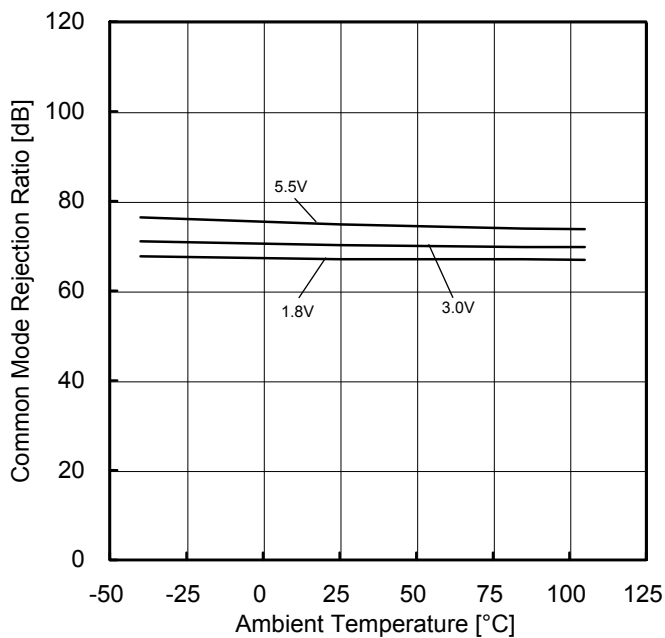


Figure 43.
Common Mode Rejection Ratio vs Ambient Temperature
(VDD=3V)

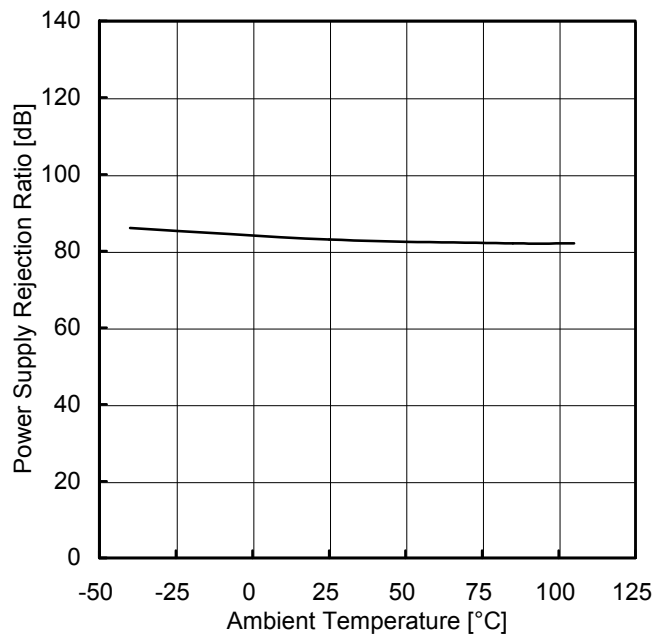


Figure 44.
Power Supply Rejection Ratio vs Ambient Temperature

(*)The above characteristics are measurements of typical sample, they are not guaranteed.
BU7262xxx: -40°C to +85°C BU7262Sxxx: -40°C to +105°C

Typical Performance Curves – Continued

OBU7262xxx, BU7262Sxxx

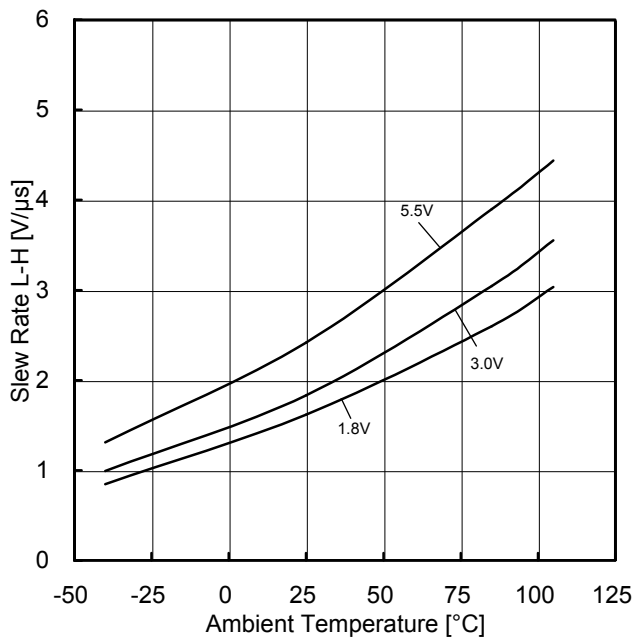


Figure 45.
Slew Rate L-H vs Ambient Temperature

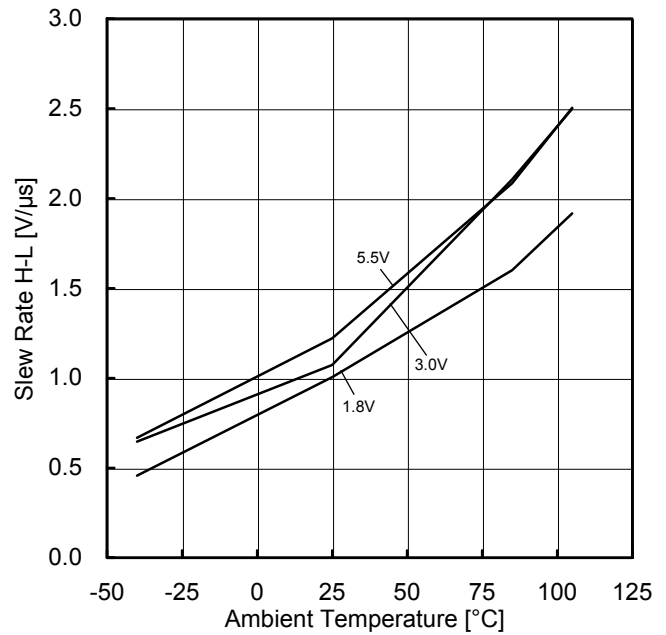


Figure 46.
Slew Rate H-L vs Ambient Temperature

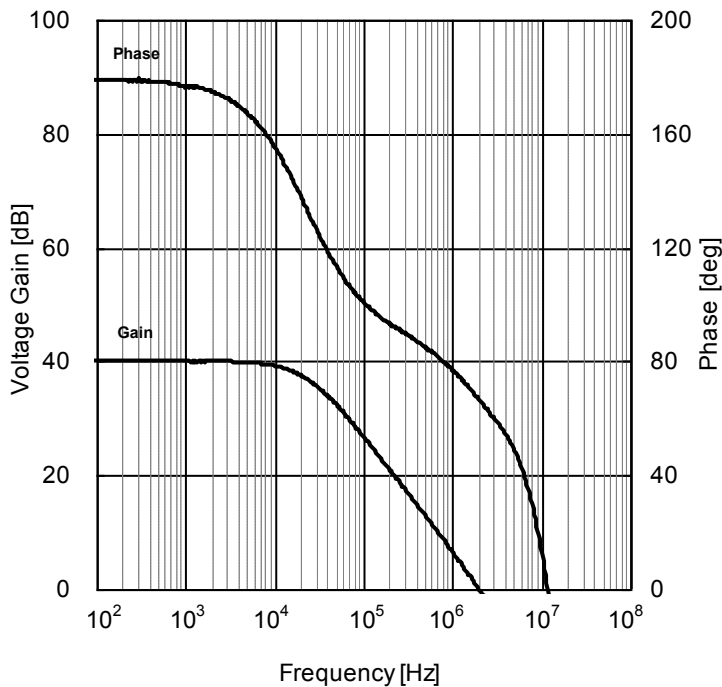


Figure 47.
Voltage Gain • Phase vs Frequency

(*)The above characteristics are measurements of typical sample, they are not guaranteed.
BU7262xxx: -40°C to +85°C BU7262Sxxx: -40°C to +105°C

Typical Performance Curves – Continued

OBU7264xx, BU7264Sxx

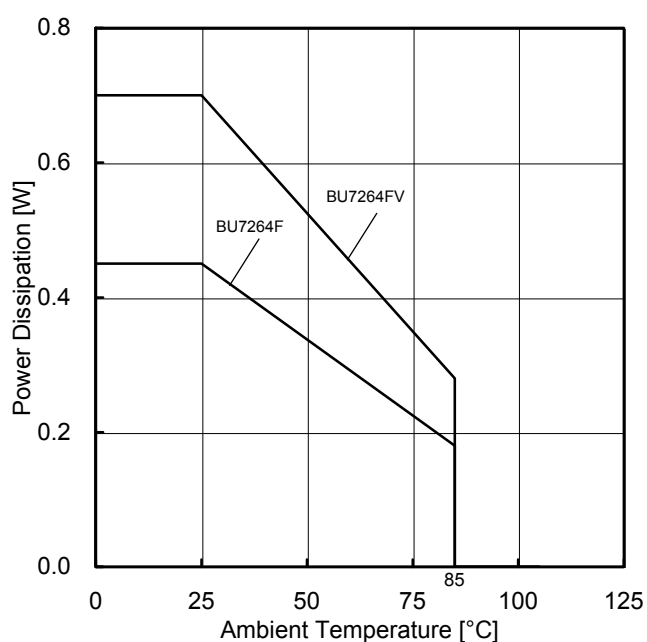


Figure 48.
Power Dissipation vs Ambient Temperature
(Derating Curve)

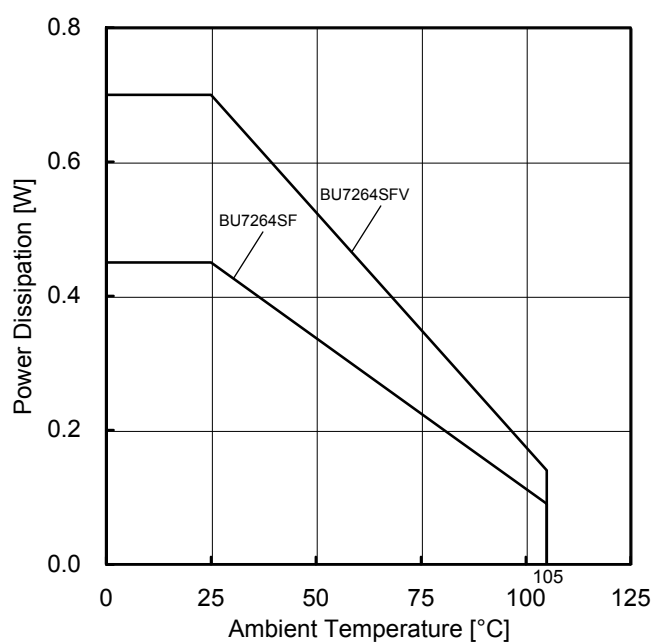


Figure 49.
Power Dissipation vs Ambient Temperature
(Derating Curve)

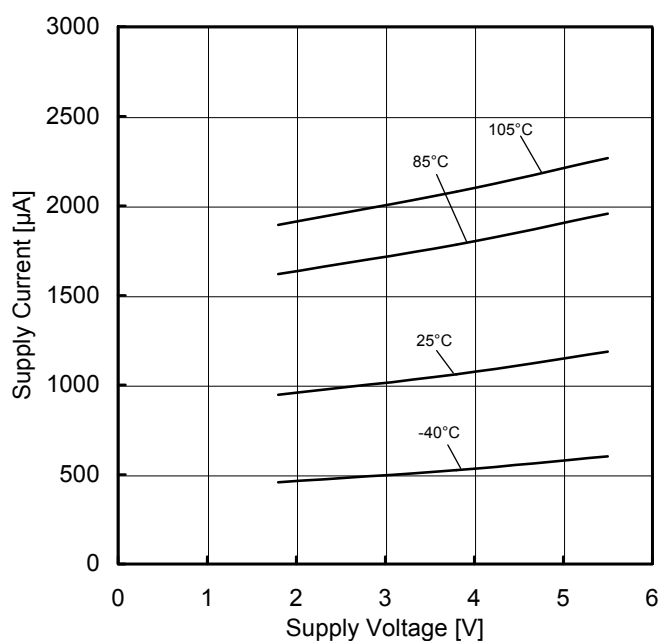


Figure 50.
Supply Current vs Supply Voltage

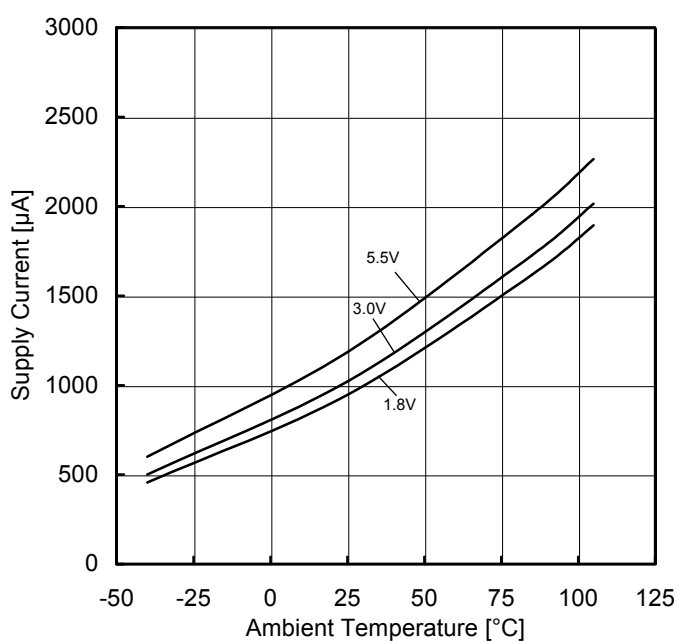


Figure 51.
Supply Current vs Ambient Temperature

(*)The above characteristics are measurements of typical sample, they are not guaranteed.

BU7264xx: -40°C to +85°C BU7264Sxx: -40°C to +105°C

Typical Performance Curves – Continued

OBU7264xx, BU7264Sxx

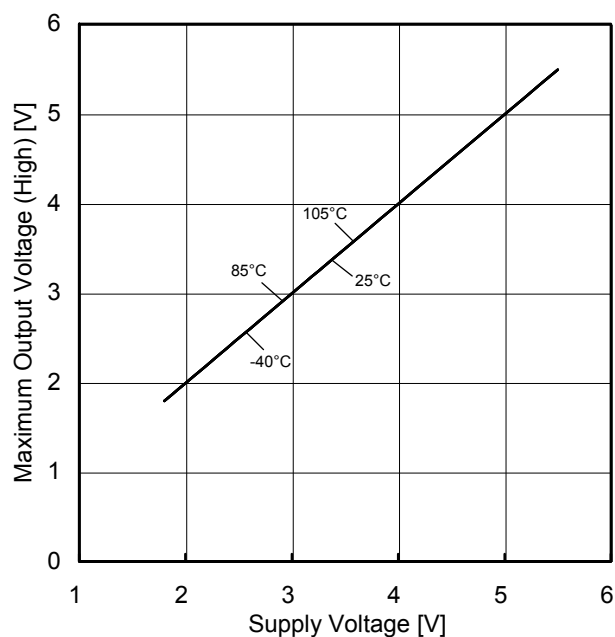


Figure 52.
Maximum Output Voltage (High) vs Supply Voltage
($R_L=10k\Omega$)

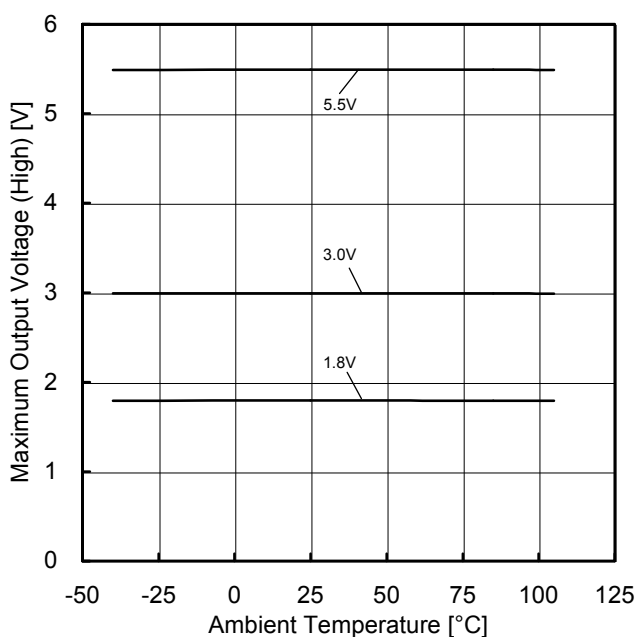


Figure 53.
Maximum Output Voltage (High) vs Ambient Temperature
($R_L=10k\Omega$)

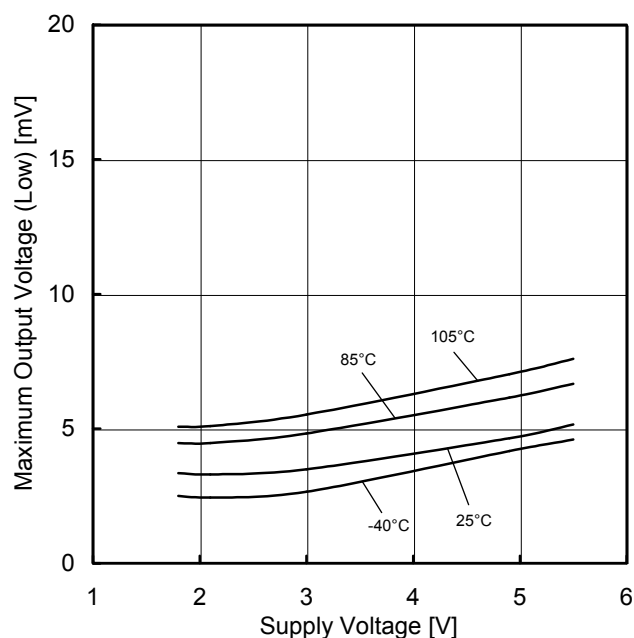


Figure 54.
Maximum Output Voltage (Low) vs Supply Voltage
($R_L=10k\Omega$)

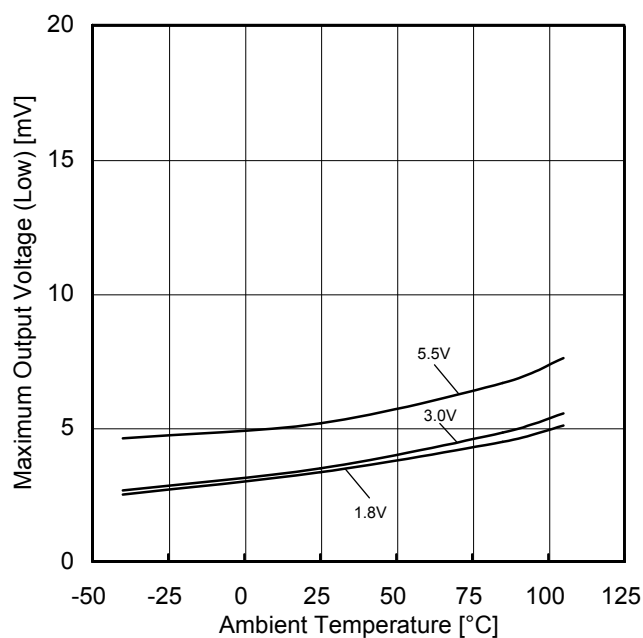


Figure 55.
Maximum Output Voltage (Low) vs Ambient Temperature
($R_L=10k\Omega$)

(*)The above characteristics are measurements of typical sample, they are not guaranteed.

BU7264xx: -40°C to +85°C BU7264Sxx: -40°C to +105°C

Typical Performance Curves – Continued

OBU7264xx, BU7264Sxx

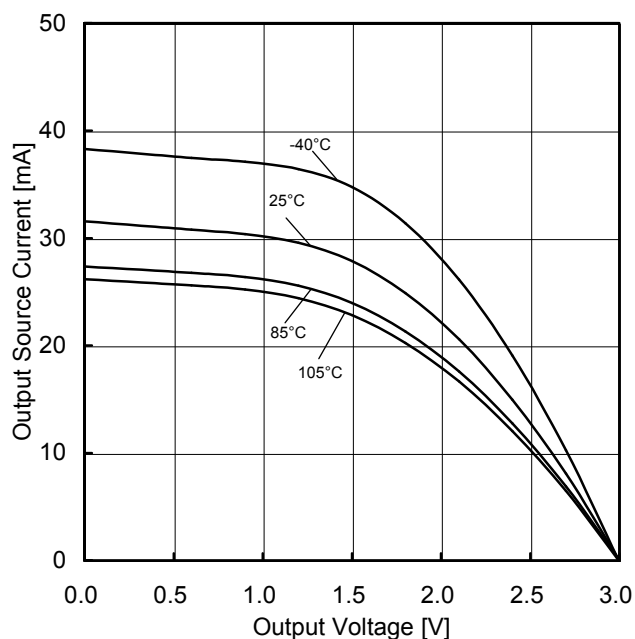


Figure 56.
Output Source Current vs Output Voltage
(VDD=3V)

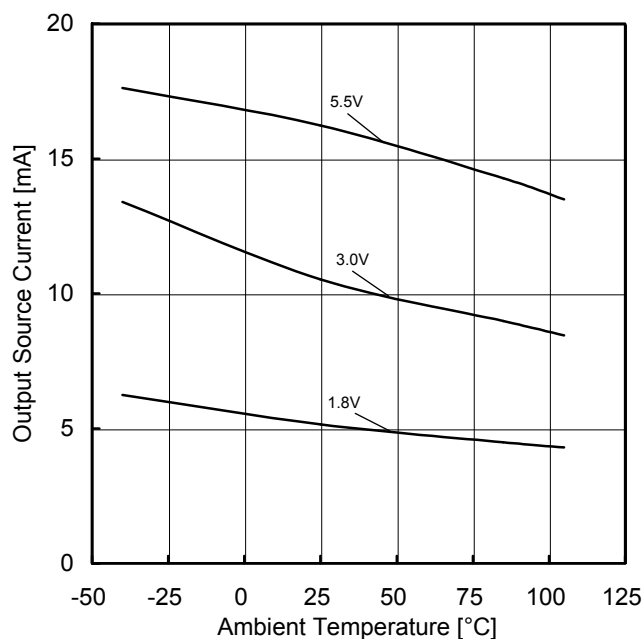


Figure 57.
Output Source Current vs Ambient Temperature
(OUT=VDD-0.4V)

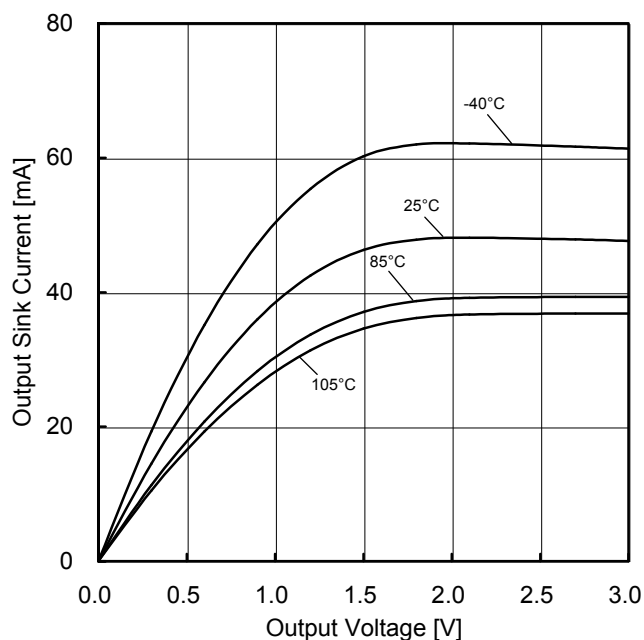


Figure 58.
Output Sink Current vs Output Voltage
(VDD=3V)

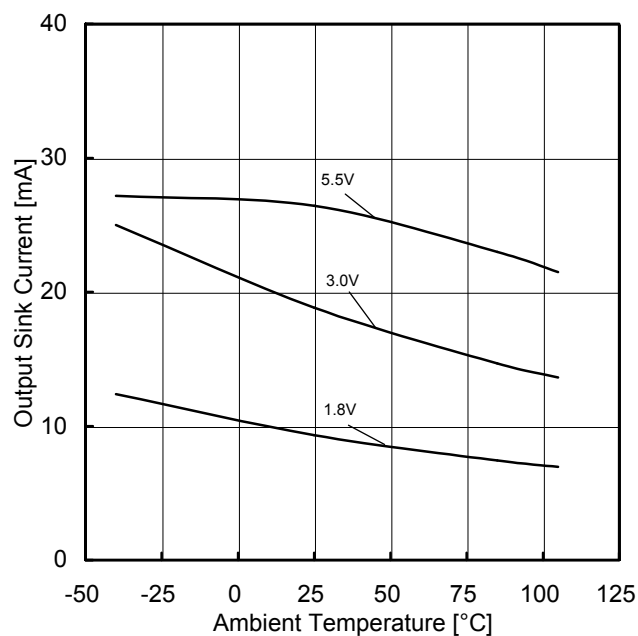


Figure 59.
Output Sink Current vs Ambient Temperature
(OUT=VSS+0.4V)

(*)The above characteristics are measurements of typical sample, they are not guaranteed.

BU7264xx: -40°C to +85°C BU7264Sxx: -40°C to +105°C

Typical Performance Curves – Continued

OBU7264xx, BU7264Sxx

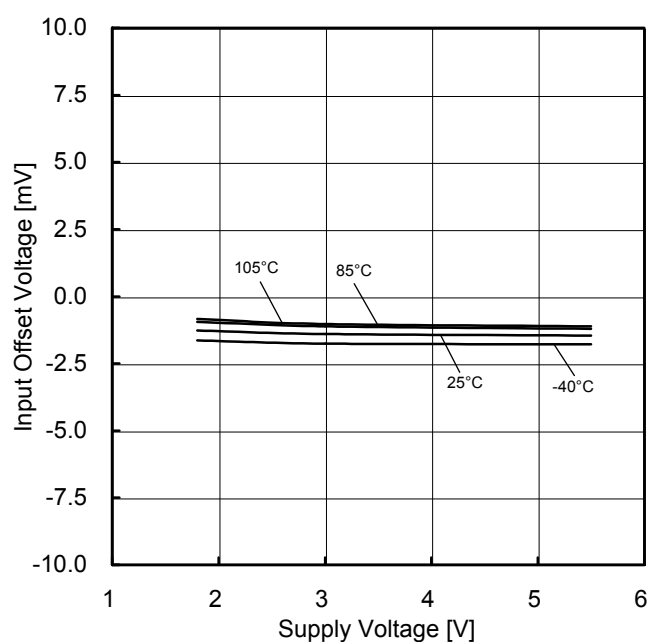


Figure 60.
Input Offset Voltage vs Supply Voltage
($V_{ICM}=V_{DD}$, $E_K=-V_{DD}/2$)

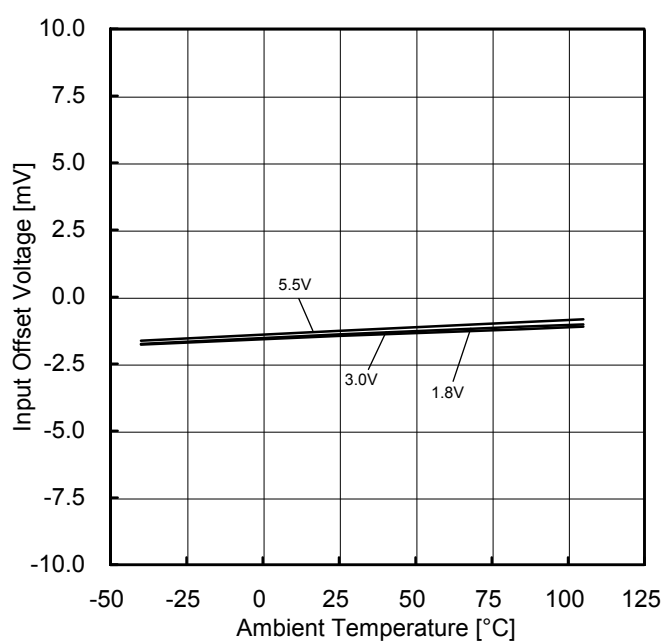


Figure 61.
Input Offset Voltage vs Ambient Temperature
($V_{ICM}=V_{DD}$, $E_K=-V_{DD}/2$)

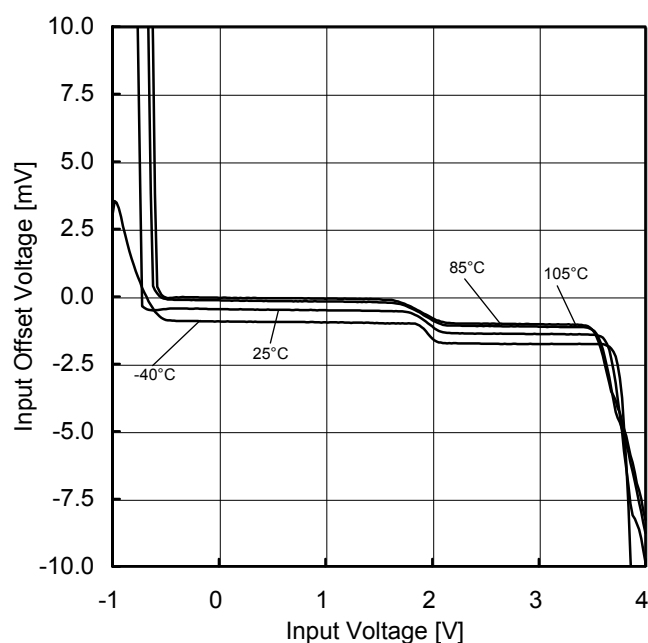


Figure 62.
Input Offset Voltage vs Input Voltage
($V_{DD}=3V$)

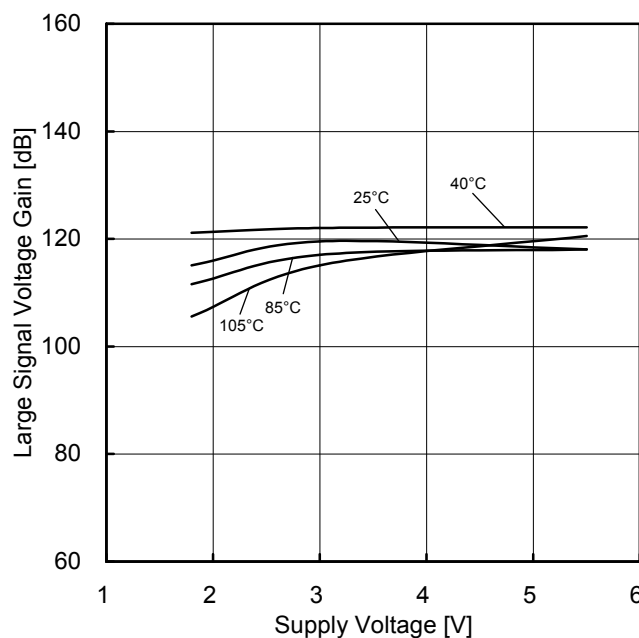


Figure 63.
Large Signal Voltage Gain vs Supply Voltage

(*)The above characteristics are measurements of typical sample, they are not guaranteed.

BU7264xx: -40°C to +85°C BU7264Sxx: -40°C to +105°C

Typical Performance Curves – Continued

OBU7264xx, BU7264Sxx

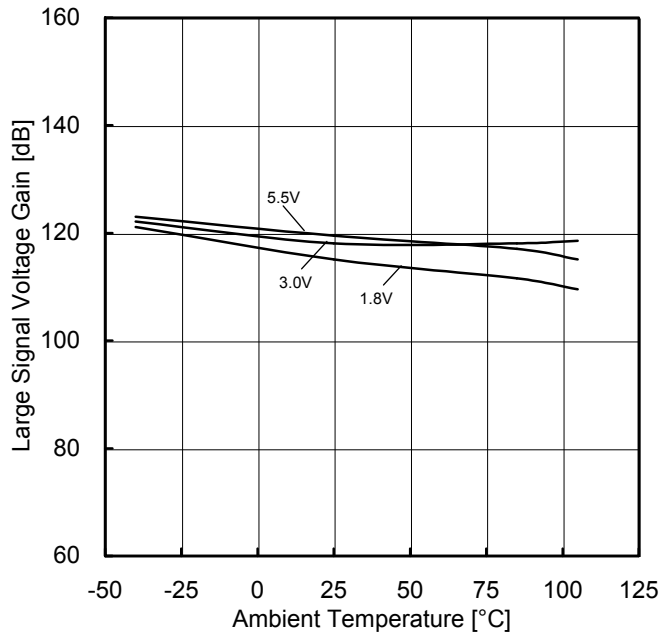


Figure 64.
Large Signal Voltage Gain vs Ambient Temperature

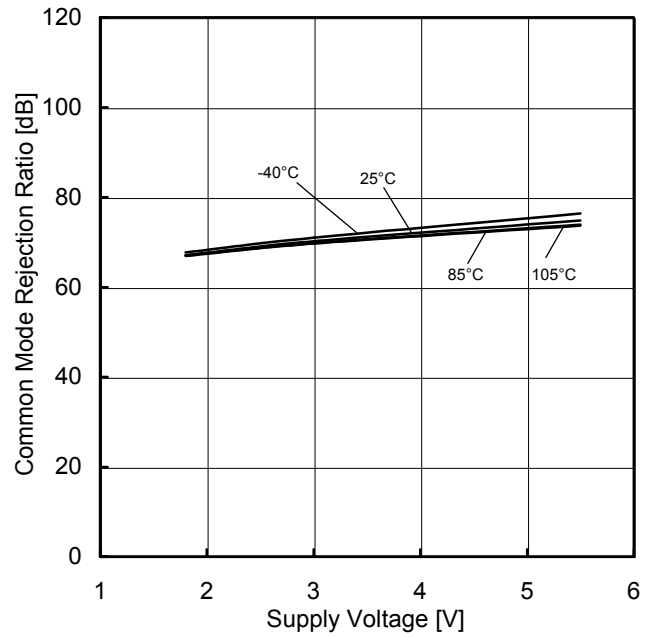


Figure 65.
Common Mode Rejection Ratio vs Supply Voltage
(VDD=3V)

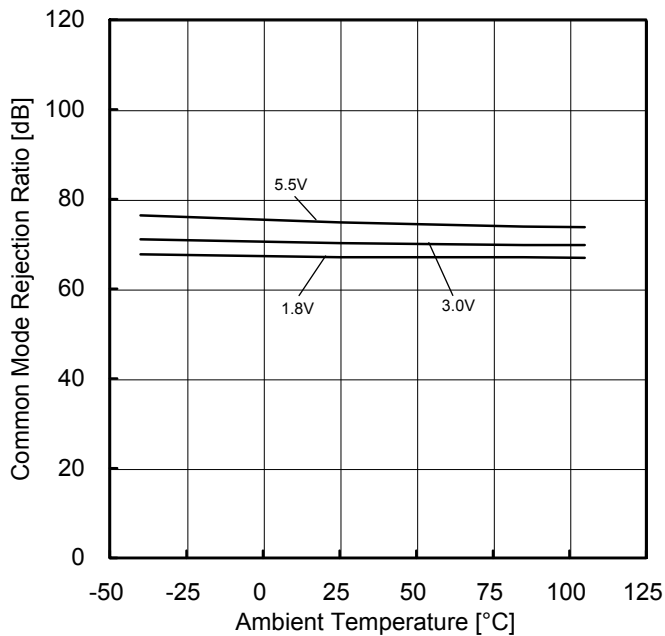


Figure 66.
Common Mode Rejection Ratio vs Ambient Temperature
(VDD=3V)

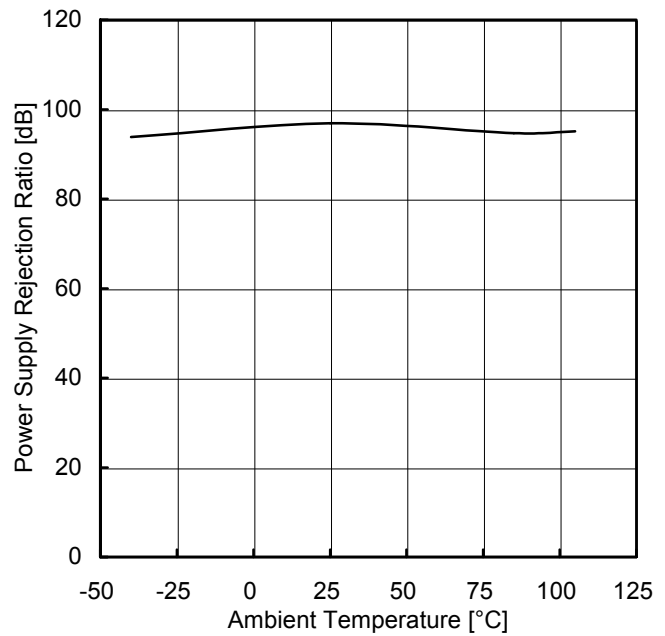


Figure 67.
Power Supply Rejection Ratio vs Ambient Temperature

(*)The above characteristics are measurements of typical sample, they are not guaranteed.
BU7264xx: -40°C to +85°C BU7264Sxx: -40°C to +105°C

Typical Performance Curves – Continued

OBU7264xx, BU7264Sxx

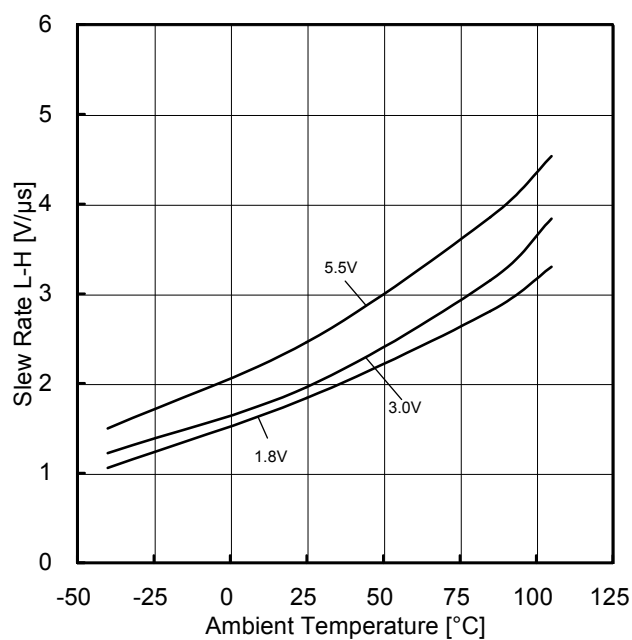


Figure 68.
Slew Rate L-H vs Ambient Temperature

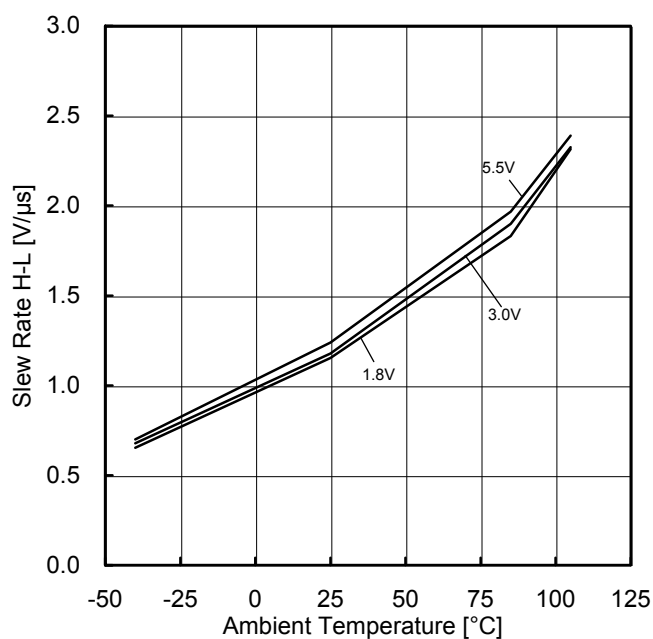


Figure 69.
Slew Rate H-L vs Ambient Temperature

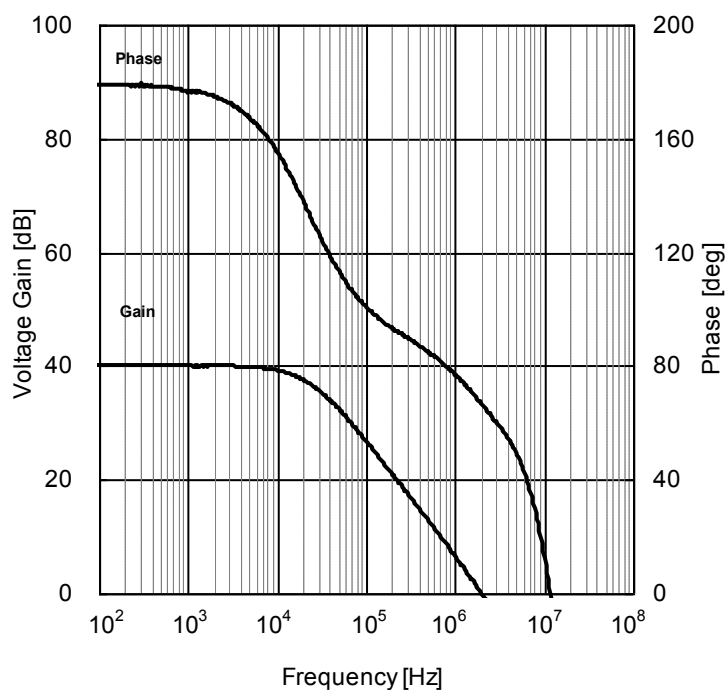


Figure 70.
Voltage Gain • Phase vs Frequency

(*)The above characteristics are measurements of typical sample, they are not guaranteed.

BU7264xx: -40°C to +85°C BU7264Sxx: -40°C to +105°C

Application Information
NULL method condition for Test Circuit 1

VDD, VSS, E _K , V _{ICM} Unit: V									
Parameter	V _F	S1	S2	S3	VDD	VSS	E _K	V _{ICM}	Calculation
Input Offset Voltage	V _{F1}	ON	ON	OFF	3	0	-1.5	3	1
Large Signal Voltage Gain	V _{F2}	ON	ON	ON	3	0	-0.5	1.5	2
	V _{F3}						-2.5		
Common-mode Rejection Ratio (Input Common-mode Voltage Range)	V _{F4}	ON	ON	OFF	3	0	-1.5	0	3
	V _{F5}							1PIN MARK	
Power Supply Rejection Ratio	V _{F6}	ON	ON	OFF	1.8	0	-0.9	0	4
	V _{F7}				5.5				

- Calculation -

1. Input Offset Voltage (V_{IO})

$$V_{IO} = \frac{|V_{F1}|}{1+R_F/R_S} \quad [V]$$

2. Large Signal Voltage Gain (A_v)

$$A_v = 20\text{Log} \frac{\Delta E_K \times (1+R_F/R_S)}{|V_{F2}-V_{F3}|} \quad [dB]$$

3. Common-mode Rejection Ratio (CMRR)

$$\text{CMRR} = 20\text{Log} \frac{\Delta V_{ICM} \times (1+R_F/R_S)}{|V_{F4} - V_{F5}|} \quad [dB]$$

4. Power Supply Rejection Ratio (PSRR)

$$\text{PSRR} = 20\text{Log} \frac{\Delta VDD \times (1+R_F/R_S)}{|V_{F6} - V_{F7}|} \quad [dB]$$

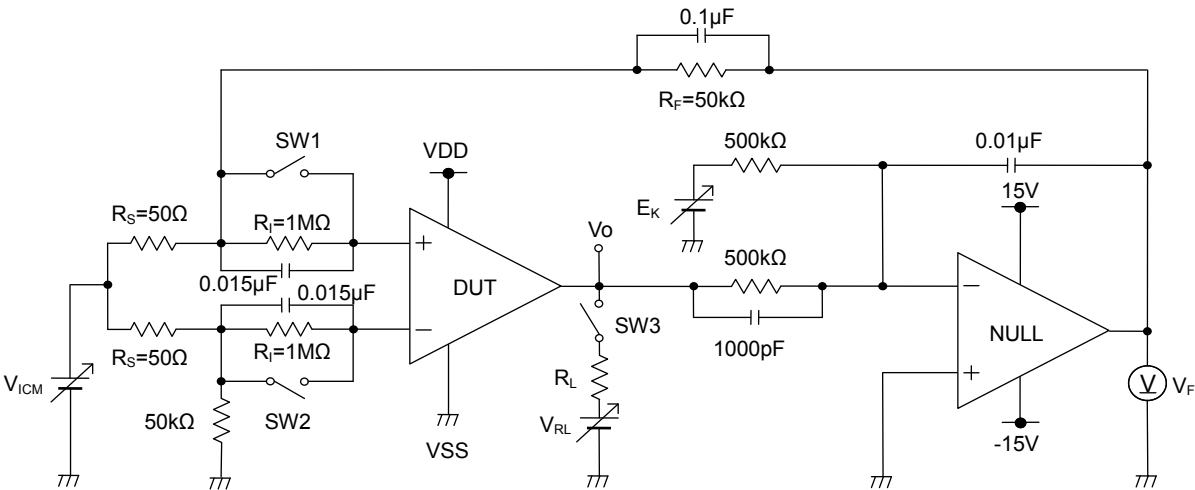


Figure 71. Test Circuit 1 (One Channel Only)

Application Information - continued
Switch Condition for Test Circuit 2

SW No.	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	SW9	SW10	SW11	SW12
Supply Current	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
Maximum Output Voltage $R_L=10k\Omega$	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF
Output Current	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF
Slew Rate	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	ON
Gain Bandwidth	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	OFF	ON

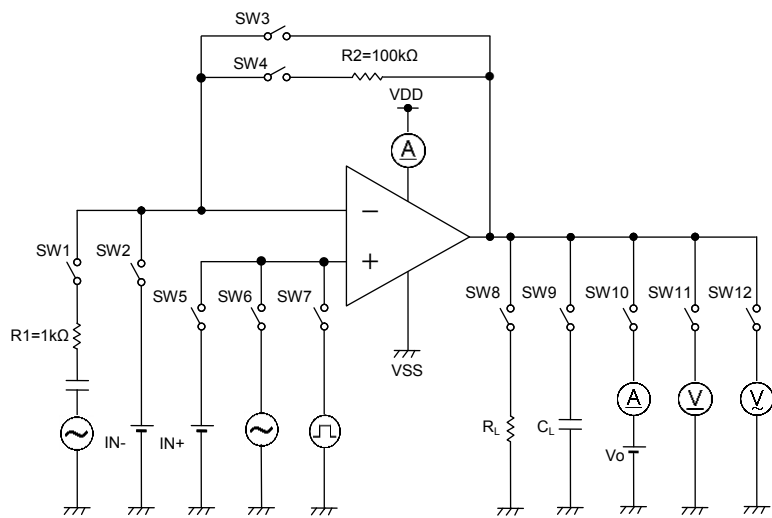


Figure 72. Test Circuit 2 (each channel)

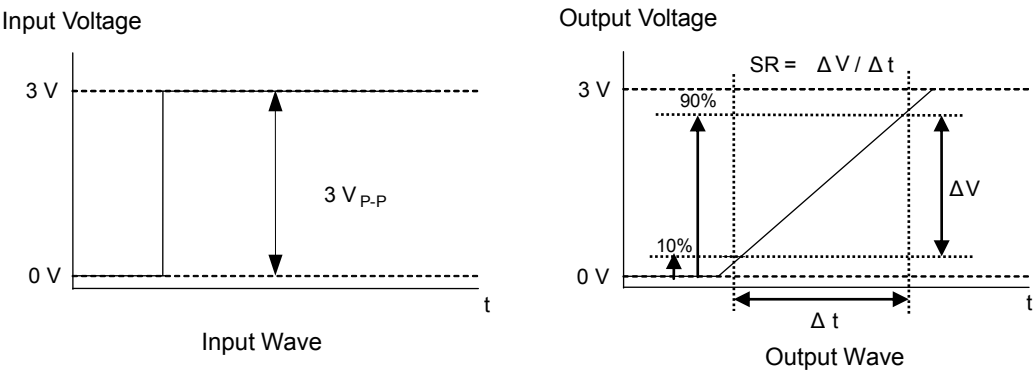


Figure 73. Slew Rate Input and Output Wave

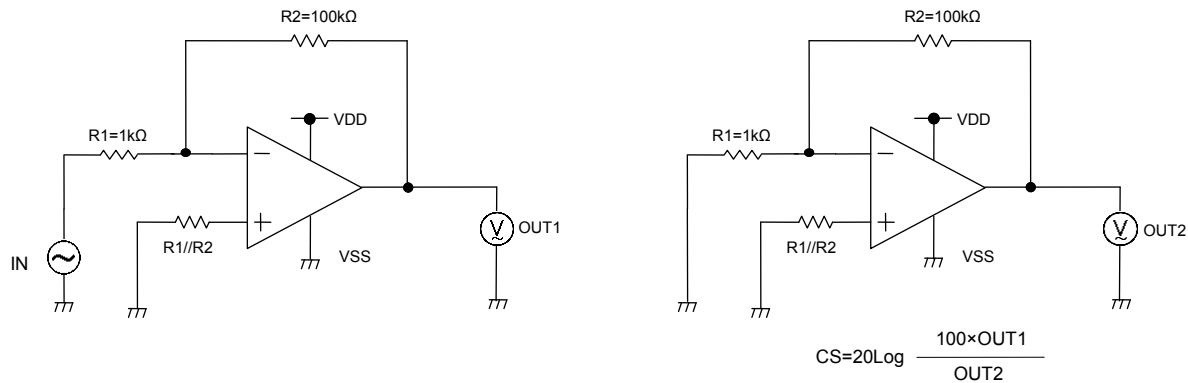
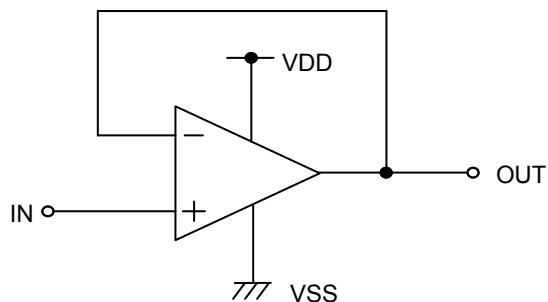


Figure 74. Test Circuit 3 (Channel Separation)

Examples of Circuit

○Voltage Follower



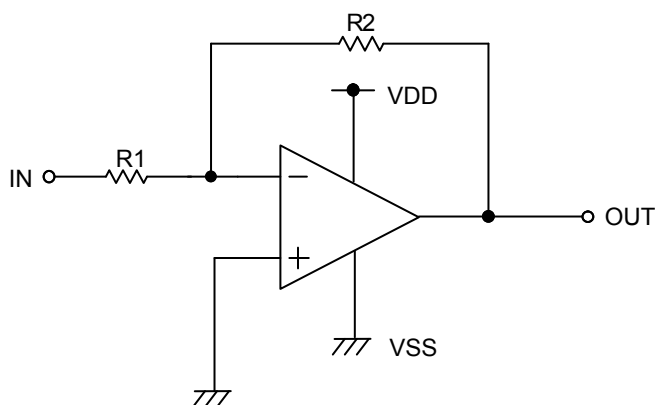
Voltage gain is 0dB.

Using this circuit, the output voltage (OUT) is configured to be equal to the input voltage (IN). This circuit also stabilizes the output voltage (OUT) due to high input impedance and low output impedance. Computation for output voltage (OUT) is shown below.

$$OUT=IN$$

Figure 75. Voltage Follower Circuit

○Inverting Amplifier



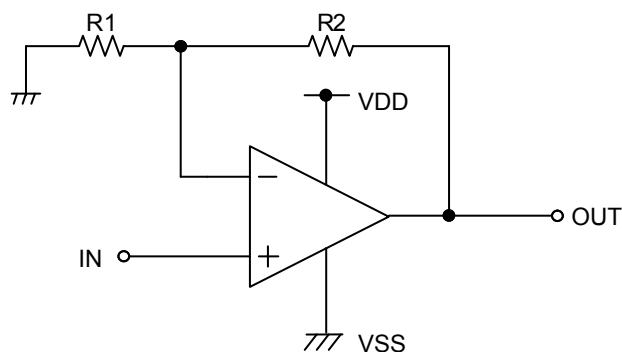
For inverting amplifier, input voltage (IN) is amplified by a voltage gain and depends on the ratio of R1 and R2. The out-of-phase output voltage is shown in the next expression

$$OUT=-(R2/R1) \cdot IN$$

This circuit has input impedance equal to R1.

Figure 76. Inverting Amplifier Circuit

○Non-inverting Amplifier



For non-inverting amplifier, input voltage (IN) is amplified by a voltage gain, which depends on the ratio of R1 and R2. The output voltage (OUT) is in-phase with the input voltage (IN) and is shown in the next expression.

$$OUT=(1 + R2/R1) \cdot IN$$

Effectively, this circuit has high input impedance since its input side is the same as that of the operational amplifier.

Figure 77. Non-inverting Amplifier Circuit

Power Dissipation

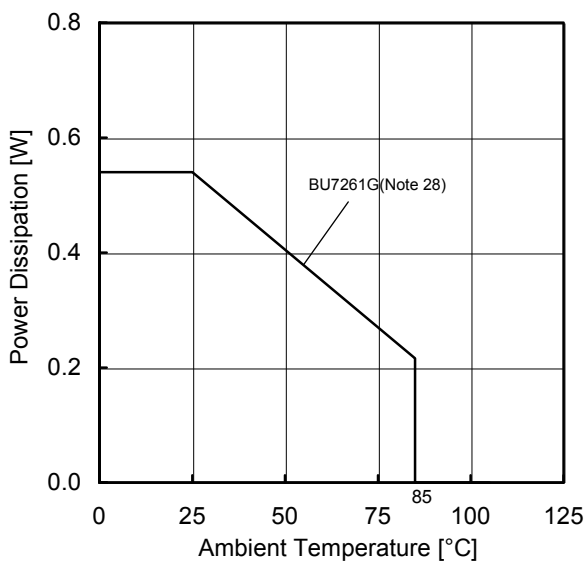
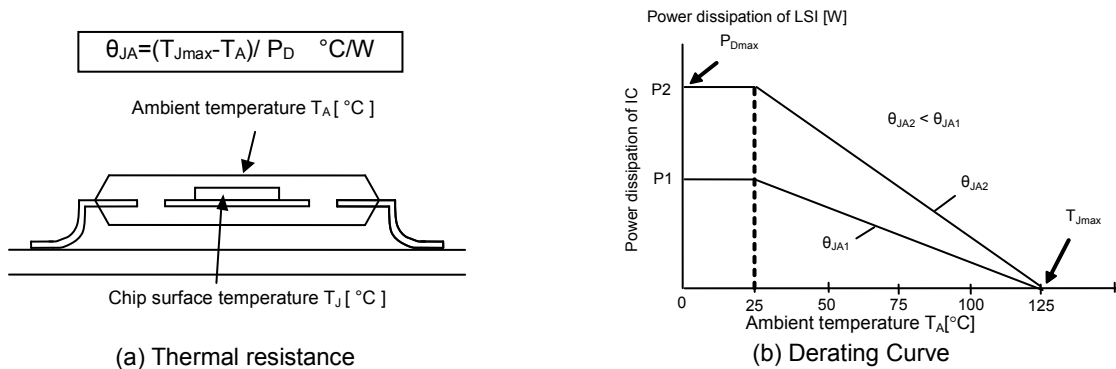
Power dissipation (total loss) indicates the power that the IC can consume at $T_A=25^{\circ}\text{C}$ (normal temperature). As the IC consumes power, it heats up, causing its temperature to be higher than the ambient temperature. The allowable temperature that the IC can accept is limited. This depends on the circuit configuration, manufacturing process, and consumable power.

Power dissipation is determined by the allowable temperature within the IC (maximum junction temperature) and the thermal resistance of the package used (heat dissipation capability). Maximum junction temperature is typically equal to the maximum storage temperature. The heat generated through the consumption of power by the IC radiates from the mold resin or lead frame of the package. Thermal resistance, represented by the symbol $\theta_{JA}^{\circ}\text{C/W}$, indicates this heat dissipation capability. Similarly, the temperature of an IC inside its package can be estimated by thermal resistance.

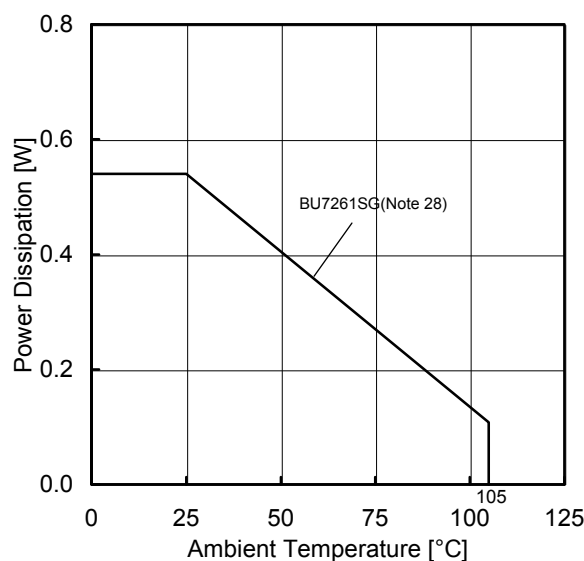
Figure 78(a) shows the model of the thermal resistance of a package. The equation below shows how to compute for the Thermal resistance (θ_{JA}), given the ambient temperature (T_A), maximum junction temperature (T_{Jmax}), and power dissipation (P_D).

$$\theta_{JA} = (T_{Jmax} - T_A) / P_D \quad ^{\circ}\text{C/W}$$

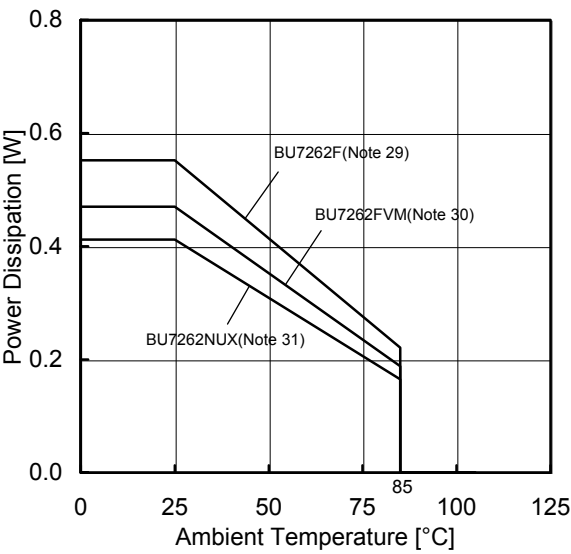
The Derating curve in Figure 78 (b) indicates the power that the IC can consume with reference to ambient temperature. Power consumption of the IC begins to attenuate at certain temperatures. This gradient is determined by Thermal resistance (θ_{JA}), which depends on the chip size, power consumption, package, ambient temperature, package condition, wind velocity, etc. This may also vary even when the same of package is used. Thermal reduction curve indicates a reference value measured at a specified condition. Figure 78(c) to 78(h) shows an example of the derating curve for BU7261G, BU7261SG, BU7262xxx, BU7262Sxxx, BU7264xx, BU7264Sxx.



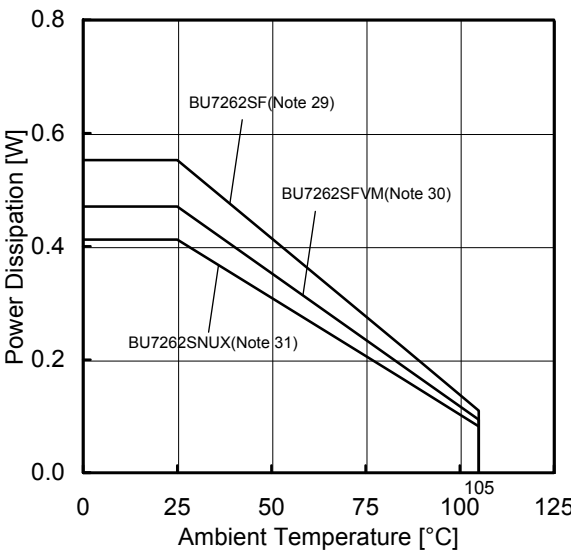
(c)BU7261G



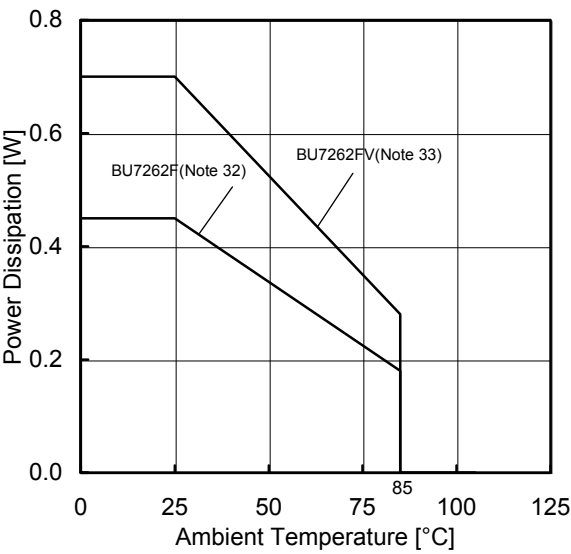
(d)BU7261SG



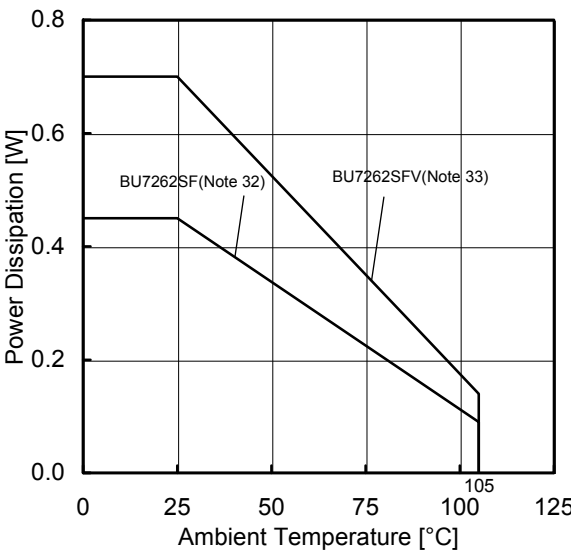
(e)BU7262F/FVM/NUX



(f)BU7262SF/SFVM/SNUX



(g)BU7264F/FV



(h)BU7264SF/SFV

(Note 28)	(Note 29)	(Note 30)	(Note 31)	(Note 32)	(Note 33)	Unit
5.4	5.5	4.7	4.1	4.5	7.0	mW/°C

When using the unit above T_A=25°C, subtract the value above per Celsius degree. Power dissipation is the value when FR4 glass epoxy board 70mm×70mm×1.6mm (copper foil area less than 3%) is mounted.

Figure 78. Thermal Resistance and Derating Curve

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the P_D stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the P_D rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

12. Regarding the Input Pin of the IC

In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

13. Unused Circuits

When there are unused op-amps, it is recommended that they are connected as in Figure 79, setting the non-inverting input terminal to a potential within the input common mode voltage range (V_{ICM}).

14. Input Voltage

Applying $V_{DD}+0.3V$ to the input terminal is possible without causing deterioration of the electrical characteristics or destruction. However, this does not ensure normal circuit operation. Please note that the circuit operates normally only when the input voltage is within the common mode input voltage range of the electric characteristics.

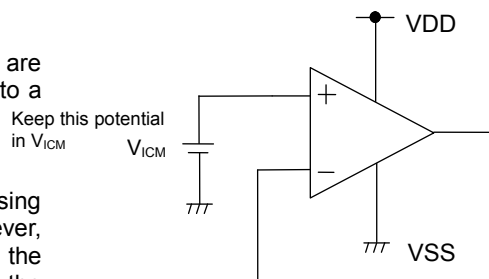


Figure 79. Example of Application Circuit for Unused Op-amp

15. Power Supply(single/dual)

The operational amplifier operates when the voltage supplied is between V_{DD} and V_{SS} . Therefore, the single supply operational amplifiers can be used as dual supply operational amplifiers as well.

16. Output Capacitor

If a large capacitor is connected between the output pin and V_{SS} pin, current from the charged capacitor will flow into the output pin and may destroy the IC when the V_{DD} pin is shorted to ground or pulled down to 0V. Use a capacitor smaller than 0.1 μF between output pin and V_{SS} pin.

17. Oscillation by Output Capacitor

Please pay attention to the oscillation by output capacitor and in designing an application of negative feedback loop circuit with these ICs.

18. Latch up

Be careful of input voltage that exceed the V_{DD} and V_{SS} . When CMOS device have sometimes occur latch up and protect the IC from abnormaly noise.

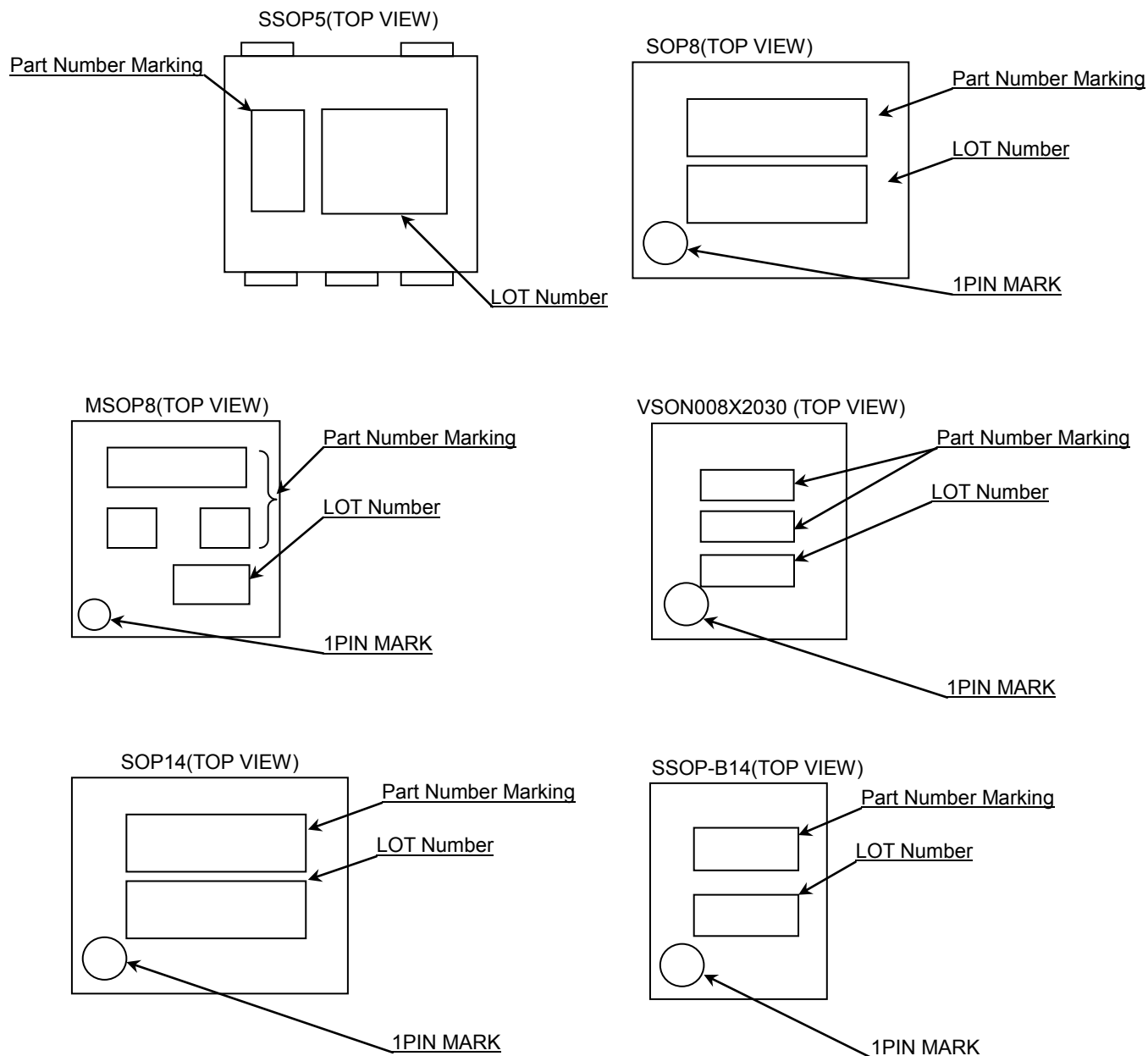
19. Decoupling Capacitor

Insert the decoupling capacitance between V_{DD} and V_{SS} , for stable operation of operational amplifier.

20. Radiation Land

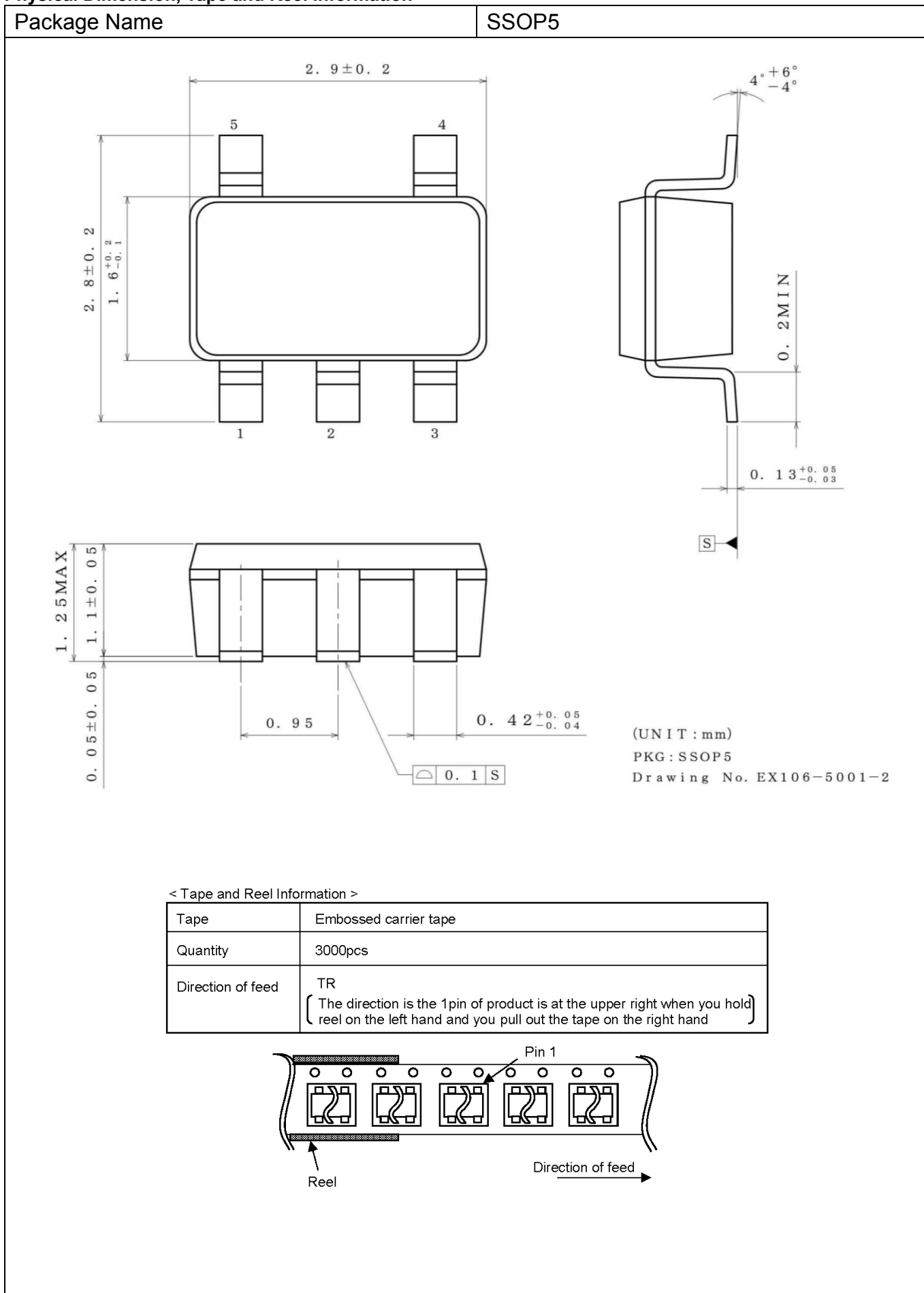
The VSON008X2030 package has a radiation land in the center of the back. Please connect to V_{SS} potential or don't connect to other terminal.

Marking Diagrams

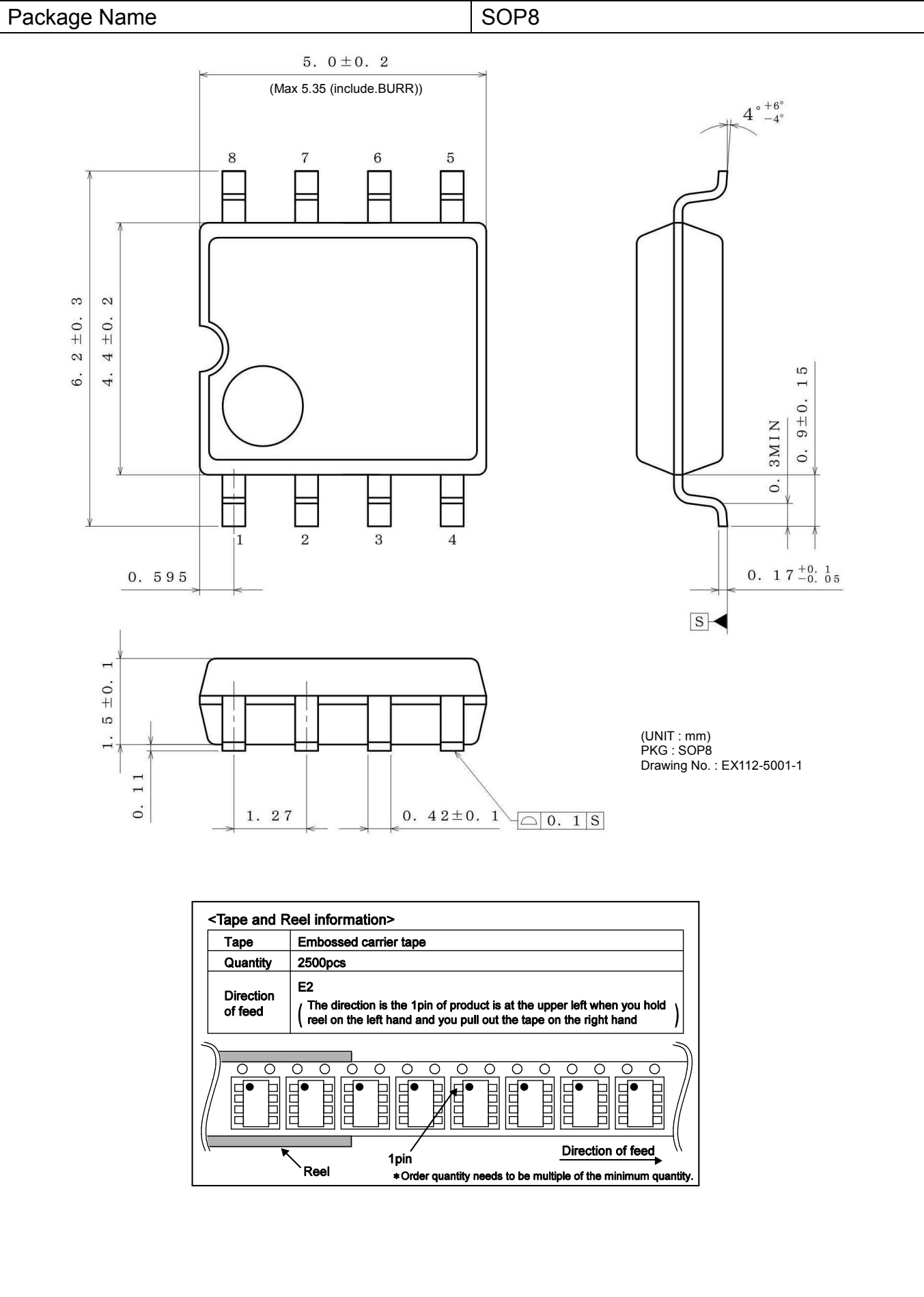


Product Name		Package Type	Marking
BU7261	G	SSOP5	AL
BU7261S	G		AX
BU7262	F	SOP8	7262
	FVM	MSOP8	
	NUX	VSON008X2030	
BU7262S	F	SOP8	7262S
	FVM	MSOP8	
	NUX	VSON008X2030	
BU7264	F	SOP14	BU7264F
	FV	SSOP-B14	7264
BU7264S	F	SOP14	BU7264SF
	FV	SSOP-B14	7264S

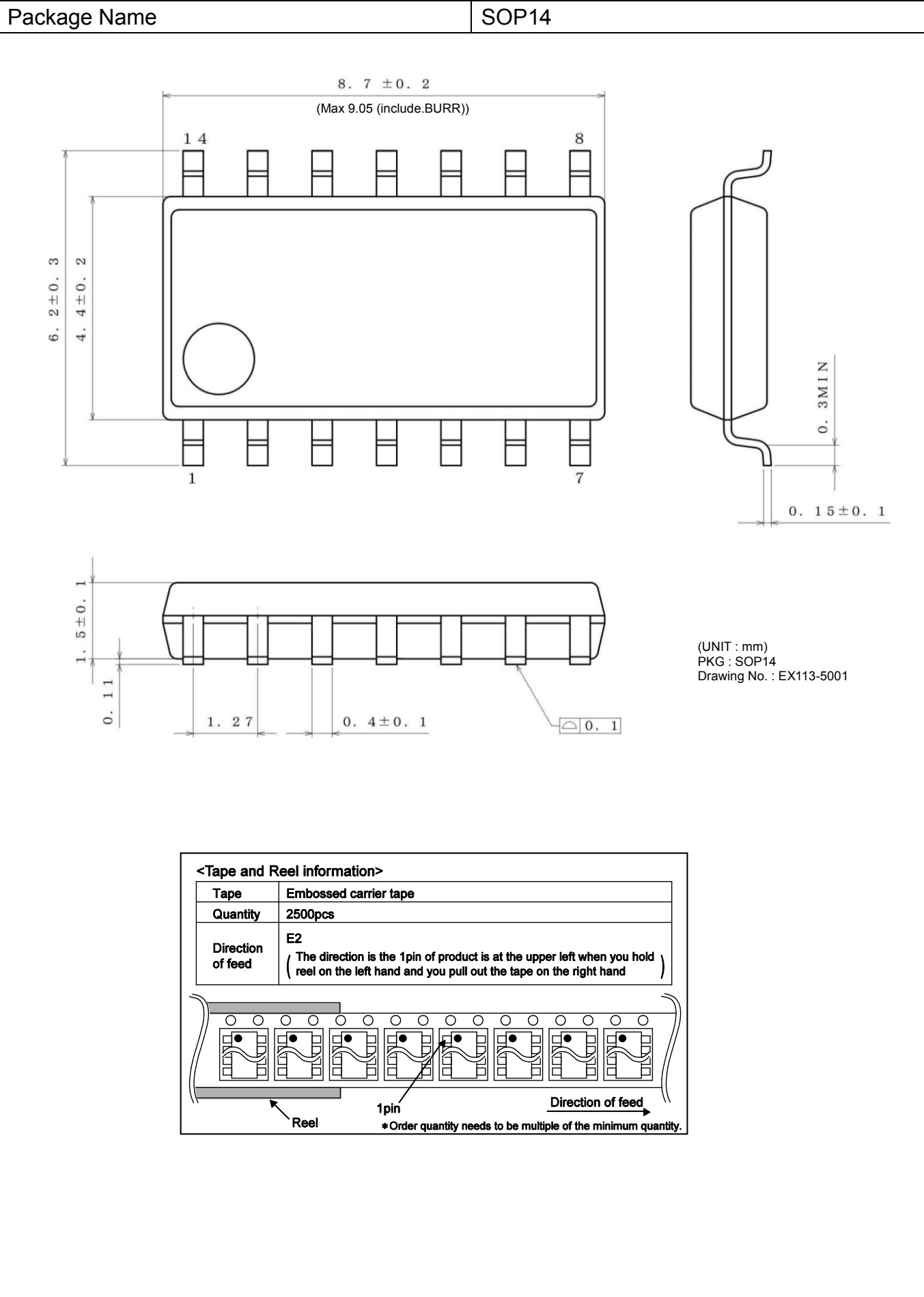
Physical Dimension, Tape and Reel Information



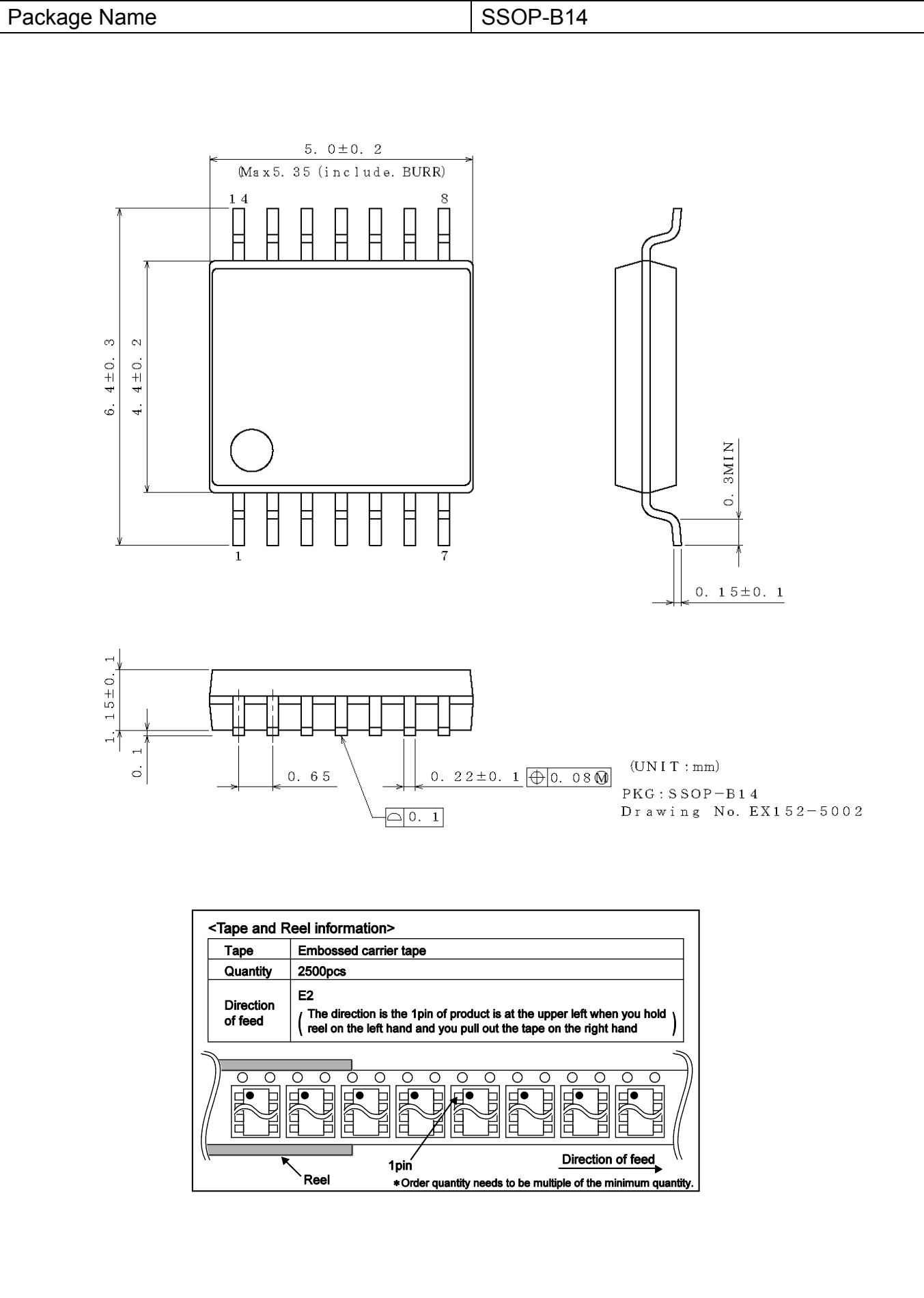
Physical Dimension, Tape and Reel Information - continued



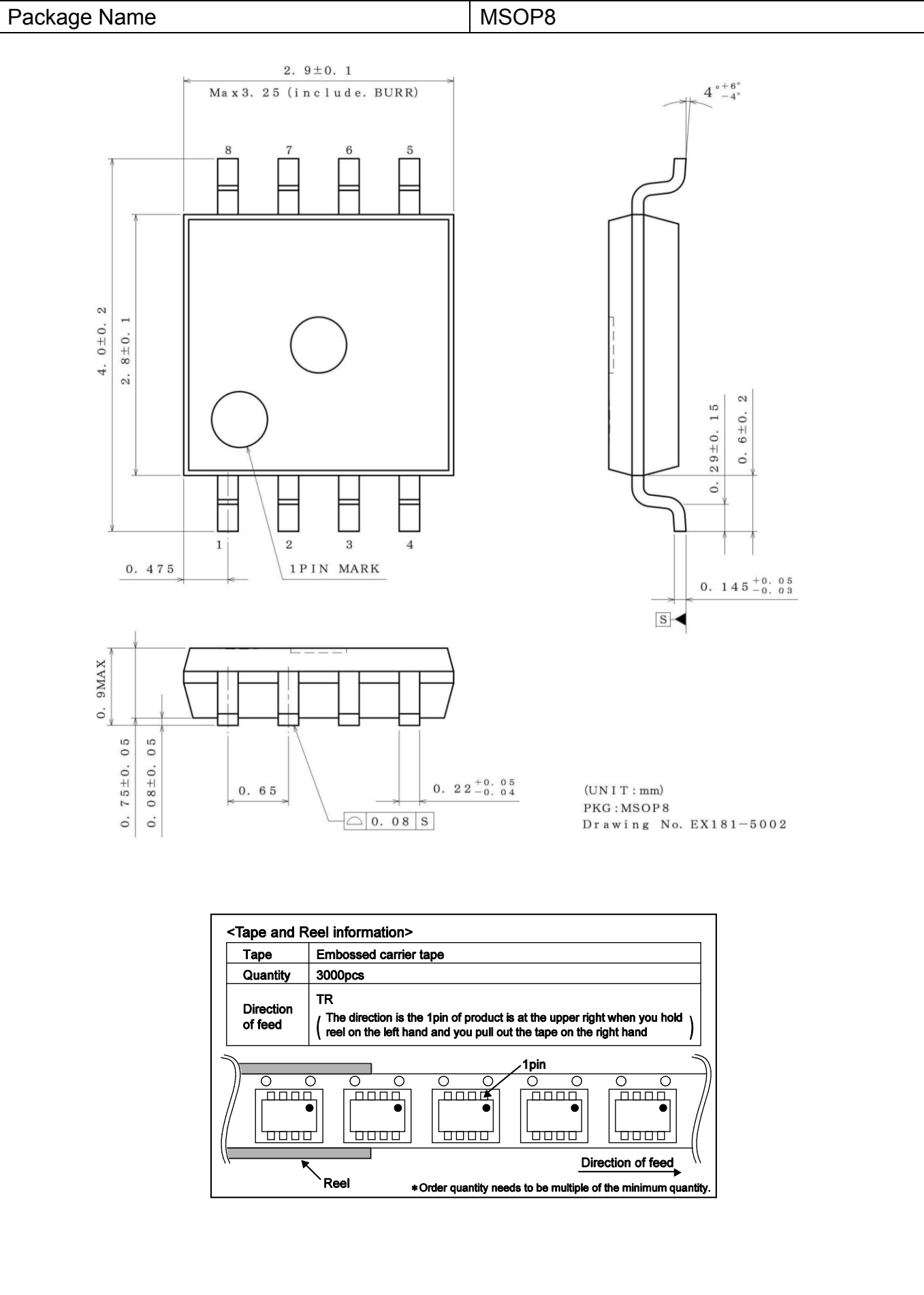
Physical Dimension, Tape and Reel Information – continued



Physical Dimension, Tape and Reel Information – continued

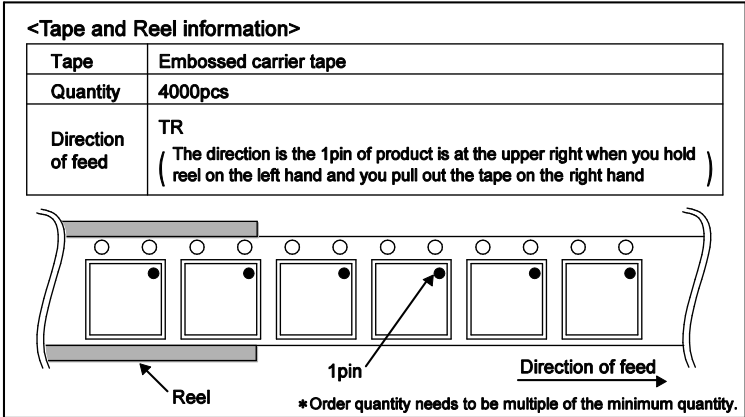
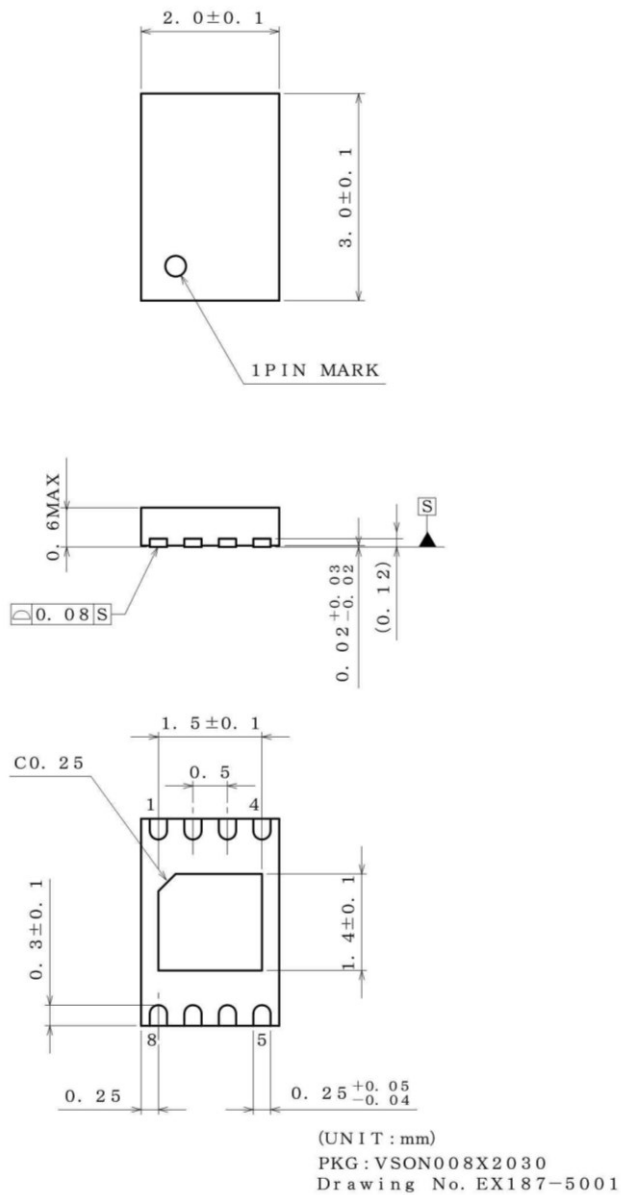


Physical Dimension, Tape and Reel Information - continued



Physical Dimension, Tape and Reel Information – continued

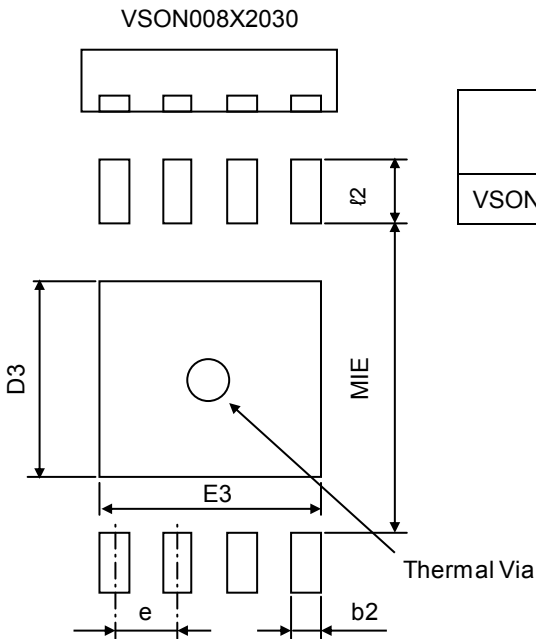
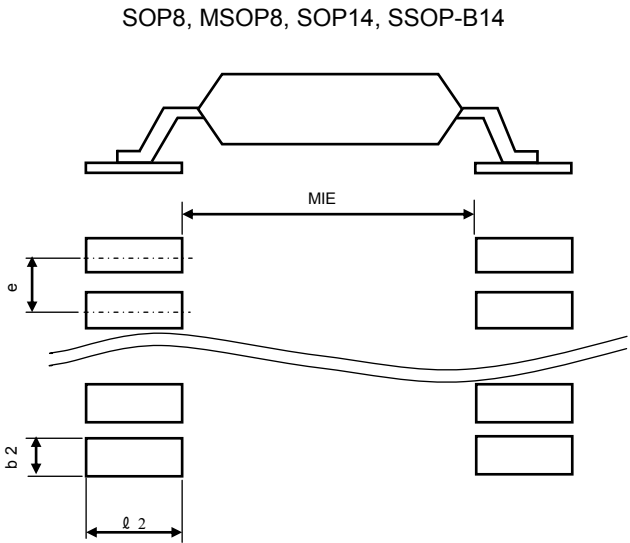
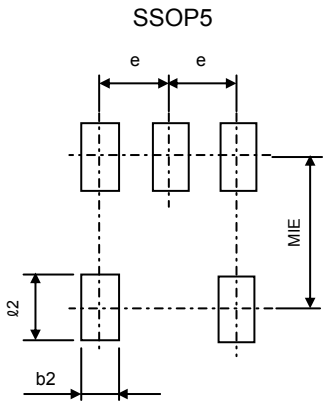
Package Name	VSON008X2030
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Land Pattern Data

All dimensions in mm

PKG	Land pitch e	Land space MIE	Land length ≥ ℓ 2	Land width b2
SSOP5	0.95	2.4	1.0	0.6
SOP8 SOP14	1.27	4.60	1.10	0.76
SSOP-B14	0.65	4.60	1.20	0.35
MSOP8	0.65	2.62	0.99	0.35
VSON008X2030	0.50	2.20	0.70	0.27



PKG	Radiation Land Length D3	Radiation Land Width E3	Thermal Via	
			Pitch	Diameter
VSON008X2030	1.2	1.6	-	Φ0.3

Revision History

Date	Revision	Changes
25.Sep.2012	001	New Release
06.Mar.2014	002	Revision is updated only
18.Apr.2014	003	Addition of BU7264FV,BU7264SFV in the Pin Configuration(Page 2.)
03.Dec.2014	004	Correction of Figure 7, 9, 30, 32, 34, 53, 55. Correction of Note 29~33. Correction of Note31 Power Dissipation(Page 33)

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JAPAN	USA	EU	CHINA
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CLASS IV		CLASS III	

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- The Products are not subject to radiation-proof design.
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- Confirm that operation temperature is within the specified range described in the product specification.
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