MAX34407

SMBus 4-Channel Wide Dynamic Range Power Accumulator

General Description

The MAX34407 is a current and voltage monitor that is specialized for determining power consumption. The device has a wide dynamic range to allow it to accurately measure power in systems that consume small to large amounts of power. The device is configured and monitored with a standard I²C/SMBus serial interface. The unidirectional current sensor offers precision high-side operation with a low full-scale sense voltage. The device automatically collects the current-sense and voltage samples. The samples are then multiplied to obtain a power value and the power values are then accumulated. Upon a command from the host, the device transfers the accumulated power samples as well as the accumulation count to a set of registers that the host can access. This transfer occurs without missing a sample and allows the host to retrieve the data not in real time, but at any time interval.

Applications

- Tablets
- Ultra Notebooks
- Smartphones

***Ordering Information* appears at end of data sheet.**

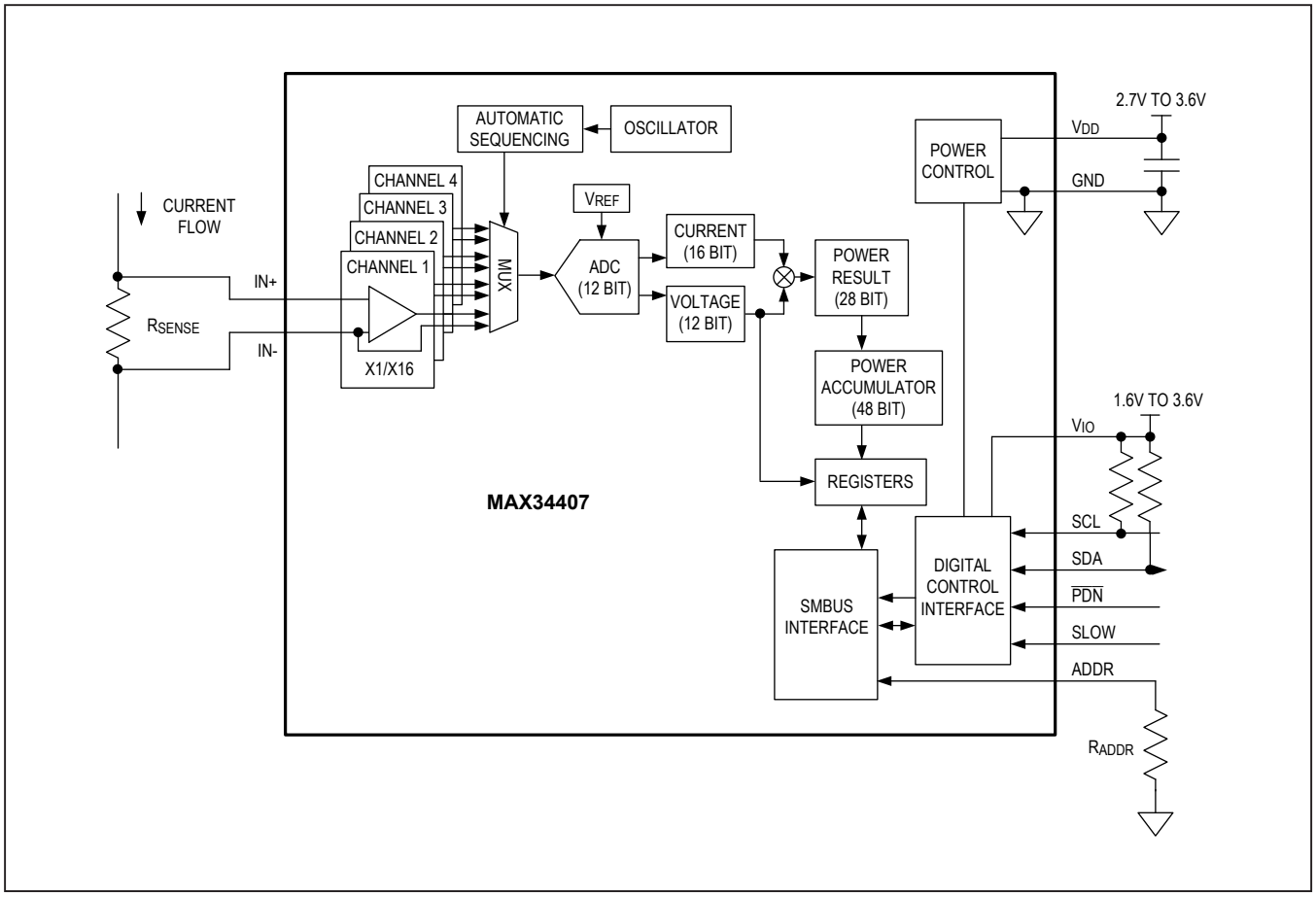
Features and Benefits

- Enables Code Optimization to Minimize Power Consumption in Portable Platforms
  - Four Power Monitors with Wide 66dB Dynamic Range
  - Measures Both Current and Voltage
  - Low Power Consumption
  - Slow Mode for Reduced Power Consumption
  - Power-Down Mode
- Minimizes Processor Overhead with Autonomous Operation
  - Per Channel 48-Bit Power Accumulators Capture 17 Minutes of Data at 1024 Samples per Second
  - Per Channel 12-Bit Voltage Registers
- High-Integration Solution Minimizes Parts Count, PCB Space, and BOM Cost
  - Wide Current Common-Mode Range of 2.5V to 15V
  - Low Full-Scale, Current-Sense Voltage of 100mV
  - I²C/SMBus Interface
  - Temperature Range: -40°C to +85°C
  - Small, 2.285mm x 2.185mm Footprint WLP Package with 16 Bumps at 0.5mm Pitch
- Ease of Development
  - Evaluation Kit with Advanced GUI Available (MAX34407EVKIT#)
  - Windows Driver Available

19-7431; Rev 0; 11/14

maxim integrated™

Typical Application Circuit and Block Diagram



Absolute Maximum Ratings

IN+ and IN- to GND .....-0.3V to +16V
Differential Input Voltage, IN+ to IN- .....±16V
V_{DD} or V_{IO} to GND .....-0.3V to +4V
SDA or SCL to GND .....-0.3V to +4V
All Other Pins .....-0.3V to V_{IO} + 0.3V (not to exceed +4V)

Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -55°C to +125°C
Soldering Temperature ..... See the IPC/JEDEC J-STD-020A Specification

Package Thermal Characteristics (Note 1)

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....49°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{DD} = 2.7V to 3.6V, V_{IO} = 1.6V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD} Operating Range			2.7		3.6	V
V_{DD} Average Supply Current (Note 2)	I_{DD}	$\overline{PDN}$ = V_{IO} and SLOW = GND		300	450	µA
		$\overline{PDN}$ = V_{IO} and SLOW = V_{IO}		2.4	4	µA
		$\overline{PDN}$ = GND		0.7	2	µA
V_{IO} Operating Range			1.6		3.6	V
V_{IO} Average Supply Current (Note 2)	I_{IO}			0.2	1	µA
Common-Mode Voltage Range (Note 3)	V_{CM}		2.5		15	V
IN+ Average Input Bias Current (Note 3)		$\overline{PDN}$ = GND or SLOW = V_{IO}		1		µA
		V_{CM} = 2.5V and V_{SENSE} = 0mV $\overline{PDN}$ = V_{IO} and SLOW = GND		3.1		
		V_{CM} = 1.5V and V_{SENSE} = 0mV $\overline{PDN}$ = V_{IO} and SLOW = GND		4.8		
Per Channel Current and Voltage Sample Rate		SLOW = GND		1024		sps
		SLOW = V_{IO}		8		sps
Per Channel Power Calculation Rate		SLOW = GND		1024		sps
		SLOW = V_{IO}		8		sps
Current Sample Resolution		V_{SENSE} < 4mV		16		Bits
Voltage Sample Resolution				12		Bits
Current-Sense Full Scale				100		mV
Voltage-Sense Full Scale				16		V
Power Measurement Accumulation Accuracy (1 Sigma Error Range with > 1000 Accumulations) (Note 4)		V_{SENSE} = 97mV		±0.8		%
		V_{SENSE} = 10mV		±1		
		V_{SENSE} = 1mV		±1.5		
		V_{SENSE} = 100µV		±8		
		V_{SENSE} = 50µV		±15		

Electrical Characteristics (continued)

(V_{DD} = 2.7V to 3.6V, V_{IO} = 1.6V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Bandwidth				200		kHz
Input Logic-High SCL/SDA/PDN/SLOW	V_{IH}		0.75 x V_{IO}			V
Input Logic-Low SCL/SDA/PDN/SLOW	V_{IL}				0.25 x V_{IO}	V
SDA Output Logic-Low	V_{OL}	I_{OL} = 4mA			0.4	V
SDA Output Leakage					±1	µA
SCL, SDA Leakage					±5	µA
SLOW, PDN Leakage					±1	µA
Power-Up Time		Measured from V_{DD} > 2.7V and V_{IO} > 1.6V and $\overline{PDN}$ deasserted to SMBus port active		650		µs

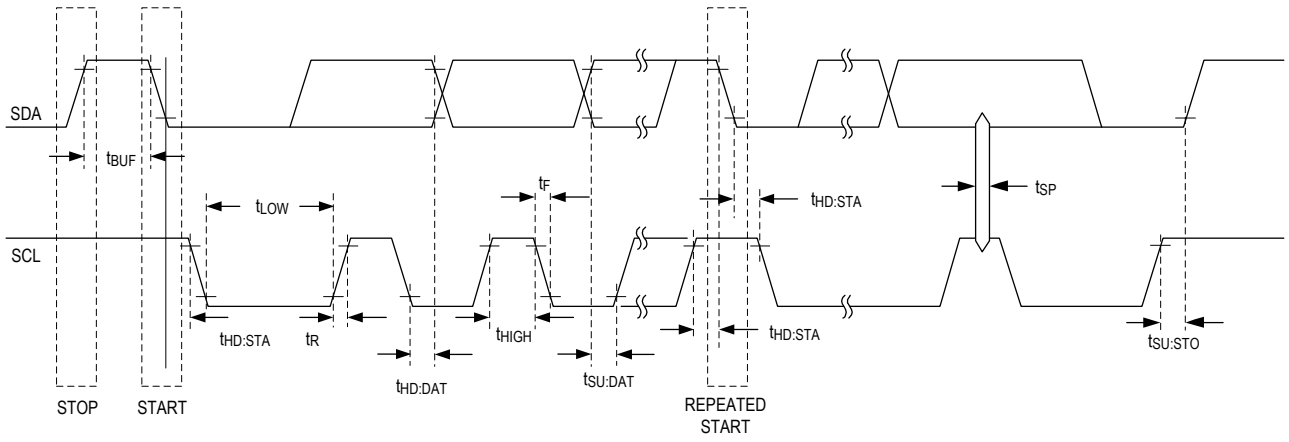
Note 2: SMBus not active.
Note 3: Common-mode voltage applies to the IN+ and IN- pins.
Note 4: Not production tested; bench characterization data.

AC Electrical Characteristics: I²C/SMBus Interface

(V_{IO} = 1.6V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{IO} = 3.3, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}		10		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$		0.6			µs
Low Period of SCL	t_{LOW}		1.3			µs
High Period of SCL	t_{HIGH}		0.6			µs
Data Hold Time	$t_{HD:DAT}$	Receive	0			ns
		Transmit	300			ns
Data Set-Up Time	$t_{SU:DAT}$		100			ns
Start Set-Up Time	$t_{SU:STA}$		0.6			µs
SDA and SCL Rise Time	t_R				300	ns
SDA and SCL Fall Time	t_F				300	ns
Stop Set-Up Time	$t_{SU:STO}$		0.6			µs
Noise Spike Reject	t_{SP}			30		ns

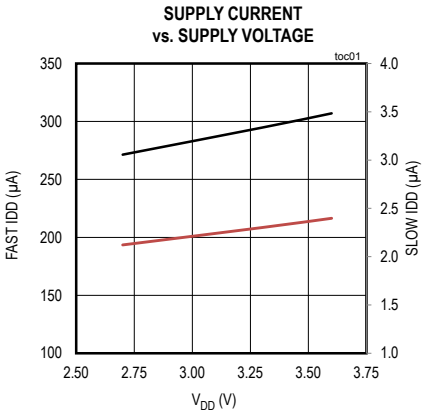
I²C/SMBus Timing

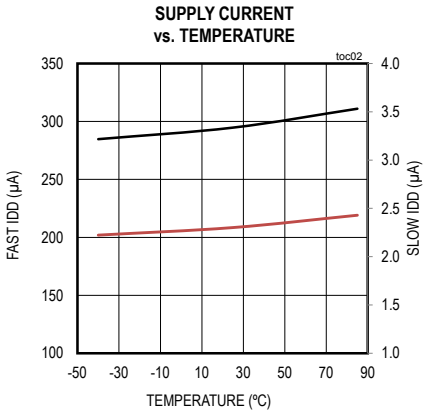


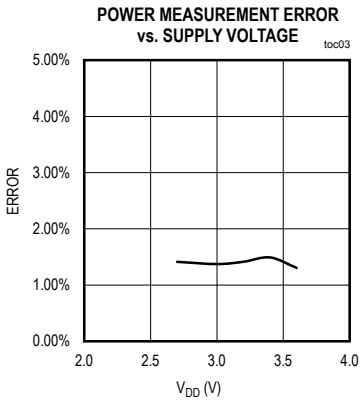
NOTE: TIMING IS REFERENCED TO $V_{IL(MAX)}$ AND $V_{IH(MIN)}$.

Typical Operating Characteristics

(V_{DD} = V_{IO} = 3.3V, T_A = +25°C, V_{CM} = 5V, V_{SENSE} = 1mV.)

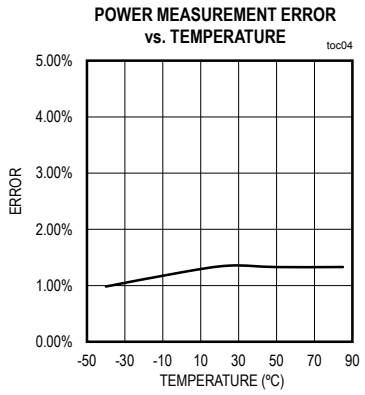


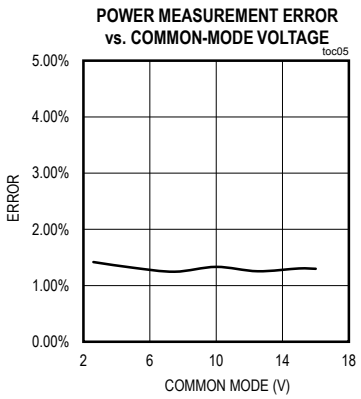


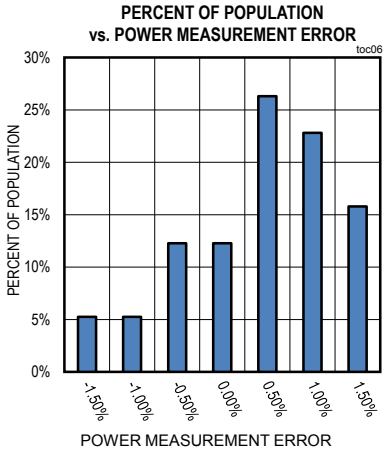


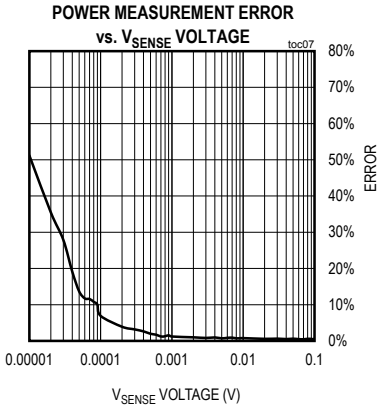
Typical Operating Characteristics (continued)

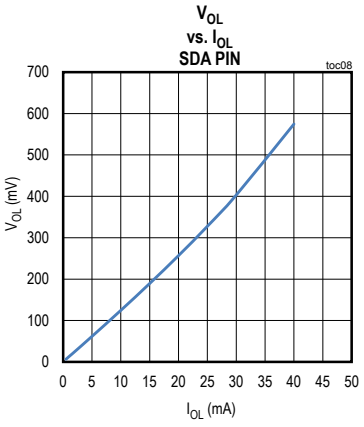
(V_{DD} = V_{IO} = 3.3V, T_A = +25°C, V_{CM} = 5V, V_{SENSE} = 1mV.)



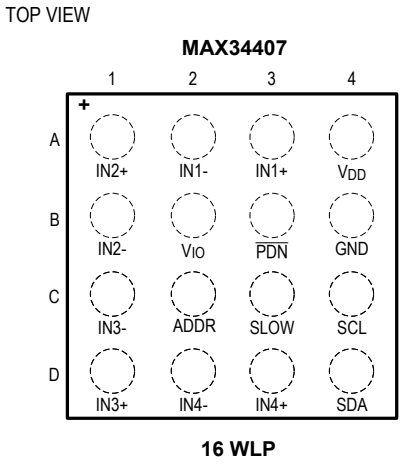








Pin Configuration



16 WLP

Pin Description

PIN	NAME	FUNCTION
A1	IN2+	External-Sense Resistor Power-Side Connection for Current-Sense Amplifier 2. Voltages can be applied to these pins in the absence of power being applied to V_{DD} or V_{IO}. Unused current-sense inputs should be tied together and left unconnected.
A2	IN1-	External-Sense Resistor Load-Side Connection for Current-Sense Amplifier 1. Voltages can be applied to these pins in the absence of power being applied to V_{DD} or V_{IO}. Unused current-sense inputs should be tied together and left unconnected.
A3	IN1+	External-Sense Resistor Power-Side Connection for Current-Sense Amplifier 1. Voltages can be applied to these pins in the absence of power being applied to V_{DD} or V_{IO}. Unused current-sense inputs should be tied together and left unconnected.
A4	V_{DD}	Supply Voltage for Current-Sense Amplifiers. +2.7V to +3.6V supply. This pin should be decoupled to GND with a 100nF ceramic capacitor. Power can be applied to V_{DD} either before or after or in the absence of V_{IO}.
B1	IN2-	External-Sense Resistor Load-Side Connection for Current-Sense Amplifier 2. Voltages can be applied to these pins in the absence of power being applied to V_{DD} or V_{IO}. Unused current-sense inputs should be tied together and left unconnected.
B2	V_{IO}	Supply Voltage for Digital Interface. +1.6V to +3.6V supply. This pin should be decoupled to GND with a 100nF ceramic capacitor. Power can be applied to V_{IO} either before or after or in the absence of V_{DD}.
B3	$\overline{PDN}$	Power-Down Mode Input. When this pin is tied low, the device is completely powered down including the I^2C/SMBus interface.
B4	GND	Ground Connection

Pin Description (continued)

PIN	NAME	FUNCTION
C1	IN3-	External-Sense Resistor Load-Side Connection for Current-Sense Amplifier 3. Voltages can be applied to these pins in the absence of power being applied to V_{DD} or V_{IO}. Unused current-sense inputs should be tied together and left unconnected.
C2	ADDR	I^2C/SMBus-Compatible Address Select Input. A resistor tied to GND from this pin selects the SMBus slave address. See the *Addressing* section for more details.
C3	SLOW	Slow Accumulate Mode Input. When this pin is tied high, the power accumulation is slowed to reduce overall device power consumption.
C4	SCL	I^2C/SMBus-Compatible Clock Input. SCL does not load the SMBus when either V_{DD} or V_{IO} is not present.
D1	IN3+	External-Sense Resistor Power-Side Connection for Current-Sense Amplifier 3. Voltages can be applied to these pins in the absence of power being applied to V_{DD} or V_{IO}. Unused current-sense inputs should be tied together and left unconnected.
D2	IN4-	External-Sense Resistor Load-Side Connection for Current-Sense Amplifier 4. Voltages can be applied to these pins in the absence of power being applied to V_{DD} or V_{IO}. Unused current-sense inputs should be tied together and left unconnected.
D3	IN4+	External-Sense Resistor Power-Side Connection for Current-Sense Amplifier 4. Voltages can be applied to these pins in the absence of power being applied to V_{DD} or V_{IO}. Unused current-sense inputs should be tied together and left unconnected.
D4	SDA	I^2C/SMBus-Compatible Data Input/Output. Output is open drain. SDA does not load the SMBus when either V_{DD} or V_{IO} is not present.

Detailed Description

The MAX34407 automatically sequences through the channels to collect samples from the common-mode voltage and the current-sense amplifiers. The 16-bit current value and the 12-bit voltage value are then multiplied to create a 28-bit power value that is then written to the power accumulator.

The MAX34407 contains a 48-bit power accumulator for each channel. This accumulator is updated 1024 times per second to allow the device to operate for at least 17 minutes without the host retrieving the results. When the host is ready to pull the latest accumulation data, it first sends the UPDATE command that causes the MAX34407 to load the latest accumulation data and accumulation count into the internal MAX34407 registers so the host can read them at any time. This type of operation allows the host to control the accumulation period. The only constraint is that the host should access the data before the accumulators can overflow. If the accumulators overflow, they do not roll over.

The MAX34407 contains a 12-bit ADC. During each sample time, a 12-bit voltage sample is resolved and a 16-bit current sample. To create a 16-bit current value from the 12-bit ADC, the device takes two current samples; one with the current sense amplifier in a high-gain mode and another with the amplifier in a low-gain mode. The high-gain setting is 16 times the low-gain setting. Based on the two current-sense ADC results, the device determines which result provides the best accuracy and fills the 16-bit current sample accordingly.

SMBus Operation

The MAX34407 uses the SMBus command/response format as described in the System Management Bus Specification Version 2.0. The structure of the data flow between the host and the slave is shown below for several different types of transactions. Data is sent MSB first. The fixed slave address of the MAX34407 is determined on device power-up by sampling the resistor tied to the ADDR pin. See the *Addressing* section for details. On device power-up, the device defaults to the CONTROL command code (01h). If the host sends an invalid command code, the device does not acknowledge (NACK) the command code. If the host attempts to read the device with an invalid command code, all ones (FFh) are returned in the data byte.

Table 1. Read Byte Format

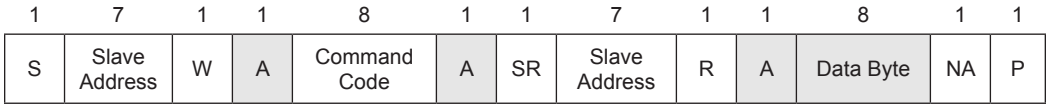


Table 2. Write Byte Format

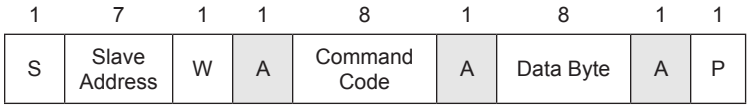


Table 3. Send Byte Format

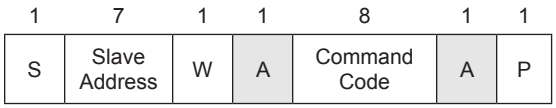
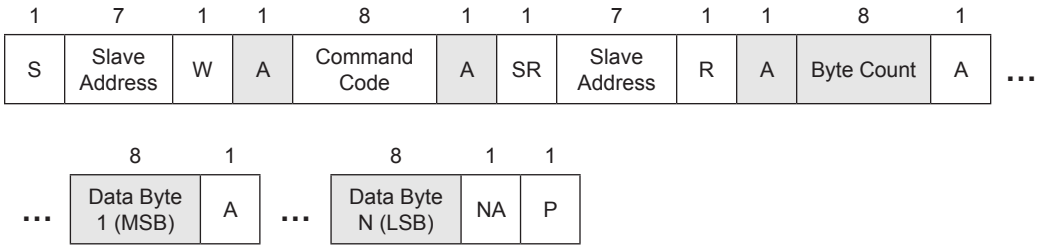


Table 4. Block Read Format



Key:
S = Start
SR = Repeated Start
P = Stop
W = Write Bit (0)
R = Read Bit (1)
A = Acknowledge (0)
NA = Not Acknowledge (1)
Shaded Block = Slave Transaction

Addressing

The MAX34407 responds to receiving its fixed slave address by asserting an ACK on the bus. The fixed slave address of the MAX34407 is determined on device power-up by sampling the resistor tied to the ADDR pin when V_{DD} rises to a valid range. See the Table 5 for more details. The device does not respond to a general call address, only when it receives its fixed slave address.

Table 5. SMBus Slave Address Select

RADDR (±1%) (kΩ)	SLAVE ADDRESS	RADDR (±1%) (Ω)	SLAVE ADDRESS
20.5	0011 110 (3Ch)	1.74k	0010 110 (2Ch)
11.0	0011 100 (38h)	931	0010 100 (28h)
5.90	0011 010 (34h)	442	0010 010 (24h)
3.16	0011 000 (30h)	Tie to GND	0010 000 (20h)

Table 6. Command Codes

COMMAND CODE	NAME	DETAILED DESCRIPTION	TYPE	NUMBER OF BYTES	POR (Note 5)
00h	UPDATE	Request Accumulator Update	Send Byte	0	—
01h	CONTROL	Device Configuration and Status	R/W Byte	1	00h
02h	ACC_COUNT	Accumulator Counter	Block Read	3	Note 6
03h	PWR_ACC_1	Power Accumulator for Channel 1	Block Read	6	Note 6
04h	PWR_ACC_2	Power Accumulator for Channel 2	Block Read	6	Note 6
05h	PWR_ACC_3	Power Accumulator for Channel 3	Block Read	6	Note 6
06h	PWR_ACC_4	Power Accumulator for Channel 4	Block Read	6	Note 6
07h	VOLTAGE_1	Voltage for Channel 1	Block Read	2	Note 6
08h	VOLTAGE_2	Voltage for Channel 2	Block Read	2	Note 6
09h	VOLTAGE_3	Voltage for Channel 3	Block Read	2	Note 6
0Ah	VOLTAGE_4	Voltage for Channel 4	Block Read	2	Note 6
0Fh	DID	Device ID and Revision	Read Byte	1	Note 7

Note 5: The acronym POR means power-on reset. This is the default value when power is applied to the device.
Note 6: These registers are set to all zeros upon POR.
Note 7: The device ID is factory set and varies based on the die revision.

Update (00h)—Send Byte

The UPDATE send byte command does not contain any data. The UPDATE command must be sent to the device before reading any of the other commands, and it must be sent after writing to the CONTROL command. After sending the UPDATE command, the host should wait at least 500µs before reading any command. Each time the device receives this command, it transfers the all of the data in the power accumulators and the accumulator counter to a set of registers that can be read with the SMBus interface, and it resets all of the counters. See Figure 1 for more details.

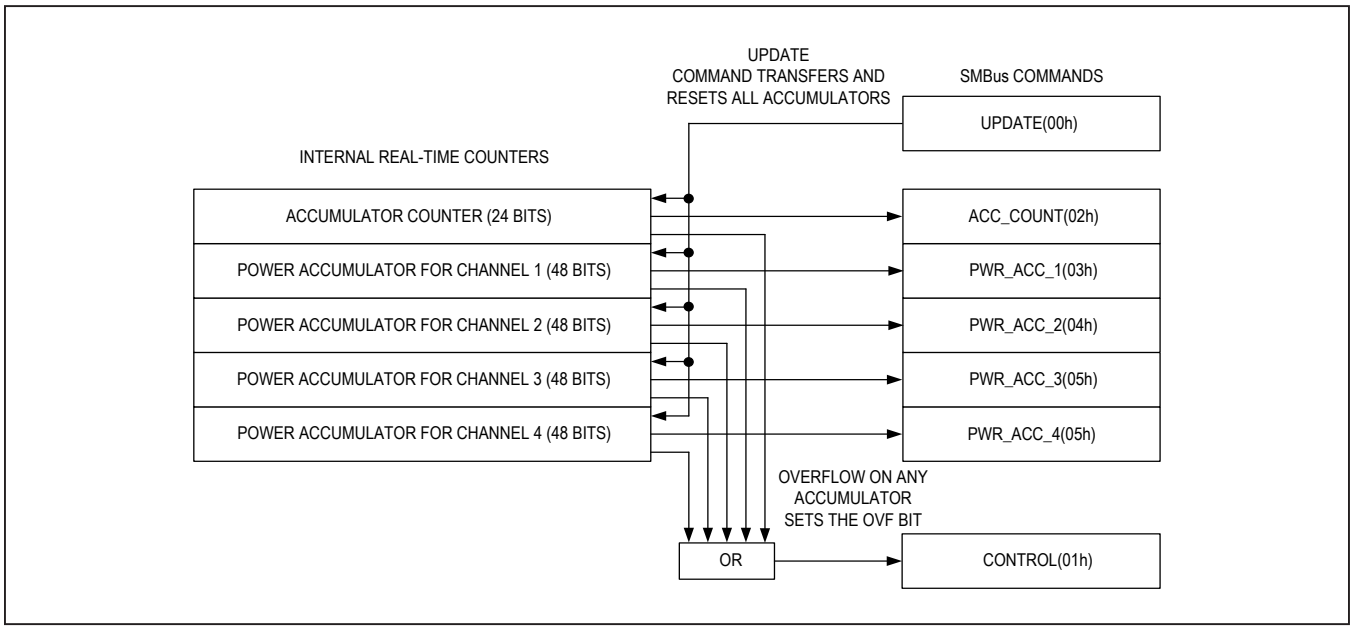


Figure 1. MAX34407 Register Structure

Table 7. Control (01h)—R/W Byte

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME:	0	0	SMM	PARK_EN	PARK1	PARK0	SLOW	OVF
POR:	0	0	0	0	0	0	0	0

Note: *Bit positions 6 and 7 must be written to 0 for proper device operation.*

Bit 5: SMM (Single Measure Mode)

When this bit is set, the device performs only one measure and accumulation cycle for the four input channels (normal scan mode) or four samples of one channel in channel park mode in response to an UPDATE command. The data can be read by issuing another UPDATE command that moves the previous UPDATE data into the SMBus read registers and starts another measurement cycle. Data should be read between UPDATE commands. UPDATE commands should be no less than 500µs apart for reliable measurements. The power accumulators remain at 48-bits even though the single calculated power is a 28-bit value. After the SMM bit is changed, the UPDATE command should be sent to reset the accumulators and perform the selected scan operation.

0 = Single-measure mode is disabled.

1 = Single-measure mode is enabled.

Bit 4: PARK_EN

This bit enables the channel park feature. If this bit is set, only one channel is enabled, and the device samples the selected channel four times faster than the normal round robin rate. The channel to monitor is selected with the PARK0 and PARK1 bits. After the PARK_EN bit is changed, the UPDATE command should be sent to clear out the accumulators and start a new accumulation period. When the channel park feature is enabled, the minimum time before the power accumulators can overflow reduces by a factor of four since the selected channel is being updated four times faster. Also, the power accumulators for the disabled channels do not contain any meaningful data.

0 = Round-robin sampling of all four channels.

1 = One channel is selected (with the PARK0/1 bits).

Bits 3 to 2: PARK1 to PARK0

If the PARK_EN (Park Enable) bit is set, then these bits select which channel is to be monitored at the exclusion of the other channels.

PARK1	PARK0	SELECTED CHANNEL
0	0	Channel 1
0	1	Channel 2
1	0	Channel 3
1	1	Channel 4

Bit 1: SLOW

This bit is logically OR'ed with the SLOW input pin. If either this bit is set or the SLOW pin is high, then the power accumulation calculation rate is slowed in order to lower the power consumption of the device.

Bit 0: OVF

This status bit is set to a one if any of the power accumulators or the accumulator counter overflows. When the accumulators or counter overflow, they do not roll over. This status bit can be cleared by writing a 0. If any of the power accumulators or the accumulator counter are still full, then this bit immediately sets again. Accumulators and the counter that have overflowed can be cleared by sending the UPDATE command.

Table 8. Accumulator Counter (02h)—Block Read

	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
NAME:	CNT23	CNT22	CNT21	CNT20	CNT19	CNT18	CNT17	CNT16
POR:	0	0	0	0	0	0	0	0
	BIT 15	**BIT 14**	**BIT 13**	**BIT 12**	**BIT 11**	**BIT 10**	**BIT 9**	**BIT 8**
NAME:	CNT15	CNT14	CNT13	CNT12	CNT11	CNT10	CNT9	CNT8
POR:	0	0	0	0	0	0	0	0
	BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
NAME:	CNT7	CNT6	CNT5	CNT4	CNT3	CNT2	CNT1	CNT0
POR:	0	0	0	0	0	0	0	0

Bits 23 to 0: CNT23 to CNT0

These bits report the number of times the accumulators have been updated. Send the UPDATE command before reading this register. By dividing the total accumulated power reported in each power accumulator by this count, the average power can be determined. The accumulator counter does not roll over. If the accumulator counter overflows, the OVF bit in the CONTROL command is set and remains set until the UPDATE command is sent.

Table 9. Power Accumulator for Channel 1 (03h)—Block Read
Power Accumulator for Channel 2 (04h)—Block Read
Power Accumulator for Channel 3 (05h)—Block Read
Power Accumulator for Channel 4 (06h)—Block Read

	BIT 47	BIT 46	BIT 45	BIT 44	BIT 43	BIT 42	BIT 41	BIT 40
NAME:	ACC47	ACC46	ACC45	ACC44	ACC43	ACC42	ACC41	ACC40
POR:	0	0	0	0	0	0	0	0
	BIT 39	**BIT 38**	**BIT 37**	**BIT 36**	**BIT 35**	**BIT 34**	**BIT 33**	**BIT 32**
NAME:	ACC39	ACC38	ACC37	ACC36	ACC35	ACC34	ACC33	ACC32
POR:	0	0	0	0	0	0	0	0
	BIT 31	**BIT 30**	**BIT 29**	**BIT 28**	**BIT 27**	**BIT 26**	**BIT 25**	**BIT 24**
NAME:	ACC31	ACC30	ACC29	ACC28	ACC27	ACC26	ACC25	ACC24
POR:	0	0	0	0	0	0	0	0
	BIT 23	**BIT 22**	**BIT 21**	**BIT 20**	**BIT 19**	**BIT 18**	**BIT 17**	**BIT 16**
NAME:	ACC23	ACC22	ACC21	ACC20	ACC19	ACC18	ACC17	ACC16
POR:	0	0	0	0	0	0	0	0
	BIT 15	**BIT 14**	**BIT 13**	**BIT 12**	**BIT 11**	**BIT 10**	**BIT 9**	**BIT 8**
NAME:	ACC15	ACC14	ACC13	ACC12	ACC11	ACC10	ACC9	ACC8
POR:	0	0	0	0	0	0	0	0
	BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
NAME:	ACC7	ACC6	ACC5	ACC4	ACC3	ACC2	ACC1	ACC0
POR:	0	0	0	0	0	0	0	0

Bits 47 to 0: ACC47 to ACC0

These bits report the total power accumulated by each channel. Send the UPDATE command before reading these registers. The power accumulators do not roll over. If any of the power accumulator overflows, the OVF bit in the CONTROL command is set and remains set until the UPDATE command is sent.

Table 10. Voltage for Channel 1 (07h)—Block Read Voltage for Channel 2 (08h)—Block Read Voltage for Channel 3 (09h)—Block Read Voltage for Channel 4 (0Ah)—Block Read

	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
NAME:	V11	V10	V9	V8	V7	V6	V5	V4
POR:	0	0	0	0	0	0	0	0
	BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
NAME:	V3	V2	V1	V0	N/A	N/A	N/A	N/A
POR:	0	0	0	0	0	0	0	0

Note: *Bit positions marked as N/A are not assigned and have no meaning. These bits can be either 0 or 1 when read.*

Bits 15 to 4: V11 to V0

These bits report the last measured common-mode voltage for each channel. The LSB bit weighting is 3.9mV (16V full scale/4096). The UPDATE command must be sent before reading the channel voltages. The host should wait 500µs after sending the UPDATE command before reading the VOLTAGE commands.

Table 11. Device ID & Revision Register (0Fh)—Read Byte

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME:	ID4	ID3	ID2	ID1	ID0	REV2	REV1	REV0
POR:	0	0	1	0	1	Factory set		

Bits 7 to 3: ID4 to ID0

These bits report the device identification (ID). The ID is fixed at 05h.

Bits 2 to 0: REV2 to REV0

These bits report the device revision. The device revision is factory set.

Applications Information

Average Power Calculation Example

The average power can be derived in an external calculation as shown below if the current sense resistor value is known.

Power accumulator (48 bit) = 0001CEFBD314h (7767577364 decimal)

Accumulator counter (24 bit) = 0005DEh (1502 decimal)

Current-sense resistor = 10mΩ

Step 1

Calculate the unscaled average power by dividing the power accumulator value with the accumulator *count value*:

0001CEFBD314h/0005DEh = 4EE921h (5171489 decimal)

Step 2

Calculate the ratio of the Step 1 result to the calculated power full-scale value which is a 28-bit value:

$5171489/2^{28} = 0.019265$

Step 3

Multiply the result from Step 2 by the correction factor listed in Table 12 that matches the current-sense resistor value:

0.019265 x 160 = 3.08W

Table 12. Correction Factors for Various Current-Sense Resistor Values

CURRENT-SENSE RESISTOR VALUE (mΩ)	FULL-SCALE CURRENT (A)	FULL-SCALE VOLTAGE (V)	POWER SCALE CORRECTION CALCULATION	POWER SCALE CORRECTION FACTOR (W)
100	1	16	1 x 16	16
50	2	16	2 x 16	32
40	2.5	16	2.5 x 16	40
25	4	16	4 x 16	64
20	5	16	5 x 16	80
15	6.667	16	6.667 x 16	106.667
10	10	16	10 x 16	160
5	20	16	20 x 16	320
4	25	16	25 x 16	400
2	50	16	50 x 16	800
1	100	16	100 x 16	1600

Kelvin Sense

For best performance, a Kelvin sense arrangement is recommended. See Figure 2. In a Kelvin sense arrangement, the voltage sensing nodes across the sense element are placed so that they measure the true voltage drop across the sense element and not any additional excess voltage drop that can occur in the copper PCB traces or the solder mounting of the sense element. Routing the differential sense lines along the same path to the MAX34407 and keeping the path short also improve the system performance.

Minimizing Trace Resistance

PCB trace resistance from the sense resistor (RSENSE) to the IN+ inputs can affect the MAX34407 power measurement accuracy. Every 1 ohm of PCB trace resistance will add about 25µV of error. It is recommended to place the sense resistors as close as possible to the MAX34407 and not to use minimum width PCB traces.

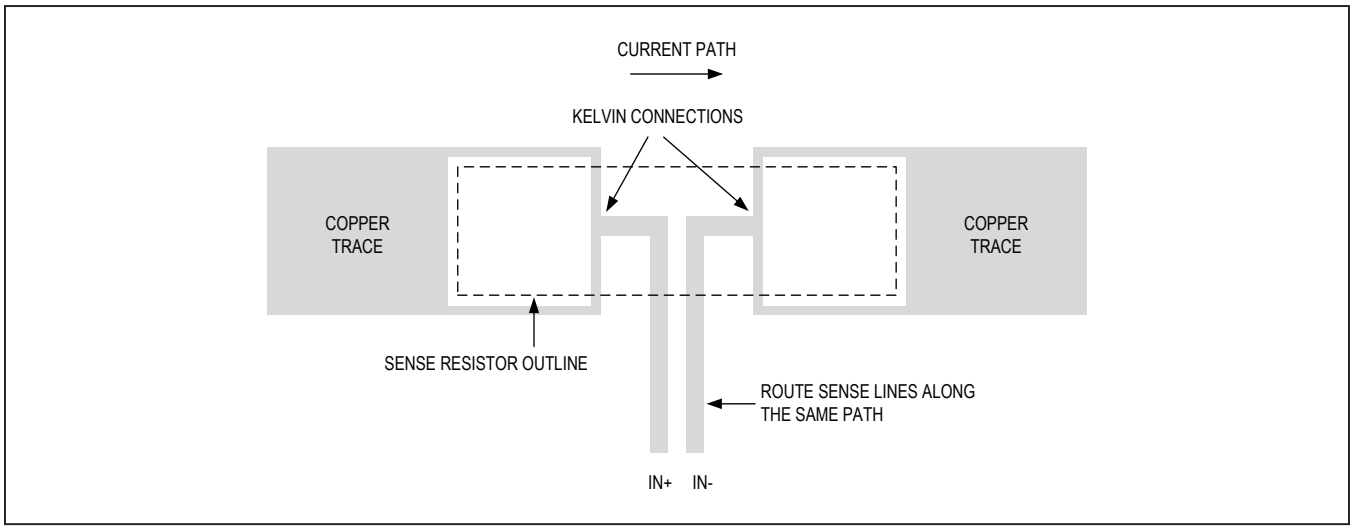


Figure 2. Kelvin Sense Connection Layout Example

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX34407EWE+	-40°C to +85°C	16 WLP
MAX34407EWE+T	-40°C to +85°C	16 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 WLP	W16N2+1	**21-0893**	Refer to **Application Note 1891**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/14	Initial release	—

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