Product data sheet

1. General description

Planar passivated four quadrant triac in a SOT428 (DPAK) surface-mountable plastic package intended for use in general purpose bidirectional switching and phase control applications.

2. Features and benefits

- · High blocking voltage capability
- · Less sensitive gate for improved noise immunity
- · Planar passivated for voltage ruggedness and reliability
- Surface-mountable package
- Triggering in all four quadrants

3. Applications

- General purpose motor controls
- · General purpose switching

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{DRM}	repetitive peak off- state voltage		-	-	800	V
I _{T(RMS)}	RMS on-state current	full sine wave; $T_{mb} \le 102 ^{\circ}\text{C}$; $\overline{\text{Fig. 1}}$; $\overline{\text{Fig. 2}}$; $\overline{\text{Fig. 3}}$	-	-	8	Α
I _{TSM}	non-repetitive peak on- state current	full sine wave; $T_{j(init)} = 25 \text{ °C}$; $t_p = 20 \text{ ms}$; Fig. 4; Fig. 5	-	-	65	Α
		full sine wave; $T_{j(init)} = 25 ^{\circ}C$; $t_p = 16.7 ms$	-	-	71	Α
T _j	junction temperature		-	-	125	°C
Static charac	teristics					
I _{GT}	gate trigger current	$V_D = 12 \text{ V; } I_T = 0.1 \text{ A; } T2+ G+;$ $T_j = 25 \text{ °C; } \frac{\text{Fig. 7}}{}$	-	5	25	mA
		$V_D = 12 \text{ V; } I_T = 0.1 \text{ A; } T2 + G-;$ $T_j = 25 \text{ °C; } \frac{\text{Fig. 7}}{}$	-	8	25	mA
		$V_D = 12 \text{ V; } I_T = 0.1 \text{ A; } T2-\text{ G-;} $ $T_j = 25 \text{ °C; } \frac{\text{Fig. 7}}{}$	-	11	25	mA
		$V_D = 12 \text{ V; } I_T = 0.1 \text{ A; } T2-\text{ G+;} $ $T_j = 25 \text{ °C; } \frac{\text{Fig. 7}}{}$	-	30	70	mA

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Symbol	Parameter	Conditions		Min	Тур	Max	Unit
I _H	holding current	V _D = 12 V; T _j = 25 °C; <u>Fig. 9</u>		-	5	20	mA
V _T	on-state voltage	I _T = 10 A; T _j = 25 °C; <u>Fig. 10</u>		-	1.3	1.65	V
Dynamic chara	Dynamic characteristics						
dV _D /dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_{j} = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit		50	250	-	V/µs
dV _{com} /dt	rate of change of commutating voltage	V_D = 400 V; T_j = 95 °C; dI_{com}/dt = 3.6 A/ ms; I_T = 8 A; gate open circuit		-	20	-	V/µs

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1	[]	T2——T1
2	T2	main terminal 2	(7 B S)	G sym051
3	G	gate		Symoor
mb	T2	mounting base; main terminal 2		
			DPAK (SOT428)	

6. Ordering information

Table 3. Ordering information

Type number	Package				
	Name	Description	Version		
BT137S-800F	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428		

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	800	V
I _{T(RMS)}	RMS on-state current	full sine wave; $T_{mb} \le 102 ^{\circ}\text{C}$; Fig. 1; Fig. 2; Fig. 3	-	8	Α
I _{TSM}	non-repetitive peak on- state current	full sine wave; $T_{j(init)}$ = 25 °C; t_p = 20 ms; Fig. 4; Fig. 5	-	65	Α
		full sine wave; T _{j(init)} = 25 °C; t _p = 16.7 ms	-	71	Α
l ² t	I ² t for fusing	t _p = 10 ms; SIN	-	21	A²s
dl _T /dt	rate of rise of on-state current	I _G = 150 mA	-	50	A/µs
I _{GM}	peak gate current		-	2	Α
P _{GM}	peak gate power		-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.5	W
T _{stg}	storage temperature		-40	150	°C
T _j	junction temperature		_	125	°C

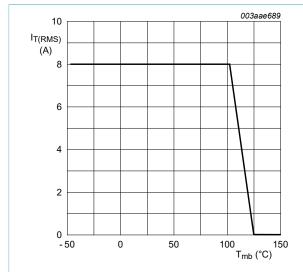


Fig. 1. RMS on-state current as a function of mounting base temperature; maximum values

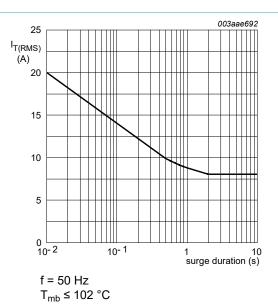


Fig. 2. RMS on-state current as a function of surge duration; maximum values

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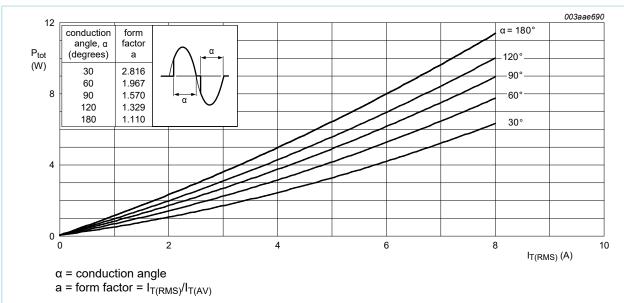
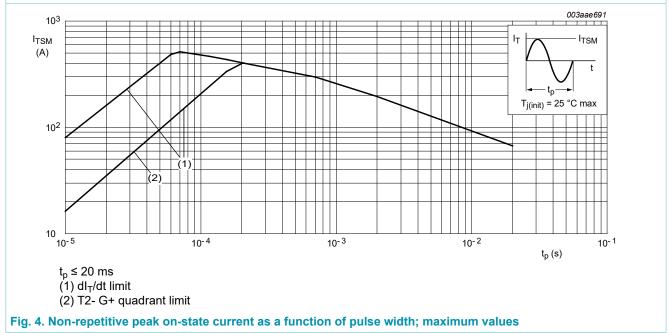


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values



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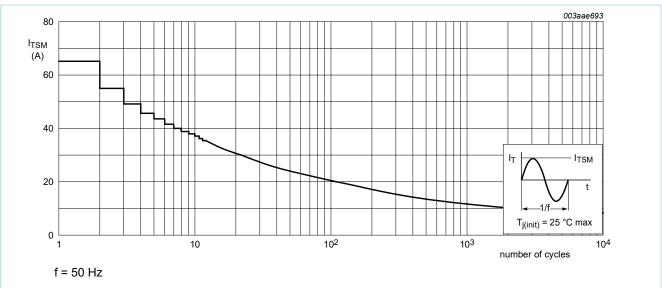


Fig. 5. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

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8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-mb)}	thermal resistance from junction to mounting base	half cycle; Fig. 6	-	-	2.4	K/W
		full cycle; Fig. 6	-	-	2	K/W
R _{th(j-a)}	thermal resistance from junction to ambient free air	PCB (FR4) mounted; minimum pad sizes	-	75	-	K/W

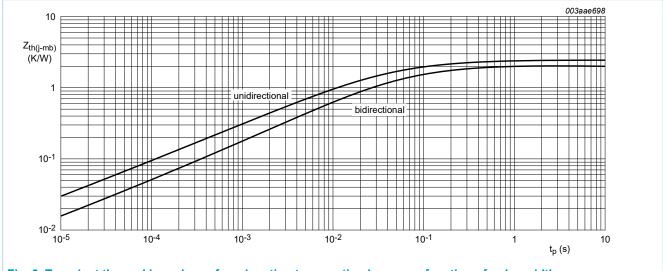


Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse width

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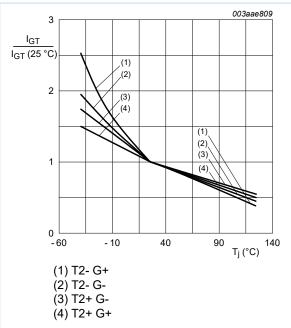
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9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics		'			
I _{GT}	gate trigger current	$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T2+ G+; $ $T_j = 25 ^{\circ}\text{C}; Fig. 7$	-	5	25	mA
		$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T2+ G-;$ $T_j = 25 ^{\circ}\text{C}; Fig. 7$	-	8	25	mA
		$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T2- \text{G-};$ $T_j = 25 ^{\circ}\text{C}; \underline{\text{Fig. 7}}$	-	11	25	mA
		$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T2- G+; $ $T_j = 25 ^{\circ}\text{C}; \underline{\text{Fig. 7}}$	-	30	70	mA
lL	latching current	$V_D = 12 \text{ V}; I_G = 0.1 \text{ A}; T2+ G+; $ $T_j = 25 ^{\circ}\text{C}; Fig. 8$	-	7	30	mA
		$V_D = 12 \text{ V}; I_G = 0.1 \text{ A}; T2+ G-;$ $T_j = 25 ^{\circ}\text{C}; Fig. 8$	-	16	45	mA
		$V_D = 12 \text{ V}; I_G = 0.1 \text{ A}; \text{ T2- G-};$ $T_j = 25 ^{\circ}\text{C}; \underline{\text{Fig. 8}}$	-	5	30	mA
		$V_D = 12 \text{ V}; I_G = 0.1 \text{ A}; \text{ T2- G+};$ $T_j = 25 ^{\circ}\text{C}; \underline{\text{Fig. 8}}$	-	7	45	mA
I _H	holding current	V _D = 12 V; T _j = 25 °C; <u>Fig. 9</u>	-	5	20	mA
V _T	on-state voltage	I _T = 10 A; T _j = 25 °C; <u>Fig. 10</u>	-	1.3	1.65	V
V_{GT}	gate trigger voltage	$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T_j = 25 \text{ °C};$ Fig. 11	-	0.7	1	V
		$V_D = 400 \text{ V}; I_T = 0.1 \text{ A}; T_j = 125 ^{\circ}\text{C};$ Fig. 11	0.25	0.4	-	V
I _D	off-state current	V _D = 800 V; T _j = 125 °C	-	0.1	0.5	mA
Dynamic ch	naracteristics		'	,		
dV _D /dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_{j} = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit	50	250	-	V/µs
dV _{com} /dt	rate of change of commutating voltage	V_D = 400 V; T_j = 95 °C; dI_{com}/dt = 3.6 A/ms; I_T = 8 A; gate open circuit	-	20	-	V/µs

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003aae697 3 I_{L} I_{L(25°C)} 2 1 - 60 - 10 40 140 T_i (°C)

Fig. 8. Normalized latching current as a function of junction temperature

Fig. 7. Normalized gate trigger current as a function of junction temperature

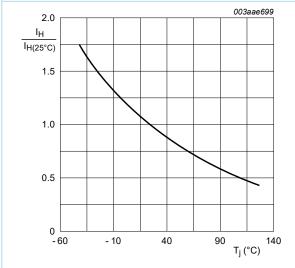
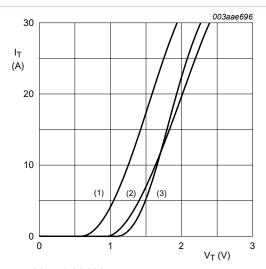


Fig. 9. Normalized holding current as a function of junction temperature



 $V_o = 1.264 \text{ V}$ $R_s = 0.038 \Omega$

(1) T_j = 125 °C; typical values (2) T_j = 125 °C; maximum values (3) T_j = 25 °C; maximum values

Fig. 10. On-state current as a function of on-state voltage

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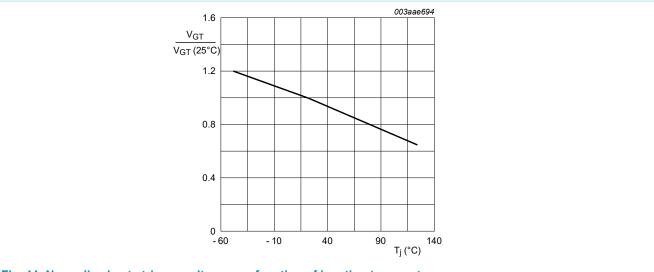
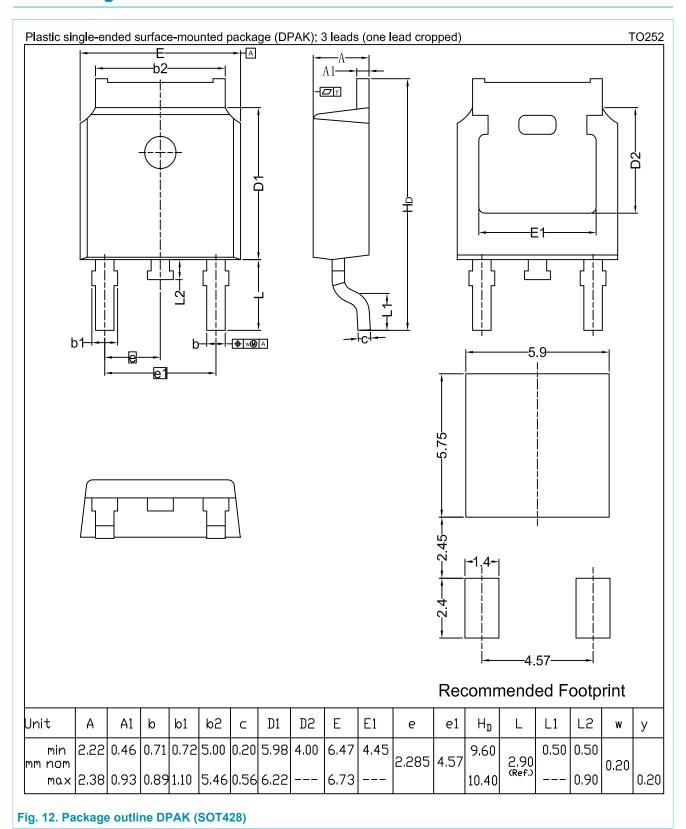


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

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10. Package outline



11. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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For more information, please visit: http://www.ween-semi.com
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