

TLE4208G

Quad Half-Bridge Driver IC

Data Sheet

Rev. 1.4, 2016-02-02

Automotive Power

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1 Overview

Features

- Driver for up to 3 motors
- Delivers up to 0.8 A continuous
- Optimized for DC motor management applications
- Very low current consumption in stand-by (Inhibit) mode
- Low saturation voltage; typ. 1.2 V total @ 25 °C; 0.4 A
- Output protected against short circuit
- Error flag diagnosis
- Overvoltage lockout and diagnosis
- Undervoltage lockout
- CMOS/TTL compatible inputs with hysteresis
- No crossover current
- Internal clamp diodes
- Overtemperature protection with hysteresis and diagnosis
- Enhanced power DSO-Package
- Green Product (RoHS compliant)
- AEC Qualified



PG-DSO-28

Description

The TLE4208G is a protected Quad-Half-Bridge-Driver designed specially for automotive and industrial motion control applications. The part is built using Infineons bipolar high voltage power technology DOPL.

In a cascade configuration up to three actuators (DC motors) can be connected between the four half-bridges. These four half-bridges are configured as 2 dual-half-bridges, which are supplied and controlled separately. Operation modes forward (cw), reverse (ccw), brake and high impedance are invoked from a standard interface.

The standard enhanced power PG-DSO-28 package meets the application requirements and saves PCB-board space and costs. Moreover the package is RoHS compliant.

Furthermore the built-in features like diagnosis, over- and undervoltage-lockout, short-circuit protection, over-temperature protection and the very low quiescent current in stand-by mode will open a wide range of automotive and industrial applications.

| Type | Package | Marking |
|----------|-----------|----------|
| TLE4208G | PG-DSO-28 | TLE4208G |

2 Block Diagram

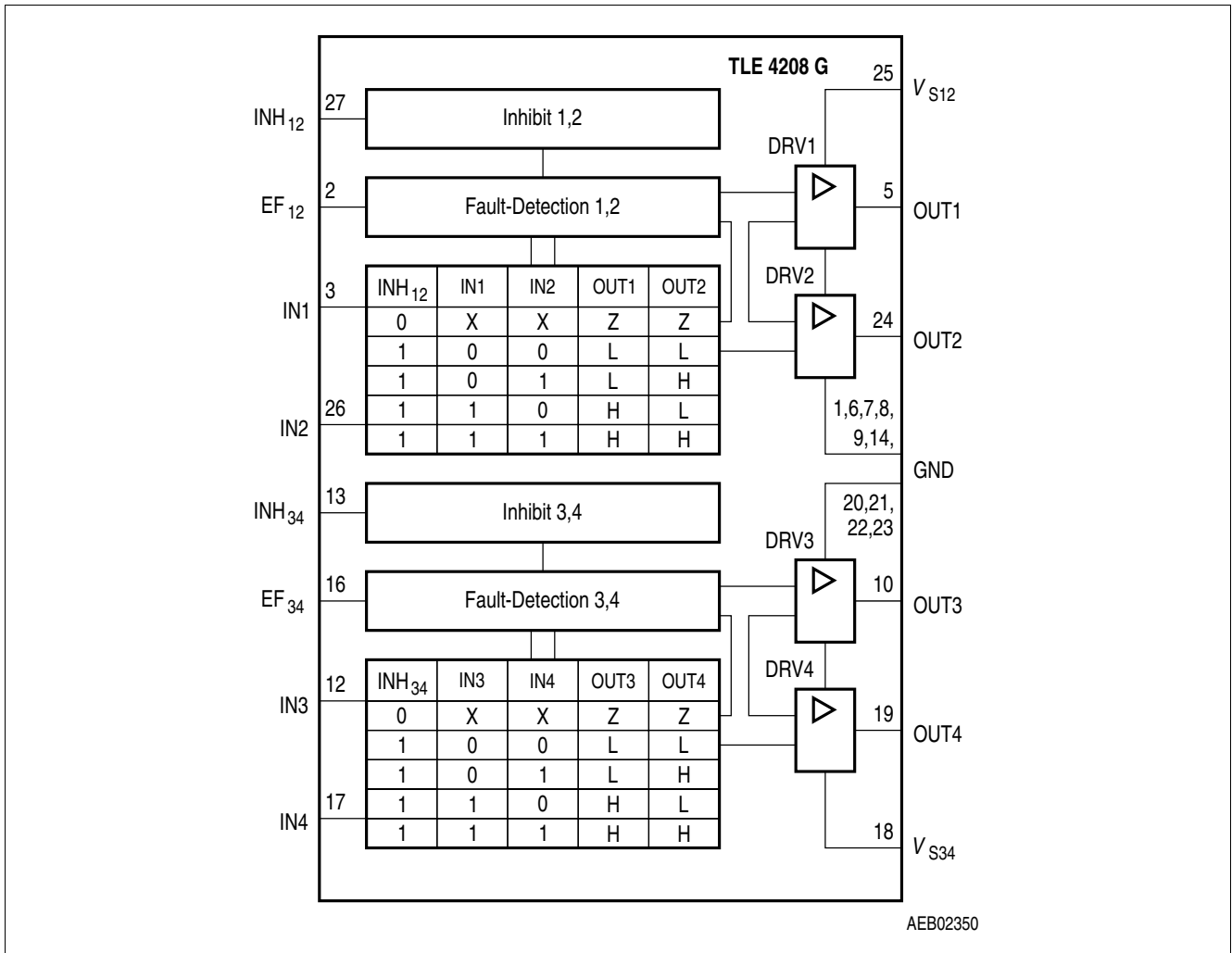


Figure 1 Block Diagram

Input Logic

Table 1 Functional Truth Table of Halfbridge 1 and 2

| INH ₁₂ | IN1 | IN2 | OUT1 | OUT2 | MODE |
|-------------------|-----|-----|------|------|----------|
| 0 | X | X | Z | Z | Stand-by |
| 1 | 0 | 0 | L | L | Brake LL |
| 1 | 0 | 1 | L | H | CW |
| 1 | 1 | 0 | H | L | CCW |
| 1 | 1 | 1 | H | H | Brake HH |

Note: Half-Bridge 1 and 2 connected to a full-bridge

Table 2 **Functional Truth Table of Halfbridge 3 and 4**

| INH ₃₄ | IN3 | IN4 | OUT3 | OUT4 | MODE |
|-------------------|-----|-----|------|------|----------|
| 0 | X | X | Z | Z | Stand-by |
| 1 | 0 | 0 | L | L | Brake LL |
| 1 | 0 | 1 | L | H | CW |
| 1 | 1 | 0 | H | L | CCW |
| 1 | 1 | 1 | H | H | Brake HH |

IN:

0 = Logic LOW

1 = Logic HIGH

X = Don't Care

OUT:

Z = Output in tristate condition

L = Output in sink condition

X = Output in source condition

Note: Half-Bridge 3 and 4 connected to a full-bridge

Table 3 **Diagnosis**

| EF ₁₂ | EF ₃₄ | Error |
|------------------|------------------|--|
| 1 | 1 | no error |
| 0 | 1 | over temperature of half-bridge 1 and 2 OR |
| 0 | 1 | over voltage of half-bridge 1 and 2 |
| 1 | 0 | over temperature of half-bridge 3 and 4 OR |
| 1 | 0 | over voltage of half-bridge 3 and 4 |
| 0 | 0 | over temperature of all half-bridges OR |
| 0 | 0 | over voltage of all half-bridge |

3 Pin Configuration

3.1 Pin Assignment

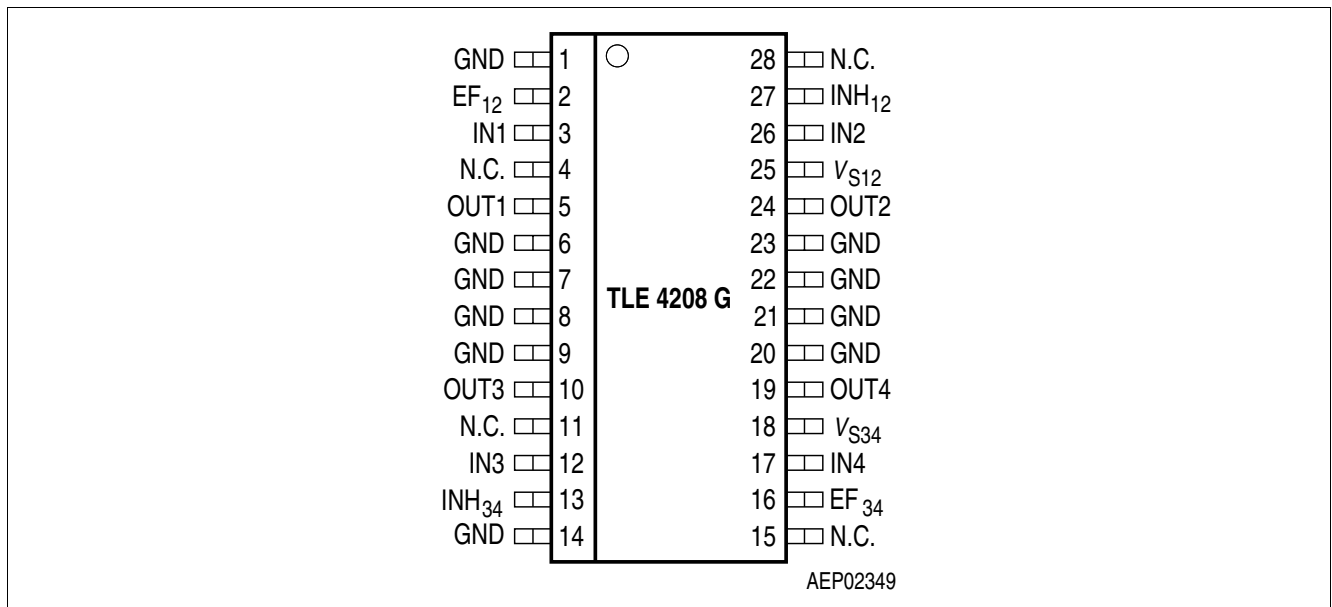


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

| Pin | Symbol | Function |
|-----------------------------------|-------------------|--|
| 1, 6, 7, 8, 9, 14, 20, 21, 22, 23 | GND | Ground ; negative reference potential for blocking capacitor |
| 2 | EF ₁₂ | Error Flag output of half-bridges 1 and 2 ; open collector; low = error |
| 3 | IN1 | Input channel of half-bridge 1 ; controls OUT 1 |
| 4, 11, 15, 28 | N.C. | Not Connected |
| 5 | OUT 1 | Power output of half-bridge 1 ; short circuit protected; with integrated clamp diodes |
| 10 | OUT 3 | Power output of half-bridge 3 ; short circuit protected; with integrated clamp diodes |
| 12 | IN3 | Input channel of half-bridge 3 ; controls OUT 3 |
| 13 | INH ₃₄ | Inhibit input of half-bridges 3 and 4 ; low = half-bridges 3 and 4 in stand-by |

Pin Configuration

| Pin | Symbol | Function |
|-----|-------------------|---|
| 16 | EF ₃₄ | Error Flag output of half-bridges 3 and 4; open collector; low = error |
| 17 | IN4 | Input channel of half-bridge 4; controls OUT 4 |
| 18 | V _{S34} | Power supply voltage of half-bridges 3 and 4; positive reference potential for blocking capacitor |
| 19 | OUT 4 | Power output of half-bridge 4; short circuit protected; with integrated clamp diodes |
| 24 | OUT 2 | Power-output of half-bridge 2; short circuit protected; with integrated clamp diodes |
| 25 | V _{S12} | Power supply voltage of half-bridges 1 and 2; positive reference potential for blocking capacitor |
| 26 | IN4 | Input channel of half-bridge 4; controls OUT 2 |
| 27 | INH ₁₂ | Inhibit input of half-bridges 1 and 2; low = half-bridges 1 and 2 in stand-by |

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 4 Absolute Maximum Ratings

$T_j = -40^\circ\text{C}$ to $+150^\circ\text{C}$; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|----------------------|--------|------|------|------|--|
| | | Min. | Typ. | Max. | | |
| Voltages | | | | | | |
| Supply Voltage | V_{S12}, V_{S34} | -0.3 | – | 45 | V | – |
| Supply Voltage | V_{S12}, V_{S34} | -1 | – | – | V | $t < 0.5\text{s}$; $I_{S12}, I_{S34} > -2\text{A}$ |
| Logic input voltages (IN1; IN2; INH ₁₂ ; IN3; IN4; INH ₃₄) | V_I | -5 | – | 20 | V | $0\text{V} < V_{S12}, V_{S34} < 45\text{V}$ |
| Logic output voltage (EF ₁₂ ; EF ₃₄) | V_{EF12}, V_{EF34} | -0.3 | – | 20 | V | $0\text{V} < V_{S12}, V_{S34} < 45\text{V}$ |
| Currents | | | | | | |
| Output Current (cont.) | I_{OUT1-4} | – | – | – | A | internally limited |
| Output Current (peak) | I_{OUT1-4} | – | – | – | A | internally limited |
| Output Current (diode) | I_{OUT1-4} | -1 | – | 1 | A | – |
| Output Current (EF) | $I_{EF12-34}$ | -2 | – | 5 | mA | – |
| Temperatures | | | | | | |
| Junction Temperature | T_j | -40 | – | 150 | °C | – |
| Storage Temperature | T_{stg} | -50 | – | 150 | °C | – |
| Thermal Resistances | | | | | | |
| Junction pin | $R_{thj-pin}$ | – | – | 25 | K/W | measured to pin 7 |
| Junction ambient | R_{thjA} | – | – | 65 | kV | – |

Notes

1. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Table 5 Functional Range

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|--------------------|---------------|------|---------------|------------|--|
| | | Min. | Typ. | Max. | | |
| Supply Voltage | V_{S12}, V_{S34} | V_{UV_OFF} | – | 18 | V | After V_{S12}, V_{S34} rising above V_{UV_ON} |
| Extended Supply Voltage Range for Operation | V_{S12}, V_{S34} | -0.3 | – | V_{UV_ON} | V | Outputs in tristate |
| Supply Voltage transients slew rate | V_{S12}, V_{S34} | -0.3 | – | V_{UV_OFF} | V/ μ s | Outputs in tristate |
| Logic input voltages (IN1; IN2; INH12; IN3; IN4; INH34) | V_I | -2 | – | 18 | V | – |
| Junction Temperature | T_j | -40 | – | 150 | °C | – |

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

4.3 General Electrical Characteristics

4.3.1 Electrical Characteristics

Table 6 Electrical Characteristics

$V_{S12} = V_{S34} = 8\text{ V to }18\text{ V}$, $INH_{12} = INH_{34} = \text{HIGH}$; $I_{OUT1-4} = 0\text{A}$; $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|-----------|--------|--------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |

Current Consumption

$INH_{12} = INH_{34} = \text{LOW}$

| | | | | | | |
|-------------------|-------|---|----|-----|---------------|---|
| Quiescent current | I_S | – | – | 100 | μA | $I_S = I_{S12} + I_{S34}$ |
| Quiescent current | I_S | – | 20 | 40 | μA | $I_S = I_{S12} + I_{S34}$; $V_{S12} = V_{S34} = 13.2\text{V}$; $T_j = 25^\circ\text{C}$ |

$INH_{12} = \text{HIGH}$ and $INH_{34} = \text{LOW}$ or $INH_{12} = \text{LOW}$ and $INH_{34} = \text{HIGH}$

| | | | | | | |
|----------------|--------------------|---|----|----|-------------|---|
| Supply current | I_{S12}, I_{S34} | – | 10 | 20 | mA | – |
| Supply current | I_{S12}, I_{S34} | – | – | 30 | mA | $I_{OUT1/3} = 0.4\text{A}$ $I_{OUT2/4} = -0.4\text{A}$ |
| Supply current | I_{S12}, I_{S34} | – | – | 50 | mA | $I_{OUT1/3} = 0.8\text{A}$ $I_{OUT2/4} = -0.8\text{A}$ |

Over- and Under Voltage Lockout

| | | | | | | |
|-----------------------|---------------|----|------|-----|------------|-------------------------------|
| UV Switch ON voltage | $V_{UV\ ON}$ | – | 6.5 | 7.5 | V | V_{S12}, V_{S34} increasing |
| UV Switch OFF voltage | $V_{UV\ OFF}$ | 5 | 6 | – | V | V_{S12}, V_{S34} decreasing |
| UV ON/ OFF hysteresis | $V_{UV\ HY}$ | – | 0.5 | – | V | $V_{UV\ ON} - V_{UV\ OFF}$ |
| OV Switch OFF voltage | $V_{OV\ OFF}$ | – | 20 | 24 | V | V_{S12}, V_{S34} increasing |
| OV Switch ON voltage | $V_{OV\ ON}$ | 18 | 19.5 | – | V | V_{S12}, V_{S34} decreasing |
| OV ON/ OFF hysteresis | $V_{OV\ HY}$ | – | 0.5 | – | V | $V_{OV\ OFF} - V_{OV\ ON}$ |

Outputs OUT1; OUT2; OUT3; OUT4

Saturation Voltages

| | | | | | | |
|--|--------------|---|------|------|------------|--------------------------|
| Source (upper) $I_{OUT12}, I_{OUT34} = -0.2\text{ A}$ | V_{SAT_U} | – | 0.85 | 1.15 | V | $T_j = 25^\circ\text{C}$ |
| Source (upper) $I_{OUT12}, I_{OUT34} = -0.4\text{ A}$ | V_{SAT_U} | – | 0.90 | 1.20 | V | $T_j = 25^\circ\text{C}$ |
| Sink (upper) $I_{OUT12}, I_{OUT34} = -0.8\text{ A}$ | V_{SAT_U} | – | 1.10 | 1.50 | V | $T_j = 25^\circ\text{C}$ |
| Sink (lower) $I_{OUT12}, I_{OUT34} = 0.2\text{ A}$ | V_{SAT_L} | – | 0.15 | 0.23 | V | $T_j = 25^\circ\text{C}$ |
| Sink (lower) $I_{OUT12}, I_{OUT34} = 0.4\text{ A}$ | V_{SAT_L} | – | 0.25 | 0.40 | V | $T_j = 25^\circ\text{C}$ |
| Sink (lower) $I_{OUT12}, I_{OUT34} = 0.8\text{ A}$ | V_{SAT_L} | – | 0.45 | 0.75 | V | $T_j = 25^\circ\text{C}$ |

| | | | | | | |
|--|-----------|---|---|-----|------------|-------------------------------------|
| Total Drop $I_{OUT12}, I_{OUT34} = 0.2\text{ A}$ | V_{SAT} | – | 1 | 1.4 | V | $V_{SAT} = V_{SAT_U} + V_{SAT_L}$ |
|--|-----------|---|---|-----|------------|-------------------------------------|

Table 6 Electrical Characteristics
 $V_{S12} = V_{S34} = 8\text{ V to }18\text{ V}$, $INH_{12} = INH_{34} = \text{HIGH}$; $I_{OUT1-4} = 0\text{ A}$; $T_j = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|------------|--------|------|------|------------------|-------------------------------------|
| | | Min. | Typ. | Max. | | |
| Total Drop $I_{OUT12}, I_{OUT34} = 0.4\text{ A}$ | V_{SAT} | – | 1.2 | 1.7 | V | $V_{SAT} = V_{SAT_U} + V_{SAT_L}$ |
| Total Drop $I_{OUT12}, I_{OUT34} = 0.8\text{ A}$ | V_{SAT} | – | 1.6 | 2.5 | V | $V_{SAT} = V_{SAT_U} + V_{SAT_L}$ |
| Clamp Diodes | | | | | | |
| Forward voltage; upper | V_{FU} | – | 1 | 1.5 | V | $I_F = 0.4\text{ A}$ |
| Upper leakage current | I_{LKU} | – | – | 5 | mA | $I_F = 0.4\text{ A}^{1)}$ |
| Forward voltage; lower | V_{FL} | – | 0.9 | 1.4 | V | $I_F = 0.4\text{ A}$ |
| Input Interface | | | | | | |
| Logic Inputs IN1; IN2; IN3; IN4 | | | | | | |
| H-input voltage | V_{IH} | – | 2.0 | 3.0 | V | – |
| L-input voltage | V_{IL} | 1.0 | 1.5 | – | V | – |
| Hysteresis of input voltage | V_{IHY} | – | 0.5 | – | V | – |
| H-input current | I_{IH} | -2 | – | 10 | μA | $V_I = 5\text{ V}$ |
| L-input current | I_{IL} | -100 | -20 | -5 | μA | $V_I = 0\text{ V}$ |
| Logic Inputs INH₁₂; INH₃₄ | | | | | | |
| H-input voltage | V_{IH} | – | 2.7 | 3.5 | V | – |
| L-input voltage | V_{IL} | 1.0 | 2.0 | – | V | – |
| Hysteresis of input voltage | V_{IHY} | – | 0.7 | – | V | – |
| H-input current | I_{IH} | – | 100 | 250 | μA | $V_{INH} = 5\text{ V}$ |
| L-input current | I_{IL} | -10 | – | 10 | μA | $V_{INH} = 0\text{ V}$ |
| Error Flags EF₁₂; EF₃₄ | | | | | | |
| L-output voltage level | V_{EFL} | – | 0.2 | 0.4 | V | $I_{EF} = 2\text{ mA}$ |
| Leakage current | I_{EFLK} | – | – | 10 | μA | $0\text{ V} < V_{EF} < 7\text{ V}$ |
| Thermal Shutdown | | | | | | |
| Thermal shutdown junction temperature | T_{jSD} | 150 | 175 | 200 | $^\circ\text{C}$ | – |
| Thermal switch-on junction temperature | T_{jSO} | 120 | – | 170 | $^\circ\text{C}$ | – |
| Temperature hysteresis | ΔT | – | 30 | – | K | – |

1) Not subject to production test, specified by design

5 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

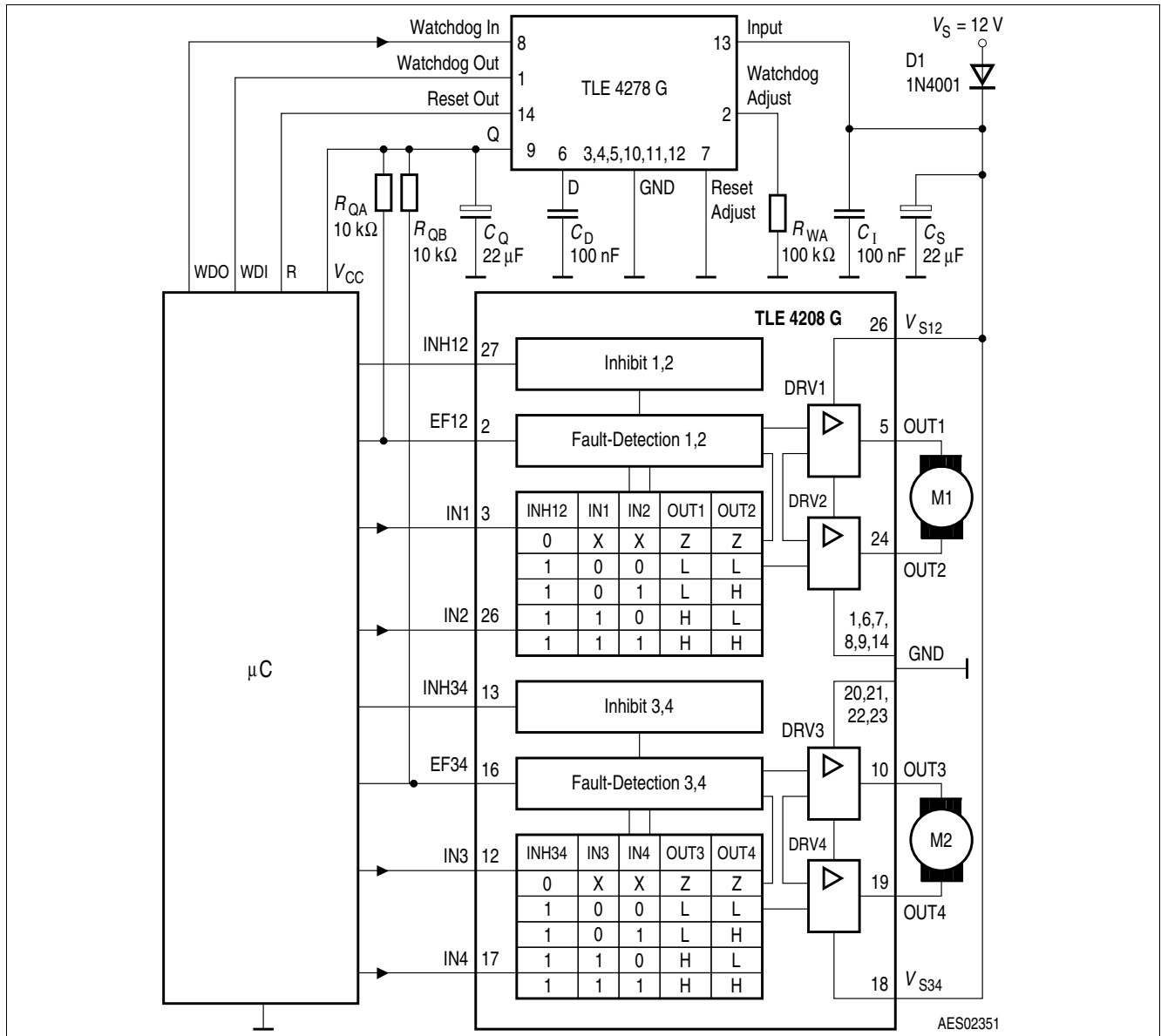
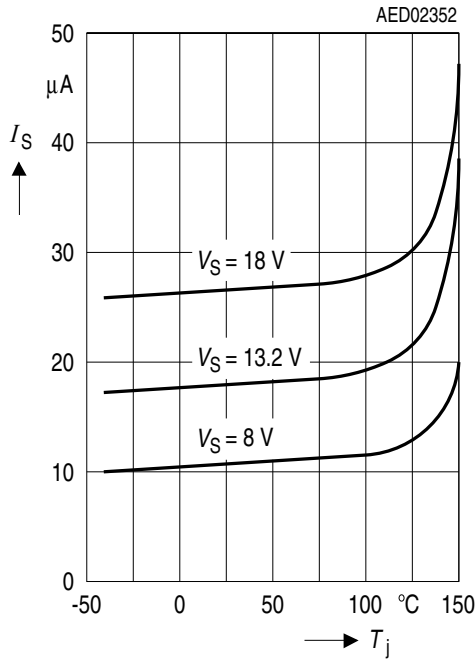


Figure 3 Application Circuit 1 (Device is used as Dual-Full-Bridge-Driver)

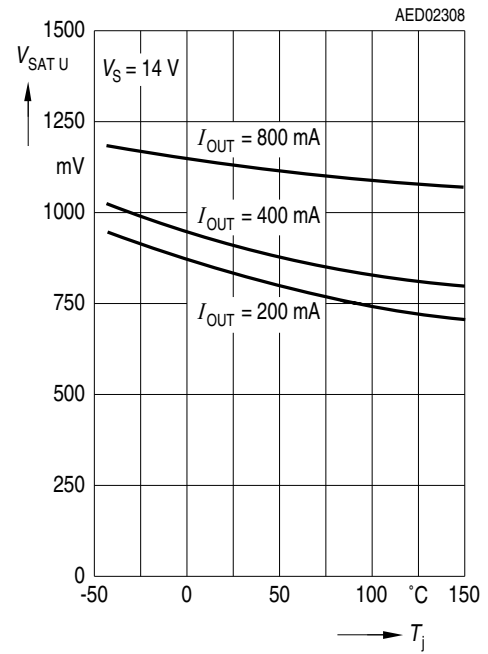
Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

Diagrams

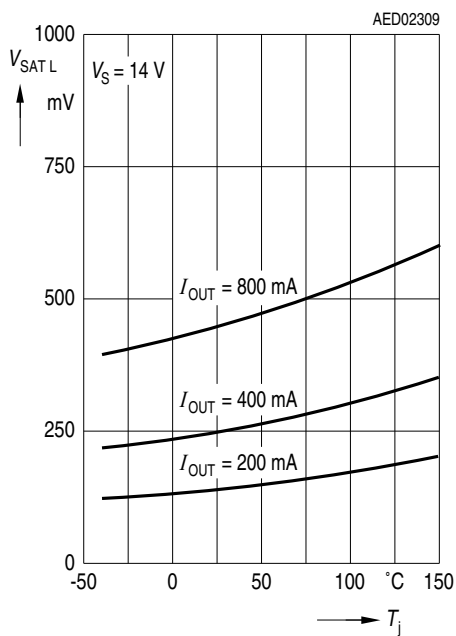
Quiescent current I_S over Temperature



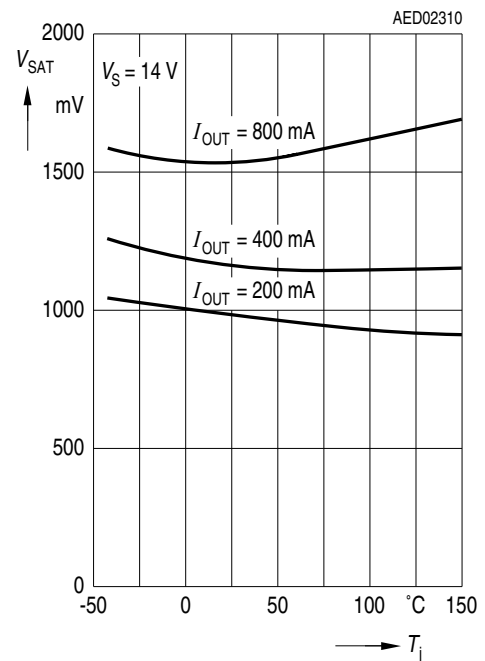
Saturation Voltage of Source $V_{SAT U}$ over Temperature



Saturation Voltage of Sink $V_{SAT L}$ over Temperature



Total Drop at outputs V_{SAT} over Temperature



6 Package Outlines

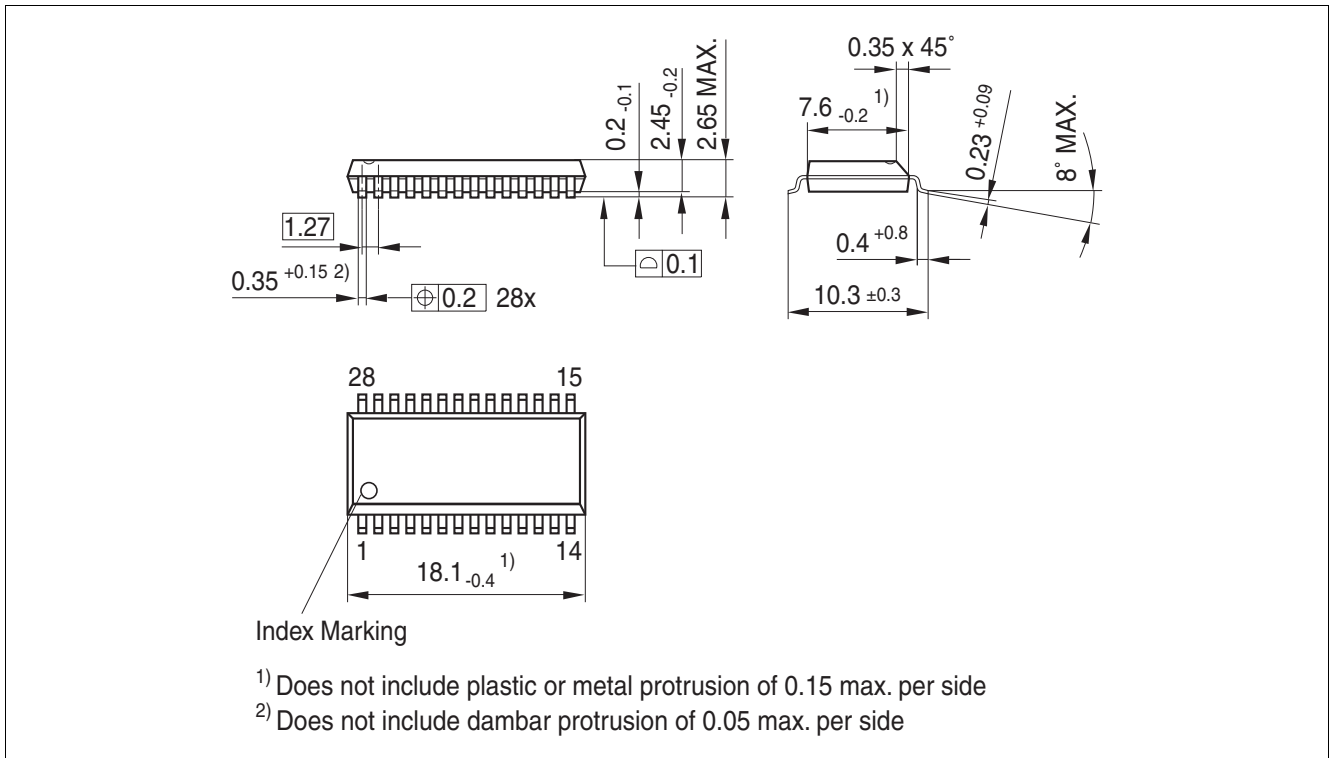


Figure 4 PG-DSO-28

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

7 Revision History

| Revision | Date | Changes |
|----------|------------|--|
| Rev. 1.4 | 2016-02-02 | Correction of typographical errors Page 10: VOFF_OFF and VOFF_ON are inverted. No change of the device behavior. Page 10,11: VS1, respectively VS2, renamed VS12 and VS34 |
| Rev. 1.3 | 2014-02-12 | Updated package designation and to latest data sheet formatting |
| Rev. 1.2 | 2011-04-11 | Updated package designation to reflect various production sites. |
| Rev. 1.1 | 2008-02-04 | Initial version of RoHS-compliant derivate of TLE4208G Page 1: added AEC certified statement Page 1 and 13: added RoHS compliance statement and Green product feature Page 1 and 3: Editorial change: deleted "fully" (The term "fully protected" often leads to misunderstandings as it is unclear with respect to which parameters). Page 1 and 14: Package changed to RoHS compliant version Page 15: added Revision History, updated Legal Disclaimer |

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