1.5 GHz to 2.4 GHz RF Vector Modulator

Data Sheet **AD8341**

FEATURES

Cartesian amplitude and phase modulation
1.5 GHz to 2.4 GHz frequency range
Continuous magnitude control of −4.5 dB to −34.5 dB
Continuous phase control of 0° to 360°
Output third-order intercept 17.5 dBm
Output 1 dB compression point 8.5 dBm
Output noise floor −150.5 dBm/Hz @ full gain
Adjustable modulation bandwidth up to 230 MHz
Fast output power disable
4.75 V to 5.25 V single-supply voltage

APPLICATIONS

RF PA linearization/RF predistortion
Amplitude and phase modulation
Variable attenuators and phase shifters
CDMA2000, WCDMA, GSM/EDGE linear power amplifiers
Smart antennas

FUNCTIONAL BLOCK DIAGRAM

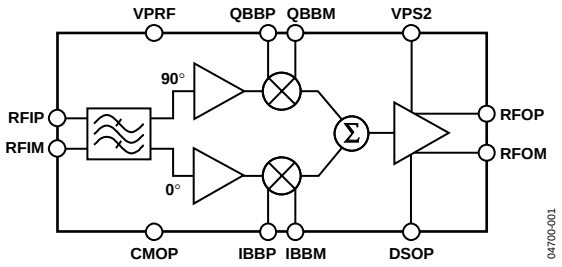


Figure 1.

GENERAL DESCRIPTION

The AD8341 vector modulator performs arbitrary amplitude and phase modulation of an RF signal. Since the RF signal path is linear, the original modulation is preserved. This part can be used as a general-purpose RF modulator, a variable attenuator/phase shifter, or a remodulator. The amplitude can be controlled from a maximum of −4.5 dB to less than −34.5 dB, and the phase can be shifted continuously over the entire 360° range. For maximum gain, the AD8341 delivers an OP1dB of 8.5 dBm, an OIP3 of 17.5 dBm, and an output noise floor of −150.5 dBm/Hz, independent of phase. It operates over a frequency range of 1.5 GHz to 2.4 GHz.

The baseband inputs in Cartesian I and Q format control the amplitude and phase modulation imposed on the RF input signal. Both I and Q inputs are dc-coupled with a ±500 mV differential full-scale range. The maximum modulation bandwidth is 230 MHz, which can be reduced by adding external capacitors to limit the noise bandwidth on the control lines.

Both the RF inputs and outputs can be used differentially or single-ended and must be ac-coupled. The RF input and output impedances are nominally 50 Ω over the operating frequency range. The DSOP pin allows the output stage to be disabled quickly in order to protect subsequent stages from overdrive. The AD8341 operates off supply voltages from 4.75 V to 5.25 V while consuming approximately 125 mA.

The AD8341 is fabricated on Analog Devices' proprietary, high performance 25 GHz SOI complementary bipolar IC process. It is available in a 24-lead, Pb-free LFCSP package and operates over a −40°C to +85°C temperature range. Evaluation boards are available.

Rev. A Document Feedback
Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **©2004–2012 Analog Devices, Inc. All rights reserved.**
Technical Support **www.analog.com**

TABLE OF CONTENTS

Specifications ... 3
Absolute Maximum Ratings ... 4
ESD Caution ... 4
Pin Configuration and Function Descriptions ... 5
Typical Performance Characteristics ... 6
Theory of Operation ... 10
RF Quadrature Generator ... 10
I-Q Attenuators and Baseband Amplifiers ... 11
Output Amplifier ... 11
Noise and Distortion ... 11
Gain and Phase Accuracy ... 11
RF Frequency Range ... 11
Applications ... 12
Using the AD8341 ... 12
RF Input and Matching ... 12
RF Output and Matching ... 13
Driving the I-Q Baseband Controls ... 13
Interfacing to High Speed DACs ... 14
CDMA2000 Application ... 14
WCDMA Application ... 15
Evaluation Board ... 17
Outline Dimensions ... 20
Ordering Guide ... 20

REVISION HISTORY

11/12—Rev. 0 to Rev. A

Changes to Figure 2 and Table 3 ... 5
Replaced Figure 42 and Figure 43 ... 19
Updated Outline Dimensions ... 20
Changes to Ordering Guide ... 20

7/04—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V, T_A = 25°C, Z_O = 50 Ω, f = 1.9 GHz, single-ended, ac-coupled source drive to RFIP through 1.2 nH series inductor, RFIM ac-coupled through 1.2 nH series inductor to common, differential-to-single-ended conversion at output using 1:1 balun.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
OVERALL FUNCTION					
Frequency Range		1.5		2.4	GHz
Maximum Gain	Maximum gain setpoint for all phase setpoints		−4.5		dB
Minimum Gain	$V_{BBI} = V_{BBQ}$ = 0 V differential (at recommended common-mode level)		−34.5		dB
Gain Control Range	Relative to maximum gain		30		dB
Phase Control Range	Over 30 dB control range		360		Degrees
Gain Flatness	Over any 60 MHz bandwidth		0.5		dB
Group Delay Flatness	Over any 60 MHz bandwidth		50		ps
RF INPUT STAGE	RFIM, RFIP (Pins 21 and 22)				
Input Return Loss	From RFIP to CMRF (with 1.2 nH series inductors)		12		dB
CARTESIAN CONTROL INTERFACE (I AND Q)	IBBP, IBBM, QBBP, QBBM (Pins 16, 15, 3, 4)				
Gain Scaling			2		1/V
Modulation Bandwidth	500 mV p-p, sinusoidal baseband input single-ended		230		MHz
Second Harmonic Distortion	500 mV p-p, 1 MHz, sinusoidal baseband input differential		41		dBc
Third Harmonic Distortion	500 mV p-p, 1 MHz, sinusoidal baseband input differential		47		dBc
Step Response	For gain setpoint from 0.1 to 0.9 (V_{BBP} = 0.5 V, V_{BBM} = 0.55 V to 0.95 V)		45		ns
	For gain setpoint from 0.9 to 0.1 (V_{BBP} = 0.5 V, V_{BBM} = 0.95 V to 0.55 V)		45		ns
Recommended Common-Mode Level			0.5		V
RF OUTPUT STAGE	RFOP, RFOM (Pins 9, 10)				
Output Return Loss	Measured through balun		7.5		dB
f = 1.9 GHz					
Gain	Maximum gain setpoint		−4.5		dB
Output Noise Floor	Maximum gain setpoint, no input		−150.5		dBm/Hz
	P_{IN} = 0 dBm, frequency offset = 20 MHz		−149		dBm/Hz
Output IP3	f1 = 1900 MHz, f2 = 1897.5 MHz, maximum gain setpoint		17.5		dBm
Adjacent Channel Power	CDMA2000, single carrier, P_{OUT} = -4 dBm, maximum gain, phase setpoint = 45° (See Figure 35)		−76		dBm
Output 1 dB Compression Point	Maximum gain		8.5		dBm
POWER SUPPLY	VPS2 (Pins 5, 6, and 14), VPRF (Pins 19 and 24), RFOP, RFOM (Pins 9 and 10)				
Positive Supply Voltage		4.75	5	5.25	V
Total Supply Current	Includes load current	105	125	145	mA
OUTPUT DISABLE	DSOP (Pin 13)				
Disable Threshold	(See Figure 24)		$V_S/2$		V
Attenuation	DSOP = 5 V		33		dB
Enable Response Time	Delay following high-to-low transition until RF output amplitude is within 10% of final value.		30		ns
Disable Response Time	Delay following low-to-high transition until device produces full attenuation		15		ns

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameters	Rating
Supply Voltage VPRF, VPS2	5.5 V
DSOP	5.5 V
IBBP, IBBM, QBBP, QBBM	2.5 V
RFOP, RFOM	5.5V
RF Input Power at Maximum Gain (RFIP or RFIM, Single-Ended Drive) Equivalent Voltage	13 dBm, re: 50 Ω 2.8 V p-p
Internal Power Dissipation	825 mW
θ_{JA} (With Pad Soldered to Board)	59 °C/W
Maximum Junction Temperature	125°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering 60 sec)	300°C

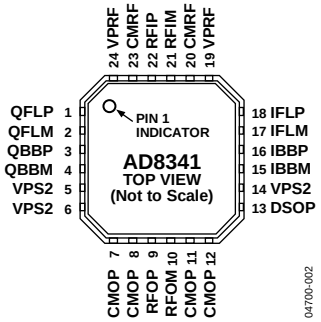
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PADDLE SHOULD BE SOLDERED TO A LOW IMPEDANCE GROUND PLANE.

Figure 2. 24-Lead Lead Frame Chip Scale Package (LFCSP)

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Function
1, 2	QFLP, QFLM	Q Baseband Input Filter Pins. Connect optional capacitor to reduce Q baseband channel low-pass corner frequency.
3, 4	QBBP, QBBM	Q Channel Differential Baseband Inputs.
5, 6, 14, 19, 24	VPS2, VPRF	Positive Supply Voltage. 4.75 V – 5.25 V.
7, 8, 11, 12, 20, 23	CMOP, CMRF	Device Common. Connect via lowest possible impedance to external circuit common.
9, 10	RFOP, RFOM	Differential RF Outputs. Must be ac-coupled. Differential impedance 50 Ω nominal.
13	DSOP	Output Disable. Pull high to disable output stage.
15, 16	IBBM, IBBP	I Channel Differential Baseband Inputs.
17, 18	IFLM, IFLP	I Baseband Input Filter Pins. Connect optional capacitor to reduce I baseband channel low-pass corner frequency.
21, 22	RFIM, RFIP	Differential RF Inputs. Must be ac-coupled. Differential impedance 50 Ω nominal.
	EP	Exposed Paddle. The exposed paddle should be soldered to a low impedance ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

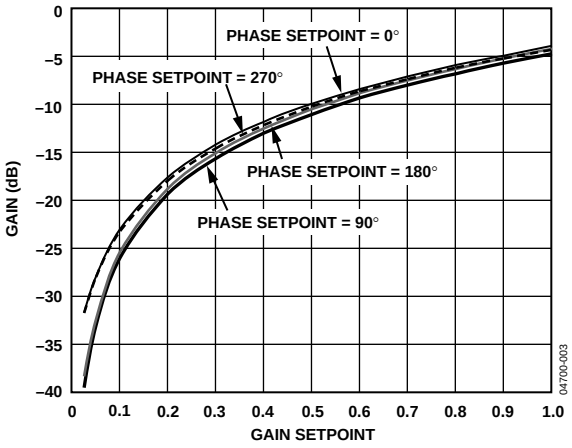


Figure 3. Gain Magnitude vs. Gain Setpoint at Different Phase Setpoints, RF Frequency = 1900 MHz

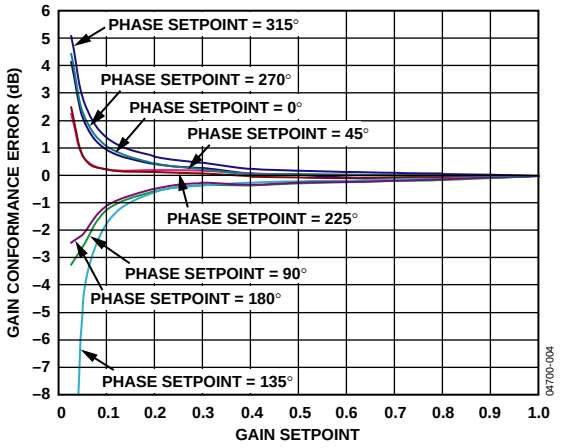


Figure 4. Gain Conformance Error vs. Gain Setpoint at Different Phase Setpoints, RF Frequency = 1900 MHz

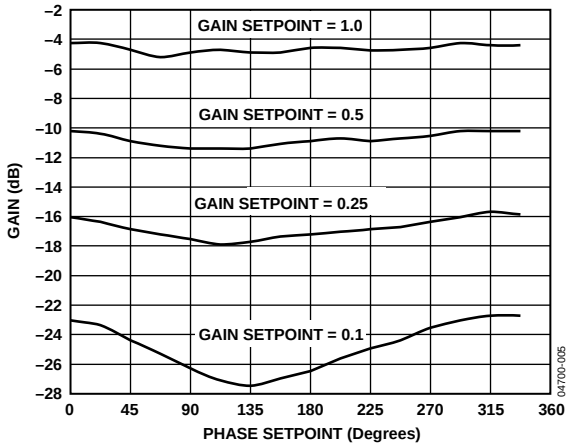


Figure 5. Gain Magnitude vs. Phase Setpoint at Different Gain Setpoints, RF Frequency = 1900 MHz

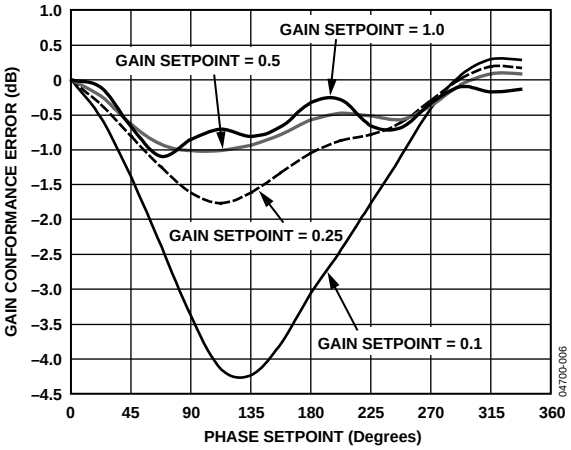


Figure 6. Gain Conformance Error vs. Phase Setpoint at Different Gain Setpoints, RF Frequency = 1900 MHz

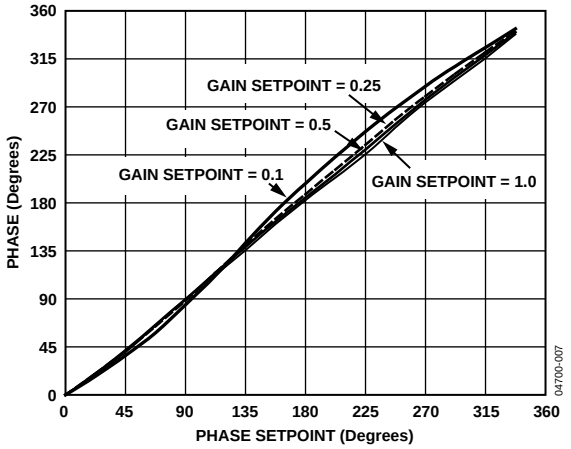


Figure 7. Phase vs. Phase Setpoint at Different Gain Setpoints, RF Frequency = 1900 MHz

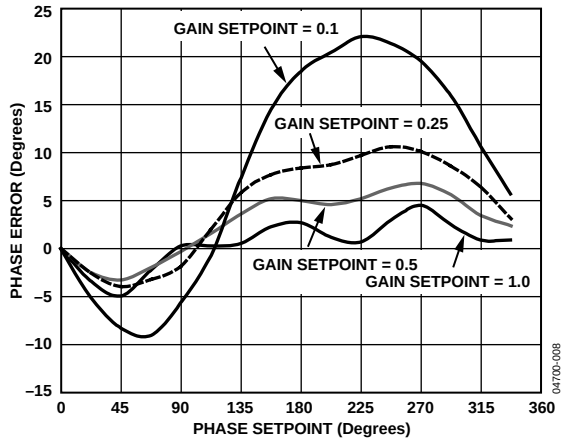


Figure 8. Phase Error vs. Phase Setpoint at Different Gain Setpoints, RF Frequency = 1900 MHz

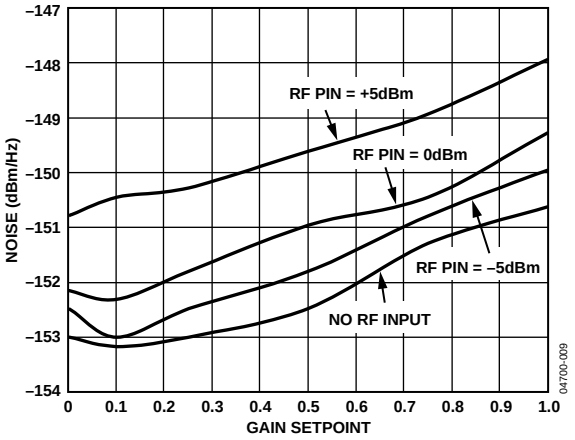


Figure 9. Output Noise Floor vs. Gain Setpoint, Noise in dBm/Hz, No Carrier, and With 1900 MHz Carrier (Measured at 20 MHz Offset) Pin = –5, 0, and +5 dBm

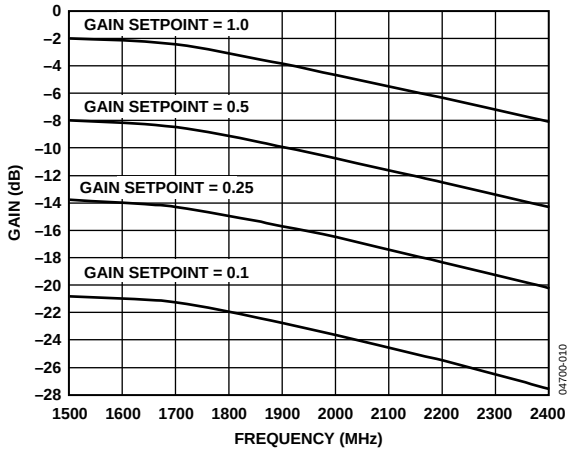


Figure 10. Gain vs. Frequency at Different Gain Setpoints, Phase Setpoint = 0°

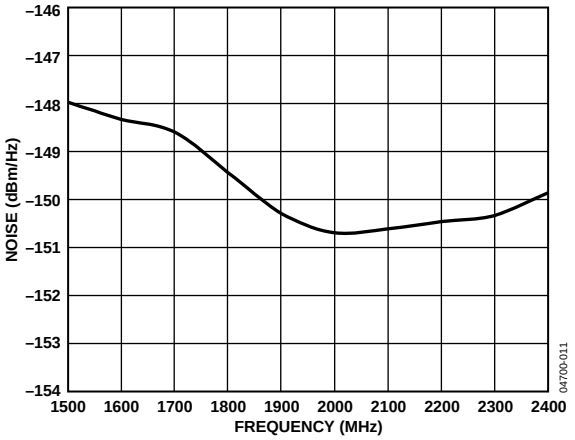


Figure 11. Output Noise Floor vs. Frequency, Maximum Gain, No RF Carrier, Phase Setpoint = 0°

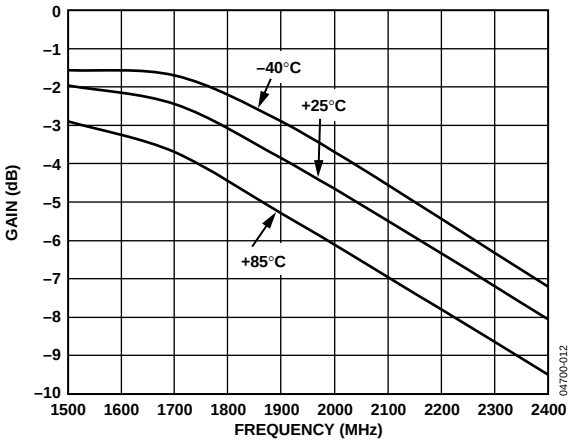


Figure 12. Gain Magnitude vs. Frequency and Temperature, Maximum Gain, Phase Setpoint = 0°

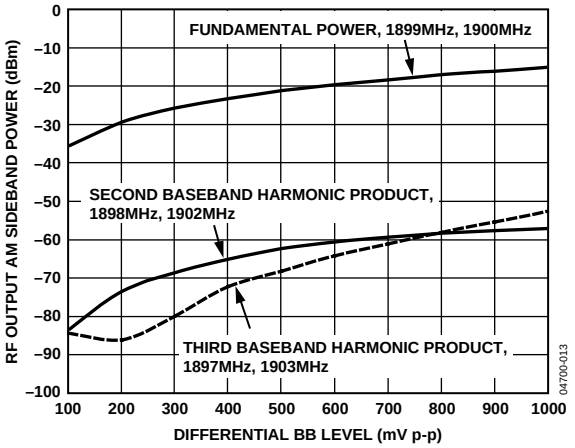


Figure 13. Baseband Harmonic Distortion (I and Q Channel, RF Input = 0 dBm, Output Balun and Cable Losses of Approximately 2 dB Not Accounted for in Plot)

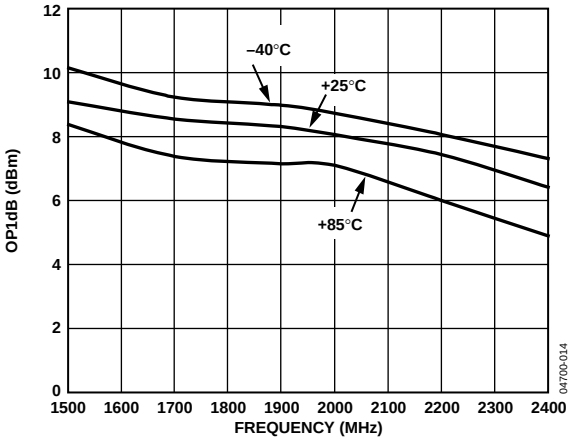


Figure 14. Output 1 dB Compression Point vs. Frequency and Temperature, Maximum Gain, Phase Setpoint = 0°

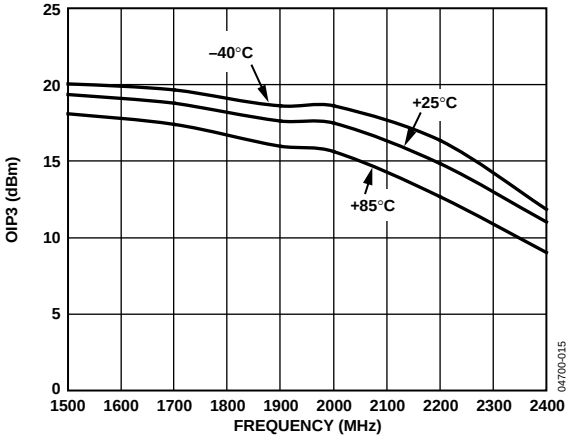


Figure 15. Output IP3 vs. Frequency and Temperature, Maximum Gain, Phase Setpoint = 0°, 2.5 MHz Carrier Spacing

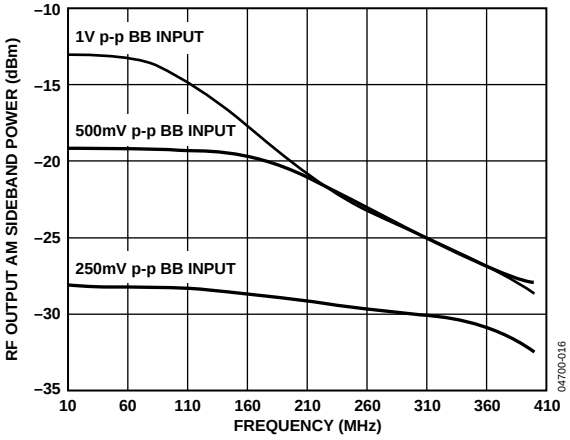


Figure 16. I/Q Modulation Bandwidth vs. Baseband Magnitude

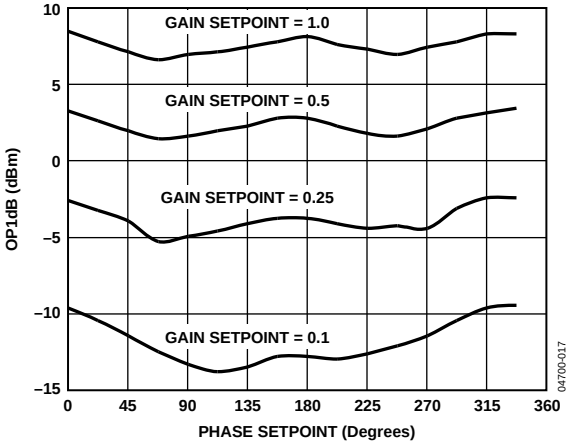


Figure 17. Output 1 dB Compression Point vs. Gain and Phase Setpoints, RF Frequency = 1900 MHz

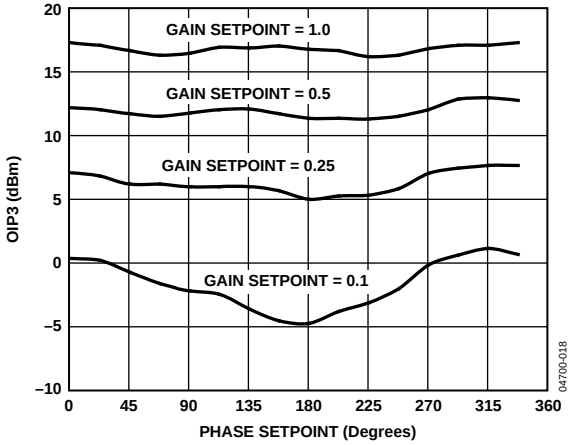


Figure 18. Output IP3 vs. Gain and Phase Setpoints, RF Frequency = 1900 MHz, 2.5 MHz Carrier Spacing

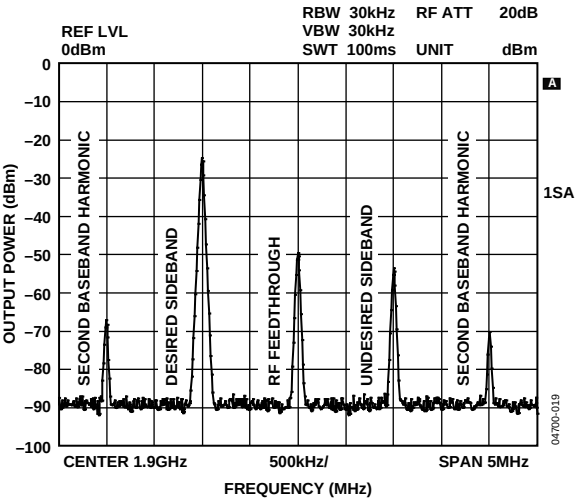


Figure 19. Single-Sideband Performance, RF Frequency = 1900 MHz, RF Input = –10 dBm; 1 MHz, 500 mV p-p Differential BB Drive

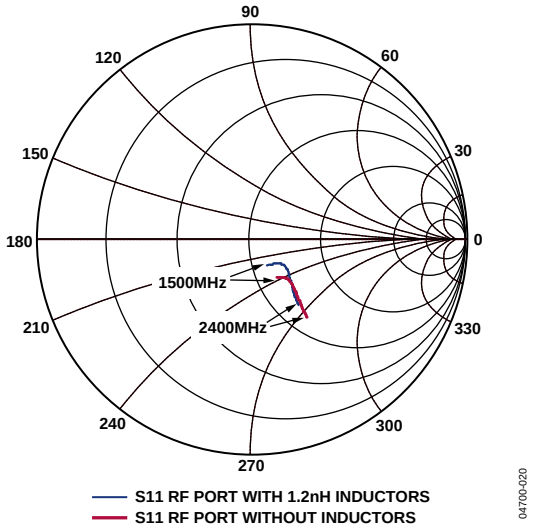


Figure 20. Input Impedance Smith Chart

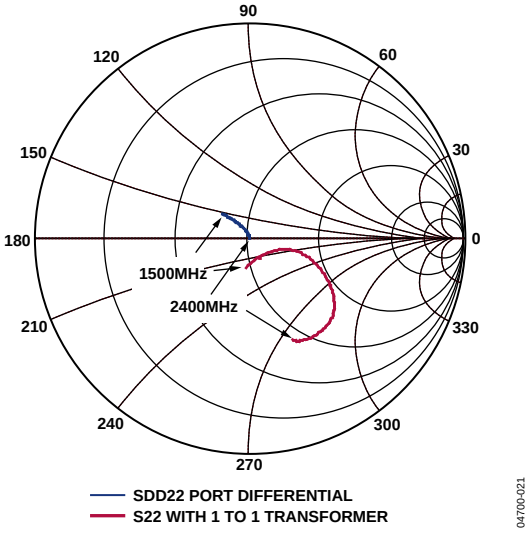


Figure 21. Output Impedance Smith Chart

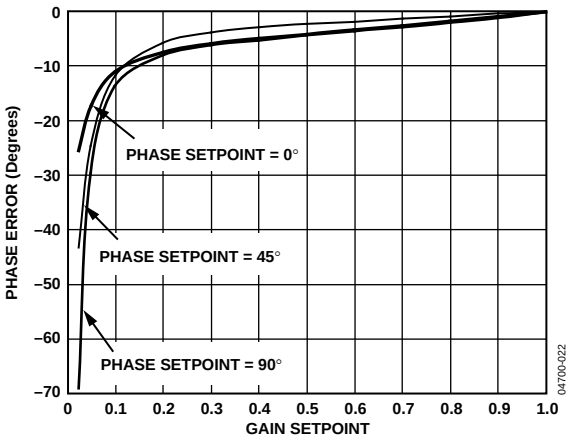


Figure 22. Phase Error vs. Gain Setpoint by Phase Setpoint, RF Frequency = 1900 MHz

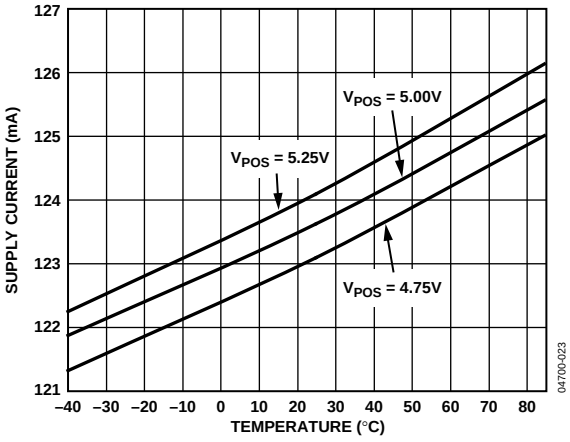


Figure 23. Supply Current vs. Temperature

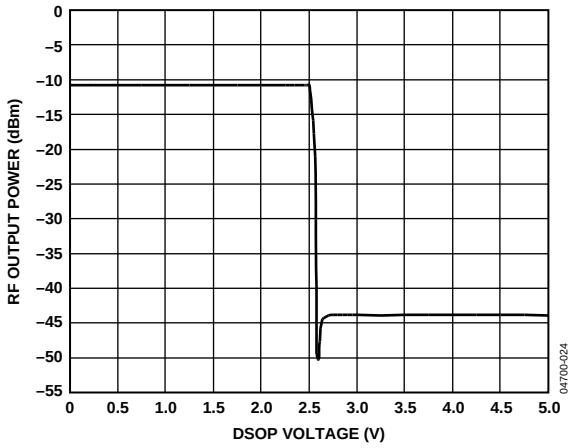


Figure 24. Output Disable Attenuation, RF Frequency = 1900 MHz, RF Input = –5 dBm

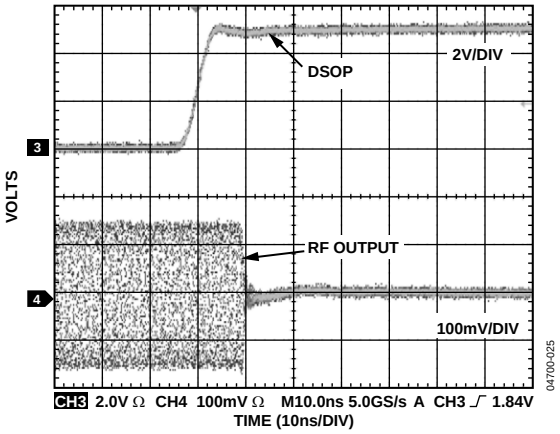


Figure 25. Output Disable Response Time, RF Frequency = 1900 MHz, RF Input = 0 dBm

THEORY OF OPERATION

The AD8341 is a linear RF vector modulator with Cartesian baseband controls. In the simplified block diagram given in Figure 26, the RF signal propagates from the left to the right while baseband controls are placed above and below. The RF input is first split into in-phase (I) and quadrature (Q) components. The variable attenuators independently scale the I and Q components of the RF input. The attenuator outputs are then summed and buffered to the output.

By controlling the relative amounts of I and Q components that are summed, continuous magnitude and phase control of the gain is possible. Consider the vector gain representation of the AD8341 expressed in polar form in Figure 27. The attenuation factors for the I and Q signal components are represented on the x- and y-axis, respectively, by the baseband inputs, V_{BBI} and V_{BBQ}. The resultant of their vector sum represents the vector gain, which can also be expressed as a magnitude and phase. By applying different combinations of baseband inputs, any vector gain within the unit circle can be programmed.

A change in sign of V_{BBI} or V_{BBQ} can be viewed as a change in sign of the gain or as a 180° phase change. The outermost circle represents the maximum gain magnitude of unity. The circle origin implies, in theory, a gain of 0. In practice, circuit mismatches and unavoidable signal feedthrough limit the minimum gain to approximately −34.5 dB. The phase angle between the resultant gain vector and the positive x-axis is defined as the phase shift. Note that there is a nominal, systematic insertion phase through the AD8341 to which the phase shift is added. In the following discussions, the systematic insertion phase is normalized to 0°.

The correspondence between the desired gain and phase setpoints, $Gain_{SP}$ and $Phase_{SP}$, and the Cartesian inputs, V_{BBI} and V_{BBQ}, is given by simple trigonometric identities

$$Gain_{SP} = \sqrt{\left[\left(V_{BBI}/V_O\right)^2 + \left(V_{BBQ}/V_O\right)^2\right]}$$

$$Phase_{SP} = \arctan\left(V_{BBQ}/V_{BBI}\right)$$

where:

V_O is the baseband scaling constant (500 mV).

V_{BBI} and V_{BBQ} are the differential I and Q baseband voltages, respectively.

Note that when evaluating the arctangent function, the proper phase quadrant must be selected. For example, if the principal value of the arctangent (known as the Arctangent(x)) is used, quadrants 2 and 3 could be interpreted mistakenly as quadrants 4 and 1, respectively. In general, both V_{BBI} and V_{BBQ} are needed in concert to modulate the gain and the phase.

Pure amplitude modulation is represented by radial movement of the gain vector tip at a fixed angle, while pure phase modulation is represented by rotation of the tip around the circle at a fixed radius. Unlike traditional I-Q modulators, the AD8341 is designed to have a linear RF signal path from input to output. Traditional I-Q modulators provide a limited LO carrier path through which any amplitude information is removed.

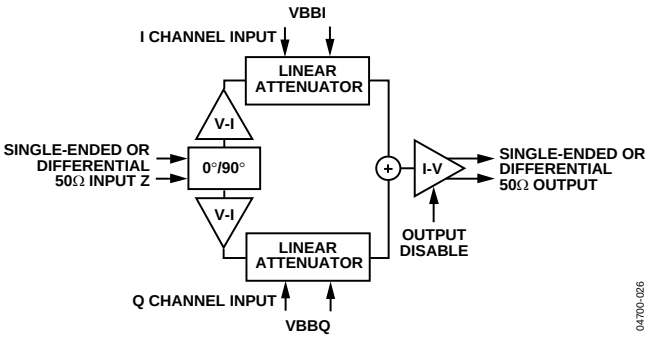


Figure 26. Simplified Architecture of the AD8341

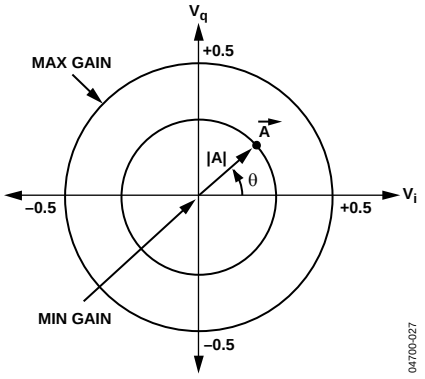


Figure 27. Vector Gain Representation

RF QUADRATURE GENERATOR

The RF input is directly coupled differentially or single-ended to the quadrature generator, which consists of a multistage RC polyphase network tuned over the operating frequency range of 1.5 GHz to 2.4 GHz. The recycling nature of the polyphase network generates two replicas of the input signal, which are in precise quadrature, i.e., 90°, to each other. Since the passive network is perfectly linear, the amplitude and phase information contained in the RF input is transmitted faithfully to both channels. The quadrature outputs are then separately buffered to drive the respective attenuators. The characteristic impedance of the polyphase network is used to set the input impedance of the AD8341.

I-Q ATTENUATORS AND BASEBAND AMPLIFIERS

The proprietary linear-responding attenuator structure is an active solution with differential inputs and outputs that offer excellent linearity, low noise, and greater immunity from mismatches than other variable attenuator methods. The gain, in linear terms, of the I and Q channels is proportional to its control voltage with a scaling factor designed to be 2/V, i.e., a full-scale gain setpoint of 1.0 (−4.5 dB) for a V_{BBI} (or a V_{BBQ}) of 500 mV. The control voltages can be driven differentially or single-ended. The combination of the baseband amplifiers and attenuators allows for maximum modulation bandwidths in excess of 200 MHz.

OUTPUT AMPLIFIER

The output amplifier accepts the sum of the attenuator outputs and delivers a differential output signal into the external load. The output pins must be pulled up to an external supply, preferably through RF chokes. When the 50 Ω load is taken differentially, an output P1dB and IP3 of 8.5 dBm and 17.5 dBm is achieved, respectively, at 1.9 GHz. The output can be taken in single-ended fashion, albeit at lower performance levels.

NOISE AND DISTORTION

The output noise floor and distortion levels vary with the gain magnitude but do not vary significantly with the phase. At the higher gain magnitude setpoints, the OIP3 and the noise floor vary in direct proportion with the gain. At lower gain magnitude setpoints, the noise floor levels off while the OIP3 continues to vary with the gain.

GAIN AND PHASE ACCURACY

There are numerous ways to express the accuracy of the AD8341. Ideally, the gain and phase should precisely follow the setpoints. Figure 4 illustrates the gain error in dB from a best fit line, normalized to the gain measured at the gain setpoint = 1.0, for the different phase setpoints. Figure 6 shows the gain error in a different form, normalized to the gain measured at phase setpoint = 0°; the phase setpoint is swept from 0° to 360° for different gain setpoints. Figure 8 and Figure 22 show analogous errors for the phase error as a function of gain and phase setpoints. The accuracy clearly depends on the region of operation within the vector gain unit circle. Operation very close to the origin generally results in larger errors as the relative accuracy of the I and Q vectors degrades.

RF FREQUENCY RANGE

The frequency range on the RF input is limited by the internal polyphase quadrature phase-splitter. The phase-splitter splits the incoming RF input into two signals, 90° out of phase, as previously described in the RF Quadrature Generator section. This polyphase network has been designed to ensure robust quadrature accuracy over standard fabrication process parameter variations for the 1.5 GHz to 2.4 GHz specified RF frequency range. Using the AD8341 as a single-sideband modulator and measuring the resulting sideband suppression is a good gauge of how well the quadrature accuracy is maintained over RF frequency. A typical plot of sideband suppression from 1.1 GHz to 2.7 GHz is shown in Figure 28. The level of sideband suppression degradation outside the 1.5 GHz to 2.4 GHz specified range will be subject to manufacturing process variations.

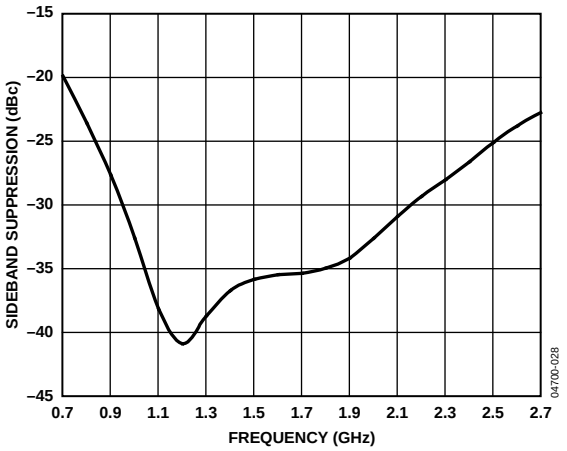


Figure 28. Sideband Suppression vs. Frequency

APPLICATIONS

USING THE AD8341

The AD8341 is designed to operate in a 50 Ω impedance system. Figure 30 illustrates an example where the RF input is driven in a single-ended fashion while the differential RF output is converted to a single-ended output with an RF balun. The baseband controls for the I and Q channels are typically driven from differential DAC outputs. The power supplies, VPRF and VPS2, should be bypassed appropriately with 0.1 µF and 100 pF capacitors. Low inductance grounding of the CMOP and CMRF common pins is essential to prevent unintentional peaking of the gain.

RF INPUT AND MATCHING

The input impedance of the AD8341 is defined by the characteristics of the polyphase network. The capacitive component of the network causes its impedance to roll-off with frequency albeit at a rate slower than 6 dB/octave. By using matching inductors on the order of 1.2 nH in series with each of the RF inputs, RFIP and RFIM, a 50 Ω match is achieved with a return loss of >10 dB over the operating frequency range. Different matching inductors can improve matching over a narrower frequency range. The single-ended and differential input impedances are exactly the same.

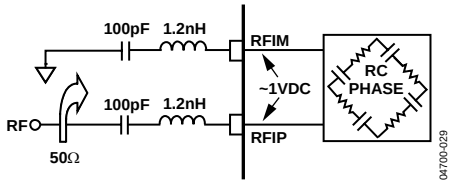


Figure 29. RF Input Interface to the AD8341 Showing Coupling Capacitors and Matching Inductors

The RFIP and RFIM should be ac-coupled through low loss series capacitors as shown in Figure 29. The internal dc levels are at approximately 1 V. For single-ended operation, one input is driven by the RF signal while the other input is ac grounded.

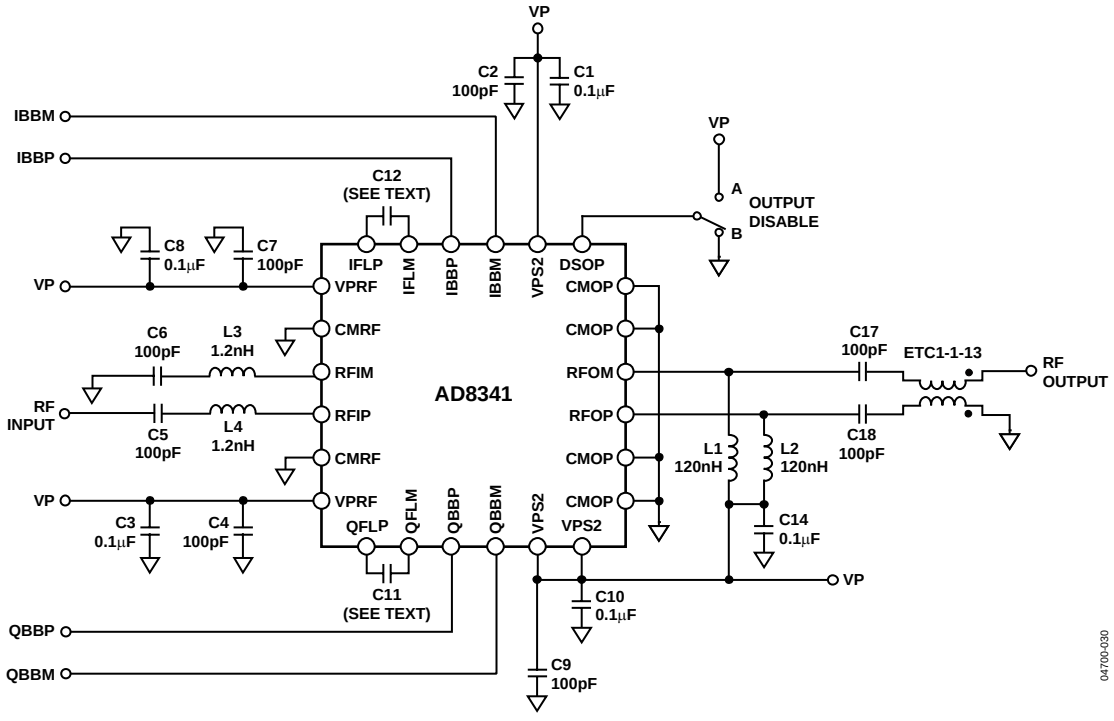


Figure 30. Basic Connections

RF OUTPUT AND MATCHING

The RF outputs of the AD8341, RFOP, and RFOM, are open collectors of a transimpedance amplifier which need to be pulled up to the positive supply, preferably with RF chokes as shown in Figure 31. The nominal output impedance looking into each individual output pin is 25 Ω. Consequently, the differential output impedance is 50 Ω.

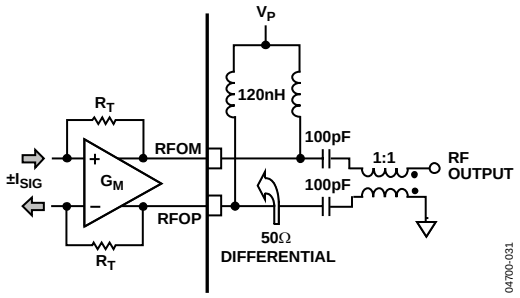


Figure 31. RF Output Interface to the AD8341 Showing Coupling Capacitors, Pull-Up RF Chokes, and Balun

Since the output dc levels are at the positive supply, ac coupling capacitors will usually be needed between the AD8341 outputs and the next stage in the system.

A 1:1 RF broadband output balun, such as the ETC1-1-13 (M/A-COM), converts the differential output of the AD8341 into a single-ended signal. Note that the loss and balance of the balun directly impact the apparent output power, noise floor, and gain/phase errors of the AD8341. In critical applications, narrow-band baluns with low loss and superior balance are recommended.

If the output is taken in a single-ended fashion directly into a 50 Ω load through a coupling capacitor, there will be an impedance mismatch. This can be resolved with a 1:2 balun to convert the single-ended 25 Ω output impedance to 50 Ω. If loss of signal swing is not critical, a 25 Ω back termination in series with the output pin can also be used. The unused output pin must still be pulled up to the positive supply. The user may load it through a coupling capacitor with a dummy load to preserve balance. The gain of the AD8341 when the output is single-ended varies slightly with dummy load value as shown in Figure 32.

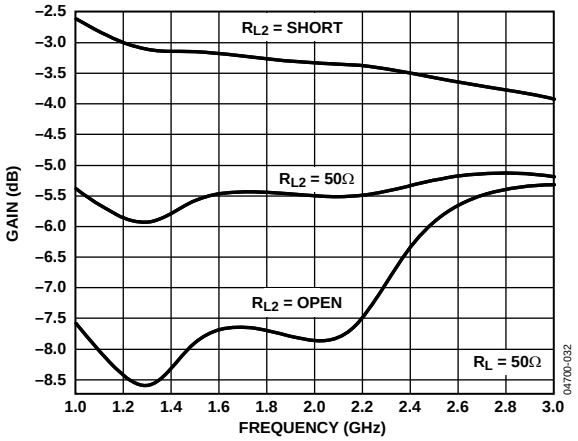


Figure 32. Gain of the AD8341 Using a Single-Ended Output with Different Dummy Loads, R_{L2}, on the Unused Output

The RF output signal can be disabled by raising the DSOP pin to the positive supply. The output disable function provides >30 dB attenuation of the input signal even at full gain. The interface to DSOP is high impedance and the shutdown and turn-on response times are <100 ns. If the disable function is not needed, the DSOP pin should be tied to ground.

DRIVING THE I-Q BASEBAND CONTROLS

The I and Q inputs to the AD8341 set the gain and phase between input and output. These inputs are differential and should normally have a common-mode level of 0.5 V. However, when differentially driven, the common mode can vary from 250 mV to 750 mV while still allowing full gain control. Each input pair has a nominal input swing of ±0.5 V differential around the common-mode level. The maximum gain of unity is achieved if the differential voltage is equal to +500 mV or −500 mV. So with a common-mode level of 500 mV, IBBP and IBBM will each swing between 250 mV and 750 mV.

The I and Q inputs can also be driven with a single-ended signal. In this case, one side of each input should be tied to a low noise 0.5 V voltage source (a 0.1 µF decoupling capacitor located close to the pin is recommended), while the other input swings from 0 V to 1 V. Differential drive generally offers superior even-order distortion and lower noise than single-ended drive.

The bandwidth of the baseband controls exceeds 200 MHz even at full-scale baseband drive. This allows for very fast gain and phase modulation of the RF input signal. In cases where lower modulation bandwidths are acceptable or desired, external filter capacitors can be connected across Pins IFLP to IFLM and QFLP to QFLM to reduce the ingress of baseband noise and spurious signal into the control path.

The 3 dB bandwidth is set by choosing C_{FLT} according to the following equation:

$$f_{3dB} \approx \frac{45\ \text{kHz} \times 10\ \text{nF}}{C_{FLT} + 0.5\ \text{pF}}$$

This equation has been verified for values of C_{FLT} from 10 pF to 0.1 µF (bandwidth settings of approximately 4.5 kHz to 43 MHz).

INTERFACING TO HIGH SPEED DACs

The AD977x family of dual DACs is well suited to driving the I and Q vector controls of the AD8341. While these inputs can in general be driven by any DAC, the differential outputs and bias level of the ADI TxDAC® family allows for a direct connection between DAC and modulator.

The AD977x family of dual DACs has differential current outputs. The full-scale current is user programmable and is usually set to 20 mA, that is, each output swings from 0 mA to 20 mA.

The basic interface between the AD9777 DAC outputs and the AD8341 I and Q inputs is shown in Figure 33. The Resistors R1 and R2 set the dc bias level according to the equation:

Bias Level = Average Output Current × R1

For example, if the full-scale current from each output is 20 mA, each output will have an average current of 10 mA. Therefore to set the bias level to the recommended 0.5 V, R1 and R2 should be set to 50 Ω each. R1 and R2 should always be equal.

If R3 is omitted, this will result in an available swing from the DAC of 2 V p-p differential, which is twice the maximum voltage range required by the AD8341. DAC resolution can be maximized by adding R3, which scales down this voltage according to the following equation:

Full Scale Swing =

$$2 \times I_{MAX}\left(R1 \,||\, (R2+R3)\right) \times \left[1 - \frac{R2}{R2+R3}\right]$$

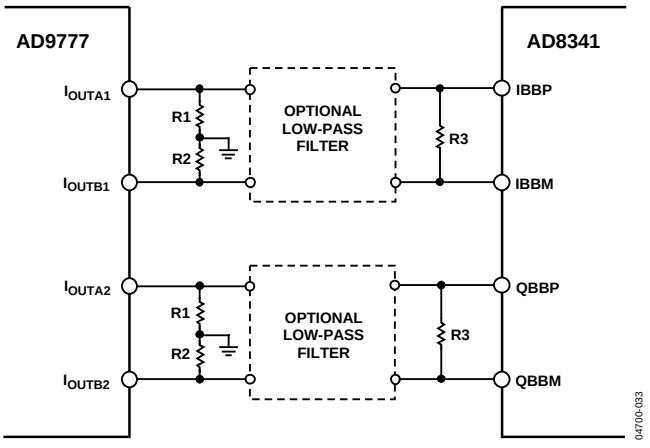


Figure 33. Basic AD9777 to AD8341 Interface

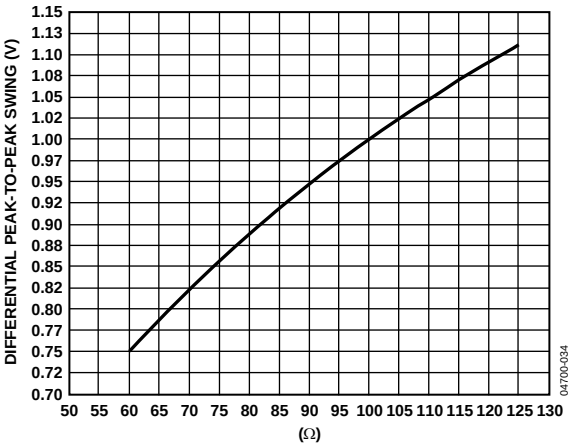


Figure 34. Peak-to-Peak DAC Output Swing vs. Swing Scaling Resistor R3 (R1 = R2 = 50 Ω)

Figure 34 shows the relationship between the value of R3 and the peak baseband voltage with R1 and R2 equal to 50 Ω. From Figure 34, it can be seen that a value of 100 Ω for R3 will provide a peak-to-peak swing of 1 V p-p differential into the AD8341's I and Q inputs.

When using a DAC, low-pass image reject filters are typically used to eliminate the Nyquist images produced by the DAC. They also provide the added benefit of eliminating broadband noise that might feed into the modulator from the DAC.

CDMA2000 APPLICATION

To test the compliance to the CDMA2000 base station standard, a single-carrier CDMA2000 test model signal (forward pilot, sync, paging, and six traffic as per 3GPP2 C.S0010-B, Table 6.5.2.1) was applied to the AD8341 at 1960 MHz. A cavity tuned filter was used to reduce noise from the signal source being applied to the device. The 6.8 MHz pass band of this filter is apparent in the subsequent spectral plots.

Figure 35 shows a plot of the spectrum of the output signal under nominal conditions. P_{OUT} is equal to −4 dBm and $V_{BBI} = V_{BBQ} = 0.353$ V, i.e., $V_{IBBP} - V_{IBBM} = V_{QBBP} - V_{QBBM} = 0.353$ V. Noise and distortion is measured in a 1 MHz bandwidth at ±2.25 MHz carrier offset (30 kHz measurement bandwidth).

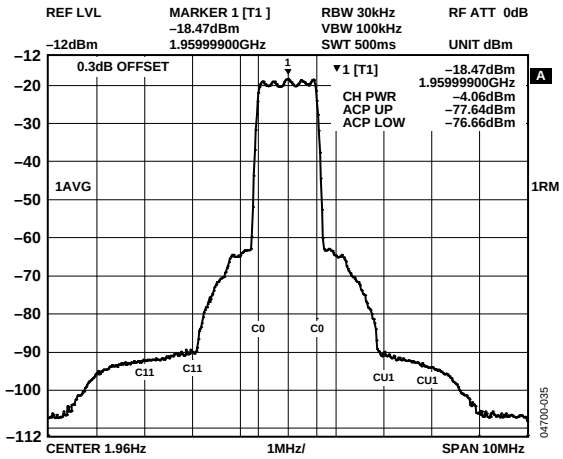


Figure 35. Output Spectrum, 1960 MHz, Single-Carrier CDMA2000 Test Model at –4 dBm, V_{BBI} = V_{BBQ} = 0.353 V, Adjacent Channel Power Measured at ±2.25 MHz Carrier Offset in 1 MHz BW Input Signal Filtered Using a Cavity Tuned Filter (Pass Band = 6.8 MHz)

Holding the differential I and Q control voltages steady at 0.353 V, input power was swept. Figure 36 shows variation in spurious content, again measured at ±2.25 MHz carrier offset in a 1 MHz bandwidth, as defined by the 3GPP2 specification.

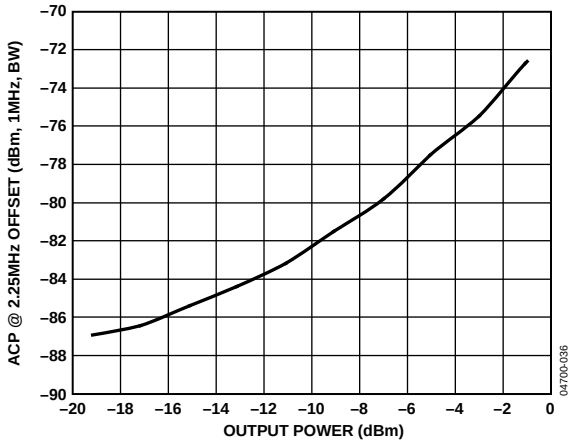


Figure 36. Adjacent Channel Power vs. Output Power, CDMA2000 Single Carrier @ 1960 MHz; ACP Measured at ±2.25 MHz Carrier Offset (1 MHz BW); V_{BBI} = V_{BBQ} = 0.353 V

With a fixed input power of 2.4 dBm, the output power was again swept by exercising the I and Q inputs. V_{BBI} and V_{BBQ} were kept equal and were swept from 100 mV to 500 mV. The resulting output power and ACP are shown in Figure 37.

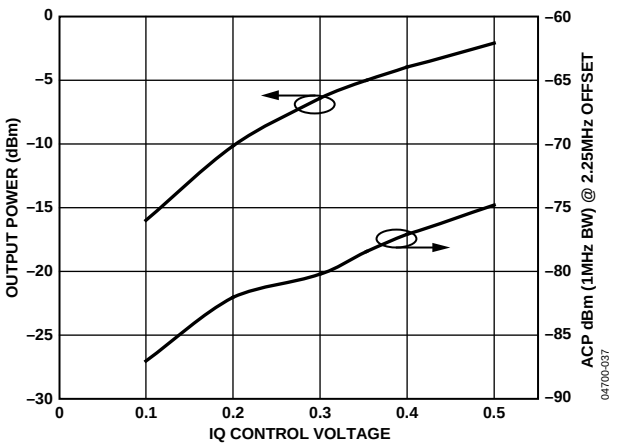


Figure 37. Output Power and ACP vs. I and Q Control Voltages, CDMA2000 Test Model, V_{BBI} = V_{BBQ}, ACP Measured at ±2.25 MHz Carrier Offset in 1 MHz BW

Figure 37 shows that for a fixed input power, the ACP (measured in dBm) tracks the output power as the gain is changed.

WCDMA APPLICATION

Figure 38 shows a plot of the output spectrum of the AD8341 transmitting a single-carrier WCDMA signal (Test Model 1-64 at 2140 MHz). The carrier power is approximately –9 dBm. The differential I and Q control voltages are both equal to 0.353 V, that is, the vector is sitting on the unit circle at 45°. At this power level, an adjacent channel power ratio of –61 dBc is achieved. The alternate channel power ratio of –72 dBc is dominated by the noise floor of the AD8341.

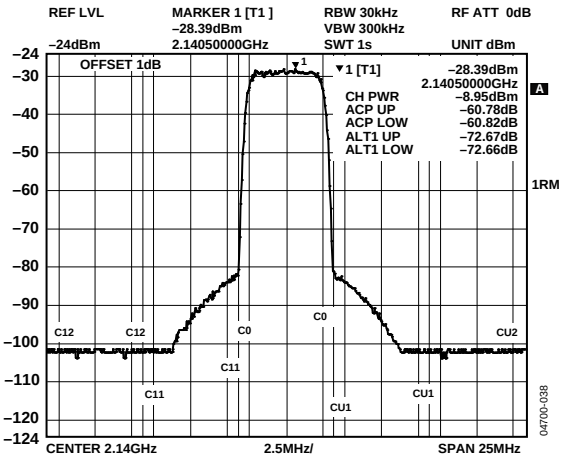


Figure 38. AD8341 Single-Carrier WCDMA Spectrum at 2140 MHz

Figure 39 shows how ACPR and noise vary with varying input power (differential I and Q control voltages are held at 0.353 V). At high power levels, both adjacent and alternate channel power ratios increase sharply. As output power drops, adjacent and alternate channel power ratios both reach minimums before the measurement becomes dominated by the noise floor of the AD8341. At this point, adjacent and alternate channel power ratios become approximately equal.

As the output power drops, the noise floor, measured in dBm in 1 MHz BW at 50 MHz carrier offset, drops slightly.

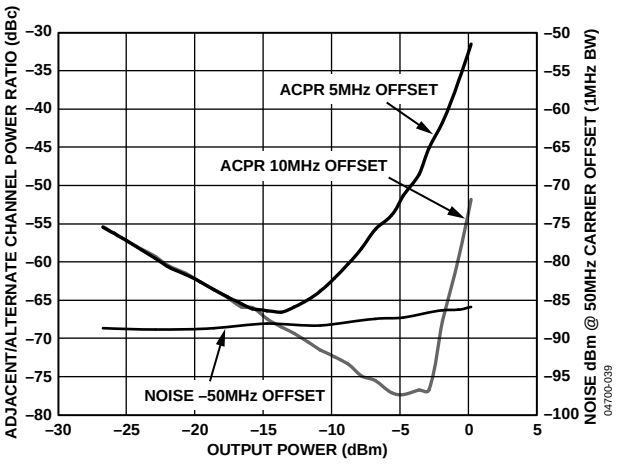


Figure 39. AD8341 ACPR and Noise vs. Output Power; Single-Carrier WCDMA (Test Model 1-64 at 2140 MHz)

Figure 40 shows how output power, ACPR, and noise vary with the differential I and Q control voltages. V_{BBI} and V_{BBQ} are tied together and are varied from 0.5 V to 50 mV.

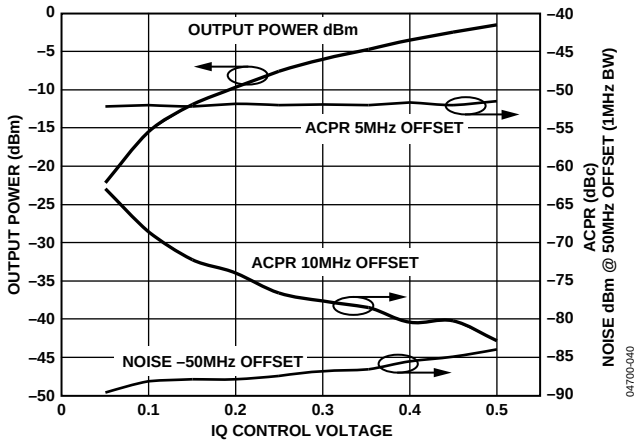


Figure 40. AD8341 Output Power, ACPR and Noise vs. V_{IQ}. Single-Carrier WCDMA (Test Model 1-64 at 2140 MHz)

In this case, adjacent channel power ratio remains constant as the (noise dominated) alternate channel power degrades roughly 1-for-1 with output power. As the I and Q control voltage drops, the noise floor again drops slowly.

EVALUATION BOARD

The evaluation board circuit schematic for the AD8341 is shown in Figure 41.

The evaluation board is configured to be driven from a single-ended 50 Ω source. Although the input of the AD8341 is differential, it may be driven single-ended, with no loss of performance.

The low-pass corner frequency of the baseband I and Q channels can be reduced by installing capacitors in the C11 and C12 positions. The low-pass corner frequency for either channel is approximated by

$$f_{3dB} \approx \frac{45\ \text{kHz} \times 10\ \text{nF}}{C_{FLT} + 0.5\ \text{pF}}$$

On this evaluation board, the I and Q baseband circuits are identical to each other, so the following description applies equally to each. The connections and circuit configuration for the Q baseband inputs are described in Table 4.

The baseband input of the AD8341 requires a differential voltage drive. The evaluation board is set up to allow such a drive by connecting the differential voltage source to QBBP and QBBM. The common-mode voltage should be maintained at approximately 0.5 V. For this configuration, Jumpers W1 through W4 should be removed.

The baseband input of the evaluation board may also be driven with a single-ended voltage. In this case, a bias level is provided to the unused input from Potentiometer R10 by installing either W1 or W2.

Setting SW1 in Position B disables the AD8341 output amplifier. With SW1 set to Position A, the output amplifier is enabled. With SW1 set to Position A, an external voltage signal, such as a pulse, can be applied to the DSOP SMA connector to exercise the output amplifier enable/disable function.

Table 4. Evaluation Board Configuration Options

Components	Function	Default Conditions
R7, R9, R11, R14, R15, R19, R20, R21, C15, C19, W3, W4	**I Channel Baseband Interface**. Resistors R7 and R9 may be installed to accommodate a baseband source that requires a specific terminating impedance. Capacitors C15 and C19 are bypass capacitors. For single-ended baseband drive, the Potentiometer R11 can be used to provide a bias level to the unused input (install either W3 or W4).	R7, R9 = Not Installed R11 = Potentiometer, 2 kΩ, 10 Turn (Bourns) R14 = 4 kΩ (Size 0603) R15 = 44 kΩ (Size 0603) R19, R20, R21 = 0 Ω (Size 0603) C15, C19 = 0.1 µF (Size 0603) W3 = Jumper (Installed) W4 = Jumper (Open)
R1, R3, R10, R12, R13, R16, R17, R18, C16, C20, W1, W2	**Q Channel Baseband Interface**. See the I Channel Baseband Interface section.	R1, R3 = Not Installed R10 = Potentiometer, 2 kΩ, 10 Turn (Bourns) R12 = 4 kΩ (Size 0603) R13 = 44 kΩ (Size 0603) R16, R17, R18 = 0 Ω (Size 0603) C16, C20 = 0.1 µF (Size 0603) W1 = Jumper (Installed) W2 = Jumper (Open)
C11, C12	**Baseband Low-Pass Filtering**. By adding Capacitor C11 between QFLP and QFLM, and C12 between IFLP and IFLM, the 3 dB low-pass corner frequency of the baseband interface can be reduced from 230 MHz (nominal). See equation in text.	C11, C12 = Not Installed
T1, C17, C18, L1, L2	**Output Interface**. The 1:1 balun transformer, T1, converts the 50 Ω differential output to 50 Ω single-ended. C17 and C18 are dc blocks. L1 and L2 provide dc bias for the output.	C17, C18 = 100 pF (Size 0603) T1 = ETC1-1-13 (M/A-COM) L1, L2 = 120 nH (Size 0603)
L3, L4, C5, C6	**Input Interface**. The input impedance of the AD8341 requires 1.2 nH inductors in series with RFIP and RFIM for optimum return loss when driven by a single-ended 50 Ω line. C5 and C6 are dc blocks.	L3, L4 = 1.2 nH (Size 0402) C5, C6 = 100 pF (Size 0603)

Components	Function	Default Conditions
C2, C4, C7, C9, C14, C1, C3, C8, C10, R2, R4, R5, R6	**Supply Decoupling**.	C2, C4, C7, C9, C14 = 0.1 µF (Size 0603) C1, C3, C8, C10 = 100 pF (Size 0603) R2, R4, R5, R6 = 0 Ω (Size 0603)
R8, SW1	**Output Disable Interface**. The output stage of the AD8341 is disabled by applying a high voltage to the DSOP pin by moving SW1 to Position B. The output stage is enabled moving SW1 to Position A. The output disable function can also be exercised by applying an external high or low voltage to the DSOP SMA connector with SW1 in Position A.	R8 = 10 kΩ (Size 0603) SW1 = SPDT (Position A, Output Enabled)

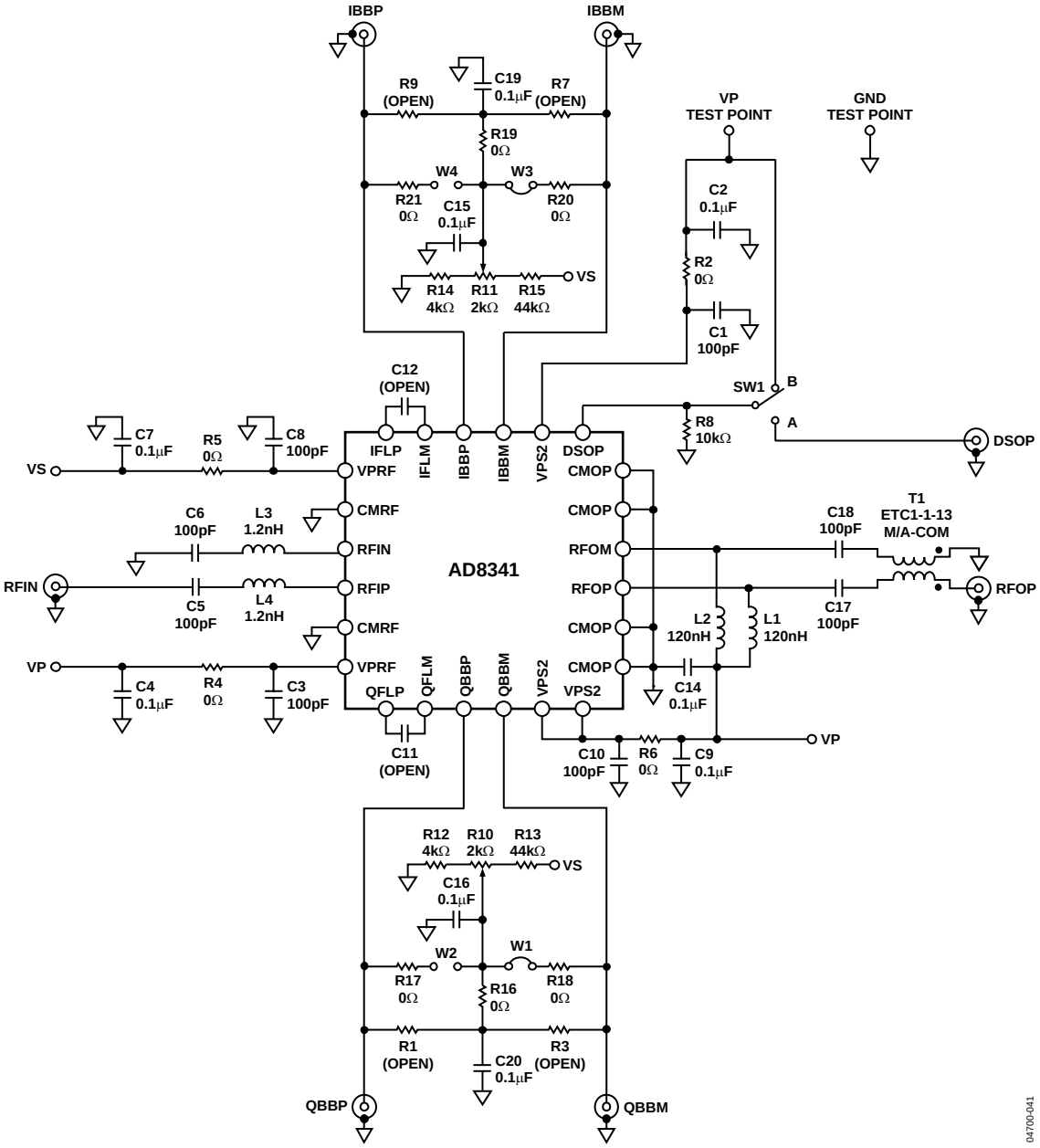
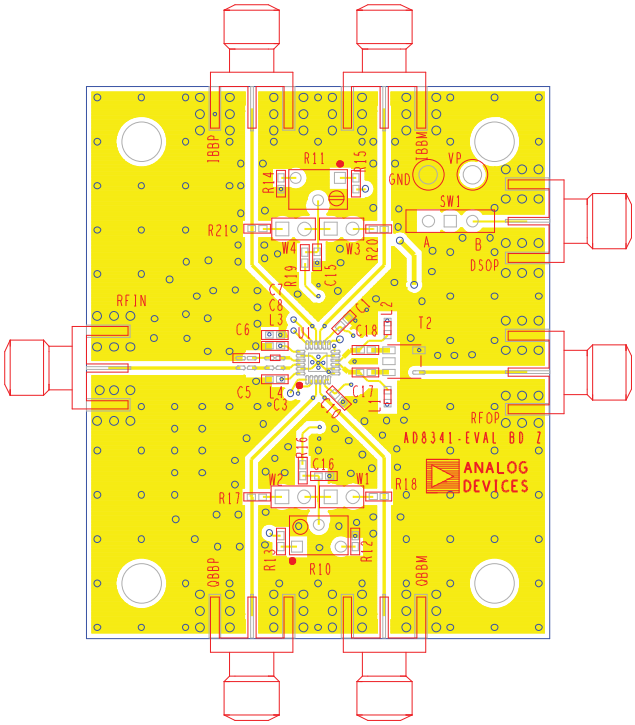
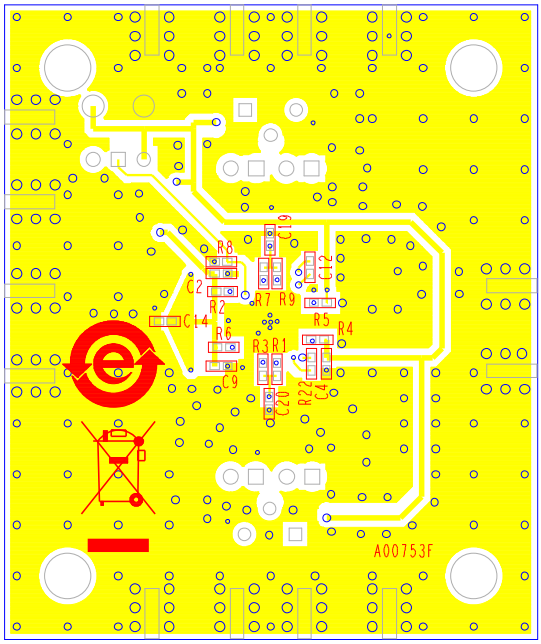


Figure 41. Evaluation Board Schematic



04700-042

Figure 42. AD8341 Evaluation Board Top Layer



04700-043

Figure 43. AD8341 Evaluation Board Bottom Layer

OUTLINE DIMENSIONS

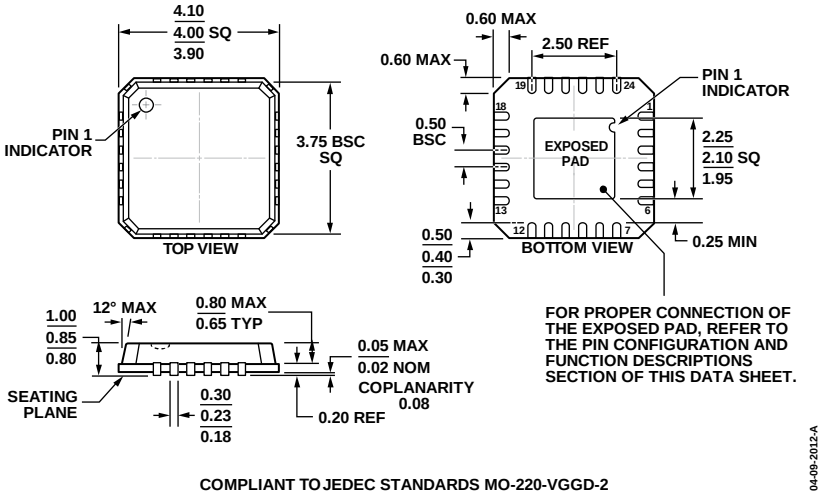


Figure 44. 24-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body Very Thin Quad
(CP-24-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option	Ordering Quantity
AD8341ACPZ-WP	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-24-1	64
AD8341ACPZ-REEL7	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-24-1	1,500
AD8341-EVALZ		Evaluation Board		1

[1] WP = Waffle pack.
[2] Z = RoHS Compliant Part.

©2004–2012 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.
D04700-0-11/12(A)

Стандарт Электрон Связь

Мы молодая и активно развивающаяся компания в области поставок электронных компонентов. Мы поставляем электронные компоненты отечественного и импортного производства напрямую от производителей и с крупнейших складов мира.

Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию .

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России , а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

Минимальные сроки поставки, гибкие цены, неограниченный ассортимент и индивидуальный подход к клиентам являются основой для выстраивания долгосрочного и эффективного сотрудничества с предприятиями радиоэлектронной промышленности, предприятиями ВПК и научно-исследовательскими институтами России.

С нами вы становитесь еще успешнее!

Наши контакты:

Телефон: +7 812 627 14 35

Электронная почта: sales@st-electron.ru

Адрес: 198099, Санкт-Петербург, Промышленная ул, дом № 19, литера Н, помещение 100-Н Офис 331