Arria 10 Device Overview

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The Arria® 10 device family consists of high-performance and power-efficient 20 nm mid-range FPGAs and SoCs.

Arria 10 device family delivers:

- Higher performance than the previous generation of mid-range and high-end FPGAs.
- Power efficiency attained through a comprehensive set of power-saving technologies.

The Arria 10 devices are ideal for high performance, power-sensitive, midrange applications in diverse markets.

Table 1: Sample Markets and Ideal Applications for Arria 10 Devices

Market	Applications
Wireless	• Channel and switch cards in remote radio heads • Mobile backhaul
Wireline	• 40G/100G muxponders and transponders • 100G line cards • Bridging • Aggregation
Broadcast	• Studio switches • Servers and transport • Videoconferencing • Professional audio and video
Computing and Storage	• Flash cache • Cloud computing servers • Server acceleration
Medical	• Diagnostic scanners • Diagnostic imaging

Market	Applications
Military	• Missile guidance and control • Radar • Electronic warfare • Secure communications

Related Information

Arria 10 Device Handbook: Known Issues
Lists the planned updates to the *Arria 10 Device Handbook* chapters.

Key Advantages of Arria 10 Devices

Table 2: Key Advantages of the Arria 10 Device Family

Advantage	Supporting Feature
Enhanced core architecture	• Built on TSMC's 20 nm process technology • 60% higher performance than the previous generation of mid-range FPGAs • 15% higher performance than the fastest previous-generation FPGA
High-bandwidth integrated transceivers	• Short-reach rates up to 28.3 Gigabits per second (Gbps) • Backplane capability up to 17.4 Gbps • Integrated 10GBASE-KR and 40GBASE-KR4 Forward Error Correction (FEC)
Improved logic integration and hard IP blocks	• 8-input adaptive logic module (ALM) • Up to 65.6 megabits (Mb) of embedded memory • Variable-precision digital signal processing (DSP) blocks • Fractional synthesis phase-locked loops (PLLs) • Hard PCI Express Gen3 IP blocks • Hard memory controllers and PHY up to 2,666 Megabits per second (Mbps)
Second generation hard processor system (HPS) with integrated ARM® Cortex™-A9 MPCore processor	• Tight integration of a dual-core ARM Cortex-A9 MPCore processor, hard IP, and an FPGA in a single Arria 10 system-on-a-chip (SoC) • Supports over 128 Gbps peak bandwidth with integrated data coherency between the processor and the FPGA fabric

Advantage	Supporting Feature
Advanced power savings	• Comprehensive set of advanced power saving features • Power-optimized MultiTrack routing and core architecture • Up to 40% lower power compared to previous generation of mid-range FPGAs • Up to 60% lower power compared to previous generation of high-end FPGAs

Summary of Arria 10 Features

Table 3: Summary of Features for Arria 10 Devices

Feature	Description
Technology	• TSMC's 20-nm SoC process technology • Allows operation at a lower V_{CC} level of 0.83 V instead of the 0.9 V standard V_{CC} core voltage
Packaging	• 1.0 mm ball-pitch Fineline BGA packaging • 0.8 mm ball-pitch Ultra Fineline BGA packaging • Multiple devices with identical package footprints for seamless migration between different FPGA densities • Devices with compatible package footprints allow migration to next generation high-end Stratix® 10 devices • RoHS, leaded(1), and lead-free (Pb-free) options
High-performance FPGA fabric	• Enhanced 8-input ALM with four registers • Improved multi-track routing architecture to reduce congestion and improve compilation time • Hierarchical core clocking architecture • Fine-grained partial reconfiguration
Internal memory blocks	• M20K—20-Kb memory blocks with hard error correction code (ECC) • Memory logic array block (MLAB)—640-bit memory

(1) Contact Altera for availability.

Feature		Description

Embedded Hard IP blocks	Variable-precision DSP	• Native support for signal processing precision levels from 18 x 19 to 54 x 54
		• Native support for 27 x 27 multiplier mode
		• 64-bit accumulator and cascade for systolic finite impulse responses (FIRs)
		• Internal coefficient memory banks
		• Preadder/subtractor for improved efficiency
		• Additional pipeline register to increase performance and reduce power
		• Supports floating point arithmetic:
		  • Perform multiplication, addition, subtraction, multiply-add, multiply-subtract, and complex multiplication.
		  • Supports multiplication with accumulation capability, cascade summation, and cascade subtraction capability.
		  • Dynamic accumulator reset control.
		  • Support direct vector dot and complex multiplication chaining multiply floating point DSP blocks.

	Memory controller	DDR4, DDR3, and DDR3L
	PCI Express®	PCI Express (PCIe®) Gen3 (x1, x2, x4, or x8), Gen2 (x1, x2, x4, or x8) and Gen1 (x1, x2, x4, or x8) hard IP with complete protocol stack, endpoint, and root port

	Transceiver I/O	• 10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC)
		• PCS hard IPs that support:
		  • 10-Gbps Ethernet (10GbE)
		  • PCIe PIPE interface
		  • Interlaken
		  • Gbps Ethernet (GbE)
		  • Common Public Radio Interface (CPRI) with deterministic latency support
		  • Gigabit-capable passive optical network (GPON) with fast lock-time support
		• 13.5G JESD204b
		• 8B/10B, 64B/66B, 64B/67B encoders and decoders
		• Custom mode support for proprietary protocols

Feature	Description

Core clock networks	• 800 MHz fabric clocking:
	  • 667 MHz external memory interface clocking with 2,666 Mbps DDR4 interface
	  • 800 MHz LVDS interface clocking with 1,600 Mbps LVDS interface
	• Global, regional, and peripheral clock networks
	• Clock networks that are not used can be gated to reduce dynamic power

Phase-locked loops (PLLs)	• High-resolution fractional synthesis PLLs:
	  • Precision clock synthesis, clock delay compensation, and zero delay buffering (ZDB)
	  • Support integer mode and fractional mode
	  • Fractional mode support with third-order delta-sigma modulation
	• Integer PLLs:
	  • Adjacent to general purpose I/Os
	  • Support external memory and LVDS interfaces

FPGA General-purpose I/Os (GPIOs)	• 1.6 Gbps LVDS—every pair can be configured as receiver or transmitter • On-chip termination (OCT) • 1.2 V to 3.0 V single-ended LVTTL/LVCMOS interfacing

External Memory Interface	• Hard memory controller— DDR4, DDR3, and DDR3L support
	  • DDR4—speeds up to 1,333 MHz/2,666 Mbps
	  • DDR3—speeds up to 1,067 MHz/2,133 Mbps
	• Soft memory controller—provides support for RLDRAM 3(2), QDR IV(2), and QDR II+

(2) Arria 10 devices support this external memory interface using hard PHY with soft memory controller.

Feature	Description

Low-power serial transceivers	• Continuous operating range:
	  • Arria 10 GX—611 Mbps to 17.4 Gbps
	  • Arria 10 GT—611 Mbps to 28.3 Gbps
	• Backplane support:
	  • Arria 10 GX—up to 16.0 Gbps
	  • Arria 10 GT—up to 17.4 Gbps
	• Extended range down to 125 Mbps with oversampling
	• ATX transmit PLLs with user-configurable fractional synthesis capability
	• Electronic Dispersion Compensation (EDC) support for XFP, SFP+, QSFP, and CFP optical module
	• Adaptive linear and decision feedback equalization
	• Transmitter pre-emphasis and de-emphasis
	• Dynamic partial reconfiguration of individual transceiver channels
	• On-chip instrumentation (EyeQ non-intrusive data eye monitoring)

Feature	Description	
HPS (Arria 10 SX devices only)	Processor and system	• Dual-core ARM Cortex-A9 MPCore processor—1.2 GHz CPU with 1.5 GHz overdrive capability • 256 KB on-chip RAM and 64 KB on-chip ROM • System peripherals—general-purpose timers, watchdog timers, direct memory access (DMA) controller, FPGA configuration manager, and clock and reset managers • Security features—anti-tamper, secure boot, Advanced Encryption Standard (AES) and authentication (SHA) • ARM CoreSight™ JTAG debug access port, trace port, and on-chip trace storage
	External interfaces	• Hard memory interface—Hard memory controller (2,666 Mbps DDR4, and 2,166 Mbps DDR3), Quad serial peripheral interface (QSPI) flash controller, NAND flash controller, direct memory access (DMA) controller, Secure Digital/MultiMediaCard (SD/MMC) controller • Communication interface— 10/100/1000 Ethernet media access control (MAC), USB On-The-GO (OTG) controllers, I^2C controllers, UART 16550, serial peripheral interface (SPI), and up to 62 HPS GPIO interfaces (48 direct-share I/Os)
	Interconnects to core	• High-performance ARM AMBA® AXI bus bridges that support simultaneous read and write • HPS–FPGA bridges—include the FPGA-to-HPS, HPS-to-FPGA, and lightweight HPS-to-FPGA bridges that allow the FPGA fabric to issue transactions to slaves in the HPS, and vice versa • Configuration bridge that allows HPS configuration manager to configure the core logic via dedicated 32-bit configuration port • FPGA-to-HPS SDRAM controller bridge—provides configuration interfaces for the multiport front end (MPFE) of the HPS SDRAM controller

Feature	Description
Configuration	• Tamper protection—comprehensive design protection to protect your valuable IP investments • Enhanced 256-bit advanced encryption standard (AES) design security with authentication • Configuration via protocol (CvP) using PCIe Gen1, Gen2, or Gen3 • Dynamic reconfiguration of the transceivers and PLLs • Fine-grained partial reconfiguration of the core fabric • Active Serial x4 Interface
Power management	• SmartVID • V_{CC} PowerManager • Low static power device options • Programmable Power Technology • Quartus® II integrated PowerPlay power analysis
Software and tools	• Quartus II design suite • Transceiver toolkit • Qsys system integration tool • DSP Builder advanced blockset • OpenCL™ support • SoC Embedded Design Suite (EDS)

Related Information

Arria 10 Transceiver PHY Overview
Provides details on Arria 10 transceivers.

Arria 10 Device Variants and Packages

Table 4: Device Variants for the Arria 10 Device Family

Variant	Description
Arria 10 GX	FPGA featuring 17.4 Gbps transceivers for short reach applications with 16.0 Gbps backplane driving capability.
Arria 10 GT	FPGA featuring: • 17.4 Gbps transceivers for short reach applications with 17.4 Gbps backplane driving capability. • 28.3 Gbps transceivers for chip-to-chip and chip-to-module applications—ideal for interfacing with CFP2 and CFP4 optical modules.
Arria 10 SX	SoC integrating ARM-based HPS and FPGA featuring 17.4 Gbps transceivers for short reach applications with 16.0 Gbps backplane driving capability.

Arria 10 GX

This section provides the available options, maximum resource counts, and package plan for the Arria 10 GX devices.

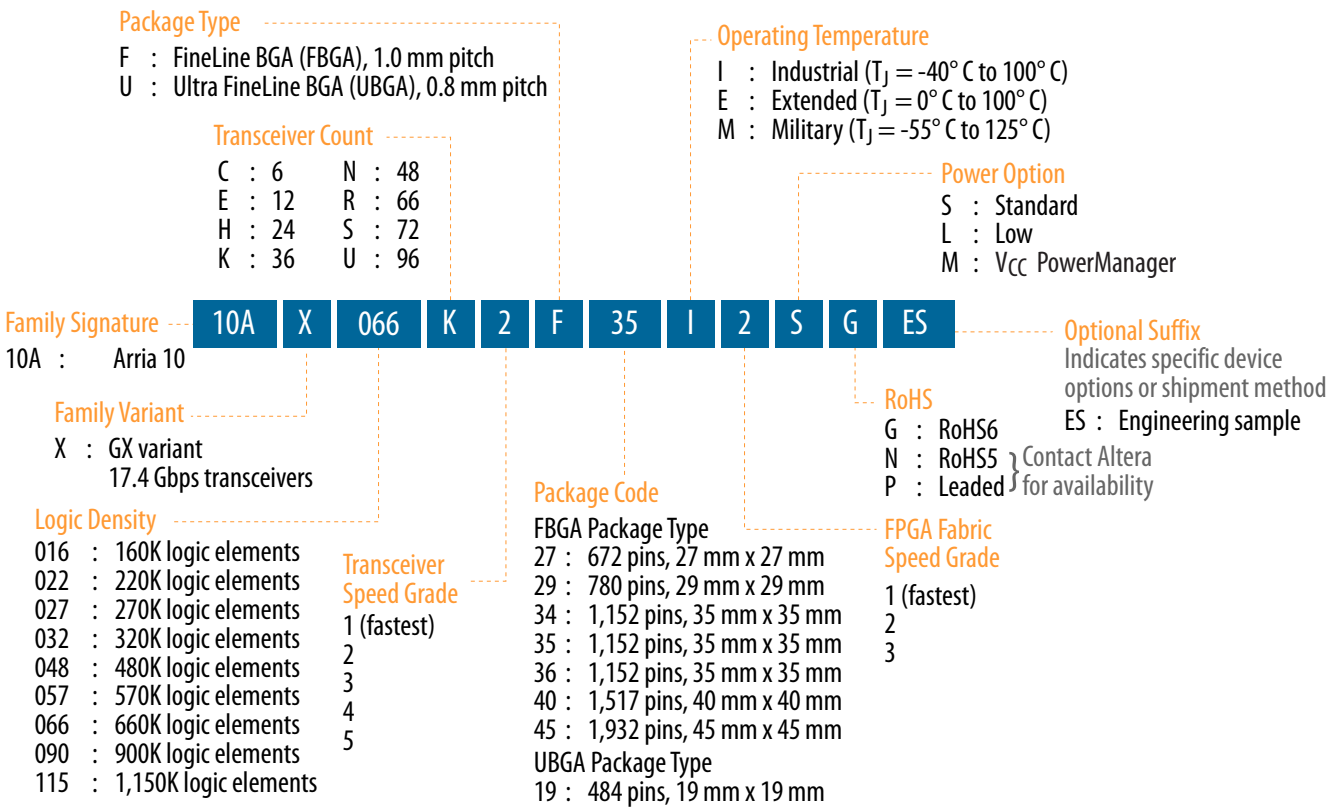
The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Altera Product Selector.

Related Information

Altera Product Selector
Provides the latest information on Altera products.

Available Options

Figure 1: Sample Ordering Code and Available Options for Arria 10 GX Devices—Preliminary



Related Information

Transceiver Performance for Arria 10 GX/SX Devices
Provides more information about the transceiver speed grade.

Maximum Resources

Table 5: Maximum Resource Counts for Arria 10 GX Devices (GX 160, GX 220, GX 270, GX 320, and GX 480) —Preliminary

Resource		Product Line				
		GX 160	GX 220	GX 270	GX 320	GX 480
Logic Elements (LE) (K)		160	220	270	320	480
ALM		61,510	83,730	101,620	118,730	181,790
Register		246,040	334,920	406,480	474,920	727,160
Memory (Kb)	M20K	8,800	11,760	15,000	17,820	28,760
	MLAB	1,050	1,833	2,451	2,864	4,404
Variable-precision DSP Block		156	191	830	985	1,368
18 x 19 Multiplier		312	382	1,660	1,970	2,736
PLL	Fractional Synthesis	6	6	8	8	12
	I/O	6	6	8	8	12
17.4 Gbps Transceiver		12	12	24	24	36
GPIO (3)		288	288	384	384	492
LVDS Pair (4)		120	120	168	168	222
PCIe Hard IP Block		1	1	2	2	2
Hard Memory Controller		6	6	8	8	12

(3) The number of GPIOs does not include transceiver I/Os. In the Quartus II software, the number of user I/Os includes transceiver I/Os.
(4) Each LVDS I/O pair can be used as differential input or output.

Table 6: Maximum Resource Counts for Arria 10 GX Devices (GX 570, GX 660, GX 900, and GX 1150)—Preliminary

Resource		Product Line			
		GX 570	GX 660	GX 900	GX 1150
Logic Elements (LE) (K)		570	660	900	1,150
ALM		217,080	250,540	339,620	427,200
Register		868,320	1,002,160	1,358,480	1,708,800
Memory (Kb)	M20K	36,000	42,620	48,460	54,260
	MLAB	5,096	5,788	9,386	12,984
Variable-precision DSP Block		1,523	1,678	1,518	1,518
18 x 19 Multiplier		3,046	3,356	3,036	3,036
PLL	Fractional Synthesis	16	16	32	32
	I/O	16	16	16	16
17.4 Gbps Transceiver		48	48	96	96
GPIO (3)		696	696	768	768
LVDS Pair (4)		324	324	384	384
PCIe Hard IP Block		2	2	4	4
Hard Memory Controller		16	16	16	16

Package Plan

Table 7: Package Plan for Arria 10 GX Devices (U19, F27, F29, and F34) — Preliminary

Refer to I/O and High Speed I/O in Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

Product Line	U19 (19 mm × 19 mm, 484-pin UBGA)			F27 (27 mm × 27 mm, 672-pin FBGA)			F29 (29 mm × 29 mm, 780-pin FBGA)			F34 (35 mm × 35 mm, 1152-pin FBGA)		
	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR
GX 160	48	192	6	48	192	12	48	240	12	—	—	—
GX 220	48	192	6	48	192	12	48	240	12	—	—	—
GX 270	—	—	—	48	192	12	48	312	12	48	336	24
GX 320	—	—	—	48	192	12	48	312	12	48	336	24
GX 480	—	—	—	—	—	—	48	312	12	48	444	24
GX 570	—	—	—	—	—	—	—	—	—	48	444	24

Product Line	U19 (19 mm × 19 mm, 484-pin UBGA)			F27 (27 mm × 27 mm, 672-pin FBGA)			F29 (29 mm × 29 mm, 780-pin FBGA)			F34 (35 mm × 35 mm, 1152-pin FBGA)		
	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR
GX 660	—	—	—	—	—	—	—	—	—	48	444	24
GX 900	—	—	—	—	—	—	—	—	—	—	504	24
GX 1150	—	—	—	—	—	—	—	—	—	—	504	24

Table 8: Package Plan for Arria 10 GX Devices (F35, F36, NF40, and KF40) — Preliminary

Refer to I/O and High Speed I/O in Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

Product Line	F35 (35 mm × 35 mm, 1152-pin FBGA)			F36 (35 mm x 35 mm, 1152-pin FBGA)			KF40 (40 mm × 40 mm, 1517-pin FBGA)			NF40 (40 mm × 40 mm, 1517-pin FBGA)		
	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR
GX 270	48	336	24	—	—	—	—	—	—	—	—	—
GX 320	48	336	24	—	—	—	—	—	—	—	—	—
GX 480	48	348	36	—	—	—	—	—	—	—	—	—
GX 570	48	348	36	48	384	36	96	600	36	48	540	48
GX 660	48	348	36	48	384	36	96	600	36	48	540	48
GX 900	—	—	—	—	432	36	—	—	—	—	600	48
GX 1150	—	—	—	—	432	36	—	—	—	—	600	48

Table 9: Package Plan for Arria 10 GX Devices (RF40, NF45, SF45, and UF45) — Preliminary

Refer to I/O and High Speed I/O in Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

Product Line	RF40 (40 mm × 40 mm, 1517-pin FBGA)			NF45 (45 mm × 45 mm) 1932-pin FBGA)			SF45 (45 mm × 45 mm) 1932-pin FBGA)			UF45 (45 mm × 45 mm) 1932-pin FBGA)		
	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR
GX 900	—	342	66	—	768	48	—	624	72	—	480	96
GX 1150	—	342	66	—	768	48	—	624	72	—	480	96

Related Information

I/O and High-Speed Differential I/O Interfaces in Arria 10 Devices chapter, Arria 10 Device Handbook
Provides the number of 3 V and LVDS I/Os, and LVDS channels for each Arria 10 device package.

Arria 10 GT

This section provides the available options, maximum resource counts, and package plan for the Arria 10 GT devices.

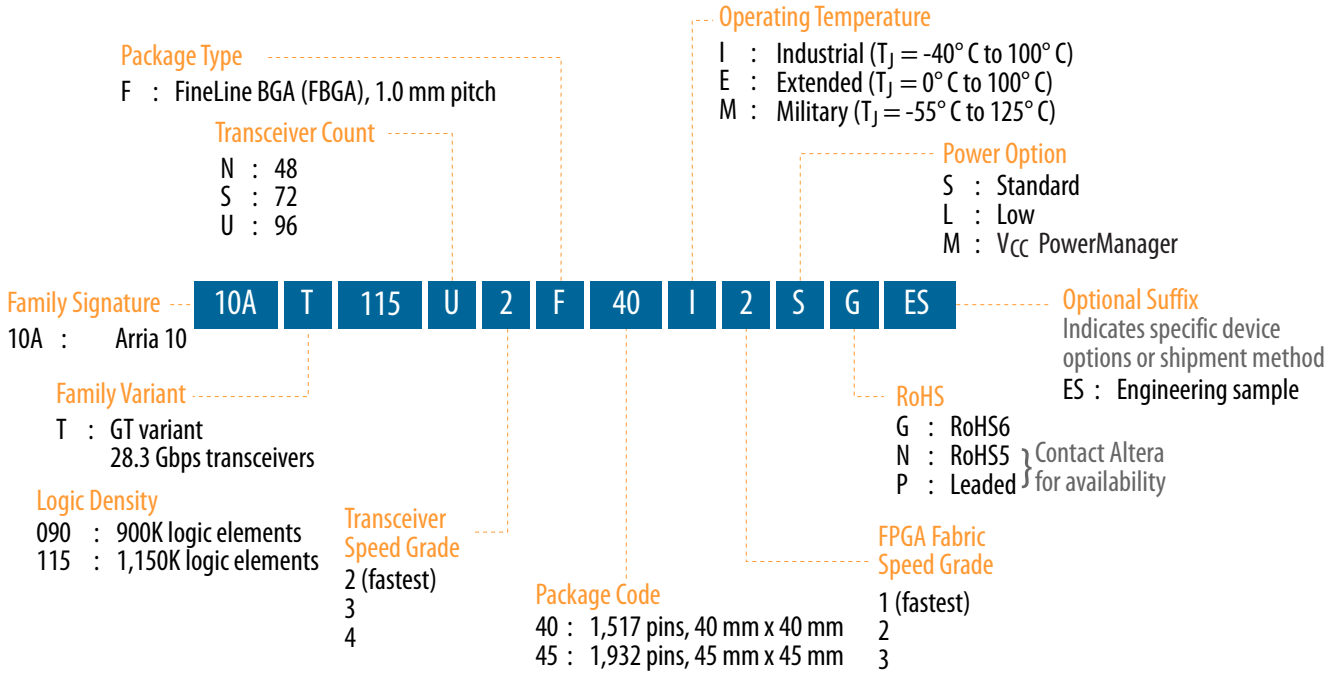
The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Altera Product Selector.

Related Information

Altera Product Selector
Provides the latest information on Altera products.

Available Options

Figure 2: Sample Ordering Code and Available Options for Arria 10 GT Devices—Preliminary



Maximum Resources

Table 10: Maximum Resource Counts for Arria 10 GT Devices—Preliminary

Resource		Product Line	
		GT 900	GT 1150
Logic Elements (LE) (K)		900	1,150
ALM		339,620	427,200
Register		1,358,480	1,708,800
Memory (Kb)	M20K	48,460	54,260
	MLAB	9,386	12,984
Variable-precision DSP Block		1,518	1,518
18 x 19 Multiplier		3,036	3,036
PLL	Fractional Synthesis	32	32
	I/O	16	16
Transceiver	17.4 Gbps	80 (5)	80 (5)
	28.3 Gbps	16	16
GPIO(6)		624	624
LVDS Pair(7)		312	312
PCIe Hard IP Block		4	4
Hard Memory Controller		16	16

Related Information

Arria 10 GT Channel Usage

Configuring GT/GX channels in Arria 10 GT devices.

(5) If all 16 GT channels are in use, 8 of the GX channels are not usable.

(6) The number of GPIOs does not include transceiver I/Os. In the Quartus II software, the number of user I/Os includes transceiver I/Os.

(7) Each LVDS I/O pair can be used as differential input or output.

Package Plan

Table 11: Package Plan for Arria 10 GT Devices —Preliminary

Refer to I/O and High Speed I/O in Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

Product Line	NF40 (40 mm × 40 mm, 1517-pin FBGA)			SF45 (45 mm × 45 mm, 1932-pin FBGA)			UF45 (45 mm × 45 mm, 1932-pin FBGA)		
	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR
GT 900	—	600	48	—	624	72	—	480	96
GT 1150	—	600	48	—	624	72	—	480	96

Related Information

I/O and High-Speed Differential I/O Interfaces in Arria 10 Devices chapter, Arria 10 Device Handbook
Provides the number of 3 V and LVDS I/Os, and LVDS channels for each Arria 10 device package.

Arria 10 SX

This section provides the available options, maximum resource counts, and package plan for the Arria 10 SX devices.

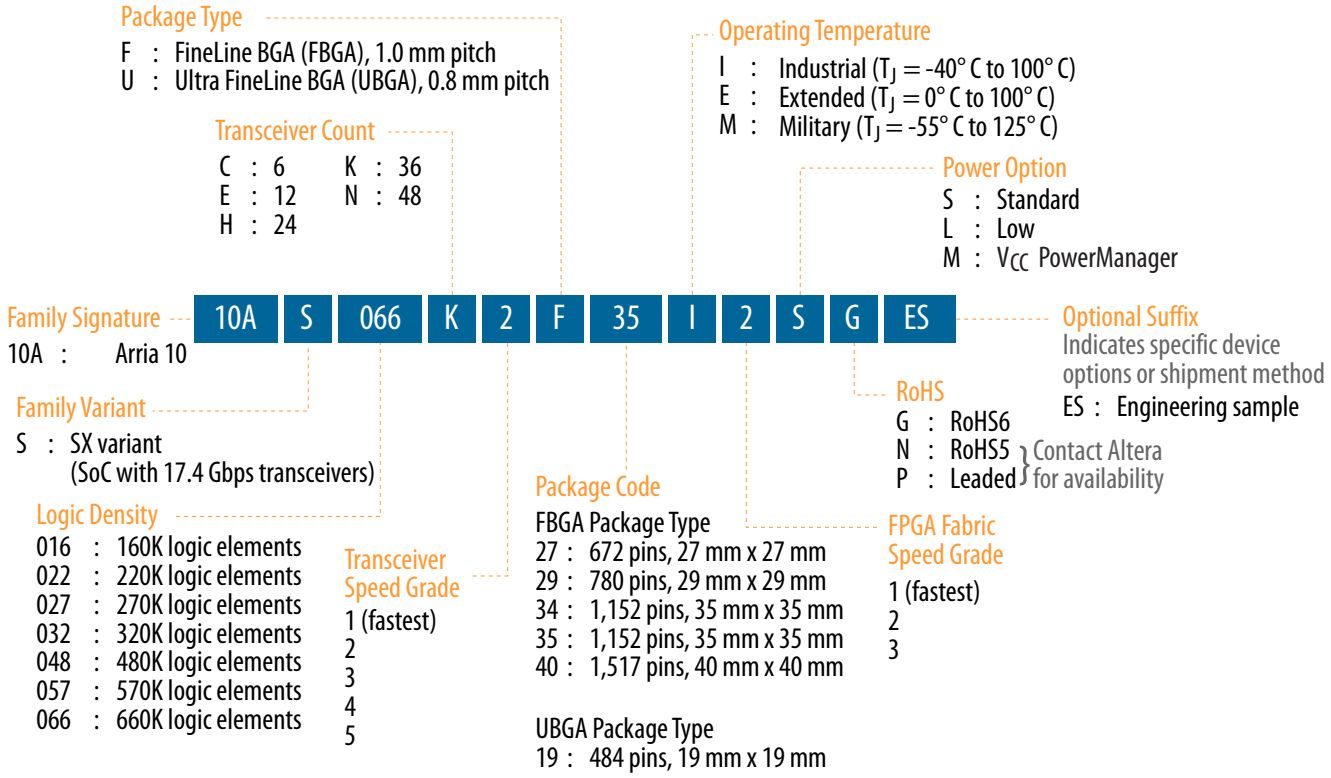
The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Altera Product Selector.

Related Information

Altera Product Selector
Provides the latest information on Altera products.

Available Options

Figure 3: Sample Ordering Code and Available Options for Arria 10 SX Devices—Preliminary



Related Information

Transceiver Performance for Arria 10 GX/SX Devices
Provides more information about the transceiver speed grade.

Maximum Resources

Table 12: Maximum Resource Counts for Arria 10 SX Devices—Preliminary

Resource		Product Line						
		SX 160	SX 220	SX 270	SX 320	SX 480	SX 570	SX 660
Logic Elements (LE) (K)		160	220	270	320	480	570	660
ALM		61,510	83,730	101,620	118,730	181,790	217,080	250,540
Register		246,040	334,920	406,480	474,920	727,160	868,320	1,002,160
Memory (Kb)	M20K	8,800	11,760	15,000	17,820	28,760	36,000	42,620
	MLAB	1,050	1,833	2,451	2,864	4,404	5,096	5,788
Variable-precision DSP Block		156	191	830	985	1,368	1,523	1,678
18 x 19 Multiplier		312	382	1,660	1,970	2,736	3,046	3,356
PLL	Fractional Synthesis	6	6	8	8	12	16	16
	I/O	6	6	8	8	12	16	16
17.4 Gbps Transceiver		12	12	24	24	36	48	48
GPIO [8]		288	288	384	384	492	696	696
LVDS Pair [9]		120	120	168	168	174	324	324
PCIe Hard IP Block		1	1	2	2	2	2	2
Hard Memory Controller		6	6	8	8	12	16	16
ARM Cortex-A9 MPCore Processor		Yes	Yes	Yes	Yes	Yes	Yes	Yes

[8] The number of GPIOs does not include transceiver I/Os. In the Quartus II software, the number of user I/Os includes transceiver I/Os.

[9] Each LVDS I/O pair can be used as differential input or output.

Package Plan

Table 13: Package Plan for Arria 10 SX Devices (U19, F27, F29, and F34) — Preliminary

Refer to I/O and High Speed I/O in Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

Product Line	U19 (19 mm × 19 mm, 484-pin UBGA)			F27 (27 mm × 27 mm, 672-pin FBGA)			F29 (29 mm × 29 mm, 780-pin FBGA)			F34 (35 mm × 35 mm, 1152-pin FBGA)		
	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR
SX 160	48	144	6	48	192	12	48	240	12	—	—	—
SX 220	48	144	6	48	192	12	48	240	12	—	—	—
SX 270	—	—	—	48	192	12	48	312	12	48	336	24
SX 320	—	—	—	48	192	12	48	312	12	48	336	24
SX 480	—	—	—	—	—	—	48	312	12	48	444	24
SX 570	—	—	—	—	—	—	—	—	—	48	444	24
SX 660	—	—	—	—	—	—	—	—	—	48	444	24

Table 14: Package Plan for Arria 10 SX Devices (F35, KF40, and NF40) — Preliminary

Refer to I/O and High Speed I/O in Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

Product Line	F35 (35 mm × 35 mm, 1152-pin FBGA)			KF40 (40 mm × 40 mm, 1517-pin FBGA)			NF40 (40 mm × 40 mm, 1517-pin FBGA)		
	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR
SX 270	48	336	24	—	—	—	—	—	—
SX 320	48	336	24	—	—	—	—	—	—
SX 480	48	348	36	—	—	—	—	—	—
SX 570	48	348	36	96	600	36	48	540	48
SX 660	48	348	36	96	600	36	48	540	48

Related Information

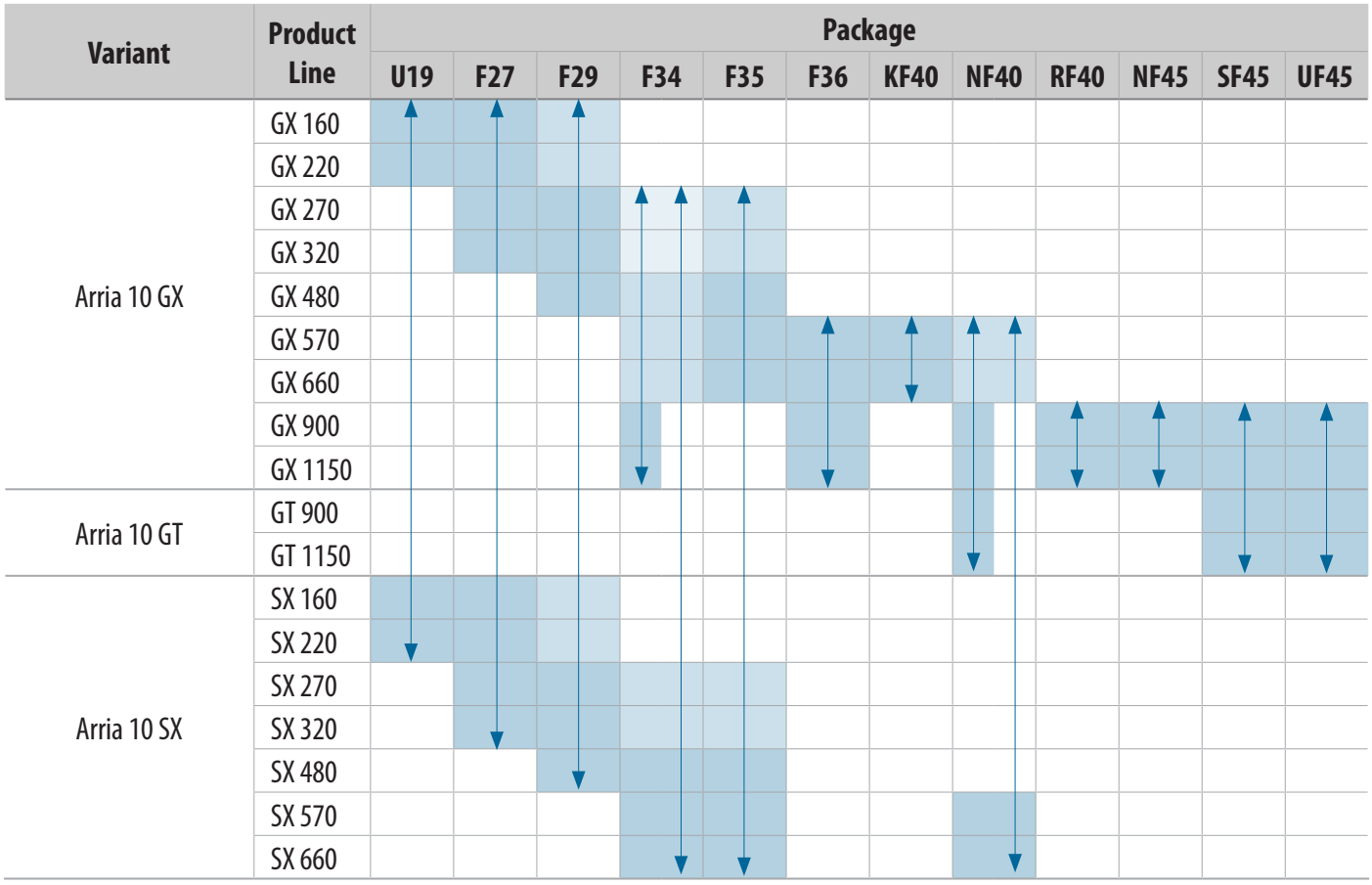
I/O and High-Speed Differential I/O Interfaces in Arria 10 Devices chapter, Arria 10 Device Handbook

Provides the number of 3 V and LVDS I/Os, and LVDS channels for each Arria 10 device package.

I/O Vertical Migration for Arria 10 Devices

Figure 4: Migration Capability Across Arria 10 Product Lines—Preliminary

- The arrows indicate the migration paths. The devices included in each vertical migration path are shaded. Devices with fewer resources in the same path have lighter shades.
- To achieve the full I/O migration across product lines in the same migration path, restrict I/Os and transceivers usage to match the product line with the lowest I/O and transceiver counts.
- An LVDS I/O bank in the source device may be mapped to a 3 V I/O bank in the target device. To use memory interface clock frequency higher than 533 MHz, assign external memory interface pins only to banks that are LVDS I/O in both devices.
- There may be nominal 0.15 mm package height difference between some product lines in the same package type.
- Some migration paths are not shown in the Quartus II software Pin Migration View.



Note: To verify the pin migration compatibility, use the Pin Migration View window in the Quartus II software Pin Planner.

Migration between Arria 10 and Stratix 10 Devices

There is footprint compatibility between Arria 10 and Stratix 10 packages. You can start developing your design with selected Arria 10 devices and then move the design to Stratix 10 devices.

For details about the migration possibilities between the two device families, contact Altera.

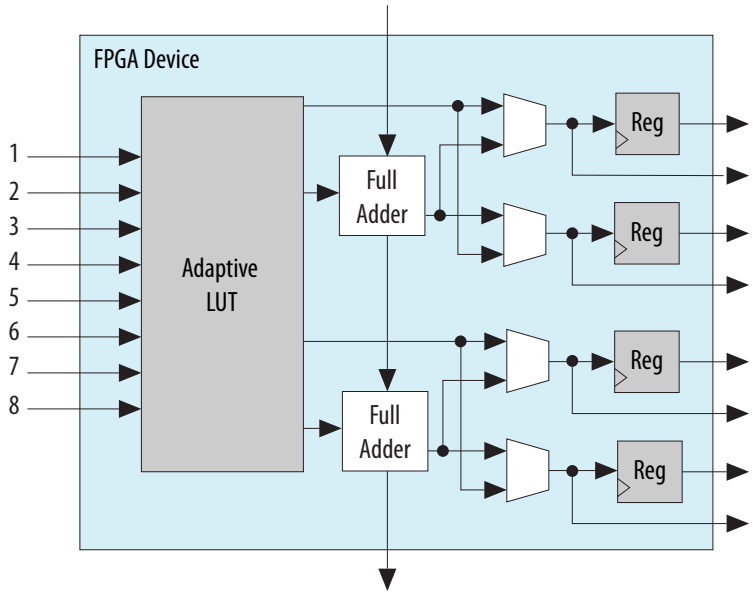
Adaptive Logic Module

Arria 10 devices use a 20 nm ALM as the basic building block of the logic fabric.

The ALM architecture is the same as the previous generation FPGAs, allowing for efficient implementation of logic functions and easy conversion of IP between the device generations.

The ALM, as shown in following figure, uses an 8-input fracturable look-up table (LUT) with four dedicated registers to help improve timing closure in register-rich designs and achieve an even higher design packing capability than the traditional two-register per LUT architecture.

Figure 5: ALM for Arria 10 Devices



The Quartus II software optimizes your design according to the ALM logic structure and automatically maps legacy designs into the Arria 10 ALM architecture.

Variable-Precision DSP Block

The Arria 10 variable precision DSP blocks support fixed-point arithmetic and floating-point arithmetic.

Features for fixed-point arithmetic:

- High-performance, power-optimized, and fully registered multiplication operations
- 18-bit and 27-bit word lengths
- Two 18 x 19 multipliers or one 27 x 27 multiplier per DSP block
- Built-in addition, subtraction, and 64-bit double accumulation register to combine multiplication results
- Cascading 19-bit or 27-bit when pre-adder is disabled and cascading 18-bit when pre-adder is used to form the tap-delay line for filtering applications

- Cascading 64-bit output bus to propagate output results from one block to the next block without external logic support
- Hard pre-adder supported in 19-bit and 27-bit modes for symmetric filters
- Internal coefficient register bank in both 18-bit and 27-bit modes for filter implementation
- 18-bit and 27-bit systolic finite impulse response (FIR) filters with distributed output adder
- Biased rounding support

Features for floating-point arithmetic:

- Multiplication, addition, subtraction, multiply-add, and multiply-subtract
- Multiplication with accumulation capability and a dynamic accumulator reset control
- Multiplication with cascade summation capability
- Multiplication with cascade subtraction capability
- Complex multiplication
- Direct vector dot product
- Systolic FIR filter

Table 15: Variable-Precision DSP Block Configurations for Arria 10 Devices

Usage Example	Multiplier Size (Bit)	DSP Block Resources
Medium precision fixed point	Two 18 x 19	1
High precision fixed or Single precision floating point	One 27 x 27	1
Fixed point FFTs	One 19 x 36 with external adder	1
Very high precision fixed point	One 36 x 36 with external adder	2
Double precision floating point	One 54 x 54 with external adder	4

Table 16: Number of Multipliers in Arria 10 Devices

The table lists the variable-precision DSP resources by bit precision for each Arria 10 device.

Variant	Product Line	Variable-precision DSP Block	Independent Input and Output Multiplications Operator		Peak Giga Floating-Point Operations per Second (GFLOPs)	Single-Precision Floating-Point Adders	18 x 19 Multiplier Adder Mode	18 x 18 Multiplier Adder Summed with 36 bit Input
			18 x 19 Multiplier	27 x 27 Multiplier				
Arria 10 GX	GX 160	156	312	156	140	156	156	156
	GX 220	192	384	192	173	192	192	192
	GX 270	830	1,660	830	720	830	830	830
	GX 320	985	1,970	985	887	985	985	985
	GX 480	1,369	2,738	1,369	1,231	1,369	1,369	1,369
	GX 570	1,523	3,046	1,523	1,371	1,523	1,523	1,523
	GX 660	1,688	3,376	1,688	1,510	1,688	1,688	1,688
	GX 900	1,518	3,036	1,518	1,366	1,518	1,518	1,518
	GX 1150	1,518	3,036	1,518	1,366	1,518	1,518	1,518
Arria 10 GT	GT 900	1,518	3,036	1,518	1,366	1,518	1,518	1,518
	GT 1150	1,518	3,036	1,518	1,366	1,518	1,518	1,518
Arria 10 SX	SX 160	156	312	156	140	156	156	156
	SX 220	192	384	192	173	192	192	192
	SX 270	830	1,660	830	720	830	830	830
	SX 320	985	1,970	985	887	985	985	985
	SX 480	1,369	2,738	1,369	1,231	1,369	1,369	1,369
	SX 570	1,523	3,046	1,523	1,371	1,523	1,523	1,523
	SX 660	1,688	3,376	1,688	1,510	1,688	1,688	1,688

Embedded Memory Blocks

The embedded memory blocks in the devices are flexible and designed to provide an optimal amount of small- and large-sized memory arrays to fit your design requirements.

Types of Embedded Memory

The Arria 10 devices contain two types of memory blocks:

- 20 Kb M20K blocks—blocks of dedicated memory resources. The M20K blocks are ideal for larger memory arrays while still providing a large number of independent ports.
- 640 bit memory logic array blocks (MLABs)—enhanced memory blocks that are configured from dual-purpose logic array blocks (LABs). The MLABs are ideal for wide and shallow memory arrays. The MLABs are optimized for implementation of shift registers for digital signal processing (DSP) applications, wide and shallow FIFO buffers, and filter delay lines. Each MLAB is made up of ten adaptive logic modules (ALMs). In the Arria 10 devices, you can configure these ALMs as ten 32 x 2 blocks, giving you one 32 x 20 simple dual-port SRAM block per MLAB.

Embedded Memory Capacity in Arria 10 Devices

Table 17: Embedded Memory Capacity and Distribution in Arria 10 Devices

Variant	Product Line	M20K		MLAB		Total RAM Bit (Kb)
		Block	RAM Bit (Kb)	Block	RAM Bit (Kb)	
Arria 10 GX	GX 160	440	8,800	1,680	1,050	9,850
	GX 220	588	11,760	2,932	1,833	13,593
	GX 270	750	15,000	3,922	2,451	17,451
	GX 320	891	17,820	4,582	2,864	20,684
	GX 480	1,438	28,760	7,046	4,404	33,164
	GX 570	1,800	36,000	8,153	5,096	41,096
	GX 660	2,133	42,620	9,260	5,788	48,448
	GX 900	2,423	48,460	15,017	9,386	57,846
	GX 1150	2,713	54,260	20,774	12,984	67,244
Arria 10 GT	GT 900	2,423	48,460	15,017	9,386	57,846
	GT 1150	2,713	54,260	20,774	12,984	67,244
Arria 10 SX	SX 160	440	8,800	1,680	1,050	9,850
	SX 220	588	11,760	2,932	1,833	13,593
	SX 270	750	15,000	3,922	2,451	17,451
	SX 320	891	17,820	4,582	2,864	20,684
	SX 480	1,438	28,760	7,046	4,404	33,164
	SX 570	1,800	36,000	8,153	5,096	41,096
	SX 660	2,133	42,620	9,260	5,788	48,448

Embedded Memory Configurations

Table 18: Supported Embedded Memory Block Configurations for Arria 10 Devices

This table lists the maximum configurations supported for the embedded memory blocks. The information is applicable only to the single-port RAM and ROM modes.

Memory Block	Depth (bits)	Programmable Width
MLAB	32	x16, x18, or x20
	64(10)	x8, x9, x10
M20K	512	x40, x32
	1K	x20, x16
	2K	x10, x8
	4K	x5, x4
	8K	x2
	16K	x1

Clock Networks and PLL Clock Sources

The clock network architecture is based on Altera's global, regional, and peripheral clock structure. This clock structure is supported by dedicated clock input pins, fractional clock synthesis PLLs, and integer I/O PLLs.

Clock Networks

The Arria 10 core clock networks are capable of up to 800 MHz fabric operation across the full industrial temperature range. For the external memory interface, the clock network supports the hard memory controller with speeds up to 2,666 Mbps in a quarter-rate transfer.

To reduce power consumption, the Quartus II software identifies all unused sections of the clock network and powers them down.

Fractional Synthesis and I/O PLLs

Arria 10 devices contain up to 32 fractional synthesis PLLs and up to 16 I/O PLLs that are available for both specific and general purpose uses in the core:

- Fractional synthesis PLLs - located in the column adjacent to the transceiver blocks
- I/O PLLs - located in each bank of the 48 I/Os

Fractional Synthesis PLLs

You can use the fractional synthesis PLLs to:

- Reduce the number of oscillators that are required on your board
- Reduce the number of clock pins that are used in the device by synthesizing multiple clock frequencies from a single reference clock source

(10) Supported through software emulation and consumes additional MLAB blocks.

The fractional synthesis PLLs support the following features:

- Reference clock frequency synthesis for transceiver CMU and Advanced Transmit (ATX) PLLs
- Clock network delay compensation
- Zero-delay buffering
- Direct transmit clocking for transceivers
- Independently configurable into two modes:
  - Conventional integer mode equivalent to the general purpose PLL
  - Enhanced fractional mode with third order delta-sigma modulation
- PLL cascading

I/O PLLs

The integer mode I/O PLLs are located in each bank of 48 I/Os. You can use the I/O PLLs to simplify the design of external memory and high-speed LVDS interfaces.

In each I/O bank, the I/O PLLs are adjacent to the hard memory controllers and LVDS SERDES. Because these PLLs are tightly coupled with the I/Os that need to use them, it makes it easier to close timing.

You can use the I/O PLLs for general purpose applications in the core such as clock network delay compensation and zero-delay buffering.

Arria 10 devices support PLL-to-PLL cascading.

FPGA General Purpose I/O

Arria 10 devices offer highly configurable GPIOs. Each I/O bank contains 48 general purpose I/Os and a high-efficiency hard memory controller.

The following list describes the features of the GPIOs:

- Consist of 3 V I/Os for high-voltage application and LVDS I/Os for differential signaling
- Support a wide range of single-ended and differential I/O interfaces
- LVDS speeds up to 1.6 Gbps
- Each LVDS pair of pins has differential input and output buffers, allowing you to configure the LVDS direction for each pair.
- Programmable bus hold and weak pull-up
- Programmable differential output voltage (V_{OD}) and programmable pre-emphasis
- Series (R_S) and parallel (R_T) on-chip termination (OCT) for all I/O banks with OCT calibration to limit the termination impedance variation
- On-chip dynamic termination that has the ability to swap between series and parallel termination, depending on whether there is read or write on a common bus for signal integrity
- Easy timing closure support using the hard read FIFO in the input register path, and delay-locked loop (DLL) delay chain with fine and coarse architecture

External Memory Interface

Arria 10 devices offer massive external memory bandwidth, with up to seven 32-bit DDR4 memory interfaces running at up to 2,666 Mbps. This bandwidth provides additional ease of design, lower power, and resource efficiencies of hardened high-performance memory controllers.

The memory interface within Arria 10 FPGAs and SoCs delivers the highest performance and ease of use. You can configure up to a maximum width of 144 bits when using the hard or soft memory controllers. If required, you can bypass the hard memory controller and use a soft controller implemented in the user logic.

Each I/O contains a hardened DDR read/write path (PHY) capable of performing key memory interface functionality such as read/write leveling, FIFO buffering to lower latency and improve margin, timing calibration, and on-chip termination.

The timing calibration is aided by the inclusion of hard microcontrollers based on Altera's Nios® II technology, specifically tailored to control the calibration of multiple memory interfaces. This calibration allows the Arria 10 device to compensate for any changes in process, voltage, or temperature either within the Arria 10 device itself, or within the external memory device. The advanced calibration algorithms ensure maximum bandwidth and robust timing margin across all operating conditions.

In addition to parallel memory interfaces, Arria 10 devices support serial memory technologies such as the Hybrid Memory Cube (HMC). The HMC is supported by the Arria 10 high-speed serial transceivers which connect up to four HMC links, with each link running at data rates up to 15 Gbps.

Related Information

External Memory Interface Spec Estimator
Provides a parametric tool that allows you to find and compare the performance of the supported external memory interfaces in Altera devices.

Memory Standards Supported by Arria 10 Devices

The I/Os are designed to provide high performance support for existing and emerging external memory standards.

Table 19: Memory Standards Supported by the Hard Memory Controller

This table lists the overall capability of the hard memory controller. For specific details, refer to the External Memory Interface Spec Estimator.

Memory Standard	Rate Support	Ping Pong PHY Support	Maximum Frequency (MHz)
DDR4 SDRAM	Quarter rate	Yes	1,067
		—	1,333
DDR3 SDRAM	Half rate	Yes	533
		—	667
	Quarter rate	Yes	1,067
		—	1,067
DDR3L SDRAM	Half rate	Yes	533
		—	667
	Quarter rate	Yes	933
		—	933

Table 20: Memory Standards Supported by the Soft Memory Controller

Memory Standard	Rate Support	Maximum Frequency (MHz)
RLDRAM 3 (11)	Quarter rate	1,200
QDR IV SRAM(11)	Quarter rate	1,067
QDR II/II+/II+ Xtreme SRAM	Full rate	333
	Half rate	633

Table 21: Memory Standards Supported by the HPS Hard Memory Controller

The hard processor system (HPS) is available in Arria 10 SoC devices only.

Memory Standard	Rate Support	Maximum Frequency (MHz)
DDR4 SDRAM	Half rate	1,333
DDR3 SDRAM	Half rate	1,067
DDR3L SDRAM	Half rate	933

Related Information

Arria 10 Device Datasheet
Lists the memory interface performance according to memory interface standards, rank or chip select configurations, and Arria 10 device speed grades.

PCIe Gen1, Gen2, and Gen3 Hard IP

Arria 10 devices contain PCIe hard IP that is designed for performance and ease-of-use:

- Includes all layers of the PCIe stack—transaction, data link and physical layers.
- Supports PCIe Gen3, Gen2, and Gen1 Endpoint and Root Port in x1, x2, x4, or x8 lane configuration.
- Operates independently from the core logic—optional configuration via protocol (CvP) allows the PCIe link to power up and complete link training in less than 100 ms while the Arria 10 device completes loading the programming file for the rest of the FPGA.
- Provides added functionality that makes it easier to support emerging features such as Single Root I/O Virtualization (SR-IOV) and optional protocol extensions.
- Provides improved end-to-end datapath protection using ECC.
- Supports FPGA configuration via protocol (CvP) using PCIe at Gen3, Gen2, or Gen1 speed.

(11) Arria 10 devices support this external memory interface using hard PHY with soft memory controller.

Related Information

PCS Features on page 33

Enhanced PCS Hard IP for Interlaken and 10 Gbps Ethernet

Interlaken Support

The Arria 10 enhanced PCS hard IP provides integrated Interlaken PCS supporting rates up to 17.4 Gbps per lane.

The Interlaken PCS is based on the proven functionality of the PCS developed for Altera's previous generation FPGAs, which demonstrated interoperability with Interlaken ASSP vendors and third-party IP suppliers. The Interlaken PCS is present in every transceiver channel in Arria 10 devices.

Related Information

PCS Features on page 33

10 Gbps Ethernet Support

The Arria 10 enhanced PCS hard IP supports 10GBASE-R PCS compliant with IEEE 802.3 10 Gbps Ethernet (10GbE). The integrated hard IP support for 10GbE and the 10 Gbps transceivers save external PHY cost, board space, and system power.

The scalable hard IP supports multiple independent 10GbE ports while using a single PLL for all the 10GBASE-R PCS instantiations, which saves on core logic resources and clock networks:

- Simplifies multiport 10GbE systems compared to XAUI interfaces that require an external XAUI-to-10G PHY.
- Incorporates Electronic Dispersion Compensation (EDC), which enables direct connection to standard 10 Gbps XFP and SFP+ pluggable optical modules.
- Supports backplane Ethernet applications and includes a hard 10GBASE-KR Forward Error Correction (FEC) circuit that you can use for 10 Gbps and 40 Gbps applications.

The 10 Gbps Ethernet PCS hard IP and 10GBASE-KR FEC are present in every transceiver channel.

Related Information

PCS Features on page 33

Low Power Serial Transceivers

Arria 10 FPGAs and SoCs include lowest power transceivers that deliver high bandwidth, throughput and low latency.

Arria 10 devices deliver the industry's lowest power consumption per transceiver channel:

- 12.5 Gbps transceivers at as low as 242 mW
- 10 Gbps transceivers at as low as 168 mW
- 6 Gbps transceivers at as low as 117 mW

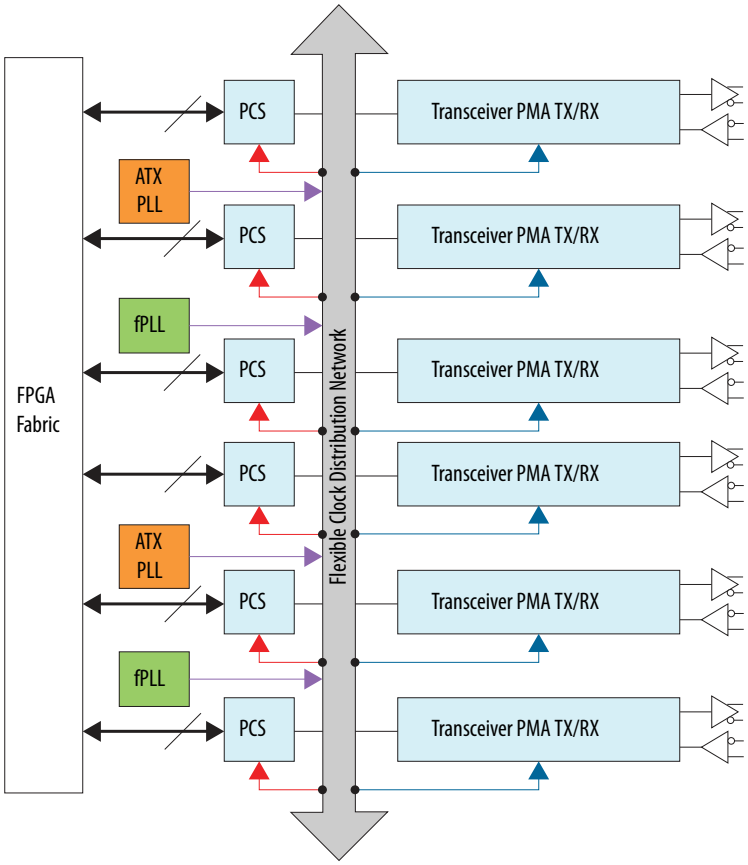
Arria 10 transceivers support various data rates according to application:

- Chip-to-chip and chip-to-module applications—from 125 Mbps up to 28.3 Gbps
- Long reach and backplane applications—from 125 Mbps up to 17.4 Gbps with advanced adaptive equalization
- Critical power sensitive applications—from 125 Mbps up to 11.3 Gbps using lower power modes

The combination of 20 nm process technology and architectural advances provide the following benefits:

- Significant reduction in die area and power consumption
- Increase of up to two times in transceiver I/O density compared to previous generation devices while maintaining optimal signal integrity
- Up to 96 total transceiver channels—you can configure up to 16 of these channels to run as fast as 28.3 Gbps
- All channels feature continuous data rate support up to the maximum rated speed

Figure 6: Arria 10 Transceiver Block Architecture



Transceiver Channels

All transceiver channels feature a dedicated Physical Medium Attachment (PMA) and a hardened Physical Coding Sublayer (PCS).

- The PMA provides primary interfacing capabilities to physical channels.
- The PCS typically handles encoding/decoding, word alignment, and other pre-processing functions before transferring data to the FPGA core fabric.

A transceiver channel consists of a PMA and a PCS block. Most transceiver banks have 6 channels. There are some transceiver banks which contain only 3 channels.

A wide variety of bonded and non-bonded data rate configurations is possible using a highly configurable clock distribution network. Up to 80 independent transceiver data rates can be configured.

The following figures are graphical representations of a top view of the silicon die, which corresponds to a reverse view for flip chip packages. Different Arria 10 devices may have different floorplans than the ones shown in the figures.

Figure 7: Device Chip Overview for Arria 10 GX and GT Devices

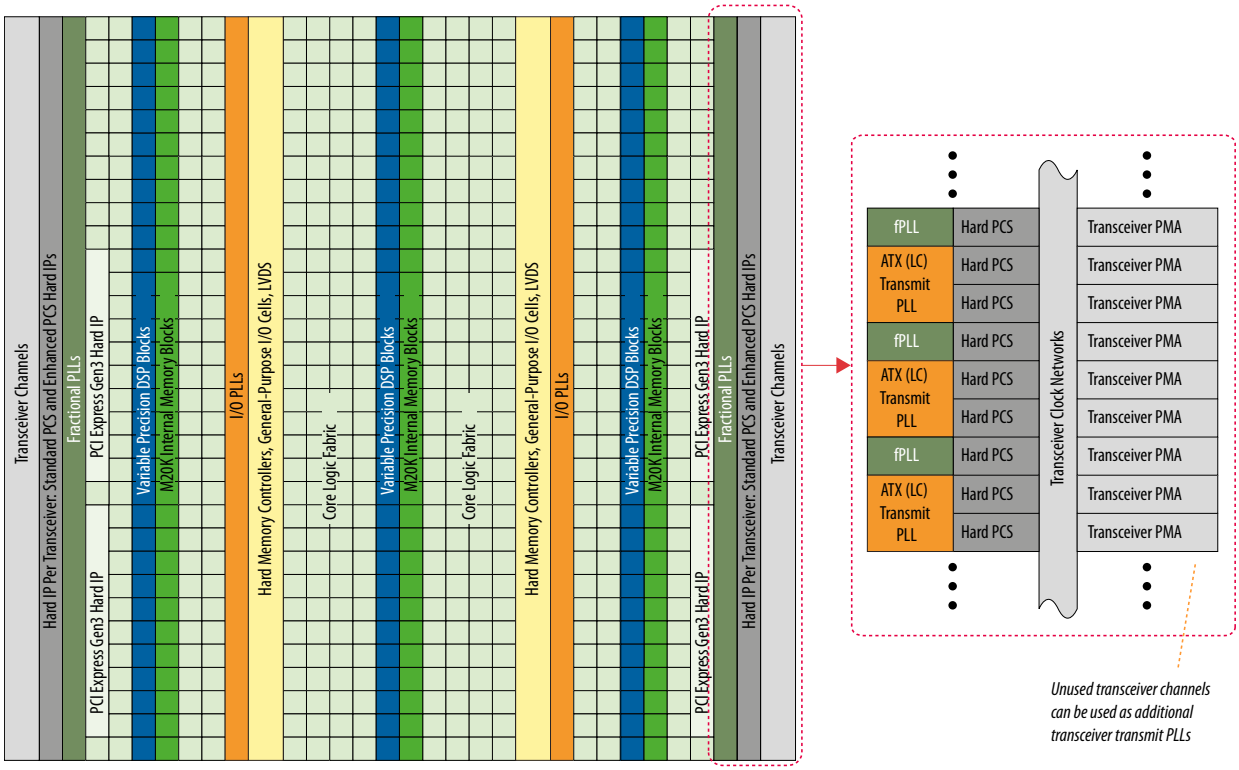
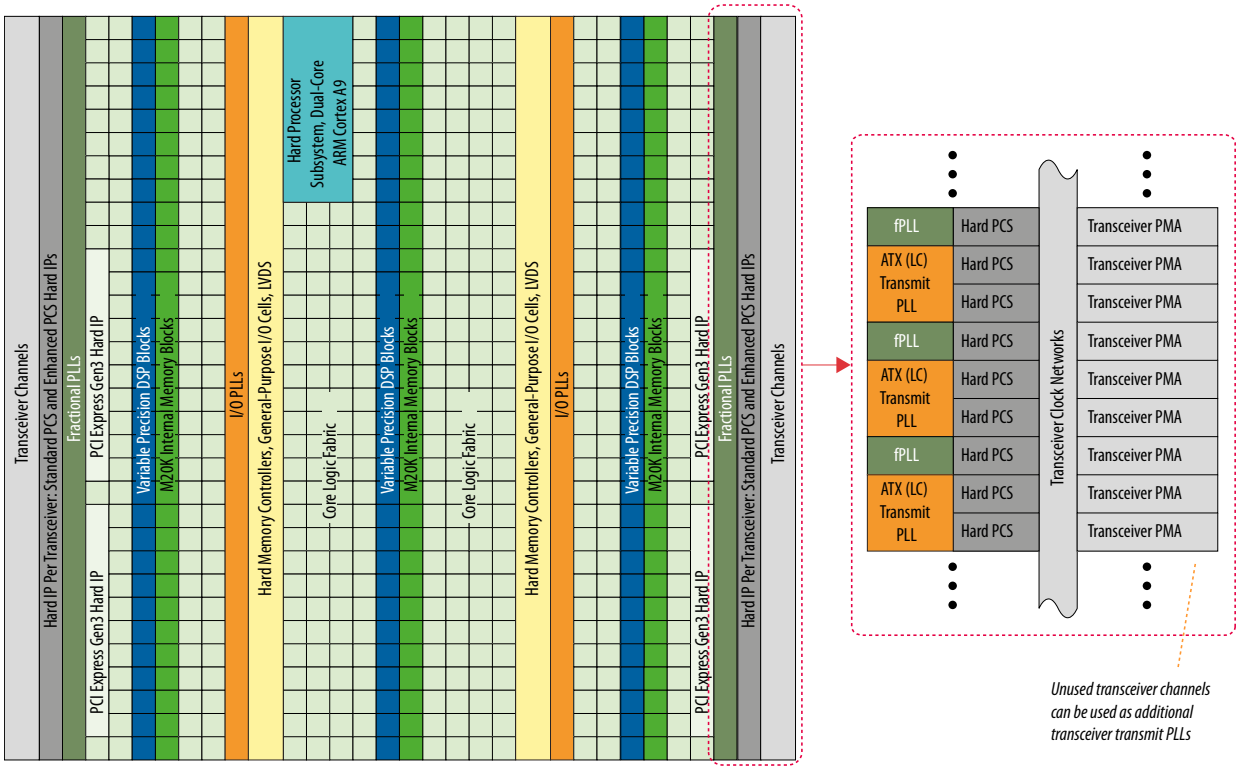


Figure 8: Device Chip Overview for Arria 10 SX Devices



PMA Features

Arria 10 transceivers provide exceptional signal integrity at data rates up to 28.3 Gbps. Clocking options include ultra-low jitter ATX PLLs (LC tank based), clock multiplier unit (CMU) PLLs, and fractional PLLs.

Each transceiver channel contains a channel PLL that can be used as the CMU PLL or clock data recovery (CDR) PLL. In CDR mode, the channel PLL recovers the receiver clock and data in the transceiver channel. Up to 80 independent data rates can be configured on a single Arria 10 device.

Table 22: PMA Features of the Transceivers in Arria 10 Devices

Feature	Capability
Chip-to-Chip Data Rates	125 Mbps to 17.4 Gbps (Arria 10 GX devices) 125 Mbps to 28.3 Gbps (Arria 10 GT devices)
Backplane Support	Drive backplanes at data rates up to 17.4 Gbps, including 10GBASE-KR compliance
Optical Module Support	SFP+/SFP, XFP, CXP, QSFP/QSFP28, CFP/CFP2/CFP4

Feature	Capability
Cable Driving Support	SFP+ Direct Attach, PCI Express over cable, eSATA
Transmit Pre-Emphasis	4-tap transmit pre-emphasis and de-emphasis to compensate for system channel loss
Continuous Time Linear Equalizer (CTLE)	Dual mode, high-gain, and high-data rate, linear receive equalization to compensate for system channel loss
Decision Feedback Equalizer (DFE)	7-fixed and 4-floating tap DFE to equalize backplane channel loss in the presence of crosstalk and noisy environments
Variable Gain Amplifier	Optimizes the signal amplitude prior to the CDR sampling and operates in fixed and adaptive modes
Altera Digital Adaptive Parametric Tuning (ADAPT)	Fully digital adaptation engine to automatically adjust all link equalization parameters—including CTLE, DFE, and variable gain amplifier blocks—that provide optimal link margin without intervention from user logic
Precision Signal Integrity Calibration Engine (PreSICE)	Hardened calibration controller to quickly calibrate all transceiver control parameters on power-up, which provides the optimal signal integrity and jitter performance
Advanced Transmit (ATX) PLL	Low jitter ATX (LC tank based) PLLs with continuous tuning range to cover a wide range of standard and proprietary protocols
Fractional PLLs	On-chip fractional frequency synthesizers to replace on-board crystal oscillators and reduce system cost
Digitally Assisted Analog CDR	Superior jitter tolerance with fast lock time
On-Die Instrumentation— EyeQ and Jitter Margin Tool	Simplifies board bring-up, debug, and diagnostics with non-intrusive, high-resolution eye monitoring (EyeQ). Also injects jitter from transmitter to test link margin in system.
Dynamic Partial Reconfiguration	Allows independent control of the Avalon memory-mapped interface of each transceiver channel for the highest transceiver flexibility
Multiple PCS-PMA and PCS-PLD interface widths	8-, 10-, 16-, 20-, 32-, 40-, or 64-bit interface widths for flexibility of deserialization width, encoding, and reduced latency

PCS Features

This table summarizes the Arria 10 transceiver PCS features. You can use the transceiver PCS to support a wide range of protocols ranging from 125 Mbps to 28.3 Gbps.

PCS	Description
Standard PCS	• Operates at a data rate up to 12 Gbps • Supports protocols such as PCI-Express, CPRI 4.2+, GigE, IEEE 1588 in Hard PCS • Implements other protocols using Basic/Custom (Standard PCS) transceiver configuration rules.
Enhanced PCS	• Performs functions common to most serial data industry standards, such as word alignment, encoding/decoding, and framing, before data is sent or received off-chip through the PMA • Handles data transfer to and from the FPGA fabric • Handles data transfer internally to and from the PMA • Provides frequency compensation • Performs channel bonding for multi-channel low skew applications
PCIe Gen3 PCS	• Supports the seamless switching of Data and Clock between the Gen1, Gen2, and Gen3 data rates • Provides support for PIPE 3.0 features • Supports the PIPE interface with the Hard IP enabled, as well as with the Hard IP bypassed

Related Information

- **PCIe Gen1, Gen2, and Gen3 Hard IP** on page 27
- **Interlaken Support** on page 28
- **10 Gbps Ethernet Support** on page 28

PCS Protocol Support

This table lists some of the protocols supported by the Arria 10 transceiver PCS. For more information about the blocks in the transmitter and receiver data paths, refer to the related information.

Protocol	Data Rate (Gbps)	Transceiver IP	PCS Support
PCIe Gen3 x1, x2, x4, x8	8.0	Native PHY (PIPE)	Standard PCS and PCIe Gen3 PCS
PCIe Gen2 x1, x2, x4, x8	5.0	Native PHY (PIPE)	Standard PCS
PCIe Gen1 x1, x2, x4, x8	2.5	Native PHY (PIPE)	Standard PCS
1000BASE-X Gigabit Ethernet	1.25	Native PHY	Standard PCS

Protocol	Data Rate (Gbps)	Transceiver IP	PCS Support
1000BASE-X Gigabit Ethernet with 1588	1.25	Native PHY	Standard PCS
10GBASE-R	10.3125	Native PHY	Enhanced PCS
10GBASE-R 1588	10.3125	Native PHY	Enhanced PCS
10GBASE-R with KR FEC	10.3125	Native PHY	Enhanced PCS
10GBASE-KR and 1000BASE-X	10.3125	1G/10GbE and 10GBASE-KR PHY	Standard PCS and Enhanced PCS
Interlaken (CEI-6G/11G)	3.125 to 17.4	Native PHY	Enhanced PCS
SFI-S/SFI-5.2	11.2	Native PHY	Enhanced PCS
10G SDI	10.692	Native PHY	Enhanced PCS
CPRI 6.0 (64B/66B)	0.6144 to 10.1376	Native PHY	Enhanced PCS
CPRI 4.2 (8B/10B)	0.6144 to 9.8304	Native PHY	Standard PCS
OBSAI RP3 v4.2	0.6144 to 6.144	Native PHY	Standard PCS
SD-SDI/HD-SDI/3G-SDI	0.143[12] to 2.97	Native PHY	Standard PCS

Related Information

Arria 10 Transceiver PHY User Guide
Provides more information about the supported transceiver protocols and PHY IP, the PMA architecture, and the standard, enhanced, and PCIe Gen3 PCS architecture.

SoC with Hard Processor System

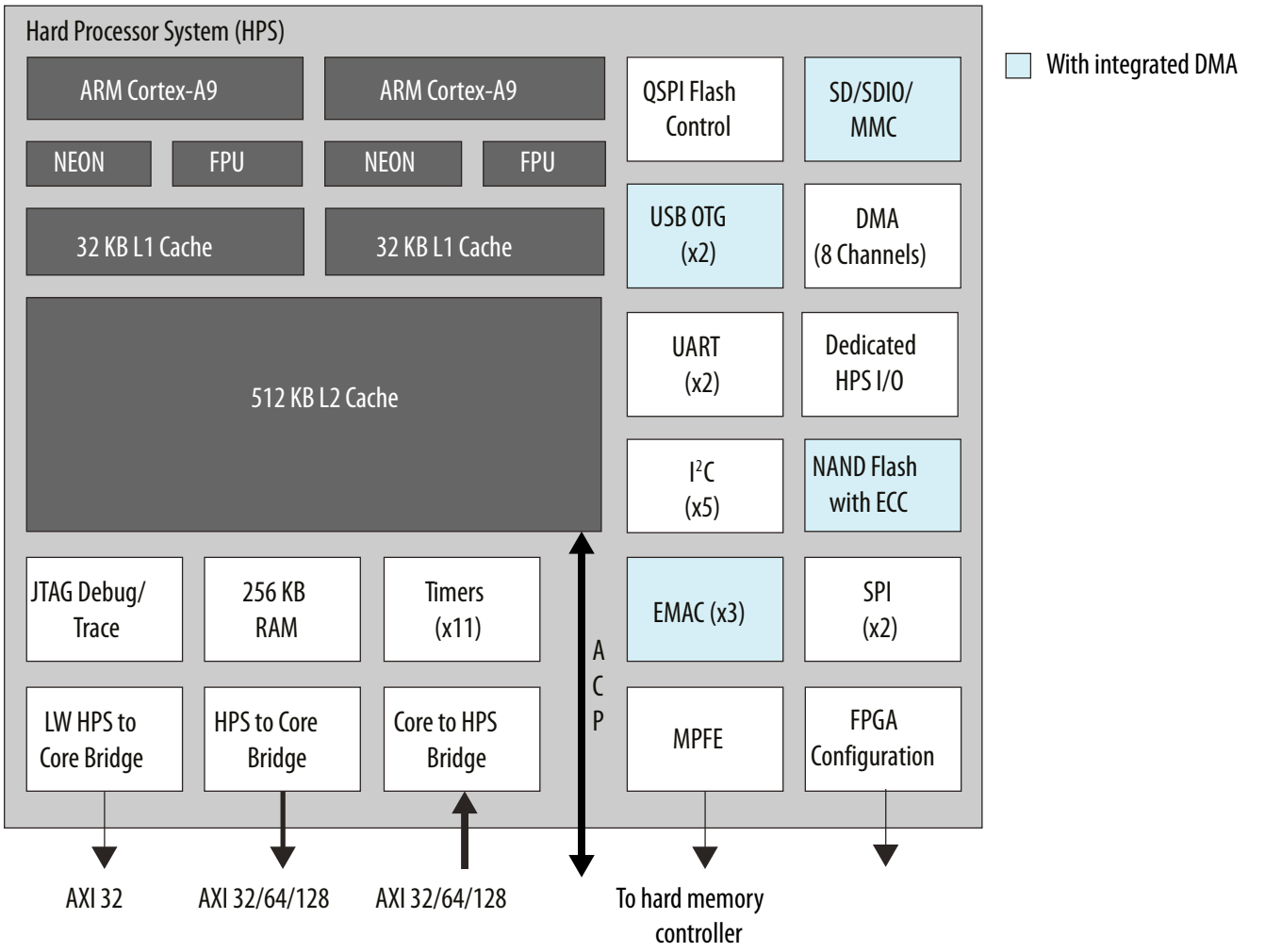
Each SoC device combines an FPGA fabric and a hard processor system (HPS) in a single device. This combination delivers the flexibility of programmable logic with the power and cost savings of hard IP in these ways:

- Reduces board space, system power, and bill of materials cost by eliminating a discrete embedded processor
- Allows you to differentiate the end product in both hardware and software, and to support virtually any interface standard
- Extends the product life and revenue through in-field hardware and software updates

[12] The 0.143 Gbps data rate is supported using oversampling of user logic that you must implement in the FPGA fabric.

Figure 9: HPS Block Diagram

This figure shows a block diagram of the HPS with the dual ARM Cortex-A9 MPCore processor.



Key Advantages of 20-nm HPS

The 20-nm HPS strikes a balance between enabling maximum software compatibility with 28-nm SoCs while still improving upon the 28-nm HPS architecture. These improvements address the requirements of the next generation target markets such as wireless and wireline communications, compute and storage equipment, broadcast and military in terms of performance, memory bandwidth, connectivity via backplane and security.

Table 23: Improvements in 20 nm HPS

This table lists the key improvements of the 20 nm HPS compared to the 28 nm HPS.

Advantages/Improvements	Description
Increased performance and overdrive capability	While the nominal processor frequency is 1.2 GHz, the 20 nm HPS offers an "overdrive" feature which enables a higher processor operating frequency. This requires a higher supply voltage value that is unique to the HPS and may require a separate regulator.
Increased processor memory bandwidth and DDR4 support	Up to 64-bit DDR4 memory at 2,666 Mbps support is available for the processor. The hard memory controller for the HPS comprises a multi-port front end that manages connections to a single port memory controller. The multi-port front end allows logic core and the HPS to share ports and thereby the available bandwidth of the memory controller.
Flexible I/O sharing	An advanced I/O pin muxing scheme allows improved sharing of I/O between the HPS and the core logic. The following types of I/O are available for SoC: • 17 dedicated I/Os—physically located inside the HPS block and are not accessible to logic within the core. The 17 dedicated I/Os are used for HPS clock, resets, and interfacing with boot devices, QSPI, and SD/MMC. • 48 direct shared I/O—located closest to the HPS block and are ideal for high speed HPS peripherals such as EMAC, USB, and others. There is one bank of 48 I/Os that supports direct sharing where the 48 I/Os can be shared 12 I/Os at a time. • Standard (shared) I/O—all standard I/Os can be shared by the HPS peripherals and any logic within the core. For designs where more than 48 I/Os are required to fully use all the peripherals in the HPS, these I/Os can be connected through the core logic.
EMAC core	Three EMAC cores are available in the HPS. The EMAC cores enable an application to support two redundant Ethernet connections; for example, backplane, or two EMAC cores for managing IEEE 1588 time stamp information while allowing a third EMAC core for debug and configuration. All three EMACs can potentially share the same time stamps, simplifying the 1588 time stamping implementation. A new serial time stamp interface allows core logic to access and read the time stamp values. The integrated EMAC controllers can be connected to external Ethernet PHY through the provided MDIO or I^2C interface.
On-chip memory	The on-chip memory is updated to 256 KB support and can support larger data sets and real time algorithms.

Advantages/Improvements	Description
ECC enhancements	Improvements in L2 Cache ECC management allow identification of errors down to the address level. ECC enhancements also enable improved error injection and status reporting via the introduction of new memory mapped access to syndrome and data signals.
HPS to FPGA Interconnect Backbone	Although the HPS and the Logic Core can operate independently, they are tightly coupled via a high-bandwidth system interconnect built from high-performance ARM AMBA AXI bus bridges. IP bus masters in the FPGA fabric have access to HPS bus slaves via the FPGA-to-HPS interconnect. Similarly, HPS bus masters have access to bus slaves in the core fabric via the HPS-to-FPGA bridge. Both bridges are AMBA AXI-3 compliant and support simultaneous read and write transactions. Up to three masters within the core fabric can share the HPS SDRAM controller with the processor. Additionally, the processor can be used to configure the core fabric under program control via a dedicated 32-bit configuration port.
FPGA configuration and HPS booting	The FPGA fabric and HPS in the SoCs are powered independently. You can reduce the clock frequencies or gate the clocks to reduce dynamic power. You can configure the FPGA fabric and boot the HPS independently, in any order, providing you with more design flexibility.
Security	New security features have been introduced for anti-tamper management, secure boot, encryption (AES), and authentication (SHA).

Features of the HPS

The HPS has the following features:

- 1.2-GHz, dual-core ARM Cortex-A9 MPCore processor with up to 1.5-GHz via overdrive
  - ARMv7-A architecture that runs 32-bit ARM instructions, 16-bit and 32-bit Thumb instructions, and 8-bit Java byte codes in Jazelle style
  - Superscalar, variable length, out-of-order pipeline with dynamic branch prediction
  - Instruction Efficiency 2.5 MIPS/MHz, which provides total performance of 7500 MIPS at 1.5 GHz
- Each processor core includes:
  - 32 KB of L1 instruction cache, 32 KB of L1 data cache
  - Single- and double-precision floating-point unit and NEON media engine
  - CoreSight debug and trace technology
  - Snoop Control Unit (SCU) and Acceleration Coherency Port (ACP)
- 512 KB of shared L2 cache
- 256 KB of scratch RAM

- Hard memory controller with support for DDR3, DDR4 and optional error correction code (ECC) support
- Multiport Front End (MPFE) Scheduler interface to the hard memory controller
- 8-channel direct memory access (DMA) controller
- QSPI flash controller with SIO, DIO, QIO SPI Flash support
- NAND flash controller (ONFI 1.0 or later) with DMA and ECC support, updated to support 8 and 16-bit Flash devices and new command DMA to offload CPU for fast power down recovery
- Updated SD/SDIO/MMC controller to eMMC 4.5 with DMA with CE-ATA digital command support
- 3 10/100/1000 Ethernet media access control (MAC) with DMA
- 2 USB On-the-Go (OTG) controllers with DMA
- 5 I^2C controllers (3 can be used by EMAC for MIO to external PHY)
- 2 UART 16550 Compatible controllers
- 4 serial peripheral interfaces (SPI) (2 Master, 2 Slaves)
- 62 programmable general-purpose I/Os, which includes 48 direct share I/Os that allows the HPS peripherals to connect directly to the FPGA I/Os
- 7 general-purpose timers
- 4 watchdog timers
- Anti-tamper, Secure Boot, Encryption (AES) and Authentication (SHA)

System Peripherals and Debug Access Port

Each Ethernet MAC, USB OTG, NAND flash controller, and SD/MMC controller module has an integrated DMA controller. For modules without an integrated DMA controller, an additional DMA controller module provides up to eight channels of high-bandwidth data transfers. Peripherals that communicate off-chip are multiplexed with other peripherals at the HPS pin level. This allows you to choose which peripherals interface with other devices on your PCB.

The debug access port provides interfaces to industry standard JTAG debug probes and supports ARM CoreSight debug and core traces to facilitate software development.

HPS–FPGA AXI Bridges

The HPS–FPGA bridges, which support the Advanced Microcontroller Bus Architecture (AMBA) Advanced eXtensible Interface (AXI™) specifications, consist of the following bridges:

- FPGA-to-HPS AMBA AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the FPGA fabric to issue transactions to slaves in the HPS.
- HPS-to-FPGA Avalon/AMBA AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the HPS to issue transactions to slaves in the FPGA fabric.
- Lightweight HPS-to-FPGA AXI bridge—a lower latency 32 bit width bus that allows the HPS to issue transactions to soft peripherals in the FPGA fabric. This bridge is primarily used for control and status register (CSR) accesses to peripherals in the FPGA fabric.

The HPS–FPGA AXI bridges allow masters in the FPGA fabric to communicate with slaves in the HPS logic, and vice versa. For example, the HPS-to-FPGA AXI bridge allows you to share memories instantiated in the FPGA fabric with one or both microprocessors in the HPS, while the FPGA-to-HPS AXI bridge allows logic in the FPGA fabric to access the memory and peripherals in the HPS.

Each HPS–FPGA bridge also provides asynchronous clock crossing for data transferred between the FPGA fabric and the HPS.

HPS SDRAM Controller Subsystem

The HPS SDRAM controller subsystem contains a multiport SDRAM controller and DDR PHY that are shared between the FPGA fabric (through the FPGA-to-HPS SDRAM interface), the level 2 (L2) cache, and the level 3 (L3) system interconnect. The FPGA-to-HPS SDRAM interface supports AMBA AXI and Avalon® Memory-Mapped (Avalon-MM) interface standards, and provides up to six individual ports for access by masters implemented in the FPGA fabric.

The HPS SDRAM controller supports up to 3 masters (command ports), 3x 64-bit read data ports and 3x 64-bit write data ports.

To maximize memory performance, the SDRAM controller subsystem supports command and data reordering, deficit round-robin arbitration with aging, and high-priority bypass features.

FPGA Configuration and HPS Booting

The FPGA fabric and HPS in the SoC FPGA are powered independently. You can reduce the clock frequencies or gate the clocks to reduce dynamic power.

The HPS and FPGA portions of the device supports two power supply options:

- Both the FPGA portion and the HPS are powered ON.
- The FPGA portion is powered ON and the HPS is powered OFF.

You can configure the FPGA fabric and boot the HPS independently, in any order, providing you with more design flexibility:

- You can boot the HPS independently. After the HPS is running, the HPS can fully or partially reconfigure the FPGA fabric at any time under software control. The HPS can also configure other FPGAs on the board through the FPGA configuration controller.
- You can power up both the HPS and the FPGA fabric together, configure the FPGA fabric first, and then boot the HPS from memory accessible to the FPGA fabric.

Hardware and Software Development

For hardware development, you can configure the HPS and connect your soft logic in the FPGA fabric to the HPS interfaces using the Qsys system integration tool in the Quartus II software.

For software development, the ARM-based SoC FPGA devices inherit the rich software development ecosystem available for the ARM Cortex-A9 MPCore processor. The software development process for Altera SoC FPGAs follows the same steps as those for other SoC devices from other manufacturers. Support for Linux, VxWorks®, and other operating systems will be available for the SoC FPGAs. For more information on the operating systems support availability, contact the Altera sales team.

You can begin device-specific firmware and software development on the Altera SoC FPGA Virtual Target. The Virtual Target is a fast PC-based functional simulation of a target development system—a model of a complete development board. The Virtual Target enables the development of device-specific production software that can run unmodified on actual hardware.

Dynamic and Partial Reconfiguration

The Arria 10 devices support dynamic and partial reconfiguration. You can use dynamic and partial reconfiguration simultaneously to enable seamless reconfiguration of both the device core and transceivers.

Dynamic Reconfiguration

You can reconfigure the PMA and PCS blocks while the device continues to operate. This feature allows you to change the data rates, protocol, and analog settings of a channel in a transceiver bank without affecting on-going data transfer in other transceiver banks. This feature is ideal for applications that require dynamic multiprotocol or multirate support.

Partial Reconfiguration

Using partial reconfiguration, you can reconfigure some parts of the device while keeping the device in operation.

Instead of placing all device functions in the FPGA fabric, you can store some functions that do not run simultaneously in external memory and load them only when required. This capability increases the effective logic density of the device, and lowers cost and power consumption.

In the Altera® solution, you do not have to worry about intricate device architecture to perform a partial reconfiguration. The partial reconfiguration capability is built into the Quartus II design software, making such time-intensive task simple.

Arria 10 devices support partial reconfiguration in the following configuration options:

- Using an internal host:
  - All supported configuration modes where the FPGA has access to external memory devices such as serial and parallel flash memory.
  - Configuration via Protocol [CvP (PCIe)]
- Using an external host—passive serial (PS), fast passive parallel (FPP) x8, FPP x16, and FPP x32 I/O interface.

Enhanced Configuration and Configuration via Protocol

Table 24: Configuration Modes and Features of Arria 10 Devices

Arria 10 devices support 1.8 V programming voltage and several configuration modes.

Mode	Data Width	Max Clock Rate (MHz)	Max Data Rate (Mbps) (13)	Decompression	Design Security	Partial Reconfiguration (14)	Remote System Update
JTAG	1 bit	33	33	—	—	—	—
Active Serial (AS) through the EPCQ-L configuration device	1 bit, 4 bits	100	400	Yes	Yes	—	Yes
Passive serial (PS) through CPLD or external microcontroller	1 bit	100	100	Yes	Yes	—	Parallel Flash Loader (PFL) IP core
Fast passive parallel (FPP) through CPLD or external microcontroller	8 bits	100	3200	Yes	Yes	Yes(15)	PFL IP core
	16 bits			Yes	Yes		
	32 bits			Yes	Yes		
Configuration via HPS	16 bits	100	3200	Yes	Yes	Yes(15)	—
	32 bits			Yes	Yes	—	
Configuration via Protocol [CvP (PCIe)]	x1, x2, x4, and x8 lanes	—	8000	Yes	Yes	Yes	—

(13) Enabling either compression, design security, or both features affects the maximum data rate. Refer to the Arria 10 Device Datasheet for more information.
(14) Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Altera for support.
(15) Supported at a maximum clock rate of 100 MHz.

You can configure Arria 10 devices through PCIe using Configuration via Protocol (CvP). The Arria 10 CvP implementation conforms to the PCIe 100 ms power-up-to-active time requirement.

SEU Error Detection and Correction

Arria 10 devices offer robust and easy-to-use single-event upset (SEU) error detection and correction circuitry.

The detection and correction circuitry includes protection for Configuration RAM (CRAM) programming bits and user memories. The CRAM is protected by a continuously running CRC error detection circuit with integrated ECC that automatically corrects one or two errors and detects higher order multi-bit errors. When more than two errors occur, correction is available through reloading of the core programming file, providing a complete design refresh while the FPGA continues to operate.

The physical layout of the Arria 10 CRAM array is optimized to make the majority of multi-bit upsets appear as independent single-bit or double-bit errors which are automatically corrected by the integrated CRAM ECC circuitry. In addition to the CRAM protection, the M20K memory blocks also include integrated ECC circuitry and are layout-optimized for error detection and correction. The MLAB does not have ECC.

Power Management

Arria 10 devices leverage the advanced 20 nm process technology, a low 0.9 V core power supply, an enhanced core architecture, and several optional power reduction techniques to reduce total power consumption by as much as 40% compared to Arria V devices and as much as 60% compared to Stratix V devices.

The optional power reduction techniques in Arria 10 devices include:

- **SmartVID**—a code is programmed into each device during manufacturing that allows a smart regulator to operate the device at lower core V_{CC} while maintaining performance
- **Programmable Power Technology**—non-critical timing paths are identified by the Quartus II software and the logic in these paths is biased for low power instead of high performance
- **V_{CC} PowerManager**—allows devices to be run at lower core voltage to trade performance for power savings
- **Low Static Power Options**—devices are available with either standard static power or low static power while maintaining performance

Furthermore, Arria 10 devices feature Altera's industry-leading low power transceivers and include a number of hard IP blocks that not only reduce logic resources but also deliver substantial power savings compared to soft implementations. In general, hard IP blocks consume up to 90% less power than the equivalent soft logic implementations.

Incremental Compilation

The Quartus II software incremental compilation feature reduces compilation time and helps preserve performance to ease timing closure. The incremental compilation feature enables the partial reconfiguration flow for Arria 10 devices.

Incremental compilation supports top-down, bottom-up, and team-based design flows. This feature facilitates modular, hierarchical, and team-based design flows where different designers compile their respective design sections in parallel. Furthermore, different designers or IP providers can develop and optimize different blocks of the design independently. These blocks can then be imported into the top level project.

Document Revision History

Date	Version	Changes
June 2015	2015.06.15	Corrected label for Arria 10 GT product lines in the vertical migration figure.
May 2015	2015.05.15	Corrected the DDR3 half rate and quarter rate maximum frequencies in the table that lists the memory standards supported by the Arria 10 hard memory controller.
May 2015	2015.05.04	• Added support for 13.5G JESD204b in the Summary of Features table. • Added a link to Arria 10 GT Channel Usage in the Arria 10 GT Package Plan topic. • Added a note to the table, Maximum Resource Counts for Arria 10 GT devices. • Updated the power requirements of the transceivers in the Low Power Serial Transceivers topic.
January 2015	2015.01.23	• Added floating point arithmetic features in the Summary of Features table. • Updated the total embedded memory from 38.38 megabits (Mb) to 65.6 Mb. • Updated the table that lists the memory standards supported by Arria 10 devices. • Removed support for DDR3U, LPDDR3 SDRAM, RLDRAM 2, and DDR2. • Moved RLDRAM 3 support from hard memory controller to soft memory controller. RLDRAM 3 support uses hard PHY with soft memory controller. • Added soft memory controller support for QDR IV. • Updated the maximum resource count table to include the number of hard memory controllers available in each device variant. • Updated the transceiver PCS data rate from 12.5 Gbps to 12 Gbps. • Updated the max clock rate of PS, FPP x8, FPP x16, and Configuration via HPS from 125 MHz to 100 MHz. • Added a feature for fractional synthesis PLLs: PLL cascading. • Updated the HPS programmable general-purpose I/Os from 54 to 62.

Date	Version	Changes
September 2014	2014.09.30	• Corrected the 3 V I/O and LVDS I/O counts for F35 and F36 packages of Arria 10 GX. • Corrected the 3 V I/O, LVDS I/O, and transceiver counts for the NF40 package of the Arria GX 570 and 660. • Removed 3 V I/O, LVDS I/O, and transceiver counts for the NF40 package of the Arria GX 900 and 1150. The NF40 package is not available for Arria 10 GX 900 and 1150.
August 2014	2014.08.18	• Updated Memory (Kb) M20K maximum resources for Arria 10 GX 660 devices from 42,660 to 42,620. • Added GPIO columns consisting of LVDS I/O Bank and 3V I/O Bank in the Package Plan table. • Added how to use memory interface clock frequency higher than 533 MHz in the I/O vertical migration. • Added information to clarify that RLDRAM3 support uses hard PHY with soft memory controller. • Added variable precision DSP blocks support for floating-point arithmetic.
June 2014	2014.06.19	Updated number of dedicated I/Os in the HPS block to 17.
February 2014	2014.02.21	Updated transceiver speed grade options for GT devices in Figure 2.
February 2014	2014.02.06	Updated data rate for Arria 10 GT devices from 28.1 Gbps to 28.3 Gbps.
December 2013	2013.12.10	• Updated the HPS memory standards support from LPDDR2 to LPDDR3. • Updated HPS block diagram to include dedicated HPS I/O and FPGA Configuration blocks as well as repositioned SD/SDIO/ MMC, DMA, SPI and NAND Flash with ECC blocks .
December 2013	2013.12.02	Initial release.

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