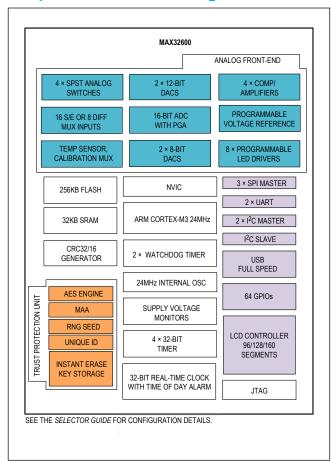
### **General Description**

The MAX32600 microcontroller is based on the industry-standard ARM® Cortex®-M3 32-bit RISC CPU operating at up to 24MHz. It includes 256KB of flash memory, 32KB of SRAM, a 2KB instruction cache, and integrated high-performance analog peripherals. The MAX32600 is available in the following package options: 192-ball, 12mm x 12mm CTBGA; 120-ball, 7mm x 7mm CTBGA; and 108-ball, 5.4mm x 4.3mm WLP.

### **Applications**

- Wearable Medical Devices
- Pulse Oximetry Measurement
- Galvanic Skin Response Measurement
- Blood Glucose Metering

### Simplified Functional Diagram



### **Benefits and Features**

- Integrated AFE Enables Precision Wellness Measurements with Minimal Discretes
  - 16-Bit ADC with Input Mux and PGA
    - Up to 500ksps Conversion Rate
    - PGA with Gain of 1, 2, 4, and 8 and Bypass Mode
    - Differential 8:1 or Single-Ended 16:1 Input Mux
    - Internal Mux Inputs for Measuring V<sub>DDA3</sub>
  - · Internal or External Voltage Reference
    - Programmable Buffers for ADC and DACs
  - Two 12-Bit DACs and Two 8-Bit DACs
  - · Four Operational Amplifiers
  - · Four Low-Power Comparators
  - · Four Uncommitted SPST Analog Switches
  - · Four Ground Switches
  - Up to Eight 100mA LED Driver Pairs (Sink)
  - · Internal Temperature Sensor
- Secure Valuable IP and Data with Robust On-Board Trust Protection Unit
  - · Trust Protection Unit for End-to-End Security
  - AES Hardware Engine
  - µMAA for ECDSA and RSA
  - · Hardware PRNG
  - Fast-Erase SRAM for Secure Key Storage
- Industry's Lowest Overall System Power Increases Battery Life
  - 175µA/MHz Active Power Executing Code from Cache
  - 1.25µA Current Consumption with Real-Time Clock Enable in LP0
  - 1.8µA Current Consumption with Data Retention and Fast 15µs Wakeup in LP1
  - · Peripheral Clock Control
  - 6-Channel DMA Engine Enables Intelligent Peripheral Operation While Micro is in Sleep Mode
- Flexible Package Options
  - 120-Ball CTBGA, 0.5mm Pitch, 7mm x 7mm
  - 192-Ball CTBGA, 0.65mm Pitch, 12mm x 12mm
  - 108-Bump WLP, 0.4mm Pitch, 5.4mm x 4.3mm

Additional Benefits and Features and Ordering Information appear at end of data sheet.

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# **Absolute Maximum Ratings**

Voltage Range on V <sub>DD</sub> and V <sub>DDA3</sub> with	Output Current (Sink) by Any I/O Pin	25mA
Respect to GND0.3V to +3.6V	Output Current (Source) by Any I/O Pin	25mA
Voltage Range on V <sub>BUS</sub> 0.3V to 5.5V	Output Current (Source) by V <sub>DDIO</sub>	100mA
Voltage Range on Any Lead with	Output Current (Sink) by LED Pins	135mA
Respect to GND (excluding V <sub>BUS</sub> )0.3V to (V <sub>DD</sub> + 0.5V)	Output Current (Source) by V <sub>REG18</sub>	50mA
Voltage Range on Analog Pins with	Operating Temperature Range	40°C to +85°C
Respect to GND0.3V to V <sub>DDA3</sub>	Storage Temperature Range	65°C to +150°C
Total Current into V <sub>DD</sub> /V <sub>DDA3</sub> Power Lines (Sink) 100mA	Soldering Temperature (reflow)	+260°C
Total Current Source V <sub>DD</sub> Power Lines (Sink)100mA		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)	
<ul> <li>108 WLP         Junction-to-Ambient Thermal Resistance (θ<sub>JA</sub>)32.99°C/W</li> <li>120 CTBGA         Junction-to-Ambient Thermal Resistance (θ<sub>JA</sub>)32°C/W         Junction-to-Case Thermal Resistance (θ<sub>JC</sub>)9°C/W</li> </ul>	192 CTBGA Junction-to-Ambient Thermal Resistance ( $\theta_{JA}$ )29.50°C/W Junction-to-Case Thermal Resistance ( $\theta_{JC}$ )9.40°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

# **Recommended DC Operating Conditions**

 $(V_{DD} = V_{RST} \text{ to } 3.6V, T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}, \text{ unless otherwise noted.}) \text{ (Note 2)}$ 

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Domain Voltage	V <sub>DD</sub>	(Note 3)	1.8		3.6	V
Analog Domain Voltage	V <sub>DDA3</sub>		2.3		3.6	V
1.8V Internal Regulator	V <sub>REG18</sub>			1.8		V
Power-Fail Warning Voltage for Supply	V <sub>PFW</sub>	Monitors V <sub>DD</sub> , PFWVSBIT = 0x0016		2.525		V
Power-Fail Reset Voltage	V <sub>RST</sub>	Monitors V <sub>DD</sub>		1.765		V
Power-On-Reset Release Voltage	V <sub>SPOR</sub>	Monitors V <sub>DD</sub> or V <sub>DDB</sub>			1.8	V
RAM Data Retention Voltage	V <sub>DRV</sub>			1.0		V
LP3 Active Current		Cache disabled, f <sub>CK</sub> = 24MHz		5		
(Note 4)	I <sub>DDLP3</sub>	Cache enabled, execution from cache, 100% hit rate, f <sub>CK</sub> = 24MHz		6.10		mA
LDO Comment		One PMU channel enabled		1.25		mA
LP2 Current	I <sub>DDLP2</sub>	Each additional PMU channel		200		μΑ
LP1 Current		RTC enabled, V <sub>DD</sub> supply current		1.8		
LPT Current	IDDLP1	RTC disabled, V <sub>DD</sub> supply current		1.4		μΑ
I DO Current	1	RTC enabled, V <sub>DD</sub> supply current		1250		n 1
LP0 Current	IDDLP0	RTC disabled, V <sub>DD</sub> supply current		850		nA
LP2 Mode Resume Time	t <sub>ONLP2</sub>	One PMU channel active		0		μs

# **Recommended DC Operating Conditions (continued)**

(V<sub>DD</sub> = V<sub>RST</sub> to 3.6V,  $T_A$  = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LP1 Mode Resume Time	t <sub>ONLP1</sub>			15		μs
LP0 Mode Resume Time	t <sub>ONLP0</sub>			26		μs
Input Low Voltage for SRSTN and All Port Pins	V <sub>IL</sub>				0.3 × V <sub>DDIO</sub>	V
Input High Voltage for SRSTN and All Port Pins	V <sub>IH</sub>		0.7× V <sub>DDIO</sub>			V
Input Hysteresis (Schmitt)	V <sub>IHYS</sub>			300		mV
Output Low Voltage for All Port Pins	V <sub>OL</sub>	V <sub>DD</sub> = 3.6V, I <sub>OL</sub> = 11mA V <sub>DD</sub> = 2.3V, I <sub>OL</sub> = 8mA		0.4	0.5 0.5	V
Output High Voltage for All Port Pins	V <sub>OH</sub>	I <sub>OH</sub> = -2mA	V <sub>DDIO</sub> - 0.5			V
Input/Output Pin Capacitance for All GPIO Port Pins	C <sub>IO</sub>			5		pF
Pullup Resistance for All GPIO	R <sub>PU25K</sub>	Normal drive mode		25		kΩ
Port Pins	R <sub>PU1M</sub>	Weak pullup enabled		1		ΜΩ
Input Leakage Current Low	I <sub>IL</sub>	V <sub>IN</sub> = 0V, internal pullup disabled	-100		+100	nA
Input Leakage Current High	l <sub>IH</sub>	V <sub>IN</sub> < V <sub>DD</sub> + 0.6V or 3.6V or whichever is lower, internal pullup disabled	-100		+100	nA
FLASH MEMORY						
Flash Erase Time	t <sub>ME</sub>	Mass erase		30		me
Flasii Erase Tillie	t <sub>ERASE</sub>	Page erase		30		ms
Flash Programming Time per Word	t <sub>PROG</sub>			60		μs
Flash Endurance		(Note 5)	20			K cycles
Data Retention	t <sub>RET</sub>	T <sub>A</sub> = +25°C (Note 5)	100			Years
LCD						
LCD Reference Voltage	V <sub>LCD</sub>	V <sub>LCD</sub> output boost voltage; V <sub>DD</sub> = 2.0V to 3.6V		3.3		V
1000		2/3 level	V <sub>ADJ</sub> +	2/3 (V <sub>LCD</sub>	- V <sub>ADJ</sub> )	
LCD Segment/Common Bias Voltage	V <sub>LCDBIAS</sub>	1/2 level	V <sub>ADJ</sub> +	1/2 (V <sub>LCD</sub>	- V <sub>ADJ</sub> )	V
voltage		1/3 level	V <sub>ADJ</sub> +	1/3 (V <sub>LCD</sub>	- V <sub>ADJ</sub> )	
		LCD_LCRA[3:0] = 0		0		
LCD Adjustment Voltage	V <sub>ADJ</sub>	LCD_LCRA[3:0] = 15		0.4 × V <sub>LCD</sub>		V
LCD Pigo Popietor	D.	Static and 1/3 bias		108		1.0
LCD Bias Resistor	R <sub>LCD</sub>	1/2 bias		72		kΩ
LCD Adjustment Resistor	R <sub>LADJ</sub>	LCD_LCRA[3:0] = 15		72		kΩ

# **Recommended DC Operating Conditions (continued)**

(V<sub>DD</sub> = V<sub>RST</sub> to 3.6V,  $T_A$  = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REAL-TIME CLOCK (RTC)						
RTC Input Frequency	f <sub>32KIN</sub>	32kHz watch crystal		32.768		kHz
DTO O a serifica o O assert	I <sub>RTC</sub>	Micro in LP2 or LP3		0.7		μA
RTC Operating Current	I <sub>RTC_LP0</sub>	Micro in LP0 or LP1		0.4		μA
RTC Initial Power-Up Time	t <sub>RTC_PUP</sub>	(Note 6)		250		ms
RTC Power Mode Transition Time from LP0/LP1 to LP2/LP3		RTC transition from low to high power drive, not required in all applications		256		ms

### **USB Electrical Characteristics**

(V<sub>DD</sub> = V<sub>RST</sub> to 3.6V,  $T_A$  = -40°C to +85°C, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
USB Supply Voltage	V <sub>BUS</sub>		4.5		5.5	V
USB PHY Supply Voltage	$V_{DDB}$	V <sub>BUS</sub> ≥ 4.0V		3.3		V
V <sub>BUS</sub> Supply Current in LP2/3 While Transmitting USB Data	1	Transmitting on D+ and D- at 12Mbps, $C_L = 50$ pF on D+ and D- to $V_{SS}$ , FRCVDD = 0		3 + I <sub>DD</sub>		mA
(Note 3)	I <sub>VBUS_TX</sub>	Transmitting on D+ and D- at 12Mbps, $C_L$ = 50 pF on D+ and D- to GND, FRCVDD = 1		3		mA
V <sub>BUS</sub> Supply Current in LP2/3 with USB Idle	I <sub>VBUS_IDLE</sub>	D+ = hi, D- = lo, FRCVDD = 18		0.4 + I <sub>DD</sub>		mA
Single-Ended Input High Voltage D+, D-	V <sub>IHD</sub>		2.0			V
Single-Ended Input Low Voltage D+, D-	V <sub>ILD</sub>				0.8	V
Output Low Voltage D+, D-	V <sub>OLD</sub>	$R_L = 1.5k\Omega$ from D+ to 3.6V			0.3	V
Output High Voltage D+, D-	V <sub>OHD</sub>	$R_L$ = 15k $\Omega$ from D+ and D- to $V_{SS}$	2.8			V
Differential Input Sensitivity D+, D-	V <sub>DI</sub>	D+ to D-	0.2			V
Common-Mode Voltage Range	V <sub>CM</sub>	Includes V <sub>DI</sub> range	0.8		2.5	V
Single-Ended Receiver Threshold	V <sub>SE</sub>		0.8		2.0	V
Single-Ended Receiver Hysteresis	V <sub>SEH</sub>			200		mV
Differential Output Signal Cross-Point Voltage	V <sub>CRS</sub>	C <sub>L</sub> = 50pF		1.65		V
D+, D- Off-State Input Impedance	R <sub>LZ</sub>		300			kΩ

### **USB Electrical Characteristics**

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Output Impedance	R <sub>DRV</sub>	Steady-state drive	28		44	Ω
D+ Pullup Resistor	D	Idle	0.9		1.575	kΩ
	R <sub>PU</sub>	Receiving	1.425		3.090	K12
USB TIMING						
D+, D- Rise Time (Transmit)	t <sub>R</sub>	C <sub>L</sub> = 50pF		12		ns
D+, D- Fall Time (Transmit)	t <sub>F</sub>	C <sub>L</sub> = 50pF		12		ns
Rise/Fall Time Matching (Transmit)	t <sub>R</sub> , t <sub>F</sub>	C <sub>L</sub> = 50pF		100		%

### **Clock Electrical Characteristics**

(V<sub>DD</sub> = V<sub>RST</sub> to 3.6V,  $T_A$  = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
External Crystal/Clock Input Frequency	fHFXIN		1		24	MHz
External Crystal Duty Cycle	tHFX_DUTY			50		%
External Clock Input Duty Cycle	txclk_duty			50		%
System Clock Frequency	f <sub>CK</sub>				24.2	MHz
System Clock Period	t <sub>CK</sub>			1/f <sub>CK</sub>		ns
Internal Relaxation Oscillator Frequency	fosc			24		MHz
Internal Relaxation Oscillator Variability	fosc_var				±1%	MHz

# **Phase-Locked Loop (PLL) Electrical Characteristics**

(V<sub>DD</sub> = V<sub>RST</sub> to 3.6V,  $T_A$  = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency	f <sub>PLL</sub>	8MHz, 12MHz, 24MHz with corresponding clock multiplier		48		MHz
Frequency Jitter		Peak-to-peak		1		ns

### **ADC/PGA Electrical Characteristics**

( $V_{DD}$  =  $V_{RST}$  to 3.6V,  $V_{DDA3}$  = 2.3V to 3.6V,  $T_A$  = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC ANALOG INPUT						
		Unipolar, AIN+ - AIN- PGA gain = 1, 2, 4, 8	0		+V <sub>REFADC</sub> / Gain	V
		Bipolar, AIN+ - AIN- PGA gain = 1, 2, 4, 8 range = 0	-V <sub>REFADC</sub> / (2 × Gain)		+V <sub>REFADC</sub> / (2 × Gain)	V
Input Voltage Range	V <sub>IN</sub>	Bipolar, AIN+ - AIN- PGA gain = 1, 2, 4, 8 range = 1	-V <sub>REFADC/</sub> Gain		+V <sub>REFADC</sub> / Gain	V
(Note 5)	- 111	Unipolar, AIN+ - AIN-, PGA bypass	0		+V <sub>REFADC</sub>	V
		Bipolar, AIN+ – AIN-, PGA bypass, range = 0	-V <sub>REFADC</sub> /2		+V <sub>REFADC</sub> /	V
		Bipolar, AIN+ - AIN-, PGA bypass, range = 1	-V <sub>REFADC</sub>		+V <sub>REFADC</sub>	V
Common-Mode Input Voltage	V <sub>CM_MIN</sub>	AIN+, AIN-		0		V
Range	V <sub>CM_MAX</sub>	AIN+, AIN-		$V_{\text{DDA3}}$		V
		$T_A = +25^{\circ}C$ , AIN0±, AIN[2:7] ± $V_{IN} = 0V < 2.0V$		1		
		$T_A = +50$ °C, AIN0±, AIN[2:7] ± $V_{IN} = 0$ V < 2.0V		4		
		$T_A = +25$ °C, AIN0±, AIN[2:7] ± $V_{IN}$ = 2.0V to 3.6V		3		
		$T_A = +50$ °C, AIN0±, AIN[2:7] ± $V_{IN}$ = 2.0V to 3.6V		8		
		T <sub>A</sub> = +25°C, AIN1+, AIN1- ± V <sub>IN</sub> = 0V < 2.0V		2		
ADC/PGA Input Leakage	l	$T_A = +50$ °C AIN1+, AIN1- ± $V_{IN} = 0$ V < 2.0V		6		
Current (Note 5)	l <sub>IL</sub>	$T_A = +25$ °C, AIN1+, AIN1- $\pm$ V <sub>IN</sub> = 2.0V to 3.6V		4		pA
		$T_A = +50$ °C, AIN1+, AIN1- $\pm$ V <sub>IN</sub> = 2.0V to 3.6V		13		
		$T_A = -40$ °C to +85°C, AIN0±, AIN[2:7] ± $V_{IN}$ = 0V < 2.0V		1	±200	
	T <sub>A</sub> AIN T <sub>A</sub> AIN	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C},$ AIN0±, AIN[2:7] ± V <sub>IN</sub> = 2.0V to 3.6V		3	±350	
		T <sub>A</sub> = -40°C to +85°C, AIN1+, AIN1- ± V <sub>IN</sub> = 0V < 2.0V		2	±300	
		$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C},$ AIN1+, AIN1- ± $V_{\text{IN}} = 2.0\text{V to } 3.6\text{V}$		5	±525	

# **ADC/PGA Electrical Characteristics (continued)**

(V<sub>DD</sub> = V<sub>RST</sub> to 3.6V,  $T_A$  = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
		PGA bypass, range = 0		7		
		PGA bypass, range = 1		4		
Lancet Occupations	0	PGA gain = 1		7		]
Input Capacitance	Cl	PGA gain = 2		13		pF
		PGA gain = 4		25		
		PGA gain = 8		49		1
DC CHARACTERISTICS						
Resolution	N		16			Bits
No Missing Codes (Note 5)			-1			LSB
Differential Nonlinearity	DNL	16-bit resolution		±0.5		LSB
Integral Nonlinearity (Note 5)	INL	V <sub>REFADC</sub> ≥ 1.5V		±1.5	±4	LSB
Tanadian Naisa		PGA bypass		3.7		LOD
Transition Noise		PGA gain = 8		8.1		LSB
Gain Error without Firmware		PGA bypass			±200	LOD
Compensation		PGA active			±225	LSB
Gain Error Temperature Coefficient		V <sub>REF</sub> ≥ 1.5V, does not include reference drift			±0.4	LSB/ °C
Offset Error without Firmware	OE	PGA bypass		0	±55	LOD
Compensation	UE	PGA active		0	80	LSB
Offset Error Temperature Coefficient		V <sub>REF</sub> ≥ 1.5V, does not include reference drift		0.1		LSB/ °C
Channel-to-Channel Offset Matching				±0.1		LSB
Channel-to-Channel Gain Matching				±0.1		LSB
Input Common-Mode Rejection	CMR	V <sub>CM</sub> = 0V to V <sub>DDA3</sub>		±1		LSB
CONVERSION RATE						
		PGA bypass			500/N <sub>d</sub>	
		PGA gain = 1			470/N <sub>d</sub>	1
Throughput Rate	F <sub>S</sub>	PGA gain = 2			470/N <sub>d</sub>	ksps
		PGA gain = 4			444/N <sub>d</sub>	
		PGA gain = 8			421/N <sub>d</sub>	
Decimation Rate	N <sub>d</sub>	Powers of 2 (Note 5)	1		128	Sp
ADC Conversion Time	t <sub>CONV</sub>	15.5 ADC <sub>FCLK</sub> cycles; ADC <sub>FCLK</sub> = 8MHz (Note 7)	1.9375			μs

# **ADC/PGA Electrical Characteristics (continued)**

 $(V_{DD} = V_{RST} \text{ to } 3.6V, T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}, \text{ unless otherwise noted.}) \text{ (Note 2)}$ 

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
		PGA bypass	187.5			
ADC Acquisition Time		PGA gain = 1	250			
	t <sub>ACQ_ADC</sub>	PGA gain = 2	250			ns
	_	PGA gain = 4	375			
		PGA gain = 8	375			
		Single sample or initial sample	0.63			
		PGA gain = 1, continuous sample	1.5			
PGA Acquisition Time	t <sub>ACQ_PGA</sub>	PGA gain = 2, continuous sample	1.5			μs
	_	PGA gain = 4, continuous sample	1.5			
		PGA gain = 8, continuous sample	1.5			
Anantona littan		External crystal or clock source		500		
Aperture Jitter	t <sub>AJ</sub>	Internal relaxation oscillator		500		ps ps
ADC Clock Frequency		(Note 5)			8	MHz
Transient Response		Full-scale step			1	CLK
Hansieni Nesponse		i uii-scale step			ı ı	cycle

### **DYNAMIC SPECIFICATIONS (Note 8)**

-0.5dB below full scale with  $V_{DDA3}$  = 3V internal,  $V_{REF}$  = 2.048V, ADC range = 1, ADC bipolar = 1, PGA bypass or PGA gain = 1x,  $f_{SAMPLE}$  = 500ksps

		Bypass mode, decimation filter N <sub>d</sub> = 1	72.4	74.8	
Signal-to-Noise Ratio (Note 9)	SNR	Decimation filter N <sub>d</sub> = 1, PGA enabled	70.8	73.6	
		Decimation filter N <sub>d</sub> = 16	80.3	85.4	]
		Decimation filter N <sub>d</sub> = 64	84.6	89.9	dB
Signal-to-Noise and Distortion		Bypass mode, decimation filter N <sub>d</sub> = 1	72.2	74.7	] ub
	SINAD	Decimation filter N <sub>d</sub> = 1, PGA enabled	70.7	73.5	
		Decimation filter N <sub>d</sub> = 16	78.6	84.5	]
		Decimation filter N <sub>d</sub> = 64	79.7	87.9	
Spurious-Free Dynamic	CEDD	PGA bypass		91	dB
Range	SFDR	PGA enabled		85	ub ub
Total Harmania Distortion	THD	PGA bypass		91	٩D
Total Harmonic Distortion	וחט	PGA enabled		91	dB
Channel-to-Channel Crosstalk		Single-ended, f <sub>INPUT</sub> < 200kHz		107	dB

# **ADC/PGA Electrical Characteristics (continued)**

 $(V_{DD} = V_{RST} \text{ to } 3.6V, T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}, \text{ unless otherwise noted.}) \text{ (Note 2)}$ 

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS		
POWER SUPPLIES								
ADC Supply Current		F <sub>S</sub> > 333.3ksps, PGA bypass, post trimmed		9.6		m A		
		F <sub>S</sub> > 333.3ksps, PGA enabled, post trimmed		11.6		– mA		
		F <sub>S</sub> ≤ 333.3ksps, PGA bypass, post trimmed		32.9		A ( )		
		F <sub>S</sub> ≤ 333.3ksps, PGA enabled, post trimmed		40.9		nA/sps		
Line Rejection	LR	V <sub>DDA3</sub> = 2.3 to 3.6V (Note 5)			±10	LSB		

DAC0/DAC1 Electrical Characteristics (V<sub>DDA3</sub> = 2.3V to 3.6V, V<sub>DD</sub> = V<sub>RST</sub> to 3.6V, R<sub>L</sub> = 10kΩ and C<sub>L</sub> = 100pF, T<sub>A</sub> = -40°C to +85°C, V<sub>REFDAC</sub> = 1.5V, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution	DAC <sub>R</sub>	Guaranteed monotonic	12			Bits
Differential Nonlinearity	DNL	Power mode = 2 or 3, noise filter enabled, T <sub>A</sub> = -0°C to +85°C, code 000h to FFFh (Note 5)	-2		+2	LSB
Integral Nonlinearity	INL	Power mode = 2 or 3, noise filter enabled, code 073h to F8Dh (Note 5)	-4		+4	LSB
Offset Error	E <sub>O</sub>	Using uncommitted op amp (Note 5)		±0.5	±4	mV
Gain Error	E <sub>G</sub>	V <sub>REFDAC</sub> = 1.5V, power mode = 2 to 3, V <sub>DDA3</sub> = 3.0V, trimmed, using firmware compensation	-8	±1	+8	LSB
		V <sub>REFDAC</sub> = 1.5V, V <sub>DDA3</sub> = 3.0V, without firmware compensation	-90		+90	
Gain Error Temperature		Temperature coefficient compensation disabled, using internal uncommitted op amp, V <sub>REFDAC</sub> = 1.5V, power mode = 3, V <sub>DDA3</sub> = 3.0V		-60		ppm/°
Compensation	E <sub>GTC</sub>	Temperature coefficient compensation enabled, using internal uncommitted op amp, VREFDAC = 1.5V, power mode = 3, VDDA3 = 3.0V		-20		С
Output Voltage Range	V <sub>O</sub>	Min code to max code (Note 5)	V <sub>SSDAC</sub> + E <sub>O</sub>		V <sub>DDA3</sub> - 0.5 + E <sub>G</sub>	V

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# **DAC0/DAC1 Electrical Characteristics (continued)**

 $(V_{DDA3}$  = 2.3V to 3.6V,  $V_{DD}$  =  $V_{RST}$  to 3.6V,  $R_L$  = 10k $\Omega$  and  $C_L$  = 100pF,  $T_A$  = -40°C to +85°C,  $V_{REFDAC}$  = 1.5V, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN TYP	MAX	UNITS
		Power mode = 3	6.1		kΩ
Output Impadance		Power mode = 2	8.9		
Output Impedance		Power mode = 1	16.3		kΩ
		Power mode = 0	97.7		kΩ
Voltage Output Settling Time		Noise filter enabled, code 400h to C00h, rising or falling, to ±0.5 LSB		4	
Voltage Output Settling Time	tsfs	Noise filter disabled, code 400h to C00h, rising or falling, to ±0.5 LSB		0.03	IIIS
0111 -		Power mode = 0, 1, or 2	12		kΩ kΩ ms V x ns μA
Glitch Energy		Power mode = 3, code 000h to A5Hh	12		V x ns
Bias Supply Current Shared		Static V <sub>REF</sub> = 2.5V	110		
	IDACx_ON	Static V <sub>REF</sub> = 1.5V	82		μΑ
		Static V <sub>REF</sub> = 2.5V Power mode = 3	438.7		
Antiivo Current		Static V <sub>REF</sub> = 2.5V Power mode = 2	301.6		μΑ
Active Current	I <sub>DAC12</sub>	Static V <sub>REF</sub> = 2.5V Power mode = 1	164.5		
		Static V <sub>REF</sub> = 2.5V Power mode = 0	27.4		
		Static V <sub>REF</sub> = 1.5V Power mode = 3	263.2		
Active Current	l	Static V <sub>REF</sub> = 1.5V Power mode = 2	181		
Active Current	IDAC12	Static V <sub>REF</sub> = 1.5V Power mode = 1	98.7		μΑ
		Static V <sub>REF</sub> = 1.5V Power mode = 0	16.5		

# **DAC0/DAC1 Electrical Characteristics (continued)**

 $(V_{DDA3}$  = 2.3V to 3.6V,  $V_{DD}$  =  $V_{RST}$  to 3.6V,  $R_L$  = 10k $\Omega$  and  $C_L$  = 100pF,  $T_A$  = -40°C to +85°C,  $V_{REFDAC}$  = 1.5V, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN TYP MAX	UNITS
Active Current		Static V <sub>REF</sub> = 2.048V Power mode = 3	359.3	
		Static V <sub>REF</sub> = 2.048V Power mode = 2	247.1	
	I <sub>DAC12</sub>	Static V <sub>REF</sub> = 2.048V Power mode = 1	124.8	μΑ
		Static V <sub>REF</sub> = 2.048V Power mode = 0	22.5	
		Static V <sub>REF</sub> = 1.024V Power mode = 3	179.7	
Active Coursest		Static V <sub>REF</sub> = 1.024V Power mode = 2	123.5	
Active Current	I <sub>DAC12</sub>	Static V <sub>REF</sub> = 1.024V Power mode = 1	67.3	μΑ
		Static V <sub>REF</sub> = 1.024V Power mode = 0	11.2	
Power-On Time		Excluding reference	10	μs

### **DAC2/DAC3 Electrical Characteristics**

 $(V_{DDA3}$  = 2.3V to 3.6V,  $V_{DD}$  =  $V_{RST}$  to 3.6V,  $R_L$  = 10k $\Omega$  and  $C_L$  = 100pF,  $T_A$  = -40°C to +85°C,  $V_{REFDAC}$  = 1.5V, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution	DAC <sub>R</sub>	Guaranteed monotonic	8			Bits
Differential Nonlinearity	DNL	Code 07h to F9h		±0.25	±1	LSB
Integral Nonlinearity	INL	Code 07h to F9h		±0.25	±1	LSB
Offset Error	E <sub>O</sub>	Internal uncommitted op amp (Note 5)		±0.5	±4	mV
Gain Error	E <sub>G</sub>	Internal reference		±2		LSB
Gain-Error Temperature Coefficient		Excludes offset and reference drift, using internal uncommitted op amp		±5		ppm of FSR/°C
Output Voltage Range	Vo	Min code to max code (Note 5)	V <sub>SSDAC</sub>		V <sub>DDA3</sub> - 0.5	V
Output Impedance				49		kΩ
Voltage Output Settling Time	tsfs	40h to C0h code swing rising or falling to ±0.5 LSB		3		μs
DAC Glitch Impulse		Major carry transitions		12		nV-s
Supply Current per DAC	I <sub>DAC</sub>	Static		62.4		μA
Power-On Time		Excluding Reference		10		μs

# **Operational Amplifier Electrical Characteristics**

(V<sub>DDA3</sub> = 2.3V to 3.6V,  $T_A$  = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS	,					
Common-Mode Rejection Ratio	CMRR	16-bit resolution		75		dB
Input Offset Voltage	V <sub>OS</sub>			±0.5	±8	mV
Input Offset Voltage Drift	V <sub>OSDRIFT</sub>			5		μV/°C
		T <sub>A</sub> = +25°C, V <sub>IN</sub> = 0V		15	200	
Input Bias Current (Note 5)	I <sub>BIAS</sub>	$T_A = 0^{\circ}C \text{ to } +50^{\circ}C, V_{IN} = 0V$			300	mV
		$T_A = -40^{\circ}C \text{ to } +85^{\circ}C, V_{IN} = 0V$			650	
		T <sub>A</sub> = +25°C		15	200	pA
Input Offset Current (Note 5)	los	T <sub>A</sub> = 0°C to +50°C			300	
		T <sub>A</sub> = -40°C to +85°C			650	
Large Signal Voltage Gain	A <sub>OL</sub>			140		dB
		en_nch_opampx = 1, en_pch_opampx = 1	V <sub>AGND</sub> - 50mV		V <sub>DDA3</sub> + 50mV	
Input Voltage Range	V <sub>IN+</sub> , V <sub>IN-</sub>	en_nch_opampx = 0, en_pch_opampx = 1	V <sub>AGND</sub> - 50mV		V <sub>DDA3</sub> + 1.05	V
		en_nch_opampx = 1, en_pch_opampx = 0	0.95		V <sub>DDA3</sub> + 50mV	

# **Operational Amplifier Electrical Characteristics (continued)**

(V<sub>DDA3</sub> = 2.3V to 3.6V,  $T_A$  = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Swing High	V <sub>OH</sub>	V <sub>DDA3</sub> - V <sub>OUT</sub> , 100kΩ load	V <sub>DDA3</sub> - 10		V <sub>DDA3</sub>	mV
Output Voltage Swing Low	V <sub>OL</sub>	V <sub>OUT</sub> - V <sub>AGND</sub> , 100kΩ load			5	mV
Output Short Circuit Current	I <sub>SC</sub>			25	50	mA
OP AMP GND SWITCHES (IN	IA+, INB+, INC	C+,IND+)				•
INx+ Capacitance	C <sub>INx+</sub>	$V_{INx+} = V_{AGND}$ , f = 1MHz (Note 5)		2		pF
On Desistance (Note 5)		V <sub>INx+</sub> = 3.0V, I <sub>INx+</sub> = 10mA		20	30	
On-Resistance (Note 5)	R <sub>ON</sub>	V <sub>INx+</sub> = 3.0V, I <sub>INx+</sub> = 50mA		20		Ω
INx+ DC Current	I <sub>INx+</sub>	(Note 5)			50	mA
AC CHARACTERISTICS						•
Gain-Bandwidth	GBW	C <sub>L</sub> = 100pF		3		MHz
Slew Rate	SR	C <sub>L</sub> = 100pF	0.85	1.6		V/µs
Input Voltage Noise Density	V <sub>n</sub>	f = 10kHz		20		nV/√Hz
Input Voltage Noise		0.1Hz ≤ f ≤ 10Hz		20		µV <sub>P-P</sub>
Input Current Noise Density	In	f = 10kHz		10		fA/√Hz
Capacitive Loading	C <sub>LOAD</sub>	No sustained oscillations, $R_{SERIES} = 0\Omega$		100		pF
Total Harmonic Distortion	THD	f = 10kHz, V <sub>OUT</sub> = 1V <sub>P-P</sub> , source follower configuration, (en_nch_ opampx = 0, en_pch_opampx = 1) or (en_nch_opampx = 1, en_pch_ opampx = 0)		-90		dB
POWER-SUPPLY CHARACT	ERISTICS					-
		en_nch_opampx = 1, en_pch_ opampx = 1		183		
Supply Current	I <sub>VDDA3</sub>	en_nch_opampx = 0, en_pch_ opampx = 1		155		μA
		en_nch_opampx = 1, en_pch_ opampx = 0		155		μΑ
Line Rejection	LR			90		dB
Turn-On Time	t <sub>ON</sub>			1.5	2.1	μs
Power-Down Output Impedance		V <sub>OUTx</sub> = 1V		1		GΩ
Power-Down Output Leakage				±1		nA
OP AMP FEEDBACK SWITC	Н					
Internal Switch On-Resistance	R <sub>INTSW</sub>			30		Ω
Ground Switch Resistance	R <sub>OPAGND</sub>			20		Ω

# **Internal Voltage Reference Electrical Characteristics**

 $(V_{DDA3}$  = 2.3V to 3.6V,  $T_A$  = -40°C to +85°C, Internal Reference Mode, 4.7 $\mu$ F capacitor at REFADC, 4.7 $\mu$ F cap at REFDAC, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INTERNAL REFERENCE						
		V <sub>DDA3</sub> = 2.3V to 3.6V, T <sub>A</sub> = +25°C	-2%	1.024	+2%	V V ppm/°C ppm/°C
Output Voltage at REFADC and REFDAC (Note 5)	VREFADC,		-1%	1.50	+1%	V
	V <sub>REFDAC</sub>	$V_{\rm DDA3}$ = 2.3V to 3.6V, $T_{\rm A}$ = +25°C	-2%	2.048	+2%	V
		V <sub>DDA3</sub> = 2.7V to 3.6V, T <sub>A</sub> = +25°C	-2%	2.50	+2%	
Output Voltage at REFADJ	V <sub>REFADJ</sub>			1.24		V
nternal Reference Temperature	_	T <sub>A</sub> = 0°C to +70°C		30		100
Coefficient (Note 5)	T <sub>CREF</sub>	T <sub>A</sub> = -40°C to +85°C			50	- ppm/°C
Temperature Coefficient	_	T <sub>A</sub> = 0°C to +70°C		5		100
Adder of Buffer with External Reference	T <sub>C</sub>	T <sub>A</sub> = -40°C to +85°C		10	pp	ppm/°C
Turn-On Time	t <sub>ON</sub>	(Note 5)		0.1+ (V <sub>REF</sub> X 1.8)	10	ms
Leakage Current with Internal	IREFADC	refadc_outen = 0		15	50	
Reference Output Disabled (Note 5)	I <sub>REFDAC</sub>	refdac_outen = 0		15	50	nA nA
REFADC and REFDAC Line Regulation				±100		μV/V
Load Regulation		$I_{SOURCE} = 0\mu A \text{ to } 500\mu A,$ $T_A = +25^{\circ}C$		10		μV/μΑ
		Internal reference only (Note 10)		33		
Reference Supply Current		REFADC buffer		270		μA
		REFDAC buffer		270		

# **External Voltage Reference Electrical Characteristics**

(V<sub>DDA3</sub> = 2.3V to 3.6V,  $T_A$  = -40°C to +85°C, External reference mode.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EXTERNAL REFERENCE AT	REFADJ					
Input Voltage Range	V <sub>REFADJ</sub>			1.24 ±3%		V
Input Resistance				250		kΩ
EXTERNAL REFERENCE AT	REFADC					
Input Voltage Range	V <sub>REFADC</sub>	V <sub>DDA3</sub> = 2.3V to 3.0V	,	1.0 to V <sub>DDA3</sub> - 0.9	5	V
		V <sub>DDA3</sub> > 3.0V		1.0 to 2.5		1
Input Capacitance				7		pF
Dynamic Input Current		500ksps, V <sub>REFADC</sub> = 2.048V		50		μA
EXTERNAL REFERENCE AT	REFDAC				'	
Input Voltage Range	Vpssp.o	V <sub>DDA3</sub> = 2.3V to 3.0V (typ)	,	1.0 to V <sub>DDA3</sub> - 0.5	5	V
	V <sub>REFDAC</sub>	V <sub>DDA3</sub> > 3.0V (typ)		1.0 to 2.5		V

# SPST Switches (SNO\_, SCM\_)

(V<sub>DDA3</sub> = 2.3V to 3.6V,  $T_A$  = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog Signal Range	V <sub>SNOX</sub> , V <sub>SCMX</sub>			0 to V <sub>DDA3</sub>		V
On-Resistance	R <sub>ON</sub>	$V_{DDA3}$ = 3.0V, $I_{SCM}$ = 50mA, $V_{SNO}$ = 0V to $V_{DDA3}$		30	50	Ω
SNO_ Off-Leakage Current		V <sub>DDA3</sub> = 3.0V, V <sub>SCM</sub> = 0V, 2V V <sub>SNO</sub> = 2V, 0V T <sub>A</sub> = +25° C (Note 5)		±30	±100	Ω pA
	I <sub>SNO_(OFF)</sub>	V <sub>DDA3</sub> = 3.0V, V <sub>SCM</sub> = 0V, 2V V <sub>SNO</sub> = 2V, 0V T <sub>A</sub> = +70°C		±60		рА
		V <sub>DDA3</sub> = 3.0V, V <sub>SCM</sub> = 0V, 2V V <sub>SNO</sub> = 2V, 0V T <sub>A</sub> = -40°C to +85°C			±1	nA

# SPST Switches (SNO\_, SCM\_) (continued)

(V<sub>DDA3</sub> = 2.3V to 3.6V,  $T_A$  = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCM_ Off-Leakage Current		V <sub>DDA3</sub> = 3.0V, V <sub>SCM</sub> = 0V, 2V V <sub>SNO</sub> = 2V, 0V T <sub>A</sub> = +25° C (Note 5)		±30	±100	n 1
	I <sub>SCM_(OFF)</sub>	V <sub>DDA3</sub> = 3.0V, V <sub>SCM</sub> = 0V, 2V V <sub>SNO</sub> = 2V, 0V T <sub>A</sub> = +70°C		±50		- pA
		V <sub>DDA3</sub> = 3.0V, V <sub>SCM</sub> = 0V, 2V V <sub>SNO</sub> = 2V, 0V T <sub>A</sub> = -40°C to +85°C			±1	nA
		V <sub>DDA3</sub> = 3.0V, V <sub>SCM</sub> = 0V, 2V T <sub>A</sub> = +25° C		±0.8		
SCM_ On-Leakage Current	I <sub>SCM_(ON)</sub>	V <sub>DDA3</sub> = 3.0V, V <sub>SCM</sub> = 0V, 2V T <sub>A</sub> = 0°C to +70°C		±1.2		nA
		V <sub>DDA3</sub> = 3.0V, V <sub>SCM</sub> = 0V, 2V T <sub>A</sub> = -40°C to +85°C		±2.0		
Turn-On/Off Time	t <sub>ON</sub> /t <sub>OFF</sub>	$V_{SCM} = 2V, R_{L} = 300\Omega, C_{L} = 35pF$		1		ns
Charge Injection	Q	V <sub>GEN</sub> = 0V, R <sub>GEN</sub> = 0, C <sub>L</sub> = 1.0nF (Note 5)			2	pC
SNO_ Off-Capacitance	C <sub>SNOx</sub>	V <sub>SNO</sub> _ = AGND, f = 1MHz (Note 5)			2.5	pF
Switch On-Capacitance	C <sub>ON</sub>	V <sub>SCM</sub> _ = V <sub>SNO</sub> _, f = 1MHz (Note 5)			5.0	pF

# CS Switches (CSA\_, CSB\_)

(V<sub>DDA3</sub> = 2.3V to 3.6V,  $T_A$  = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Low Voltage	Va	V <sub>CSBx</sub> = 500mV, I <sub>CSx</sub> = 35mA, V <sub>DDA3</sub> > 2.3V		0.7		V
Output Low Voltage	V <sub>OL</sub>	$V_{CSBx}$ = 350mV, $I_{CSx}$ = 50mA, $V_{DDA3}$ > 2.5V		0.6		V
CSA_, CSB_ DC Current	I <sub>CSx</sub>	Maximum combined current for up to 4 CSA/CSB pairs (Note 5)			100	mA

### **Temperature Sensor**

 $(V_{DDA3} = 2.3V \text{ to } 3.6V, T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}, \text{ unless otherwise noted.}) \text{ (Note 2)}$ 

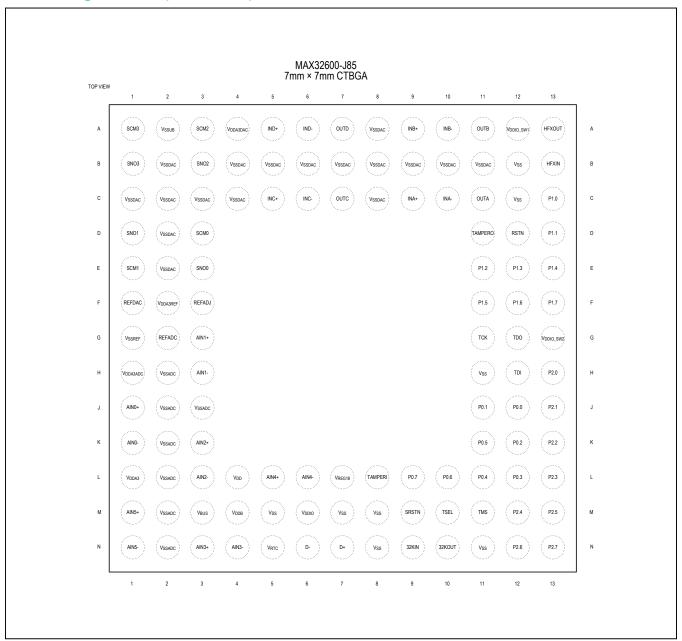
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INTERNAL TEMPERATURE S	ENSOR					
Temperature Resolution				0.11		°C/LSB
Internal Sensor Measurement Error		External voltage reference		±3		°C
EXTERNAL TEMPERATURE	SENSOR					
	I <sub>AIN1P0</sub>	AinCurrentEn = 1 AinCurrentSel = 00 V <sub>AIN1P</sub> < (V <sub>DDA3</sub> - 0.5V)		4		
Current Sourced onto AIN1P	I <sub>AIN1P1</sub>	AinCurrentEn = 1 AinCurrentSel = 01 V <sub>AIN1P1</sub> < (V <sub>DDA3</sub> - 0.5V)		60		
(Note 5)	I <sub>AIN1P2</sub>	AinCurrentEn = 1 AinCurrentSel = 10 V <sub>AIN1P2</sub> < (V <sub>DDA3</sub> - 0.5V)		64		- μΑ
	I <sub>AIN1P3</sub>	AinCurrentEn = 1 AinCurrentSel = 11 V <sub>AIN1P3</sub> < (V <sub>DDA3</sub> - 0.5V)		120		

- Note 2: Specifications to -40°C are guaranteed by design and are not production tested. Typical = 25°C, V<sub>DD</sub> = 3V, unless otherwise specified.
- Note 3: FRCVDD is 1 when firmware forces all power to be sourced from main battery VDD rather than VBUS.
- Note 4: Measured on the  $V_{DD}$  pin and the part not in reset. All inputs are tied to GND or  $V_{DD}$ . Outputs do not source/sink any current. Execution from internal 24MHz relaxation oscillator, cache disabled, internal LDO disabled.
- Note 5: Guaranteed by design.
- Note 6: Initial startup of RTC from power up of MAX32600. This does not apply if RTC is running and changing power modes.
- Note 7: During consecutive samples, conversion time overlaps acquisition time.
- Note 8: AC electrical specifications are guaranteed by design and are not production tested.
- Note 9: 10kHz sine-wave input signal.
- Note 10: In order to perform ADC measurements, the internal reference must be turned on even when using external voltage reference.

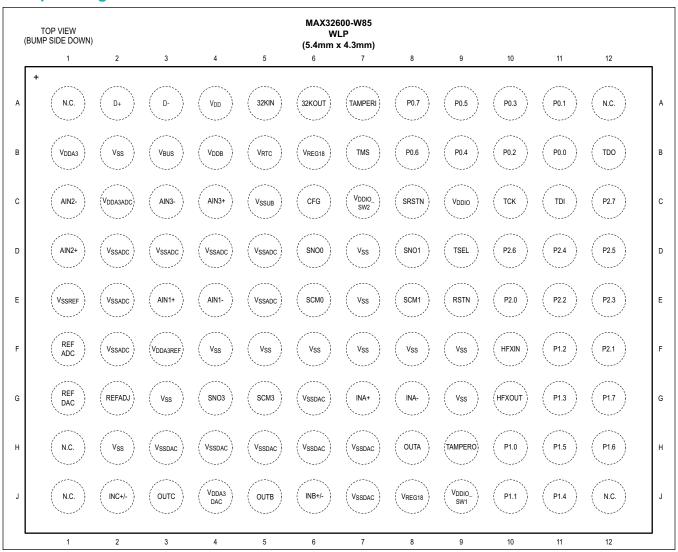
# **Ball Configurations**

									X32600- × 12mm									
OP VIEV	V 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A		VSSDAC	SCM3	VSSDAC	INC+	INC-	ООТС	VSSDAC	INB+	(INB-	ОИТВ	VSSDAC	HFXOUT	Vss	P0.2	P0.5	P0.7	
В	SCM2	V <sub>SSDAC</sub>	SN03	V <sub>SSDAC</sub>	V <sub>SSDAC</sub>	V <sub>SSDAC</sub>	Vssdac	V <sub>SSDAC</sub>	Vssdac	V <sub>SSDAC</sub>	V <sub>SSDAC</sub>	V <sub>SSDAC</sub>	HFXIN	V <sub>SS</sub>	P0.1	P0.4	P0.6	(P1.0)
С	SNO2	VSSDAC	VSSDAC	VSSDAC	(IND+	(IND-)	ООТО	VDDA3DAC	INA+	(INA-	OUTA	VSSDAC	TAMPERO	P0.0	P0.3	Vss	(P1.1)	(P1.2)
D	SCM0	VSSDAC	SCM1													P1.3	(P1.4)	P1.5
E	SN00	VSSDAC	SN01													P2.0	(P1.6)	(P1.7)
F	Vssadc	VSSADC	VSSADC													P2.1	(P22)	(P2.3)
G	AIN1+	VSSADC	AIN0+													P2.4	P2.5	P2.6
н	AIN1-	VSSADC	AIN0-					VDDA3REF	REFADJ	VssuB	VDDIO					RSTN	P3.0	P2.7
J	Vssadc	VSSADC	VSSADC					REFDAC	Vss	Vss	VDDIO					Vss	P3.2	P3.1
к	AIN3+	VSSADC	AIN2+					REFADC	Vss	Vss	VREG18					P3.5	P3.4	P3.3
L	AIN3-	VSSADC	AIN2-					VSSREF	VDDA3	VDD	VREG18					P4.0	(P3.7)	P3.6
М	Vssadc	VSSADC	VDDA3ADC													P4.3	P4.2	(P4.1)
N	AIN5+	VSSADC	AIN4+													P4.6	P4.5	P4.4
Р	AIN5-	VSSADC	AIN4-													P5.1	P5.0	P4.7
R	Vssadc	VSSADC	Vssadc						/*** <u>\</u>				<i></i>		/**\	P5.4	P5.3	P5.2
Т	AIN6+	VSSADC	VSSADC	Vssadc	VADJ	(b)	VBUS	VDDB	тск	TSEL	TAMPERI	P7.6	Vss	(P7.1)	P6.6	Vss	(P5.6	P5.5
U	AIN6-	Vssadc	AIN7+	VSSADC	VLCD2	(b+)	Vss	32KOUT	SRSTN	ТОО	(TDI)	P7.5	P7.3	(P7.0	P6.5	(P6.3)	P6.1	P5.7
٧ [		Vssadc	AIN7-	Vssadc	VLCD1	VLCD	Vss	32KIN	VRTC	TMS	P7.7	P7.4	P7.2	P6.7	P6.4	(P6.2	P6.0	
-	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18

# **Ball Configurations (continued)**



# **Bump Configuration**



# **Ball/Bump Descriptions**

ВА	LL	BUMP		
MAX32600-P85 (192 BALL)	MAX32600-J85 (120 BALL)	MAX32600-W85 (WLP)	NAME	FUNCTION
CLOCK PINS				
V8	N9	A5	32KIN	32kHz Clock Input. Connect to 32kHz crystal.
U8	N10	A6	32KOUT	32kHz Clock Output. Connect to 32kHz crystal.
B13	B13	F10	HFXIN	High-Frequency Crystal Input. Connect an external crystal or resonator between HFXIN and HFXOUT as the high-frequency system clock. Alternatively, HFXIN is the input for an external high-frequency clock source when HFXOUT is shorted to ground.
A13	A13	G10	HFXOUT	High-Frequency Crystal Output. Connect an external crystal or resonator between HFXIN and HFXOUT as the high-frequency system clock. To use an external high-frequency clock source as the system clock, connect HFXOUT to ground and apply clock source to HFXIN.
ANALOG PINS				
G3, H3	J1, K1	_	AIN0+, AIN0-	Analog Input. This pair of analog inputs can function as two single-ended inputs or one differential pair. In single-ended mode, AIN0+acts as input AIN0 and AIN0- acts as input AIN8.
G1, H1	G3, H3	E3, E4	AIN1+, AIN1-	Analog Input. This pair of analog inputs can function as two single-ended inputs or one differential pair. In single-ended mode, AIN1+acts as input AIN1 and AIN1-acts as input AIN9.
K3, L3	K3, L3	D1, C1	AIN2+, AIN2-	Analog Input. This pair of analog inputs can function as two single-ended inputs or one differential pair. In single-ended mode, AIN2+acts as input AIN2 and AIN2- acts as input AIN10.
K1, L1	N3, N4	C4, C3	AIN3+, AIN3-	Analog Input. This pair of analog inputs can function as two single-ended inputs or one differential pair. In single-ended mode, AIN3+acts as input AIN3 and AIN3-acts as input AIN11.
N3, P3	L5, L6	_	AIN4+, AIN4-	Analog Input. This pair of analog inputs can function as two single-ended inputs or one differential pair. In single-ended mode, AIN4+acts as input AIN4 and AIN4- acts as input AIN12.
N1, P1	M1, N1	_	AIN5+, AIN5-	Analog Input. This pair of analog inputs can function as two single-ended inputs or one differential pair. In single-ended mode, AIN5+acts as input AIN5 and AIN5- acts as input AIN13.
T1, U1	_	_	AIN6+, AIN6-	Analog Input. This pair of analog inputs can function as two single-ended inputs or one differential pair. In single-ended mode, AIN6+acts as input AIN6 and AIN6- acts as input AIN14.
U3, V3	_	_	AIN7+, AIN7-	Analog Input. This pair of analog inputs can function as two single-ended inputs or one differential pair. In single-ended mode, AIN7+ acts as input AIN7 and AIN7- acts as input AIN15.

BA	<b>LL</b>	BUMP		
MAX32600-P85 (192 BALL)	MAX32600-J85 (120 BALL)	MAX32600-W85 (WLP)	NAME	FUNCTION
REFERENCE P	INS			
K8	G2	F1	REFADC	Internal ADC Reference Pin. If using the internal reference, this pin must be connected to ground through at least a 4.7µF ceramic chip capacitor. In an external reference is used, it is input on this pin.
H9	F3	G2	REFADJ	If an external bandgap input is used to provide the basis for the internal ADC and DAC reference generation, it is input on this pin.
J8	F1	G1	REFDAC	Internal DAC Reference Pin. If using the internal reference, this pin must be connected to ground through at least a 4.7µF ceramic chip capacitor. In an external reference is used, it is input on this pin.
OP AMP/COMP	ARATOR PINS			
C9	C9	G7	INA+	Op Amp A Positive Input
C10	C10	G8	INA-	Op Amp A Negative Input
C11	C11	H8	OUTA	Op Amp A Output
A9	A9	_	INB+	Op Amp B Positive Input
A10	A10	_	INB-	Op Amp B Negative Input
_	_	J6	INB+/-	Op Amp B Positive/Negative Input. INB+ and INB- are both bonded out to bump J6.
A11	A11	J5	OUTB	Op Amp B Output
A5	C5	_	INC+	Op Amp C Positive Input
A6	C6	_	INC-	Op Amp C Negative Input
_	_	J2	INC+/-	Op Amp C Positive/Negative Input. INC+ and INC- are both bonded out to bump J2.
A7	C7	J3	OUTC	Op Amp C Output
C5	A5	<del>_</del>	IND+	Op Amp D Positive Input
C6	A6	_	IND-	Op Amp D Negative Input
C7	A7	_	OUTD	Op Amp D Output
USB FUNCTION	N PINS			
U6	N7	A2	D+	USB D+ Signal. This bidirectional pin carries the positive differential data or single-ended data. Connect this pin to a USB "B" connector. This pin is weakly pulled high internally when the USB is disabled.
Т6	N6	А3	D-	USB D- Signal. This bidirectional pin carries the negative differential data or single-ended data. Connect this pin to a USB "B" connector. This pin is weakly pulled high internally when the USB is disabled.
Т7	М3	В3	V <sub>BUS</sub>	USB V <sub>BUS</sub> Supply Voltage. Connect V <sub>BUS</sub> to a positive 5.0V power supply. Bypass V <sub>BUS</sub> to ground with a 1.0µF ceramic capacitor as close as possible to the V <sub>BUS</sub> pin.
Т8	M4	B4	V <sub>DDB</sub>	$3.3V$ Regulated $V_{BUS}$ Output. This pin must be connected to ground with a $4.7\mu F$ ceramic capacitor as close as possible to the $V_{DDB}$ pin.

ВА		вимр			
MAX32600-P85 (192 BALL)	MAX32600-J85 (120 BALL)	MAX32600-W85 (WLP)	NAME	FUNCTION	
RESET PINS					
H16	D12	E9	RSTN	Hardware Reset (Active Low) Input. Entire chip is reset (POR) except for RTC circuitry.	
U9	М9	C8	SRSTN	Software Reset (Active Low) Input. Resets ARM core and digital peripherals/registers that are normally cleared by a system reset. Does not affect the RTC or POR-reset-only settings; does not reset the ARM debug engine or JTAG debugger state. After sampling SRSTN as a logic 0, SRSTN is driven low for 6 clock cycles. Additionally, SRSTN is driven low for at least 6 clock cycles due to a watchdog reset, firmware reboot, ARM reset request, ARM lockup, or power-fail event.	
ANALOG SPST	SWITCHES			·	
D1	D3	E6	SCM0	Analog Switch 0 Common Terminal	
E1	E3	D6	SNO0	Analog Switch 0 Normally Open Terminal	
D3	E1	E8	SCM1	Analog Switch 1 Common Terminal	
E3	D1	D8	SNO1	Analog Switch 1 Normally Open Terminal	
B1	A3	_	SCM2	Analog Switch 2 Common Terminal	
C1	В3	_	SNO2	Analog Switch 2 Normally Open Terminal	
A3	A1	G5	SCM3	Analog Switch 3 Common Terminal	
В3	B1	G4	SNO3	Analog Switch 3 Normally Open Terminal	
TAMPER DETE	CTION PINS				
T11	L8	A7	TAMPERI	Connect to TAMPERO through a PCB trace that is uninterrupted. Used by trust protection unit (TPU) to prevent external tampering of the system. If the TAMPERO signal is interrupted, TAMPERI causes a tamper event to the device.	
C13	D11	Н9	TAMPERO	Connect to TAMPERI through a PCB trace that is uninterrupted. Used by TPU to prevent external tampering of the system. If the TAMPERO signal is interrupted, TAMPERI causes a tamper event to the device.	
JTAG PINS					
Т9	G11	C10	TCK	JTAG TCK Pin, Weak Pullup	
U11	H12	C11	TDI	JTAG TDI Pin, Weak Pullup	
U10	G12	B12	TDO	JTAG TDO Pin	
V10	M11	В7	TMS	JTAG TMS Pin, Weak Pullup	
T10	M10	D9	TSEL	JTAG TSEL Pin, Weak Pullup	
POWER PINS					
L10	L4	A4	V <sub>DD</sub>	Digital Supply Voltage. This pin must be connected to ground through at least a 4.7µF external ceramic chip capacitor.	

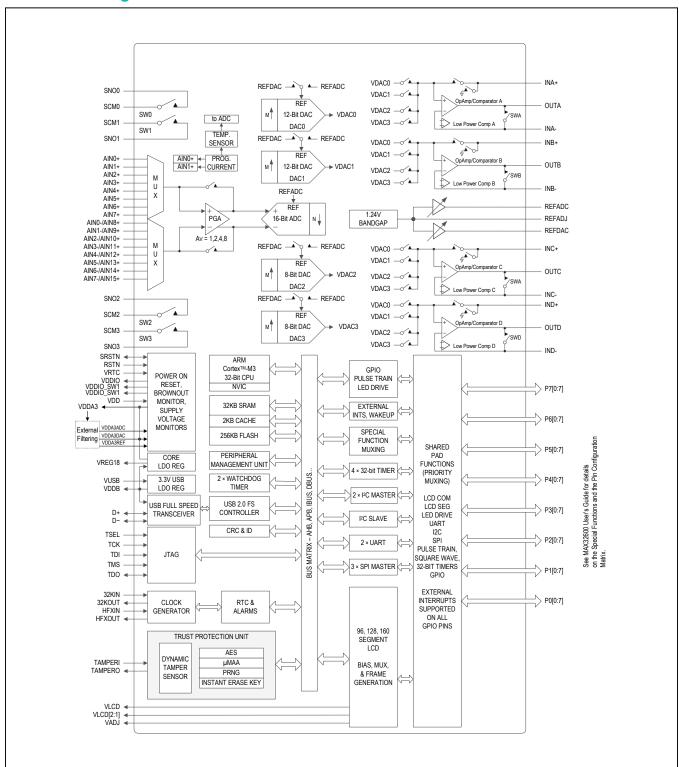
BA	LL	BUMP			
MAX32600-P85 (192 BALL)	MAX32600-J85 (120 BALL)	MAX32600-W85 (WLP)	NAME	FUNCTION	
K11, L11	L7	B6, J8	VREG18	Regulator Capacitor. This pin must be connected to ground through at least a $1.0\mu\text{F}$ external ceramic-chip capacitor. The capacitor must be placed as close to this pin as possible. No external devices other than the capacitor should be connected to this pin. Note: On the WLP package, the capacitor should be placed as close as possible to bump B6.	
V9	N5	B5	V <sub>RTC</sub>	3V Nominal Backup Supply Input Voltage. Connect to 3V nominal power supply. This pin must be connected to ground through a 1.0µF external ceramic chip capacitor.	
A14, B14, C16, J9, J10, J16, K9, K10, T13, T16, U7, V7	B12, C12, H11, M5, M7, M8, N8, N11	H2, G3, G9, F4–F9, E7, D7, B2	V <sub>SS</sub>	Digital Ground	
F1, F2, F3, G2, H2, J1, J2, J3, K2, L2, M1, M2, N2, P2, R1, R2, R3, T2, T3, T4, U2, U4, V2, V4	H2, J2, J3, K2, L2, M2, N2	D2–D5, E2, E5, F2	Vssadc	ADC Ground	
A2, A4, A8, A12, B2, B4–B12, C2, C3, C4, C12, D2, E2	A8, B2, B4– B11, C1–C4, C8, D2, E2	G6, H3–H7, J7	VSSDAC	DAC Ground	
L8	G1	E1	VSSREF	Reference Ground	
H10	A2	C5	VSSUB	Substrate Ground. Connect to V <sub>SS</sub> .	
L9	L1	B1	V <sub>DDA3</sub>	Analog Supply Voltage. This pin must be connected to ground through a 1.0µF external ceramic chip capacitor.	
М3	H1	C2	V <sub>DD</sub> A3ADC	ADC Analog Supply Voltage. This pin must be connected to ground through a 10µF external ceramic chip capacitor.	
C8	A4	J4	V <sub>DD</sub> A3DAC	DAC Analog Supply Voltage. This pin must be connected to ground through a 1.0µF external ceramic chip capacitor.	
H8	F2	F3	V <sub>DD</sub> A3REF	Analog Reference Supply Voltage. This pin must be connected to ground through a 1.0µF external ceramic chip capacitor.	
H11, J11	M6	C9	V <sub>DDIO</sub>	I/O Supply Voltage. This pin must be connected to ground through at least a 1.0μF external ceramic chip capacitor.	
_	A12	J9	V <sub>DDIO</sub> SW1	Switchable I/O Supply Voltage 1. Connect to either the VREG18 (1.8V) or V <sub>DDIO</sub> (3V) supply to set the I/O supply rail for ports P0 and P1. This pin must be connected to ground through at least at 1.0µF external ceramic chip capacitor. Note: Port P6 and P7 are always powered from V <sub>DDIO</sub> .	

ВА		BUMP			
MAX32600-P85 (192 BALL)	MAX32600-J85 (120 BALL)	MAX32600-W85 (WLP)	NAME	FUNCTION	
_	G13	C7	V <sub>DDIO</sub> _ SW2	Switchable I/O Supply Voltage 2. Connect to either the VREG18 (1.8V) or VDDIO (3V) supply to set the I/O supply rail for ports P2, P3, P4, and P5. This pin must be connected to ground through at least a 1.0µF external ceramic chip capacitor. Note: Port P6 and P7 are always powered from VDDIO.	
LCD PINS					
V6	_	_	V <sub>LCD</sub>	LCD Bias Control Voltage. Highest LCD drive voltage used with static bias. If using LCD functionality, this pin must be connected to ground through at least a 1.0µF external ceramic chip capacitor.	
V5	_		V <sub>LCD1</sub>	LCD Bias Voltage 1. LCD drive voltage used with 1/2 and 1/3 LCD bias. An internal resistor-divider sets the voltage. External resistors and capacitors can be used to change the LCD voltage or drive capability at this pin. If using LCD functionality, this pin must be connected to ground through at least a 1.0µF external ceramic chip capacitor.	
U5	_	_	V <sub>LCD2</sub>	LCD Bias Voltage 2. LCD drive voltage used with 1/3 LCD bias. An internal resistor-divider sets the voltage. External resistors and capacitors can be used to change LCD voltage or drive capability at this pin. If using LCD functionality, this pin must be connected to ground through at least a 1.0µF external ceramic chip capacitor.	
Т5	_	_	VADJ	LCD Adjustment Voltage. Connect to an external resistor to provide external control of the LCD contrast. Leave disconnected for internal contrast adjustment. If using LCD functionality, this pin must be connected to ground through at least a 1.0µF external ceramic chip capacitor.	
GENERAL-PUR	RPOSE I/O				
C14	J12	B11	P0.0		
B15	J11	A11	P0.1		
A15	K12	B10	P0.2	General-Purpose, Digital, I/O and Alternate Functions. These port	
C15	L12	A10	P0.3	pins function as bidirectional I/O pins. All port pins default to high-	
B16	L11	В9	P0.4	impedance mode with weak pullups after a reset. All alternate	
A16	K11	A9	P0.5	functions must be enabled from software.	
B17	L10	B8	P0.6		
A17	L9	A8	P0.7		

ВА	.LL	BUMP		
MAX32600-P85 (192 BALL)	MAX32600-J85 (120 BALL)	MAX32600-W85 (WLP)	NAME	FUNCTION
B18	C13	H10	P1.0	
C17	D13	J10	P1.1	
C18	E11	F11	P1.2	General-Purpose, Digital, I/O and Alternate Functions. These port
D16	E12	G11	P1.3	pins function as bidirectional I/O pins. All port pins default to high-
D17	E13	J11	P1.4	impedance mode with weak pullups after a reset. All alternate
D18	F11	H11	P1.5	functions must be enabled from software.
E17	F12	H12	P1.6	
E18	F13	G12	P1.7	
E16	H13	E10	P2.0	
F16	J13	F12	P2.1	
F17	K13	E11	P2.2	General-Purpose, Digital, I/O and Alternate Functions. These port
F18	L13	E12	P2.3	pins function as bidirectional I/O pins. All port pins default to high-
G16	M12	D11	P2.4	impedance mode with weak pullups after a reset. All alternate
G17	M13	D12	P2.5	functions must be enabled from software.
G18	N12	D10	P2.6	
H18	N13	C12	P2.7	
H17	_	_	P3.0	
J18	_	_	P3.1	
J17	_	_	P3.2	General-Purpose, Digital, I/O and Alternate Functions. These port
K18	_	_	P3.3	pins function as bidirectional I/O pins. All port pins default to high-
K17	_	_	P3.4	impedance mode with weak pullups after a reset. All alternate
K16	_	_	P3.5	functions must be enabled from software.
L18	_	_	P3.6	
L17			P3.7	
L16	_	_	P4.0	
M18	_	_	P4.1	
M17	_	_	P4.2	General-Purpose, Digital, I/O and Alternate Functions. These port
M16	_	_	P4.3	pins function as bidirectional I/O pins. All port pins default to high-
N18	_	_	P4.4	impedance mode with weak pullups after a reset. All alternate
N17	_	_	P4.5	functions must be enabled from software.
N16	_	_	P4.6	
P18			P4.7	

ВА	<b>LL</b>	ВИМР		
MAX32600-P85 (192 BALL)	MAX32600-J85 (120 BALL)	MAX32600-W85 (WLP)	NAME	FUNCTION
P17	_	_	P5.0	
P16	_	_	P5.1	
R18	_	_	P5.2	General-Purpose, Digital, I/O and Alternate Functions. These port
R17	_	_	P5.3	pins function as bidirectional I/O pins. All port pins default to high-
R16	_	_	P5.4	impedance mode with weak pullups after a reset. All alternate
T18	_	_	P5.5	functions must be enabled from software.
T17	_	_	P5.6	
U18	_	_	P5.7	
V17	_	_	P6.0	
U17	_	_	P6.1	
V16	_	_	P6.2	General-Purpose, Digital, I/O and Alternate Functions. These port
U16	_	_	P6.3	pins function as bidirectional I/O pins. All port pins default to high-
V15	_	_	P6.4	impedance mode with weak pullups after a reset. All alternate
U15	_	_	P6.5	functions must be enabled from software.
T15	_	_	P6.6	
V14	_	_	P6.7	
U14	_	_	P7.0	
T14	_	_	P7.1	
V13	_	_	P7.2	General-Purpose, Digital, I/O and Alternate Functions. These port
U13	_	_	P7.3	pins function as bidirectional I/O pins. All port pins default to high-
V12	_	_	P7.4	impedance mode with weak pullups after a reset. All alternate
U12			P7.5	functions must be enabled from software.
T12	_	_	P7.6	
V11			P7.7	
_	_	A1, A12, H1, J1, J12	N.C.	Not Connected. Leave unconnected.
_	_	C6	CFG	Must Be Tied to V <sub>DDIO</sub> .

# **Functional Diagram**



### **Detailed Description**

The MAX32600 microcontroller is based on the industry-standard ARM Cortex-M3 32-bit RISC CPU and includes 256KB of flash memory, 32KB of SRAM, and a 2KB 2-way set associative cache. The device includes three SPI master interfaces, two UARTs, two I<sup>2</sup>C master interfaces and one I<sup>2</sup>C slave interface, four 32-bit timers (each of which can be optionally split into dual 16-bit timers), a real-time clock (RTC) with three programmable alarms, dual independent windowed watchdog timers, and four supply voltage monitors with multiple user-selectable, low-voltage detection levels.

For system security and integrity checking, a trust protection unit (TPU) is optionally available that includes all necessary features to secure communications and protect internal data and firmware.

Integrated high-performance analog peripherals include a 16-bit ADC with input buffer, programmable gain amplifier, and a dual 8:1 differential (or 16:1 single-ended) input mux, two 12-bit DACs, two 8-bit DACs, four operational amplifiers with comparator mode, four low-power comparators, an internal temperature sensor, a high-precision internal programmable reference, and four SPST analog switches.

Amultichannel PMU (peripheral management unit) interface, with operation during run mode and low-power sleep mode, can be used to configure and transfer data to and from peripherals including the ADC, DACs, communications ports, USB, TPU, and the CRC hardware module.

#### **ARM Cortex-M3 Core**

The device is based on the ARM Cortex M3 32-bit RISC CPU, which implements the ARMv7-M architectural profile. The implementation of the Cortex M3 core used in the device is targeted for a maximum operating frequency of 24MHz and provides the following features:

- 32-bit data path with mixed 16-bit and 32-bit instructions (Thumb<sup>®</sup>-2 instruction set)
- Single-cycle multiplication and hardware-based division operations
- Nested vectored interrupt controller (NVIC) with multiple interrupt priority levels and nested interrupt support

- 32-bit byte address data pointers for a maximum addressable 4GB memory space, shared by code memory, data memory, ARM core peripherals and device-specific peripherals
- Low-power, highly energy efficient core reduces power consumption
- Built-in debug functionality with JTAG port (connects to internal debug access port)
- Power-saving sleep and deep sleep modes with fast wake-up

### **Interrupt Sources**

The devices include the ARM Nested Vector Interrupt Controller (NVIC) providing high-speed, deterministic response, interrupt masking, and multiple interrupt sources. Each peripheral is connected to the NVIC and can have multiple interrupt flags indicating the specific source of the interrupt within the peripheral. The device supports up to 64 distinct interrupt sources (including internal and external interrupts), with eight priority levels.

#### **Low Power Modes**

The MAX32600 has multiple operating modes with many user-configurable options offering significant flexibility in total power consumption. These options are stored in the data retention power domain registers and are continuously powered across all modes of operation. The registers dictate which analog and digital peripherals are intended to remain enabled during low power modes. Likewise, there are dedicated system registers that dictate the configuration of features during run modes. The MAX32600 supports four power modes: LP0: STOP, LP1: STANDBY, LP2: PMU, and LP3: RUN.

The low power modes (LP0: STOP and LP1: STANDBY) are under the control of the Power Sequencer, while LP2: PMU is controlled by the PMU, and the LP3: RUN mode is controlled by the ARM core.

The VRTC power pin (powered by battery or super cap) ensures that this domain is always on during battery change or other loss-of-power events on the main supply.

Thumb is a registered trademark of ARM Ltd.

### **PMU**

The device's peripheral management unit (PMU) is a DMA-based linked list processing engine. The PMU can perform operations and data transfers involving memory and/or peripherals in the Advanced Peripheral Bus (APB) and Advanced High-performance Bus (AHB) peripheral memory space while the main CPU is in a sleep state. This allows low-overhead peripheral operations (for which intensive CPU resources are not required) to be performed without the CPU, significantly reducing overall power consumption. Additionally, for certain analog and digital operations, switching the CPU off and handling the operations using the PMU provides a lower-noise environment that is critical for obtaining optimum analog-to-digital converter (ADC) and digital-to-analog converter (DAC) performance.

#### **CRC Module**

A CRC hardware module is included to provide fast calculations and data integrity checks by application software. The CRC module supports both the CRC-16-CCITT and CRC-32 polynomials. The CRC-16 and CRC-32 calculation engines operate independently in parallel; each CRC engine has a programmable start seed and can be used to calculate checksums of arbitrarily long data sequences. Data can be loaded either directly or using the PMU; the CRC-16-CCITT completes in two clock cycles and the CRC-32 completes in four clock cycles for each data input calculated.

#### **Watchdog Timers**

The device provides two independent watchdog timers (WDT) with window support. The watchdog timers are independent and have multiple clock source options to ensure system security. The watchdog uses a 32-bit timer with prescaler to generate the watchdog reset. When enabled, the watchdog timers must be fed prior to timeout or within a window of time if window mode is enabled. Failure to feed the watchdog timer during the programmed timing window results in a watchdog timeout.

#### 32-Bit/16-Bit Timers

The device includes four 32-bit timers that are usable for timing, capture/compare, or generation of pulse-width modulated (PWM) signals. Each 32-bit timer can optionally be split into a pair of 16-bit timers. The capture/compare, input/output, and PWM options are available on the 32-bit timers only.

Features of the 32-bit timers include the following:

 32-bit counter with one-shot and continuous autoreload modes

- Programmable prescaler for timer input clock
- External I/O pin option allows selectable input or output function for each timer instance using GPIO pin
- Output mode can be used for PWM output generation or timer rollover output
- Input mode can be used for timer input (counter mode), clock gating or capture, limited to an input frequency of one-fourth the peripheral clock frequency
- Timer interrupt

#### **Real-Time Clock**

A binary real-time clock (RTC) keeps the time of day in a 32-bit timer with resolution programmable from 244µs to 1 second. With a 1-second tick frequency, the RTC can count up to 139 years before rolling over. Two time-of-day alarms can be used to trigger an interrupt or wake up the devices from low-power mode when the RTC timer reaches a specified value; a separate sub-second alarm can be set to trigger on a programmable subdivide of the RTC tick period. For example, with a 1-second RTC resolution, the sub-second alarm can be triggered every second, every 500ms, every 250ms, every 125ms, and so on down to a minimum of 244µs.

#### **USB Device Controller**

The integrated USB controller is compliant with the USB 2.0 specification, providing full-speed operation as a USB peripheral device. Integrating the USB physical interface (PHY) allows direct connection to the USB cable, reducing board space and overall system cost. An integrated voltage regulator enables smart switching between the main supply and  $V_{BUS}$  when connected to a USB host controller.

The USB controller includes a dedicated DMA engine (separate from the PMU) that is used to transfer data to and from the endpoint buffers located in SRAM. A total of seven endpoint buffers are supported with configurable selection of IN or OUT, in addition to Endpoint 0, which is used for control purposes only.

### I<sup>2</sup>C Master/Slave Interfaces

Two I<sup>2</sup>C master interfaces and one I<sup>2</sup>C slave interface are available for communication with a wide variety of other I<sup>2</sup>C-enabled peripherals. The I<sup>2</sup>C bus is a 2-wire, bidirectional bus using a ground line and two bus lines, the serial data line (SDA) and the serial clock line (SCL). Both the SDA and SCL lines must be driven as open-collector/drain outputs. External resistors (R<sub>P</sub>) are required pull the lines to a logic-high state.

The device supports both the master and slave protocols. In the master mode, the interfaces have ownership of the I<sup>2</sup>C bus, drive the clock, and generate the START and STOP signals. This allows them to send data to a slave or receive data from a slave as required. In slave mode, the interfaces rely on an externally generated clock to drive SCL and respond to data and commands only when requested by the I<sup>2</sup>C master device.

#### **SPI Master Interfaces**

The device has three SPI master interface ports. Each SPI controller provides an independent master-mode serial communication channel that communicates synchronously with peripheral SPI devices in a single or multiple slave system. The third SPI instance is intended for future Bluetooth module communication.

The SPI controllers support half- or full-duplex communications with single, dual, or quad data transmission modes, and can be operated in master mode only. Multiple slave select lines are available with configurable polarity, and optional slave ready (SR) inputs can be used for hardware flow control for SPI devices that support this function.

### **UART Interfaces**

The device has two serial communication interfaces. The universal asynchronous receiver-transmitter (UART) interface ports support full-duplex asynchronous communications. The two UARTs implemented on the devices are identical in behavior and can be configured independently.

UART features include the following:

- 2-wire interface
- Programmable transmit and receive interrupts
- Independent baud-rate generators
- Programmable even/odd/no parity modes
- Programmable start/stop bit options
- Character lengths of 5/6/7/8 bits supported
- Optional hardware flow control (RTS/CTS)

### **LCD Controller**

The 192-ball MAX32600 include an LCD controller with a boost regulator that interfaces directly to common low-voltage liquid crystal displays. By integrating the LCD controller in hardware, the device allows designs that require only an LCD glass rather than a considerably

more expensive LCD module. Every character in an LCD glass is composed of one or more segments, each of which is activated by selecting the appropriate segment and common signal.

The LCD controller can multiplex combinations of up to 40 segment outputs (SEG0 to SEG39) and four common signal outputs (COM0 to COM3). Unused segment outputs can be used as standard GPIO port pins. The segments are easily addressed by writing to dedicated display memory. Once the LCD controller settings and display memory have been initialized, the 21-byte display memory is periodically scanned, and the segment and common signals are generated automatically at the selected display frequency, with no additional CPU intervention required.

The design is further simplified and cost reduced by the inclusion of software-adjustable internal voltage-dividers to control display contrast, using either  $V_{DDIO}$  or an external voltage. If desired, contrast can also be controlled with an external resistor network.

Features of the LCD controller include the following:

- Automatic LCD segment and common-drive signal generation
- Integrated boost regulator ensures LCD operation over entire digital operating range
- Flexible LCD clock source selection with adjustable frame frequency
- Internal voltage-divider resistors eliminate requirement for external components
- Internal adjustable resistor allows contrast adjustment without external components
- Four display modes are supported by the LCD controller:
- Static (COM0)
- 1/2 duty multiplexed with 1/2 bias voltages (COM[0:1])
- 1/3 duty multiplexed with 1/3 bias voltages (COM[0:2])
- 1/4 duty multiplexed with 1/3 bias voltages (COM[0:3])

The voltages available for driving the LCD are  $V_{LCD}$ ,  $V_{LCD} \times 2/3$ ,  $V_{LCD} \times 1/3$ , and  $V_{ADJ}$ . The 1/2-bias mode, which uses an output level of  $V_{LCD} \times 1/2$ , requires two of the LCD voltage supply pins ( $V_{LCD2}$  and  $V_{LCD1}$ ) to be shunted together externally.

### 16-Bit ADC with PGA

The devices include a 16-bit analog-to-digital converter (ADC) with a 16-channel analog input multiplexer, to allow selection of an analog input from one of 16 input lines (single-ended mode) or one pair of eight input pairs (differential mode). The differential mode supports fully differential signal inputs.

The front end PGA allows programmable gain settings of x1, x2, x4, and x8 before the input sample is converted. An anti-aliasing filter is included between the output of the PGA and the ADC sample conversion stage.

The ADC reference voltage is selectable between  $V_{DDA3}$  and the dedicated ADC reference level. The ADC reference level can be set by software to one of four output levels—1.024V, 1.5V, 2.048V, and 2.5V—based on the 1.24V reference bandgap.

# ADC/DAC Internal/External Reference and Programmable Output Buffers

Two programmable reference levels (one used by the ADC, one used by the DACs) are included, and each can be individually set to one of four output levels. An external reference can also be provided at the REFADJ pin; if this feature is used, the external reference voltage is used in place of the 1.24V bandgap output, and the programmable output levels for the ADC and DAC references shift accordingly.

#### 12-Bit Voltage Output DACs

The device includes two 12-bit voltage output DACs that output single-ended voltages. The reference used by these DACs is selectable between the DAC reference level and the ADC reference level. Each DAC instance includes PMU channel access to allow output values to be loaded to the DAC directly from memory.

### 8-Bit Voltage Output DACs

The device includes two 8-bit voltage output DACs that output single-ended voltages. The reference used by these DACs is selectable between the DAC reference level and the ADC reference level. Each DAC instance includes PMU channel access to allow output values to be loaded to the DAC directly from memory.

# Uncommitted Op Amps with Comparator Mode

The device contains four uncommitted operational amplifiers. Any unused op amp should be connected with its positive input pin grounded and the negative input pin and output pin shorted together. Each op amp can be switched between amplifier and comparator mode under software control.

Each op amp contains an integrated internal switch that can be used to short the negative/inverting input pin to the output pin of the op amp under software control, putting the op amp in a voltage follower mode. In this configuration, the op amp can be used as an output buffer for any of the four DAC outputs. Any of the four DAC outputs may optionally be internally connected to the noninverting inputs of one or more of the four op amps, under software control.

#### **Uncommitted SPST Analog Switches**

The device contains four uncommitted SPST analog switches that can be opened and closed under software control. All SPST switches are open by default following any reset or power-on reset. The SPST switches support input voltages from ground to  $V_{\rm DDA3}$ .

### **Temperature Sensor**

The device includes an internal temperature sensor that can be read using the ADC, and additionally supports a mode for an external temperature sensor, which is connected to the same ADC input pair.

### **Additional Benefits and Features**

- Industry-Standard Core and Flexible Peripherals Enable Rapid Prototyping for Improved Time to Market
  - · ARM Cortex-M3 32-Bit RISC CPU Single-Cycle Multiplication Nested Vectored Interrupt Controller
  - Memory

256KB Flash Memory with 2KB Instruction Cache 32KB SRAM

- · Supply Voltage
  - 1.8V to 3.6V Digital Supply Voltage 2.3V to 3.6V Analog Supply Voltage
- · Tool Chains Supported Include GNU, Eclipse, and IAR
- Low Power Wakeup (LP0/LP1)

**RTC Timeout** 

244µs Resolution

Multiple Timer Wakeup Options

All 64 GPIO Level Sensitive

**USB** Power Detection

- Peripheral Management Unit (PMU)
  - PMU Services Peripherals While CPU is in Sleep Mode
  - Saves Power when ARM Cortex-M3 Core is Inactive
  - 6 PMU Channels. Each with Read/Write Access to All AHB and APB Devices
- Digital and Communication Peripherals
  - 4 × 32-Bit Timers, Configurable to 8 x 16-Bit 32-Bit Real-Time Clock with Subsecond Alarm and Two Time-of-Day Alarms

Dedicated Backup Supply Pin and Trickle Charge Four Programmable Supply Voltage Detectors

Power-On-Reset/Brownout Reset

Two Programmable Windowed Watchdog Timers Three SPI Masters, Two UARTs, Two I<sup>2</sup>C Masters, and One I<sup>2</sup>C Slave Port

Up to 64 GPIO Pins with External Interrupt and Wake from Low-Power Mode Support

- 2.0 Full-Speed Compliant USB Integrated Transceiver with Regulator, On-Chip Termination and Pullup Resistors 5V to 3.3V Regulation with Integrated Supply
  - Management to Enable USB-Compliant Switching Dedicated USB DMA Engine Allows Automatic Transfer of Endpoint Data to/from SRAM
- Pulse Train Engine with Eight Digital Output Channels and 5 Analog Control Outputs
- · Clock Sources

USB Device Interface

32kHz Crystal Oscillator for Accurate RTC External High-Frequency Crystal Oscillator PLL Generates 48MHz USB Clock (2x/4x/6x HFX) Internal 24MHz ±1% Relaxation Oscillator

LCD Controller

96. 128. or 160 Seaments

4 x 24, 4 x 32, 4 x 40

Static, 1/2, 1/3, and 1/4 Duty Cycle Boost Converter for 3.3V V<sub>I CD</sub> Operation Adjustment Resistor for Contrast Control Eliminates

Requirement for External Components

# **Ordering Information**

PART	TEMP RANGE	PIN-PACKAGE
MAX32600-P85A+	-40°C to +85°C	192 CTBGA
MAX32600-P85B+	-40°C to +85°C	192 CTBGA
MAX32600-J85A+	-40°C to +85°C	120 CTBGA
MAX32600-J85B+	-40°C to +85°C	120 CTBGA
MAX32600-W85A+	-40°C to +85°C	108 WLP
MAX32600-W85B+	-40°C to +85°C	108 WLP

<sup>+</sup>Denotes a lead(Pb)-free/RoHS-compliant package.

# **Package Information**

For the latest package outline information and land patterns (footprints), go to <a href="https://www.maximintegrated.com/packages">www.maximintegrated.com/packages</a>. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

	CKAGE YPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
192	CTBGA	X19222+1C	<u>21-0712</u>	_
120	CTBGA	X12077+1C	21-0899	_
108	8 WLP	W1084A5+1	21-1075	_

### **Selector Table**

PART	FLASH (KB)	SRAM (KB)	ADC CHANNELS	TRUST PROTECTION UNIT (TPU)	LCD	PIN-PACKAGE
MAX32600-P85A+	256	32	16 × 1, 8 × 2	No	160-segment	12mm × 12mm CTBGA
MAX32600-P85B+	256	32	16 × 1, 8 × 2	Yes	160-segment	12mm × 12mm CTBGA
MAX32600-J85A+	256	32	12 × 1, 6 × 2	No	No LCD	7mm × 7mm CTBGA
MAX32600-J85B+	256	32	12 × 1, 6 × 2	Yes	No LCD	7mm × 7mm CTBGA
MAX32600-W85A+	256	32	6 × 1, 3 × 2	No	No LCD	5.4mm × 4.3mm WLP
MAX32600-W85B+	256	32	6 × 1, 3 × 2	Yes	No LCD	5.4mm × 4.3mm WLP

### **Package/Feature Details**

FEATURE	5.4mm x 4.3mm WLP	7mm x 7mm CTBGA	12mm x 12mm CTBGA
LCD	_	_	160-segment
GPIO (8-bit ports)	3	3	8
ADC inputs	6 single/ 6 differential	12 single/ 6 differential	16 single/ 8 differential
Internal only op amp	1	0	0
External input, external output op amp	2	0	0
Fully external op amp control	1	4	4
Two-pad switches	3	4	4
Shared-pad switches	1	0	0

# **Revision History**

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/14	Initial release	_
1	10/14	Added WLP package and updated specifications in the <i>Electrical Characteristics</i> table	1–3, 5–7, 11–13, 15–24, 29, 30
2	11/14	Revised Benefits and Features section	1, 30
3	12/14	Updated Simplified Functional Diagram, Electrical Characteristics table notes, Ball/Bump Descriptions, Detailed Description, and USB Device Controller sections, Package/Feature Details table, and replaced ball configurations	1–18, 20–34
4	6/15	Replaced the Simplified Functional Diagram; updated the electrical characteristics tables; updated the SRSTN bump description; added the Low Power Modes and PMU sections; added LP0/LP1 information to Additional Benefits and Features section	1–17, 23, 29, 33
5	7/15	Added Note 5 to two DC Characteristics parameters (No Missing Codes and Integral Nonlinearity)	7
6	2/16	Updated Package Thermal Characteristics, ADC/PGA Electrical Characteristics, Internal Voltage Reference Electrical Characteristics, Ball/Bump Description, Detailed Description, Low Power Modes, I <sup>2</sup> C Master/Slave Interfaces sections	2, 8, 14, 21, 22, 27, 29, 30

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

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