

QUICK START GUIDE FOR DEMONSTRATION CIRCUIT 671

POWER-OVER-ETHERNET INTERFACE CONTROLLER

LTC4257CS8-1

DESCRIPTION

Demonstration circuit 671 provides a complete IEEE 802.3af interface and isolated 3.3V power supply solution for use in PD Phone applications. The LTC®4257 performs signature, classification, and power interface functions to switch power to a 48V to 3.3V isolated Flyback converter featuring the LT1737.

The LTC4257-1 simplifies Powered Device (PD) design by incorporating the 25k Ω signature resistor, classification current source, inrush current limit, under-voltage lockout, thermal current limit, and power good signaling, all in a single 8-pin package. The LT1737 provides efficient conversion from 48V to 3.3V.

Design files for this circuit board are available. Call the LTC factory.

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Table 1. Typical Performance Summary

PARAMETER	CONDITION	VALUE
Maximum Turn On Voltage	PD Power Up	42V
Minimum Turn Off Voltage	PD Power Down	30V
Minimum Operating Input Voltage	In from PSE	36V
Maximum Operating Input Voltage	In from PSE	57V
Maximum Input Power	In from PSE	12.95W
Maximum Input Current	In from PSE, Vin = 37V	350mA
	In from PSE, Vin = 57V	230mA
Maximum Output Current	Vin = 37V	3.3A
Output Voltage V _{OUT}		3.3V $\pm$ 2%

QUICK START PROCEDURE

Demonstration circuit 671 connects to a PSE for quick evaluation of the LTC4257-1 with the LT1737. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

1. Set JP1 to a selected PD Class of 0 through 4.
2. Set JP2 to Enable to enable the LTC4257-1.
3. Connect a 0 to 3.3A load and meters to the VOUT pins.
4. Connect with an Ethernet cable from an IEEE802.3af compliant PSE to J2.

OPERATION

Demonstration circuit 671 interfaces with a customer's Power-Over-Ethernet test setup per Figure 1. The front end of the demo circuit implements required Ethernet transformer coupling via transformer T2. Common-mode termination (R1, R2, R30, R31) is provided along with a 2KV capacitor (C2). The demo circuit is setup to allow data to pass in and back out of the demo circuit while the DC671 performs IEEE 802.3af interface functions. The Power Sourcing Equipment (PSE) is connected to J2 and the PHY is optionally connected to J1.

Schottky diodes used in a diode bridge configuration on the input signal lines and the spare lines on the front end allows the PD to meet the auto-polarity requirements of IEEE802.3af. Because of the smaller voltage drop than standard diodes, they also provide higher efficiency than typical diode bridges.

The PD is required to have 0.1uF of capacitance during detection and this is provided by C11. It is also required to have at least 5uF of capacitance after the in-rush circuit, provided by capacitors C7, C8 and C15.

This demo circuit allows detection and power classification of the PD per the IEEE 802.3af specification. During the detection process of a PD, the LTC4257-1 displays the proper 25k Ω signature resistor. A current source is implemented within the LTC4257-1 and is programmed by the selection of a single external resistor. The class 0-4 current sources can easily be set in this demo circuit with the placement of a single jumper on JP1.

After detection and classification, the PD is powered up. When the voltage exceeds the LTC4257-1 turn-on UVLO, power is switched over to the switching regulator. The Power Good output pulls active low to signal to the LT1737 to begin operation. This allows for the capacitors to be charged first before the regulator starts to avoid exceeding the limited inrush current.

For the PD to remain powered on, it must present to the PSE both AC and DC components of the Maintain

Power Signature (MPS). The LTC4257-1 holds its 25k signature resistance to satisfy the AC MPS. However, the PD must hold the DC MPS by drawing at least 10mA or the PSE may disconnect power. This demonstration circuit draws more than 10mA when on. Therefore an IEEE compliant PSE would maintain power after detection due to the DC load current.

JP2 enables or disables the LTC4257-1 functions and 25k Ω signature resistance.

The synchronous Flyback converter operates at a nominal switching frequency of 200kHz, controlled by the LT1737. Galvanic isolation is met with transformers T1 and T3. C23 is used as a local bypass to reduce common-mode currents.

The primary side power path is comprised of T1, Q3, R15, and C8. These components should be as close as possible when laying out the printed circuit board. Power is transferred during the off time of Q3. Q6 is the secondary synchronous rectifier. C4 to C6 form the secondary output filter. L1, C7, and C8 form the primary input filter. An auxiliary winding on T1 performs two functions: it provides output feedback information and supplies bias voltage to the LT1737. A driver, comprised of Q7 and Q8, synchronizes with the LT1737 via T3 to provide gate drive to the secondary switching MOSFET. The output voltage can be modified with the selection of R13 and R23.

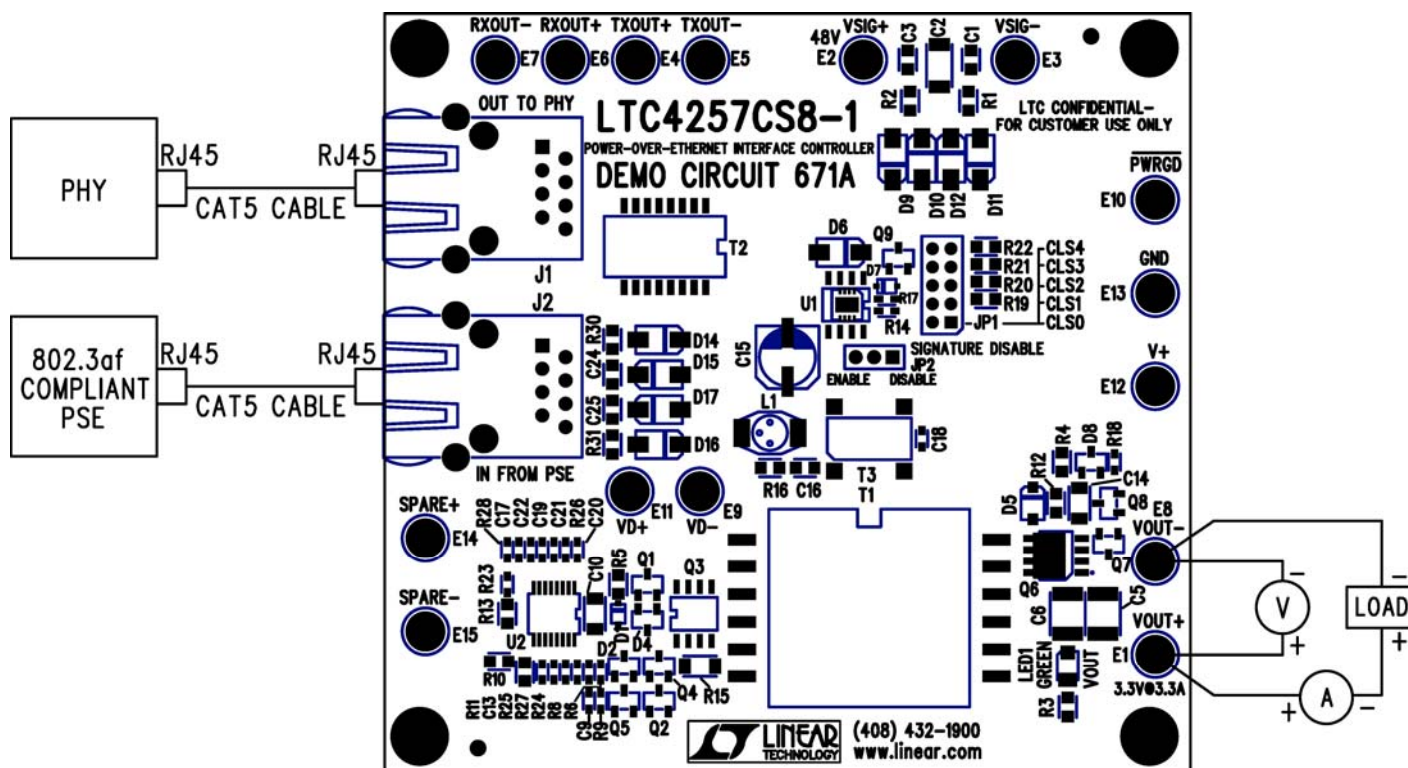
The maximum input power of a PD is 12.95W. IEEE802.3af specifies that at 37V, the steady-state input current to a PD is limited to a maximum of 350mA and the designer must insure their PD does not draw more than this amount while in the highest power mode. To avoid an over-current situation (350 to 400mA for over 50ms, or above 400mA) during startup, this demo circuit also implements a soft-start function. The output voltage of LTC4257-1 ramps up to the final value over several milliseconds while the input current stays below the 350mA limit.

SAFETY AND ISOLATION

The demo board is designed to meet the requirements of UL 60950, 3rd Edition for basic insulation in secondary circuits. The input is considered a TNV-2 circuit, and the output is SELV. The transformer is designed to meet the basic insulation requirement with an isolation voltage of 1500VDC. The core is considered part of the secondary circuit.

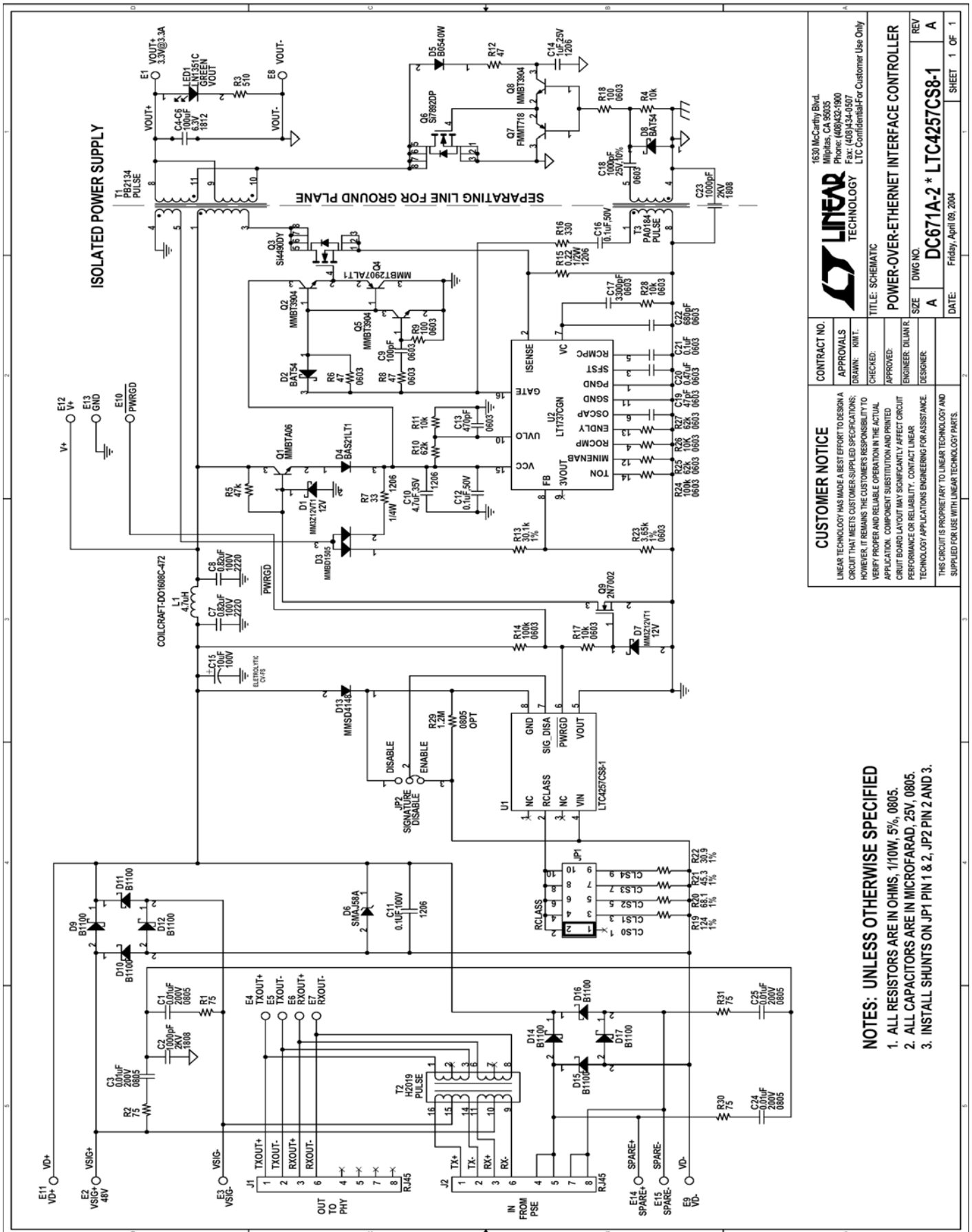
ADDITIONAL INFORMATION

Refer to the LTC4257-1 and LT1737 datasheets for detailed information about the operation of each chip. The demo circuit schematic and parts list are available as well as the circuit board layout to assist in implementing this circuit in customer applications. Contact Linear Technology for a complete range of solutions for Power-Over-Ethernet applications along with a full line of power conversion products.



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POWER-OVER-ETHERNET INTERFACE CONTROLLER



CUSTOMER NOTICE LINEAR TECHNOLOGY HAS MADE A BEST EFFORT TO DESIGN A CIRCUIT THAT MEETS CUSTOMER-SUPPLIED SPECIFICATIONS. HOWEVER, IT REMAINS THE CUSTOMER'S RESPONSIBILITY TO VERIFY PROPER AND RELIABLE OPERATION IN THE ACTUAL APPLICATION. COMPONENT SUBSTITUTION AND PRINTED CIRCUIT BOARD LAYOUT MAY SIGNIFICANTLY AFFECT CIRCUIT PERFORMANCE OR RELIABILITY. CONTACT LINEAR TECHNOLOGY APPLICATIONS ENGINEERING FOR ASSISTANCE.		CONTRACT NO. APPROVALS DRAWN: KMT CHECKED: APPROVED: ENGINEER: DULAH DESIGNER:	
NOTES: UNLESS OTHERWISE SPECIFIED 1. ALL RESISTORS ARE IN OHMS, 1%W, 5%, 0805. 2. ALL CAPACITORS ARE IN MICROFARAD, 25V, 0805. 3. INSTALL SHUNTS ON JP1 PIN 1 & 2, JP2 PIN 2 AND 3.		POWER-OVER-ETHERNET INTERFACE CONTROLLER TITLE: SCHEMATIC SIZE: A DWG NO: DC671A-2 * LTC4257CS8-1 REV: A	
THIS CIRCUIT IS PROPRIETARY TO LINEAR TECHNOLOGY AND SUPPLIED FOR USE WITH LINEAR TECHNOLOGY PARTS.		DATE: Friday, April 09, 2004 SHEET 1 OF 1	



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