

# Advanced Doherty Alignment Module (ADAM)

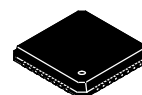
The MMDS25254H is an integrated module designed for use in base station transmitters in conjunction with high power Doherty amplifiers. The device is designed to enable accurate alignment of phase and amplitude on the carrier and peaking amplifiers to ensure performance consistency, in particular for asymmetric implementations. The MMDS25254H enables superior linearity-efficiency trade-off while improving output power. It contains a 90° coupler, digitally selectable phase shifters and step attenuators, and operates from a single voltage supply. The MMDS25254H is suitable for transmit protocols such as W-CDMA, UMTS and LTE using frequencies from 2300 to 2700 MHz, and is controlled using a serial peripheral interface (SPI).

## Features

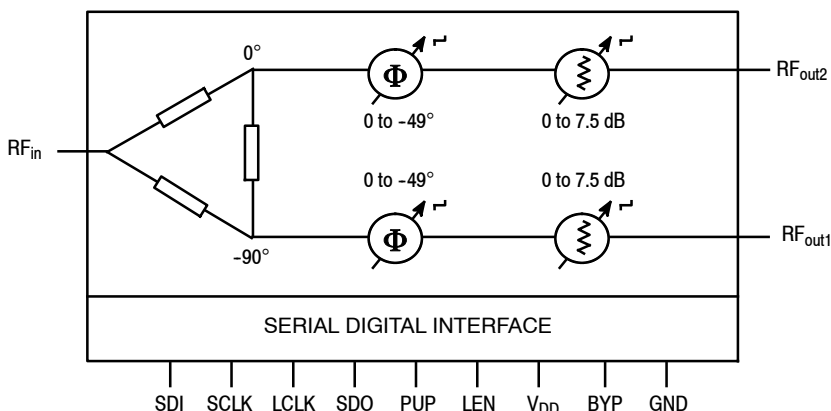
- Frequency: 2300–2700 MHz
- Maximum RF Input Power: 25 dBm (CW)
- Low Loss Power Splitter
- 0.5 dB Step Programmable Attenuators with 7.5 dB Maximum Range
- 7° per Bit Phase Shifters with 49° Maximum Range
- Power up into a Selectable State
- Single 5 Volt Supply
- Supply Current: 12 mA
- 50 Ohm Operation (no external matching required)
- TTL/CMOS/SPI Interface (1.8 V, 3.3 V Logic)
- Cost-effective 32-pin, 6 mm QFN Surface Mount Plastic Package
- In Tape and Reel. T1 Suffix = 1,000 Units, 16 mm Tape Width, 7-inch Reel.

**MMDS25254HT1**

**2300–2700 MHz  
ADAM – ADVANCED DOHERTY  
ALIGNMENT MODULE**



**QFN 6 × 6**



**Figure 1. Functional Block Diagram**

**Table 1. Maximum Ratings**

| Rating                                   | Symbol    | Value         | Unit |
|------------------------------------------|-----------|---------------|------|
| Supply Voltage                           | $V_{DD}$  | 6             | V    |
| Logic Inputs (SCLK, LCLK, LEN, PUP, SDI) | $V_{in}$  | -0.5 to +3.63 | V    |
| RF Input Power (CW)                      | $P_{in}$  | 25            | dBm  |
| Storage Temperature Range                | $T_{stg}$ | -65 to +150   | °C   |
| Junction Temperature                     | $T_J$     | 150           | °C   |

**Table 2. Recommended Operating Conditions**

| Characteristic                          | Symbol   | Min | Max | Unit |
|-----------------------------------------|----------|-----|-----|------|
| Supply Voltage                          | $V_{DD}$ | 4.5 | 5.5 | V    |
| DC Input Voltage (SCLK, LCLK, LEN, SDI) | $V_{in}$ | 0   | 3.3 | V    |

**Table 3. Electrical Characteristics** ( $V_{DD} = 5$  Vdc, 2650 MHz,  $T_A = 25^\circ\text{C}$ , 50 ohm system, in Freescale Application Circuit)

| Characteristic                                                  | Symbol           | Min                | Typ | Max                 | Unit  |
|-----------------------------------------------------------------|------------------|--------------------|-----|---------------------|-------|
| Insertion Loss (Includes 3 dB power division and 2.5 dB loss)   | $I_L$            | —                  | 5.5 | —                   | dB    |
| Max Transition Time (rising edge of LCLK to RF <sub>out</sub> ) | $t_{transition}$ | —                  | 350 | —                   | ns    |
| Power Input @ 1dB Compression                                   | $P_{1dB}$        | —                  | 35  | —                   | dBm   |
| Supply Current                                                  | $I_{DD}$         | 10                 | 11  | 12                  | mA    |
| Isolation (S32)                                                 | $ S_{32} $       | —                  | 25  | —                   | dB    |
| Input Return Loss (S11)                                         | IRL              | —                  | 15  | —                   | dB    |
| Output Return Loss (S22, S33)                                   | ORL              | —                  | 15  | —                   | dB    |
| Third Order Output Intercept Point                              | OIP3             | —                  | 45  | —                   | dBm   |
| Phase Step                                                      | $\Delta\Phi$     | —                  | 7   | —                   | °/bit |
| Phase Control Range                                             | $\Delta\Phi$     | —                  | 49  | —                   | °     |
| Attenuation Step                                                | $\Delta R$       | —                  | 0.5 | —                   | dB    |
| Attenuation Control Range                                       | $\Delta R$       | —                  | 7.5 | —                   | dB    |
| Max Input Voltage Logic Low                                     | $V_{IL}$         | —                  | —   | 0.4                 | V     |
| Min Input Voltage Logic High                                    | $V_{IH}$         | 1.6                | —   | —                   | V     |
| SDO Output Voltage High                                         | $V_{OH}$         | 1.8 <sup>(1)</sup> | —   | $0.6 \times V_{DD}$ | V     |
| SDO Output Voltage Low                                          | $V_{OL}$         | 0                  | —   | 0.4                 | V     |
| Clock Frequency (50% Duty Cycle)                                | $f_{SCLK}$       | —                  | —   | 26                  | MHz   |

1. Load = 20 pF @ maximum clock frequency.

**Table 4. Thermal Characteristics**

| Characteristics                                                                                                                                                                             | Symbol          | Value <sup>(2)</sup> | Unit |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|----------------------|------|
| Thermal Resistance, Junction to Case<br>Case Temperature 107°C, $P_{out} = 0.02$ W, Maximum Phase and Attenuation State, $P_{in} = 25$ dBm CW, 2650 MHz, $V_{DD} = 5$ Vdc, $I_{DD} = 11$ mA | $R_{\theta JC}$ | 16                   | °C/W |

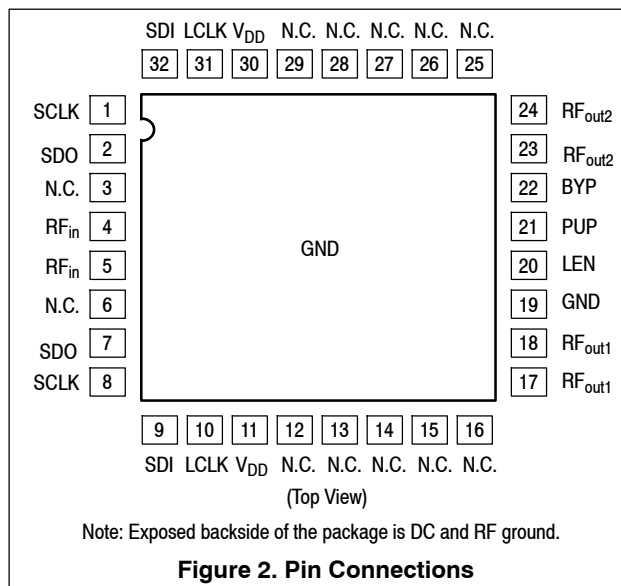
**Table 5. ESD Protection Characteristics**

| Test Methodology                      | Class |
|---------------------------------------|-------|
| Human Body Model (per JESD22-A114)    | 1C    |
| Machine Model (per EIA/JESD22-A115)   | A     |
| Charge Device Model (per JESD22-C101) | III   |

**Table 6. Moisture Sensitivity Level**

| Test Methodology                     | Rating | Package Peak Temperature | Unit |
|--------------------------------------|--------|--------------------------|------|
| Per JESD22-A113, IPC/JEDEC J-STD-020 | 3      | 260                      | °C   |

2. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>.  
Select Documentation/Application Notes – AN1955.



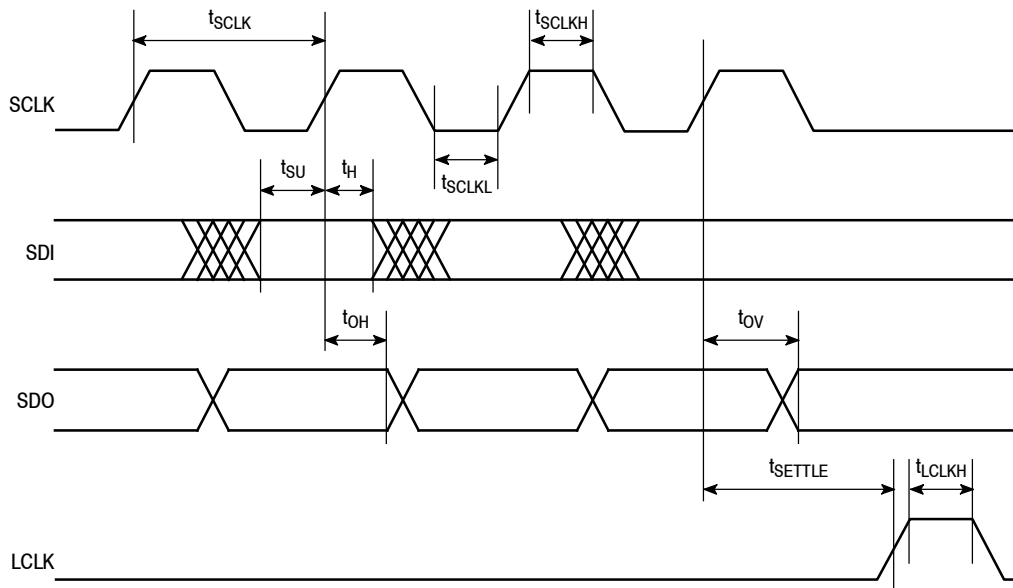
**Table 7. Package Pin Description**

| Pin Number                                   | Pin Function       | Pin Description                                                                                                                                                              |
|----------------------------------------------|--------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1, 8 <sup>(1)</sup>                          | SCLK               | Serial Data Clock                                                                                                                                                            |
| 2 <sup>(2)</sup> , 7 <sup>(1)</sup>          | SDO                | Serial Data Output                                                                                                                                                           |
| 3, 6, 12, 13, 14, 15, 16, 25, 26, 27, 28, 29 | N.C.               | No Connection                                                                                                                                                                |
| 4, 5 <sup>(3)</sup>                          | RF <sub>in</sub>   | RF Input (DC Block Needed)                                                                                                                                                   |
| 9, 32 <sup>(1)</sup>                         | SDI                | Serial Data Input                                                                                                                                                            |
| 10, 31 <sup>(1)</sup>                        | LCLK               | Latch Clock                                                                                                                                                                  |
| 11, 30 <sup>(1)</sup>                        | V <sub>DD</sub>    | Supply Voltage (attenuators, phase shifters, SPI)                                                                                                                            |
| 17, 18 <sup>(3)</sup>                        | RF <sub>out1</sub> | RF Output 1 (peaking amplifier path)                                                                                                                                         |
| 19                                           | GND                | Ground                                                                                                                                                                       |
| 20 <sup>(4)</sup>                            | LEN                | Logic Enable (active low)                                                                                                                                                    |
| 21 <sup>(5)</sup>                            | PUP                | Power-up Programming: <ul style="list-style-type: none"> <li>Minimum attenuation/minimum phase (0 dB/0°)</li> <li>Maximum attenuation/maximum phase (7.5 dB/-49°)</li> </ul> |
| 22 <sup>(6)</sup>                            | BYP                | InternalCore Bypass Voltage (external 100 nF bypass capacitor)                                                                                                               |
| 23, 24 <sup>(3)</sup>                        | RF <sub>out2</sub> | RF Output 2 (carrier amplifier path)                                                                                                                                         |

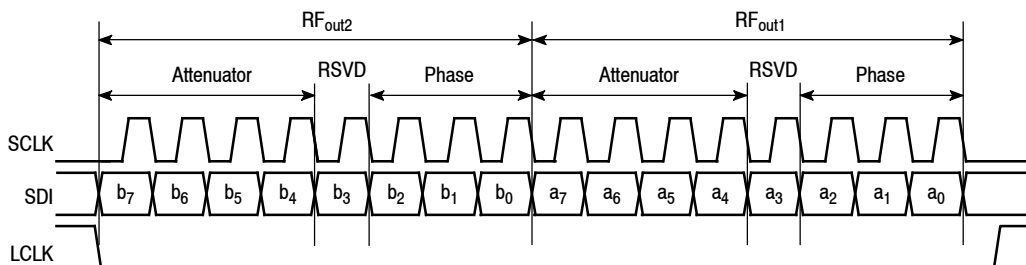
- Redundant pins are internally connected. User can connect to either of the internally connected paired pins: 1 and 8, 2 and 7, 9 and 32, 10 and 31, and 11 and 30.
- The ADAM SPI interface can be connected to a common SPI bus, provided the SDO pin is not connected, and treated as a write-only device.
- Each RF pin pair should be tied together.
- Logic low enables normal SPI operation. Logic high disables SPI and places device at 0 dB attenuation and 0° phase shift.
- Logic low places device at 0 dB attenuation and 0° phase shift at power up. Logic high places device at 7.5 dB attenuation and -49° phase shift. Because PUP pin has internal pull up, logic high can be set by no connection to pin. Alternatively, it can be connected to BYP or a user-controlled V<sub>in</sub>.
- Requires external capacitive decoupling to ground.

**Table 8. Serial Interface Timing Parameters**

| Symbol                    | Parameter                                                      | Min  | Typ | Max | Units |
|---------------------------|----------------------------------------------------------------|------|-----|-----|-------|
| $t_{SCLK}$                | Serial Clock Period                                            | 38.5 | —   | —   | ns    |
| $t_{SCLKH}$               | Serial Clock Pulse Width High                                  | 10   | —   | —   | ns    |
| $t_{SCLKL}$               | Serial Clock Pulse Width Low                                   | 10   | —   | —   | ns    |
| $t_{SU}$                  | Serial Data Input Setup Time to SCLK Rising Edge               | —    | —   | 5   | ns    |
| $t_H$                     | Serial Data Input Hold Time from SCLK Rising Edge              | —    | —   | 2   | ns    |
| $t_{OH}$                  | Serial Data Output Hold Time from SCLK Rising Edge             | 1.6  | —   | —   | ns    |
| $t_{OV} (10 \text{ pF})$  | Serial Data Output Propagation Delay from SCLK Rising Edge     | —    | 5   | 9   | ns    |
| $t_{OV} (50 \text{ pF})$  | Serial Data Output Propagation Delay from SCLK Rising Edge     | —    | 15  | 26  | ns    |
| $t_{OV} (150 \text{ pF})$ | Serial Data Output Propagation Delay from SCLK Rising Edge     | —    | 35  | 65  | ns    |
| $t_{SETTLE}$              | Serial Clock Rising Edge Setup Time to Latch Clock Rising Edge | —    | —   | 27  | ns    |
| $t_{LCLKH}$               | Latch Clock Pulse Width High                                   | 10   | —   | —   | ns    |



**Figure 3. Serial Interface Timing Diagram**



**Note:** Bits a3/b3 are reserved (RSVD) for future use. Always write these bits as zero (0).

**Figure 4. Serial Interface Bits Diagram**

**Table 9. Logic Truth Table — RF<sub>in</sub> to RF<sub>out1</sub>**

| a7 | a6 | a5 | a4 | Attenuation (dB) |
|----|----|----|----|------------------|
| L  | L  | L  | L  | 0                |
| L  | L  | L  | H  | 0.5              |
| L  | L  | H  | L  | 1.0              |
| L  | L  | H  | H  | 1.5              |
| L  | H  | L  | L  | 2.0              |
| L  | H  | L  | H  | 2.5              |
| L  | H  | H  | L  | 3.0              |
| L  | H  | H  | H  | 3.5              |
| H  | L  | L  | L  | 4.0              |
| H  | L  | L  | H  | 4.5              |
| H  | L  | H  | L  | 5.0              |
| H  | L  | H  | H  | 5.5              |
| H  | H  | L  | L  | 6.0              |
| H  | H  | L  | H  | 6.5              |
| H  | H  | H  | L  | 7.0              |
| H  | H  | H  | H  | 7.5              |

| a2 | a1 | a0 | Phase Shift (°) |
|----|----|----|-----------------|
| L  | L  | L  | 0               |
| L  | L  | H  | -7              |
| L  | H  | L  | -14             |
| L  | H  | H  | -21             |
| H  | L  | L  | -28             |
| H  | L  | H  | -35             |
| H  | H  | L  | -42             |
| H  | H  | H  | -49             |

**Table 10. Logic Truth Table — RF<sub>in</sub> to RF<sub>out2</sub>**

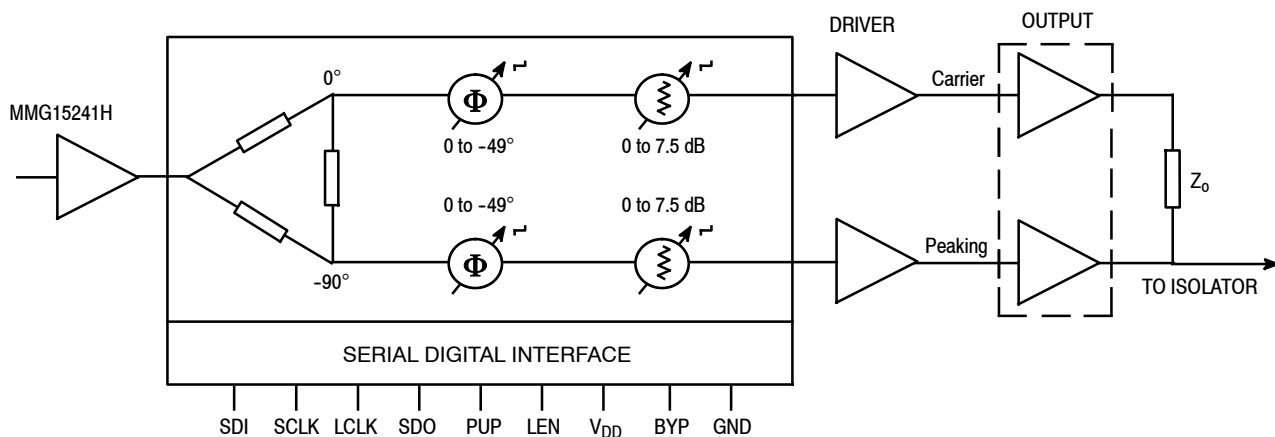
| b7 | b6 | b5 | b4 | Attenuation (dB) |
|----|----|----|----|------------------|
| L  | L  | L  | L  | 0                |
| L  | L  | L  | H  | 0.5              |
| L  | L  | H  | L  | 1.0              |
| L  | L  | H  | H  | 1.5              |
| L  | H  | L  | L  | 2.0              |
| L  | H  | L  | H  | 2.5              |
| L  | H  | H  | L  | 3.0              |
| L  | H  | H  | H  | 3.5              |
| H  | L  | L  | L  | 4.0              |
| H  | L  | L  | H  | 4.5              |
| H  | L  | H  | L  | 5.0              |
| H  | L  | H  | H  | 5.5              |
| H  | H  | L  | L  | 6.0              |
| H  | H  | L  | H  | 6.5              |
| H  | H  | H  | L  | 7.0              |
| H  | H  | H  | H  | 7.5              |

| b2 | b1 | b0 | Phase Shift (°) |
|----|----|----|-----------------|
| L  | L  | L  | 0               |
| L  | L  | H  | -7              |
| L  | H  | L  | -14             |
| L  | H  | H  | -21             |
| H  | L  | L  | -28             |
| H  | L  | H  | -35             |
| H  | H  | L  | -42             |
| H  | H  | H  | -49             |

**Note:** ADAM contains a 16-bit shift register, with the last bit connected to the SDO signal. The SDO pin is intended for daisy-chaining multiple ADAM devices rather than being used as an SPI bus connection; the SDO output is always actively driven, so it should not be directly connected to the SPI bus.

**Table 11. Power-up Programming (PUP) State**

| LCLK               | PUP | Function                                                             |
|--------------------|-----|----------------------------------------------------------------------|
| X                  | 0   | Minimum Attenuation/Minimum Phase (0 dB/0°)                          |
| X                  | 1   | Maximum Attenuation/Maximum Phase (7.5 dB/-49°)                      |
| On 1st rising edge | X   | Normal Operation on 1st Rising Edge LCLK and Subsequent Rising Edges |


**Figure 5. Typical Doherty Base Station Alignment Block Diagram**

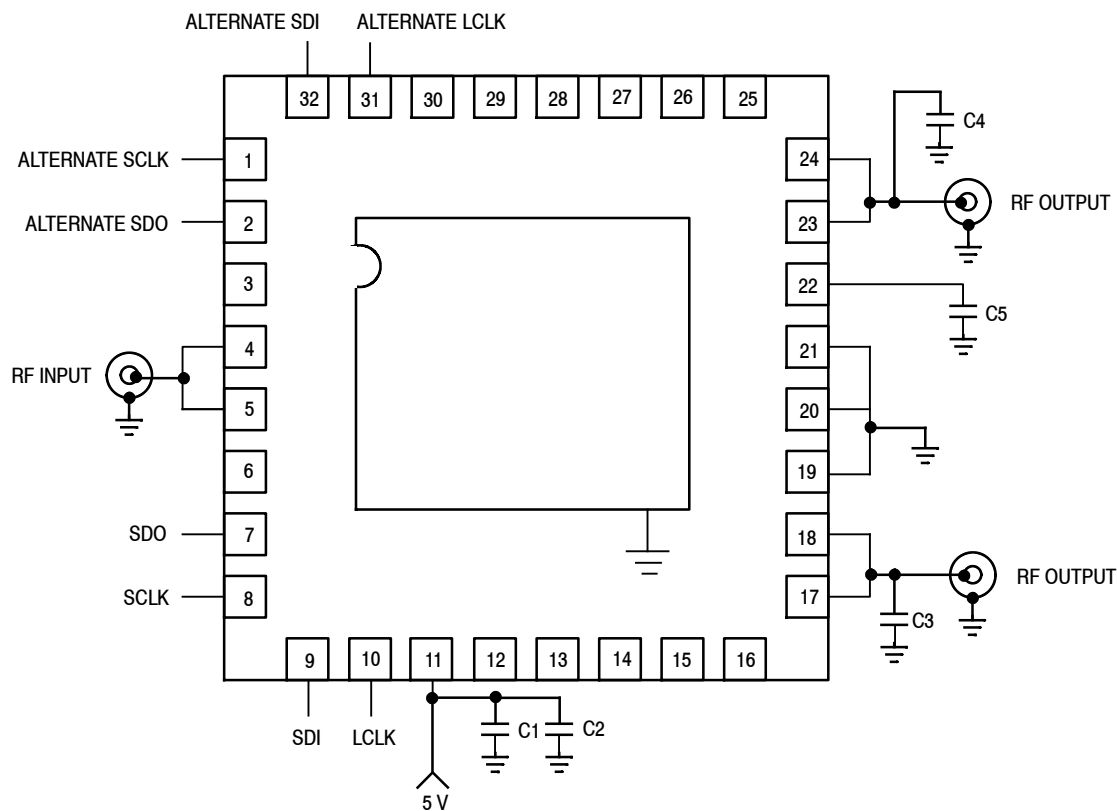
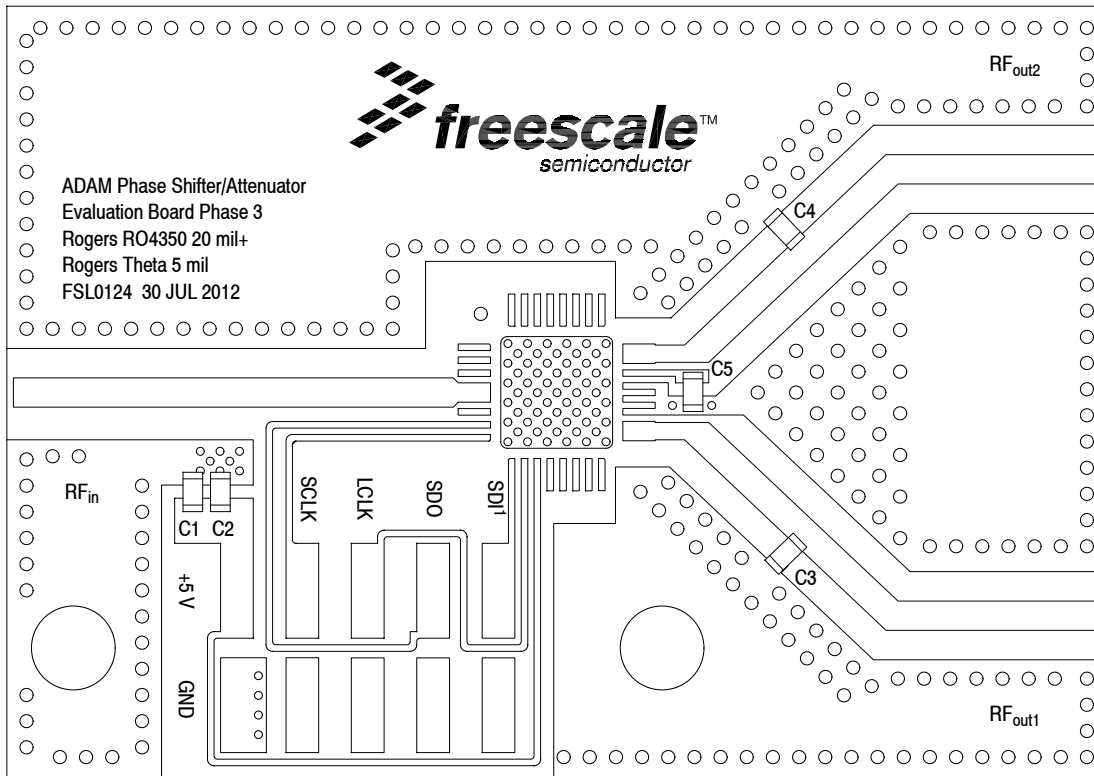


Figure 6. MMDS25254H Test Circuit Schematic

Table 12. MMDS25254H Test Circuit Component Designations and Values

| Part   | Description                | Part Number        | Manufacturer |
|--------|----------------------------|--------------------|--------------|
| C1     | 22 pF Chip Capacitor       | GRM1885C1H220JA01J | Murata       |
| C2     | 100 pF Chip Capacitor      | GRM1885C1H101JA01J | Murata       |
| C3, C4 | 0.4 pF Chip Capacitors     | 06035J0R4ABT       | AVX          |
| C5     | 0.1 $\mu$ F Chip Capacitor | GRM155R61A104KA01D | Murata       |
| PCB    | 0.02", $\epsilon_r = 3.48$ | RO4350             | Rogers       |

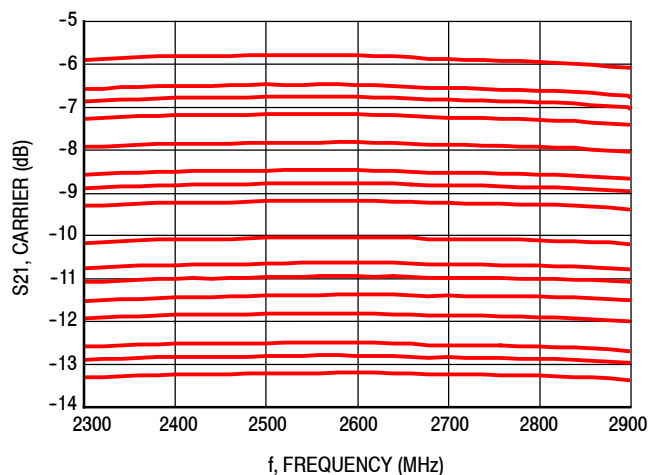


**Figure 7. MMDS25254H Test Circuit Component Layout**

**Table 12. MMDS25254H Test Circuit Component Designations and Values**

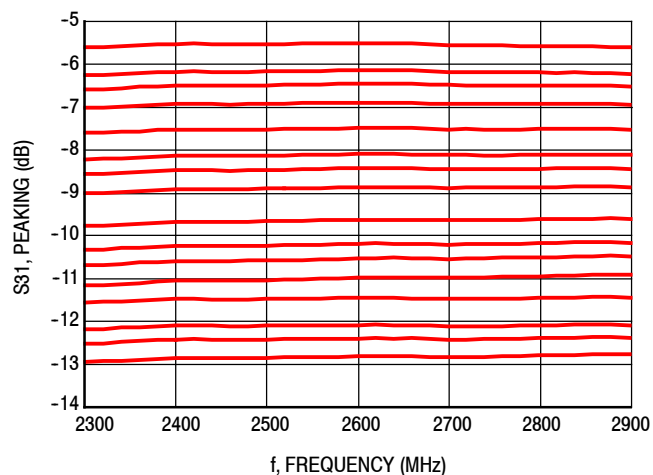
| Part   | Description                | Part Number        | Manufacturer |
|--------|----------------------------|--------------------|--------------|
| C1     | 22 pF Chip Capacitor       | GRM1885C1H220JA01J | Murata       |
| C2     | 100 pF Chip Capacitor      | GRM1885C1H101JA01J | Murata       |
| C3, C4 | 0.4 pF Chip Capacitors     | 06035J0R4ABT       | AVX          |
| C5     | 0.1 $\mu$ F Chip Capacitor | GRM155R61A104KA01D | Murata       |
| PCB    | 0.02", $\epsilon_r = 3.48$ | RO4350             | Rogers       |

(Test Circuit Component Designations and Values repeated for reference.)



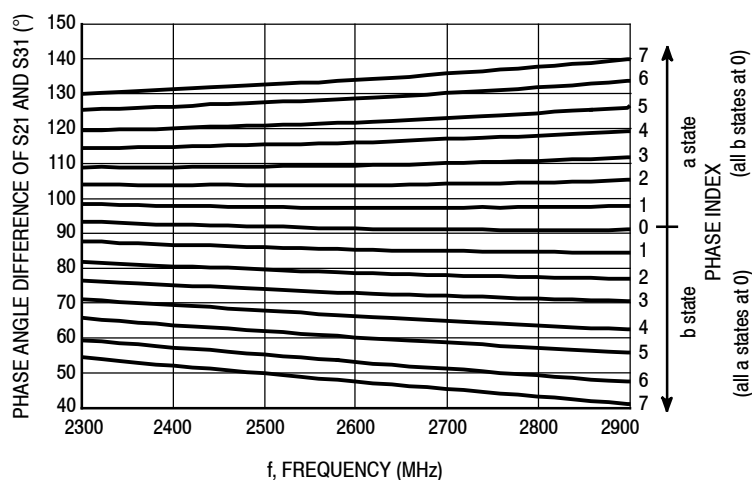
**Note:** S21 is a combination of static insertion loss and selected path attenuation.

**Figure 8. S21 versus Attenuation State versus Frequency**



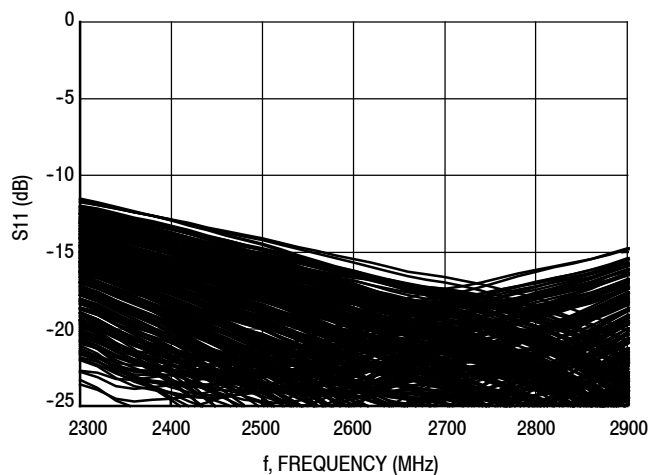
**Note:** S31 is a combination of static insertion loss and selected path attenuation.

**Figure 9. S31 versus Attenuation State versus Frequency**

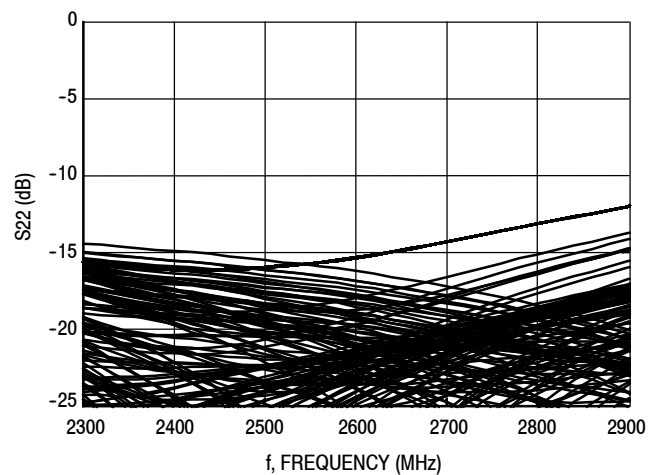


**Note:** The phase angle difference is a combination of insertion phase and selected phase adjustment.

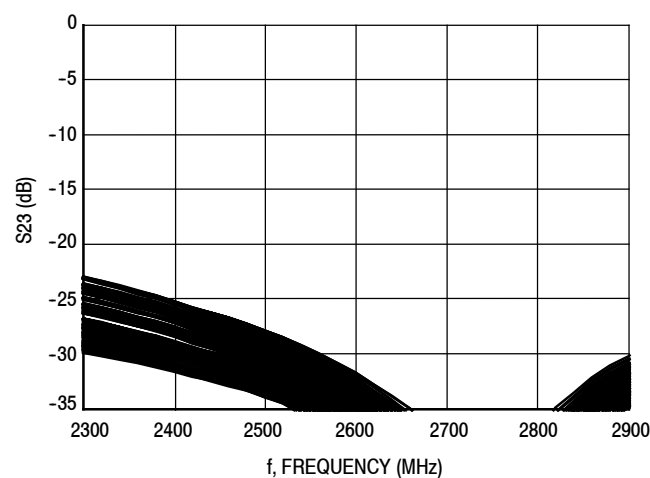
**Figure 10. Phase Angle Difference of S21 and S31 versus Phase State versus Frequency**



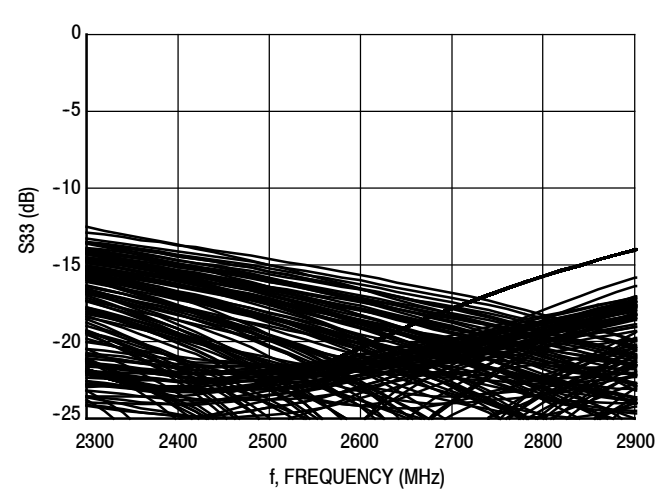
**Figure 11. S11 versus Frequency**



**Figure 12. S22 versus Frequency**

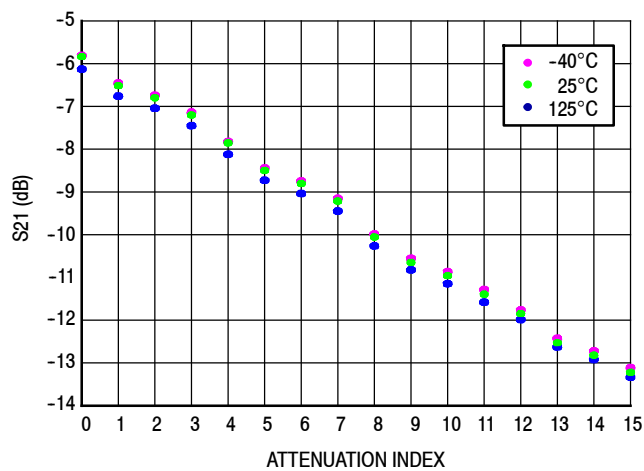


**Figure 13. S23 versus Frequency**

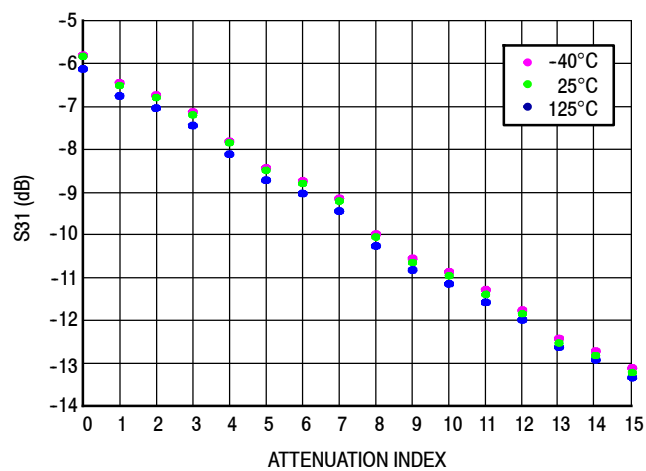


**Figure 14. S33 versus Frequency**

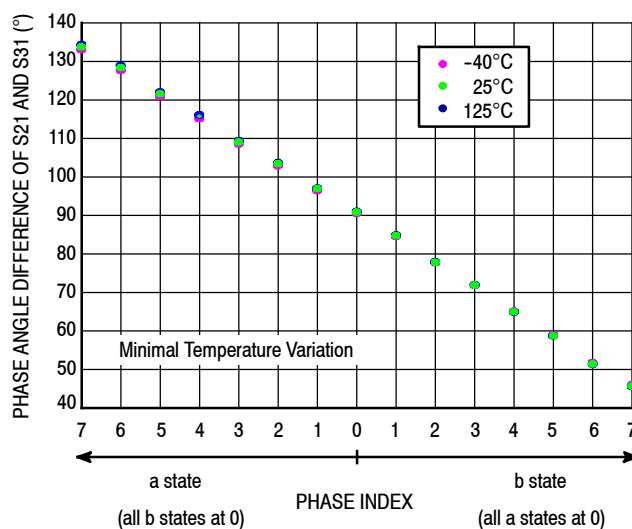
**Note:** A total of 256 states are plotted in Figures 11 to 14. Graph measurements include 128 states for the carrier side (combinations of all phase and amplitude states), with the peaking side set to 0 dB attenuation and 0° phase. Measurements also include 128 states for the peaking side (combinations of all phase and amplitude states) with the carrier side set to 0 dB attenuation and 0° phase.



**Figure 15. S21 versus Attenuation State versus Temperature**



**Figure 16. S31 versus Attenuation State versus Temperature**



**Figure 17. Phase Angle Difference of S21 and S31 versus Phase State versus Temperature**

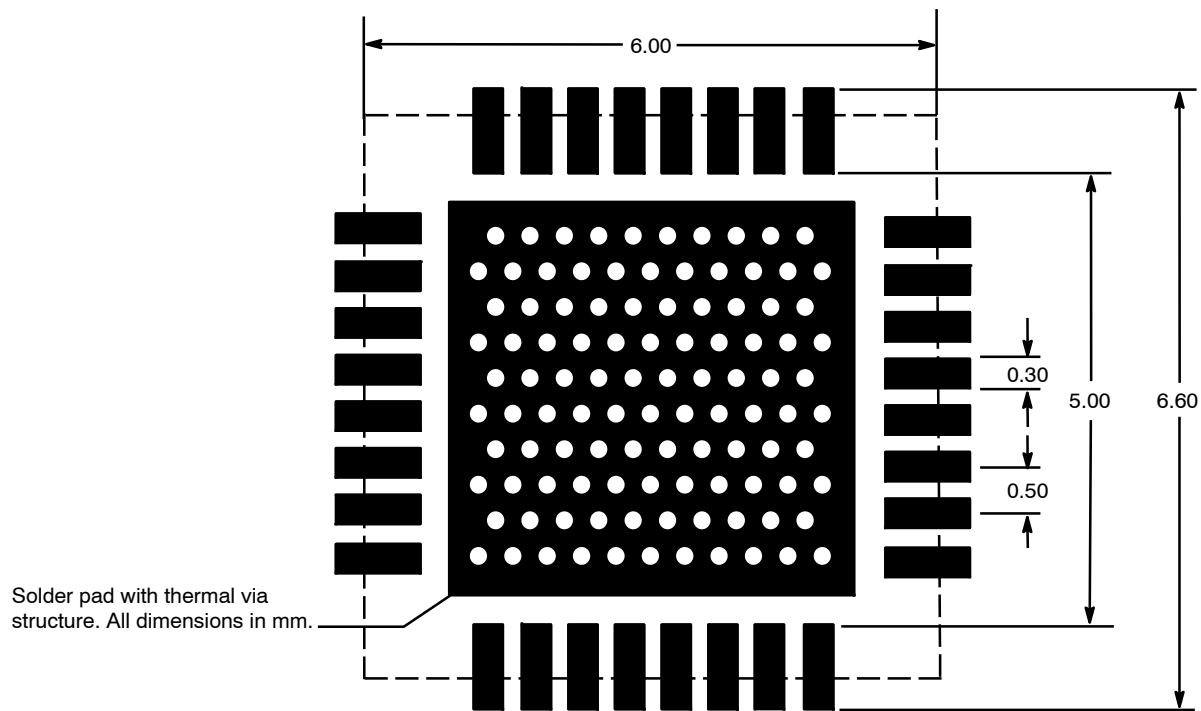
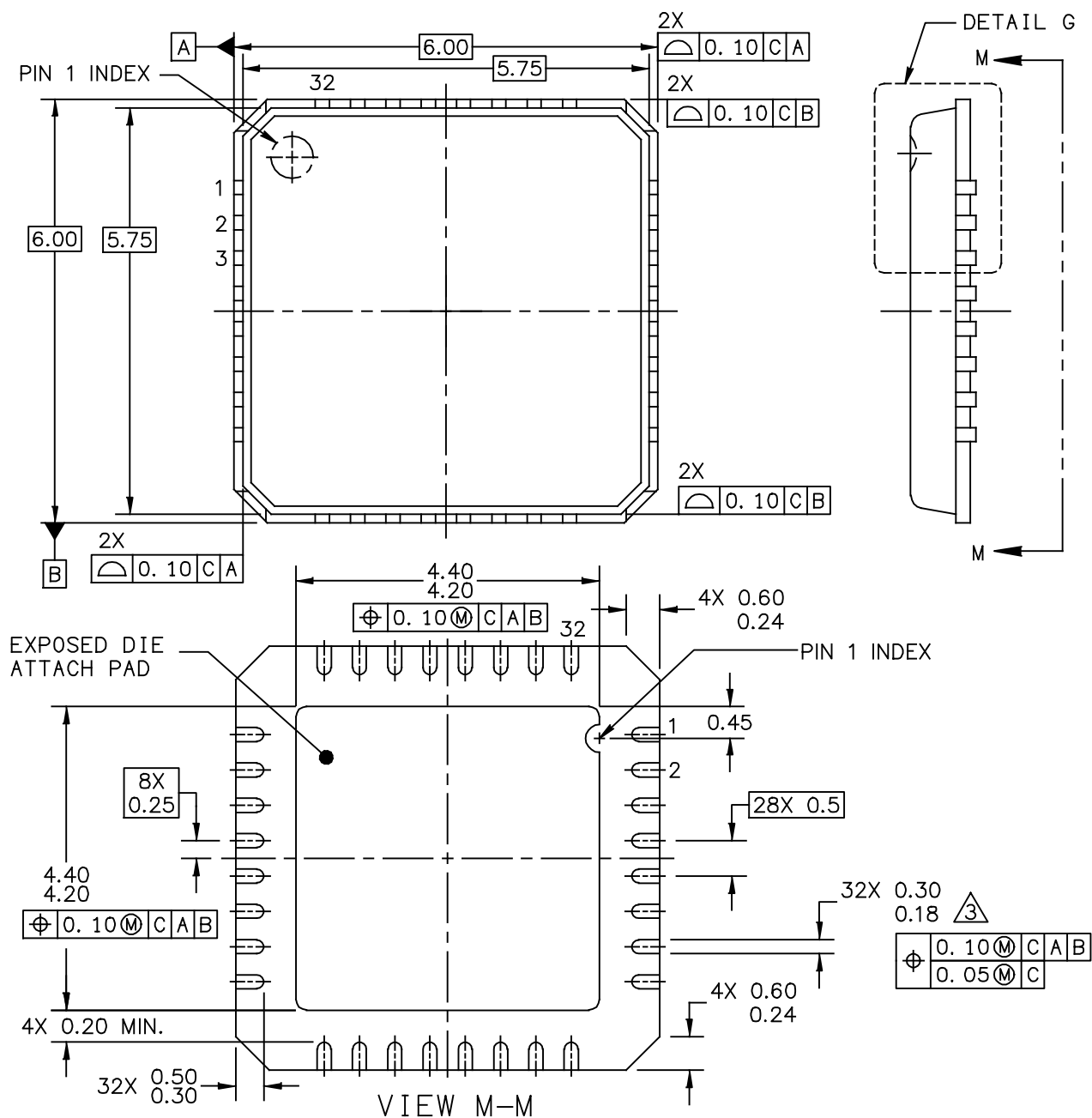


Figure 18. PCB Pad Layout for PQFN 6 x 6

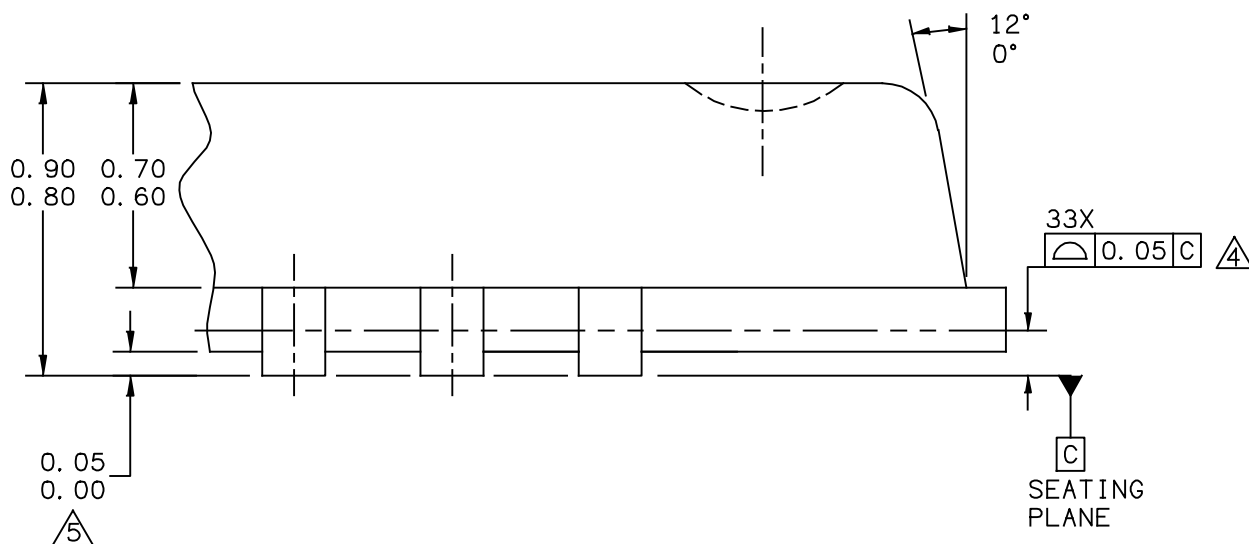


Figure 19. Product Marking

## PACKAGE DIMENSIONS



|                                                                                                       |  |                          |  |                            |  |
|-------------------------------------------------------------------------------------------------------|--|--------------------------|--|----------------------------|--|
| © FREESCALE SEMICONDUCTOR, INC.<br>ALL RIGHTS RESERVED.                                               |  | MECHANICAL OUTLINE       |  | PRINT VERSION NOT TO SCALE |  |
| TITLE:<br>THERMALLY ENHANCED QUAD<br>FLAT NON-LEADED PACKAGE (QFN)<br>6 X 6 X 0.85, 32 I/O, 0.5 PITCH |  | DOCUMENT NO: 98ASA00395D |  | REV: 0                     |  |
|                                                                                                       |  | CASE NUMBER: 2235-01     |  | 03 NOV 2011                |  |
|                                                                                                       |  | STANDARD: NON-JEDEC      |  |                            |  |



DETAIL G  
VIEW ROTATED 90° CW

|                                                                                                       |                    |                            |             |
|-------------------------------------------------------------------------------------------------------|--------------------|----------------------------|-------------|
| © FREESCALE SEMICONDUCTOR, INC.<br>ALL RIGHTS RESERVED.                                               | MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE |             |
| TITLE:<br>THERMALLY ENHANCED QUAD<br>FLAT NON-LEADED PACKAGE (QFN)<br>6 X 6 X 0.85, 32 I/O, 0.5 PITCH |                    | DOCUMENT NO: 98ASA00395D   | REV: 0      |
|                                                                                                       |                    | CASE NUMBER: 2235-01       | 03 NOV 2011 |
|                                                                                                       |                    | STANDARD: NON-JEDEC        |             |

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING & TOLERANCING PER ASME Y14.5 – 2009.
3. THIS DIMENSION APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. THIS DIMENSION APPLIES ONLY FOR TERMINALS.
6. MOLD FLASH OR PLATING COVERAGE ON THE RING PAD AREA SHALL BE ALLOWABLE

|                                                                                                       |  |                          |  |                            |  |
|-------------------------------------------------------------------------------------------------------|--|--------------------------|--|----------------------------|--|
| © FREESCALE SEMICONDUCTOR, INC.<br>ALL RIGHTS RESERVED.                                               |  | MECHANICAL OUTLINE       |  | PRINT VERSION NOT TO SCALE |  |
| TITLE:<br>THERMALLY ENHANCED QUAD<br>FLAT NON-LEADED PACKAGE (QFN)<br>6 X 6 X 0.85, 32 I/O, 0.5 PITCH |  | DOCUMENT NO: 98ASA00395D |  | REV: 0                     |  |
|                                                                                                       |  | CASE NUMBER: 2235-01     |  | 03 NOV 2011                |  |
|                                                                                                       |  | STANDARD: NON-JEDEC      |  |                            |  |

## PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

### Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

### Software

- .s3p File
- Large Signal Simulation

### Development Tools

- Printed Circuit Boards
- Evaluation/Development Boards and Systems (file includes ADAM User's Guide)

For Software and Tools, do a Part Number search at <http://www.freescale.com>, and select the "Part Number" link. Go to the Software & Tools tab on the part's Product Summary page to download the respective tool.

## FAILURE ANALYSIS

At this time, because of the physical characteristics of the part, failure analysis is limited to electrical signature analysis. In cases where Freescale is contractually obligated to perform failure analysis (FA) services, full FA may be performed by third party vendors with moderate success. For updates contact your local Freescale Sales Office.

## REVISION HISTORY

The following table summarizes revisions to this document.

| Revision | Date      | Description                                                                                                                                                                                                                                           |
|----------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0        | May 2014  | <ul style="list-style-type: none"> <li>• Initial release of data sheet</li> </ul>                                                                                                                                                                     |
| 1        | Jan. 2015 | <ul style="list-style-type: none"> <li>• Table 7, Functional Pin Description, for pins 4 and 5: pin description for RF<sub>in</sub> (pins 4 and 5) updated to include additional information needed for pin connection configuration, p. 3</li> </ul> |

### ***How to Reach Us:***

**Home Page:**  
[freescale.com](http://freescale.com)

**Web Support:**  
[freescale.com/support](http://freescale.com/support)

Information in this document is provided solely to enable system and software implementers to use Freescale products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document.

Freescale reserves the right to make changes without further notice to any products herein. Freescale makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. Freescale does not convey any license under its patent rights nor the rights of others. Freescale sells products pursuant to standard terms and conditions of sale, which can be found at the following address: [freescale.com/SalesTermsandConditions](http://freescale.com/SalesTermsandConditions).

Freescale and the Freescale logo are trademarks of Freescale Semiconductor, Inc., Reg. U.S. Pat. & Tm. Off. All other product or service names are the property of their respective owners.

© 2014–2015 Freescale Semiconductor, Inc.



**Стандарт  
Электрон  
Связь**

Мы молодая и активно развивающаяся компания в области поставок электронных компонентов. Мы поставляем электронные компоненты отечественного и импортного производства напрямую от производителей и с крупнейших складов мира.

Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию .

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России , а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

Минимальные сроки поставки, гибкие цены, неограниченный ассортимент и индивидуальный подход к клиентам являются основой для выстраивания долгосрочного и эффективного сотрудничества с предприятиями радиоэлектронной промышленности, предприятиями ВПК и научно-исследовательскими институтами России.

С нами вы становитесь еще успешнее!

**Наши контакты:**

**Телефон:** +7 812 627 14 35

**Электронная почта:** [sales@st-electron.ru](mailto:sales@st-electron.ru)

**Адрес:** 198099, Санкт-Петербург,  
Промышленная ул, дом № 19, литера Н,  
помещение 100-Н Офис 331